



June 1997

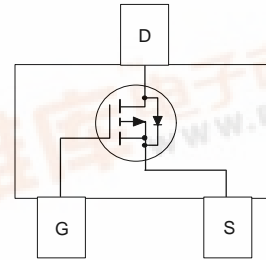
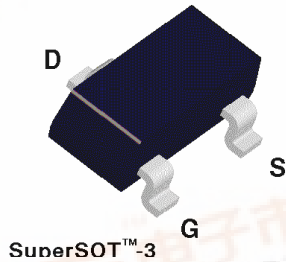
## NDS332P P-Channel Logic Level Enhancement Mode Field Effect Transistor

### General Description

These P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

### Features

- 1 A, -20 V,  $R_{DS(ON)} = 0.41 \Omega @ V_{GS} = -2.7 V$   
 $R_{DS(ON)} = 0.3 \Omega @ V_{GS} = -4.5 V.$
- Very low level gate drive requirements allowing direct operation in 3V circuits.  $V_{GS(th)} < 1.0V.$
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Exceptional on-resistance and maximum DC current capability.
- Compact industry standard SOT-23 surface Mount package.

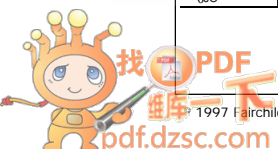


### Absolute Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	NDS332P	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage - Continuous	$\pm 8$	V
$I_D$	Drain Current - Continuous (Note 1a)	-1	A
	- Pulsed	-10	
$P_D$	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5	W
		0.46	
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ C$

### THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	$^\circ C/W$



**Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>OFF CHARACTERISTICS</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$	
			$T_J = 55^\circ\text{C}$			-10	$\mu\text{A}$
$I_{GSS}$	Gate - Body Leakage Current	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA	
$I_{GSS}$	Gate - Body Leakage Current	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA	
<b>ON CHARACTERISTICS</b> (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.6	-1	V	
			$T_J = 125^\circ\text{C}$	-0.3	-0.45		-0.8
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -2.7\text{ V}, I_D = -1\text{ A}$		0.35	0.41	$\Omega$	
			$T_J = 125^\circ\text{C}$		0.5		0.74
				$V_{GS} = -4.5\text{ V}, I_D = -1.1\text{ A}$			0.26
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -2.7\text{ V}, V_{DS} = -5\text{ V}$	-1.5			A	
			$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-2.5			
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -1\text{ A}$		2.2		S	
<b>DYNAMIC CHARACTERISTICS</b>							
$C_{iss}$	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		195		pF	
$C_{oss}$	Output Capacitance			105		pF	
$C_{rss}$	Reverse Transfer Capacitance			40		pF	
<b>SWITCHING CHARACTERISTICS</b> (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = -6\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		8	15	ns	
$t_r$	Turn - On Rise Time			30	45	ns	
$t_{D(off)}$	Turn - Off Delay Time			25	45	ns	
$t_f$	Turn - Off Fall Time			27	45	ns	
$Q_g$	Total Gate Charge		$V_{DS} = -5\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}$		3.7	5	nC
$Q_{gs}$	Gate-Source Charge			0.5		nC	
$Q_{gd}$	Gate-Drain Charge			0.9		nC	

## Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
I <sub>S</sub>	Maximum Continuous Source Current				-0.42	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -0.42 A (Note 2)		-0.75	-1.2	V

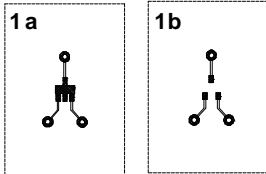
Notes:

1. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)} @ T_J$$

Typical R<sub>θJA</sub> using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- a. 250°C/W when mounted on a 0.02 in<sup>2</sup> pad of 2oz copper.
- b. 270°C/W when mounted on a 0.001 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

## Typical Electrical Characteristics

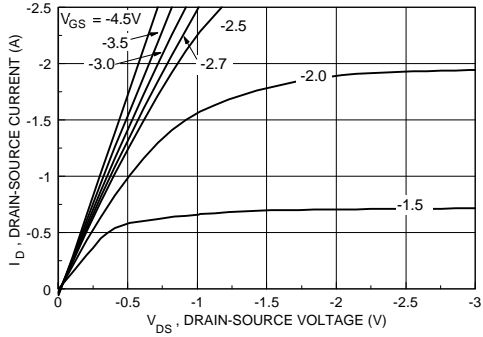


Figure 1. On-Region Characteristics.

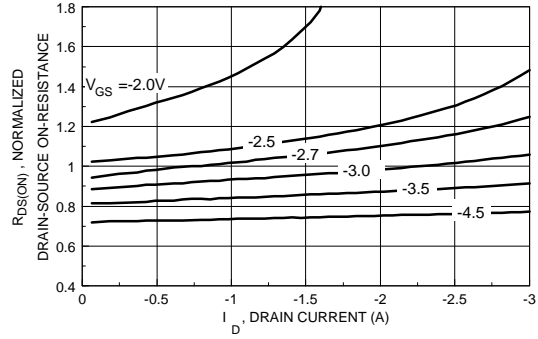


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

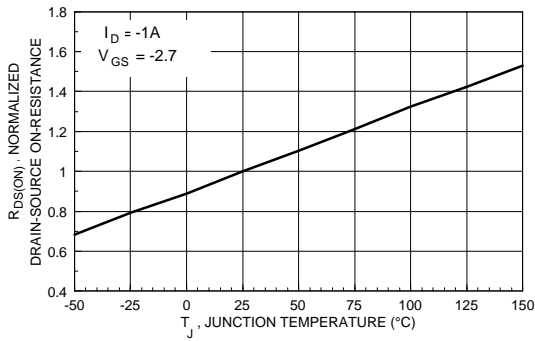


Figure 3. On-Resistance Variation with Temperature.

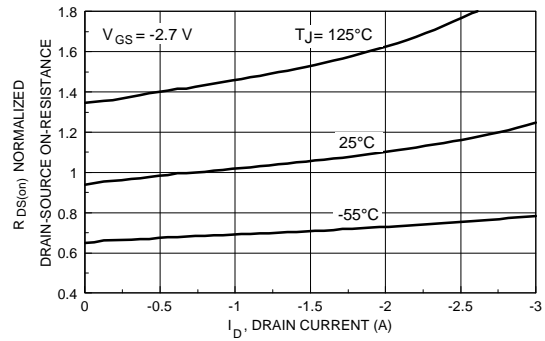


Figure 4. On-Resistance Variation with Drain Current and Temperature.

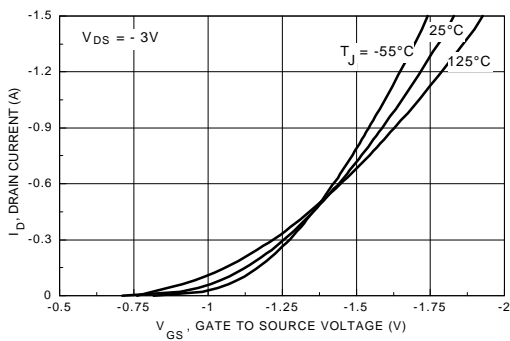


Figure 5. Transfer Characteristics.

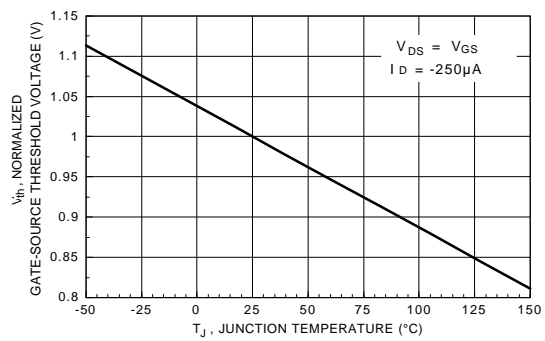


Figure 6. Gate Threshold Variation with Temperature.

### Typical Electrical Characteristics (continued)

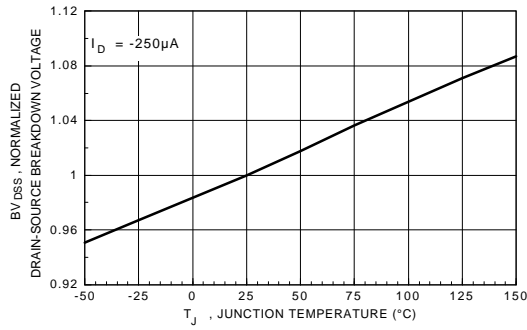


Figure 7. Breakdown Voltage Variation with Temperature.

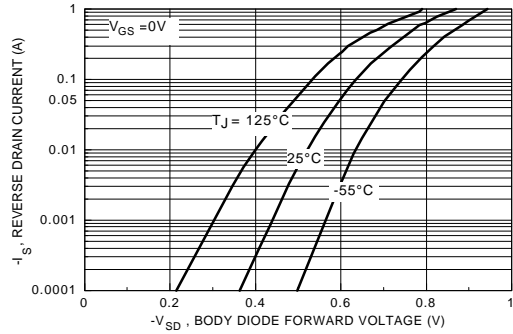


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature.

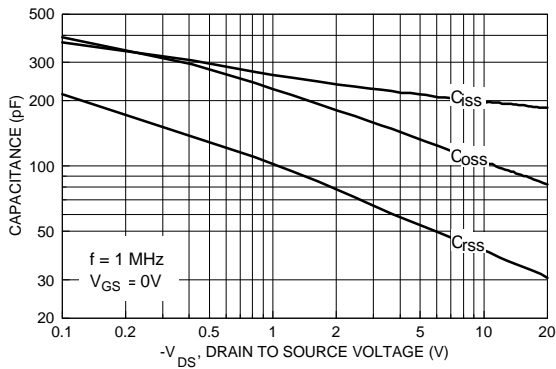


Figure 9. Capacitance Characteristics.

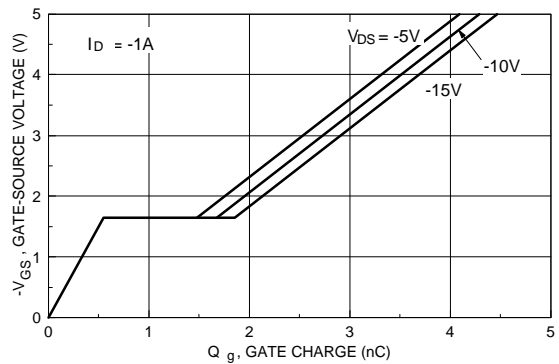


Figure 10. Gate Charge Characteristics.

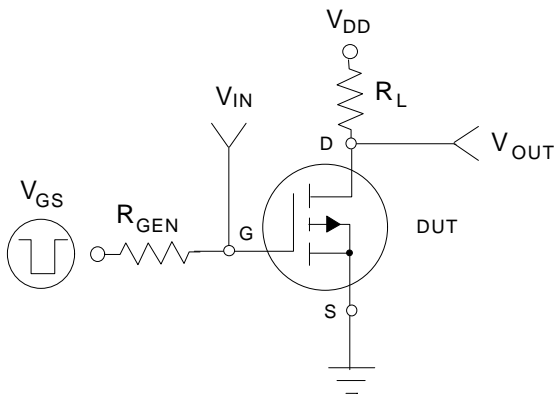


Figure 11. Switching Test Circuit.

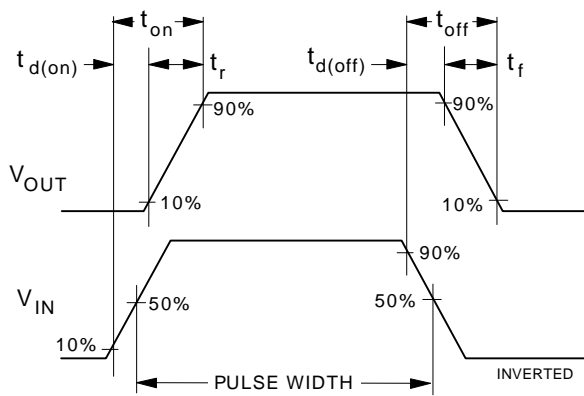
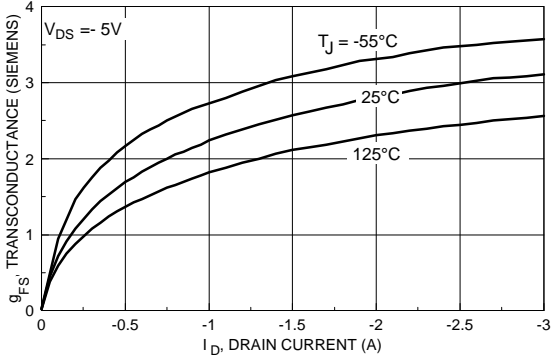
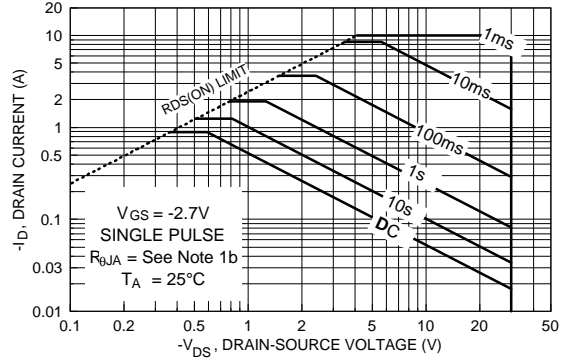


Figure 12. Switching Waveforms.

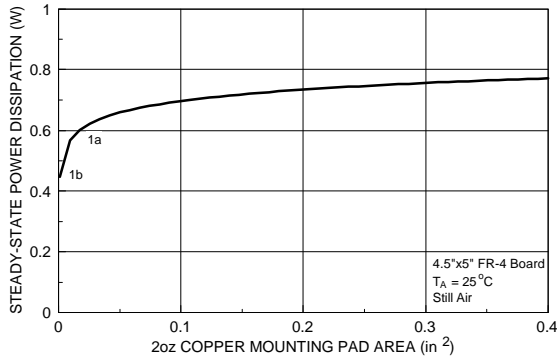
**Typical Electrical Characteristics (continued)**



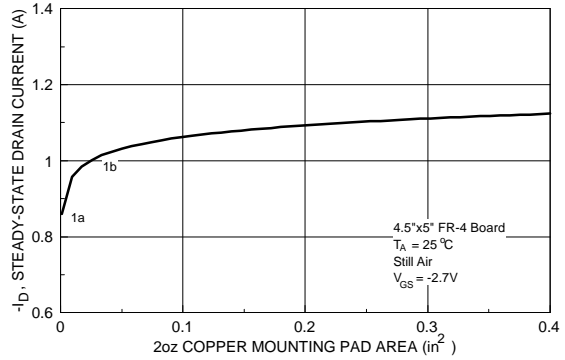
**Figure 13. Transconductance Variation with Drain Current and Temperature.**



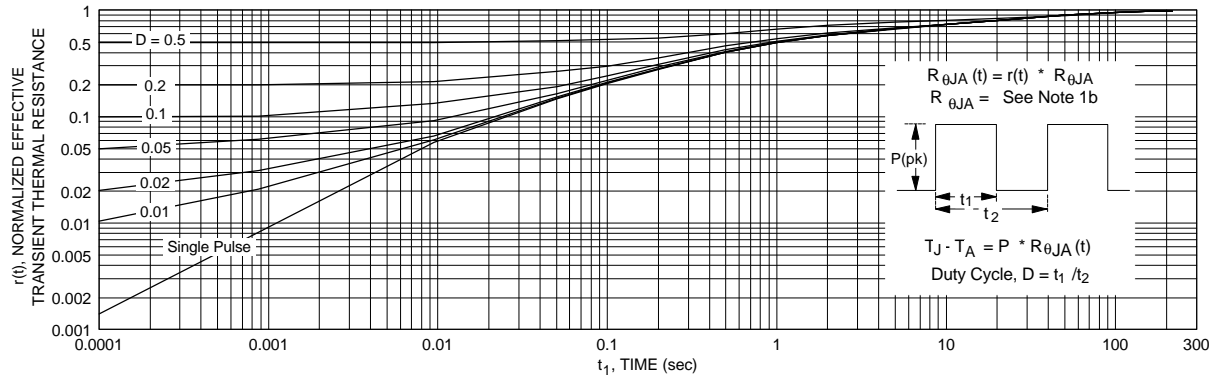
**Figure 14. Maximum Safe Operating Area.**



**Figure 15. SuperSOT™ - 3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**



**Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**



**Figure 17. Transient Thermal Response Curve.**

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.