6-Bit A/D converter (parallel outputs) NE5037

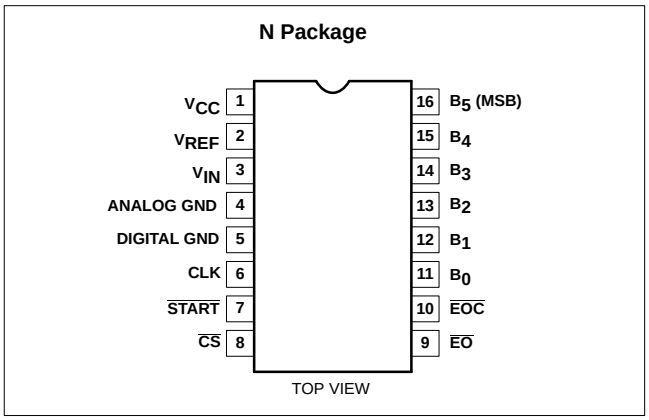
DESCRIPTION

The NE5037 is a low cost, complete successive-approximation analog-to-digital (A/D) converter, fabricated using Bipolar/I^2L technology. With an external reference voltage, the NE5037 will accept input voltages between 0V and V_{REF}. An external $\overline{START}$ pulse of at least 300ns in duration will provide the 6-bit result of the conversion in parallel format. Full conversion with no missing codes occurs in 9µs.

FEATURES

- TTL-compatible inputs and outputs
- 3-State output buffer
- Easy interface to CMOS microprocessors
- Fast conversion—9µs
- Guaranteed no missing codes over full temp range
- Single-supply operation, +5V
- Positive true binary outputs
- High-impedance analog inputs

PIN CONFIGURATION



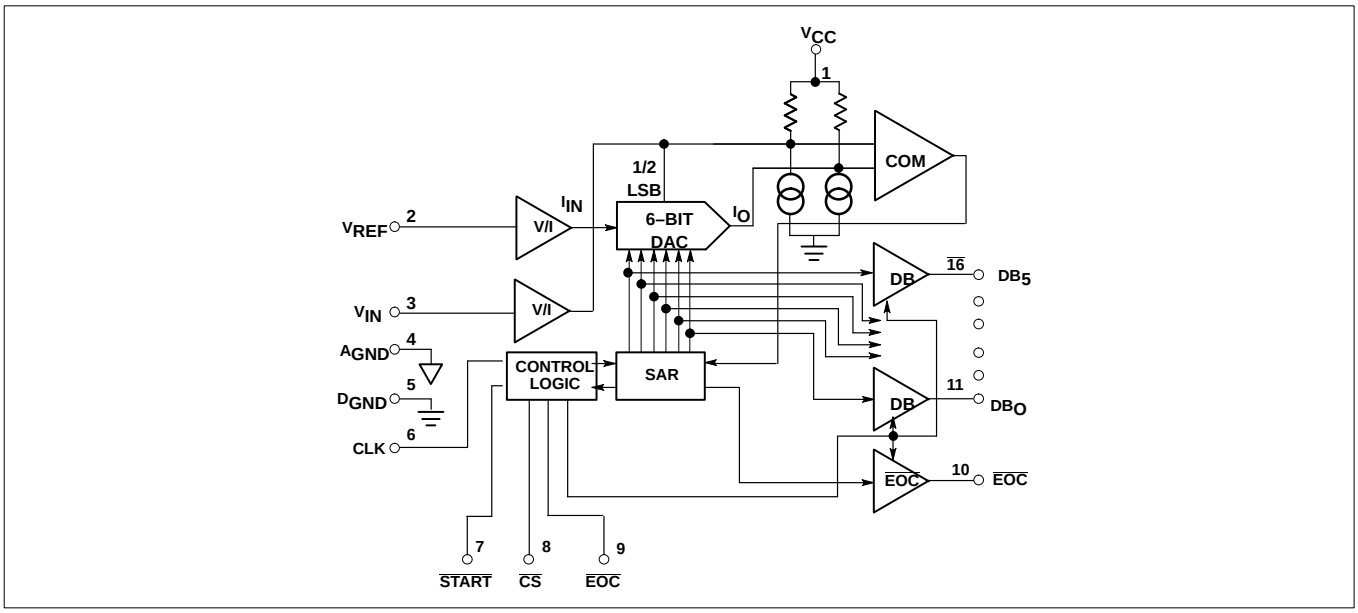
APPLICATIONS

- Temperature control
- µP-based appliances
- Light level monitors
- Head position sensing
- Electronic toys
- Joystick interface

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE5037N	0406C

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	7	V
V_{REF}	Reference voltage	7	V
$V_{IN(Analog)}$	Analog input voltage	7	V
$V_{IN(Digital)}$	Digital input voltage ($\overline{CS}$, $\overline{OE}$, $\overline{START}$, CLK)	7	V
D_{OUT}	Data outputs (DB0 to DB5)		
	3-state mode	7	V
	Enabled mode (each output)	5	mA
$\overline{EOC}$	End of conversion	V_{CC}	
Δ_{GND}	Analog GND to digital GND	±1	V
T_A	Operating temperature range	0 to 70	°C
T_{STG}	Storage temperature range	-65 to 150	°C
T_{SOLD}	Lead soldering temperature (10 seconds)	300	°C
P_D	Maximum power dissipation, T_A=25°C (still-air)[1]		
	N package	1450	mW

NOTES:
1. Derate above 25°C at the following rates:
   N package=11.6mW/°C

DC ELECTRICAL CHARACTERISTICS

V_{CC}=5.0V; V_{REF}=2.0V; Clock=1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Resolution		6	6	6	Bits
	Relative accuracy[1,2]			1/4	1/2	LSB
V_{CC}	Positive supply voltage		+4.75	+5.0	+5.50	V
ε_{FS}	Full-scale gain error[2,3,4]	V_{REF}=2.0V, T_A=25°C		±1	±2	LSB
ε_{ZS}	Zero-scale offset error[2]	V_{REF}=2.0V, T_A=25°C		±1/2	-1/2, +2	LSB
PSR	Power supply rejection, Max change in full-scale[2]	V_{REF}=2.0V, 4.75V≤V_{CC}≤5.5V		±1/2	±1	LSB
I_{IN}	Analog input bias current	0≤V_{IN}≤2.5V		1	10	µA
I_{REF}	Reference bias current	0≤V_{REF}≤2.5V		1	10	µA
R_{IN}	Analog input resistance		3	30		MΩ
V_{IH}	Logic ”1’ input voltage		2.0			V
V_{IL}	Logic ”0’ input voltage				0.8	V
I_{IH}	Logic ”1’ input current				10	µA
I_{IL}	Logic ”0’ input current			1	10	µA
I_{OH}	Logic ”1’ output current[5]	2.4V≤V_{OH}	300			µA
I_{OL}	Logic ”0’ output current[5]	V_{OL}≤0.4V	1.6			mA
I_{OZ}	3-State leakage current			±0.1	±40	µA
I_{CC}	Positive supply current			18	24	mA
P_D	Power dissipation				132	mW

NOTES:
1. Relative accuracy is defined as the deviation of the code transition points from the ideal code transition points on a straight line drawn from zero-scale to full-scale of the device.
2. Specifications given in LSBs refer to the weight of the least significant bit at the 6-bit level which is 1.56% of the full-scale voltage.
3. Full-scale gain error is the deviation of the full-scale code transition point (111110 to 111111) from its ideal value.
4. The analog input voltage (V_{IN}) range is 0V to V_{REF} nominally, with the output remaining at 111111 even though the input may increase from V_{REF} to V_{CC}. (For optimum performance, V_{REF} can be any value from 1.5V to 2.5V.)
5. The data outputs have active pull-ups. The $\overline{EOC}$ line is open-collector with a nominal 5kΩ internal pull-up resistor.

AC ELECTRICAL CHARACTERISTICS

V_{CC}=5.0V; V_{REF}=2.0V; Clock=1MHz; 0°C ≤ T_A ≤ 70°C unless otherwise specified. Typical values are specified at 25°C (Refer to AC test figures.)

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	LIMITS			UNIT
					Min	Typ	Max	
f_{MAX}	Maximum clock frequency				1			MHz
t_W	Start pulse width				300			ns
	Minimum positive/negative clock pulse width				300			ns
t_{CONV}	Conversion time						9	Clock cycles
$t_{P\ (OUT\ DATA)}$	Propagation delay[1]	Data out	$\overline{OE}$	T_A=25°C t_R=t_F≤20ns			500	ns
$t_{P\ (OUT\ EOC)}$	Propagation delay[2]	$\overline{EOC}$	Clock	T_A=25°C t_R=t_F≤20ns			800	ns
$t_{P\ (3\text{-}STATE)}$	Propagation delay, 3-State	3-State Data	$\overline{OE}$	T_A=25°C t_R=t_F≤20ns			500	ns

NOTES:
1. Propagation delay of data outputs is defined as the delay in the data outputs reading their final value after the low going edge of $\overline{OE}$.
2. Propagation delay of $\overline{EOC}$ is defined as the delay in $\overline{EOC}$ going low, following the low going edge of the 9th clock pulse after the start pulse.

CIRCUIT DESCRIPTION

NE5037 is a complete 6-bit, parallel output, microprocessor compatible, A/D converter which incorporates the successive-approximation method. The chip includes the internal control logic, the successive-approximation register (SAR), 6-bit DAC, comparator and output buffers. An externally-generated clock source (max frequency=1MHz) must be provided to Pin 6. An external reference voltage supplied to Pin 2 sets the full-scale range of the A/D converter.

The $\overline{CS}$ pin must be at a low level prior to the start of the conversion process. Upon receipt of a $\overline{START}$ pulse, the internal control logic resets the SAR. On the first low-going edge of the clock pulse, successive approximation conversion commences. Successive bits beginning with the MSB (D5) are supplied to the input of the internal 6-bit current output DAC by the I^2L successive approximation register.

The comparator determines whether the output current of the DAC is greater or less than the input current, which is converted from the unknown analog input voltage through the V/I converter. If the DAC output is greater, that bit of the DAC is set to ”0’ and the corresponding output buffer goes to ”0’ simultaneously. If it is less, it stays at ‘1’ and the output buffer also stays at ‘1’. On successive clock pulses, successive bits of the DAC are tried and the corresponding output buffer represents the bits of the DAC. On the eighth low-going edge of the clock pulse (after the receipt of the start pulse), the $\overline{EOC}$ pin goes low, thereby indicating that the conversion is complete. The output data is now valid. In order to access the result of the conversion, the $\overline{OE}$ pin must be set to a low level. $\overline{EOC}$ is reset to a high state when $\overline{OE}$ is low. When $\overline{OE}$ is in a ”1’ state, the output buffers are in a high impedance state.

Refer to Figure 1 for the timing diagram.

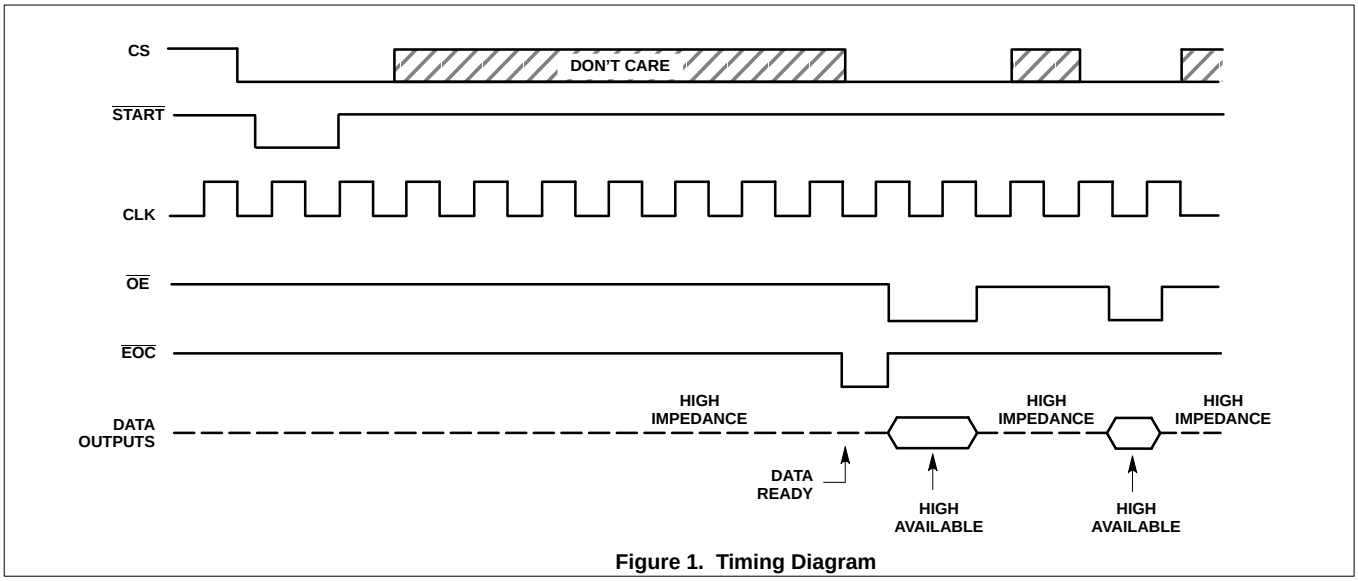


Figure 1. Timing Diagram

TRANSFER CHARACTERISTICS

The ideal transfer characteristic of the NE5037 is shown in Figure 2.

The NE5037 is designed to have a nominal LSB offset so that the code transition points are located LSB on either side of the exact analog inputs for a given code.

Thus the first transition (000000 to 000001) will occur at an input of LSB (15.63mV with a V_{REF} of 2.0V). Subsequent transitions will occur at nominal increments of 1 LSB. The last transition (to full-scale—111111) will occur at 62.5 LSB (1.953V at V_{REF} of 2.0V).

LAYOUT PRECAUTIONS

Analog ground (Pin 4) and digital ground (Pin 5) are not connected internally and should be connected together as close to the device as possible for optimum performance. The circuit will operate with as much as ±200mV between the two grounds but some degradation will occur. The leads to the analog inputs should be kept as short as possible to minimize noise pick-up. Input bypass capacitors from the analog inputs to ground will eliminate noise pick-up. Power supplies should be decoupled with at least 1µF located close to the device to minimize the effects of noise spikes.

The reference input and the analog voltage input must both remain stable during conversion to insure accuracy and proper operation. This can be done by adequately bypassing these inputs and/or keeping the impedance of these inputs at or below 2kΩ.

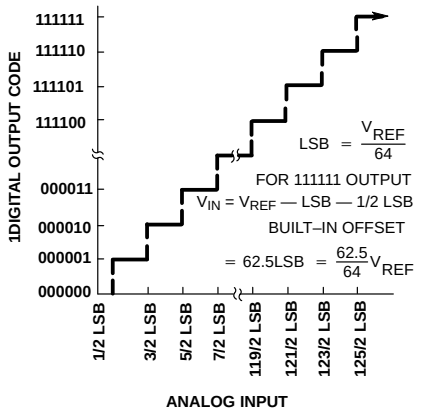
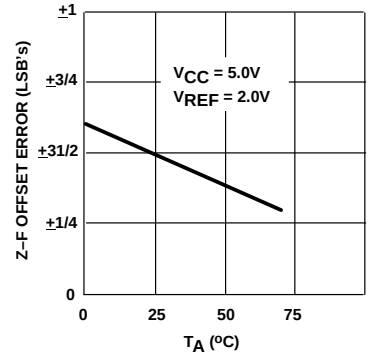


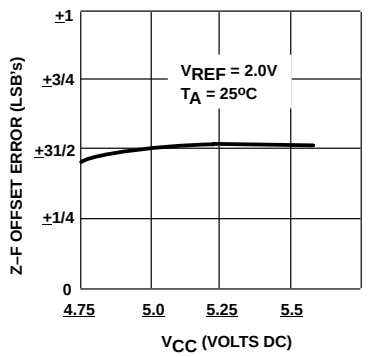
Figure 2. Ideal Transfer Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

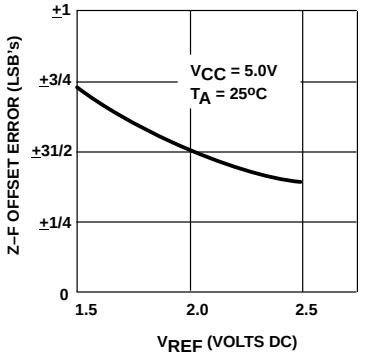
Zero–Scale Offset Error vs Temp



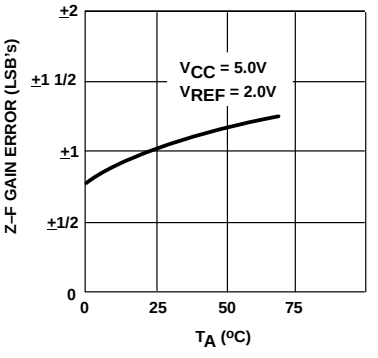
Zero–Scale Offset Error vs v_{cc}



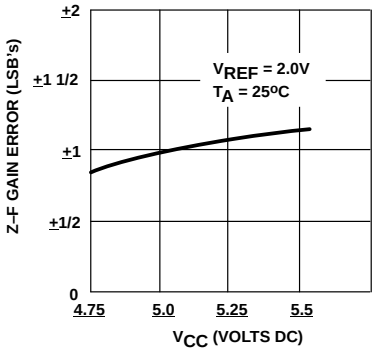
Zero–Scale Offset Error vs v_{REF}



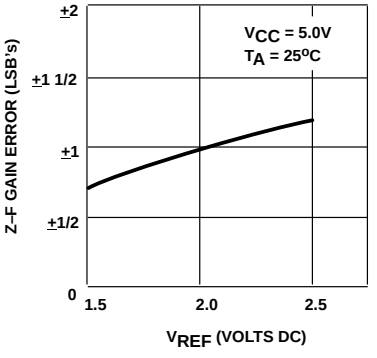
Full–Scale GAIN Error vs Temp



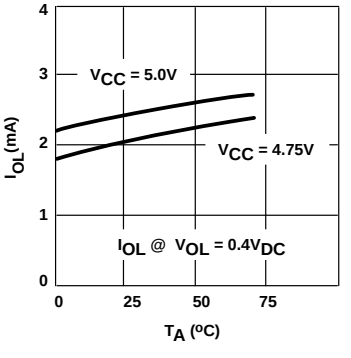
Full–Scale Gain Error vs v_{cc}



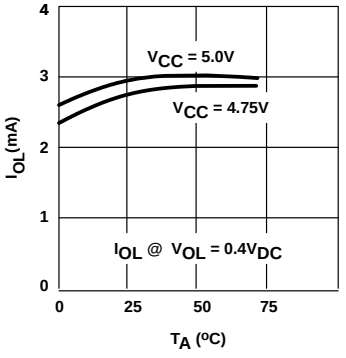
Full–Scale Gain Error vs v_{REF}



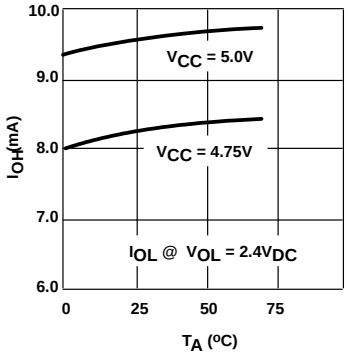
I_{OL} vs Temp (Data Output)



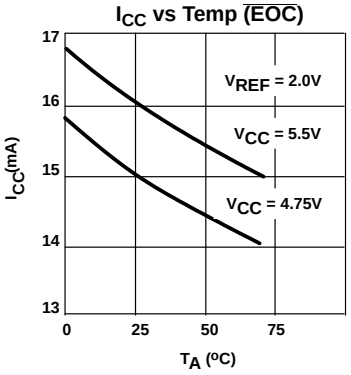
I_{OL} vs Temp ($\overline{EOC}$)



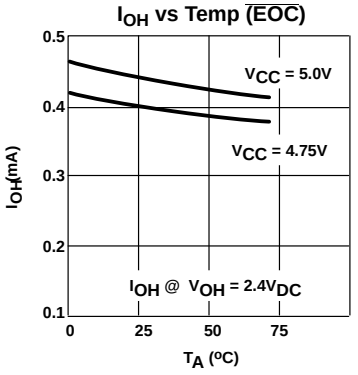
I_{OH} vs Temp (Data Output)



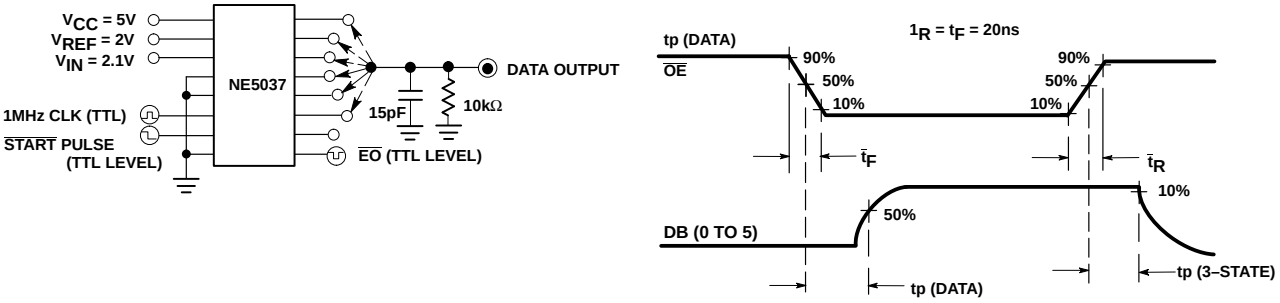
I_{CC} vs Temp ($\overline{EOC}$)



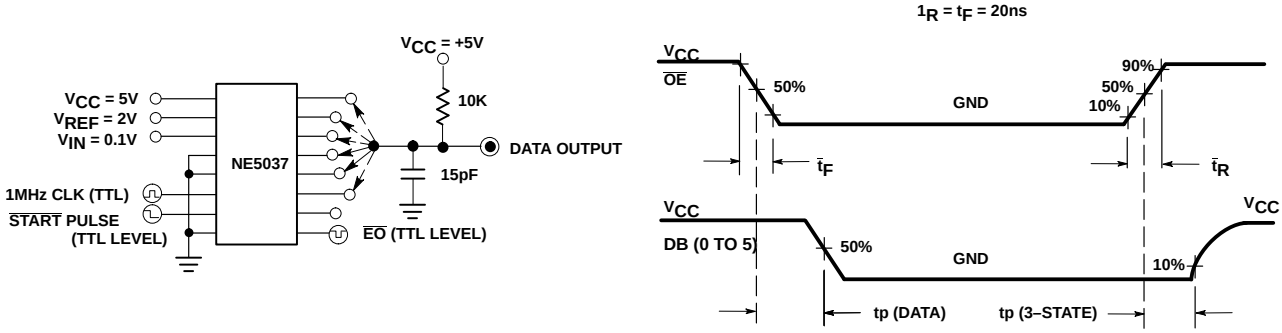
I_{OH} vs Temp ($\overline{EOC}$)



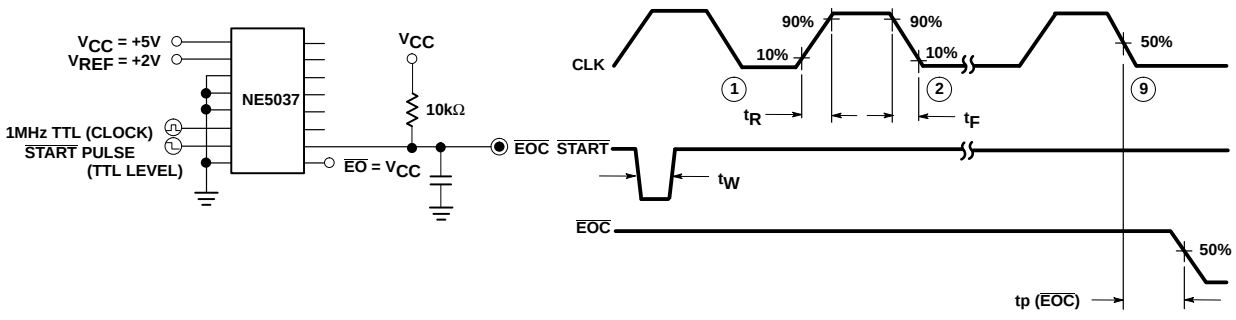
AC TEST CIRCUITS AND WAVEFORMS



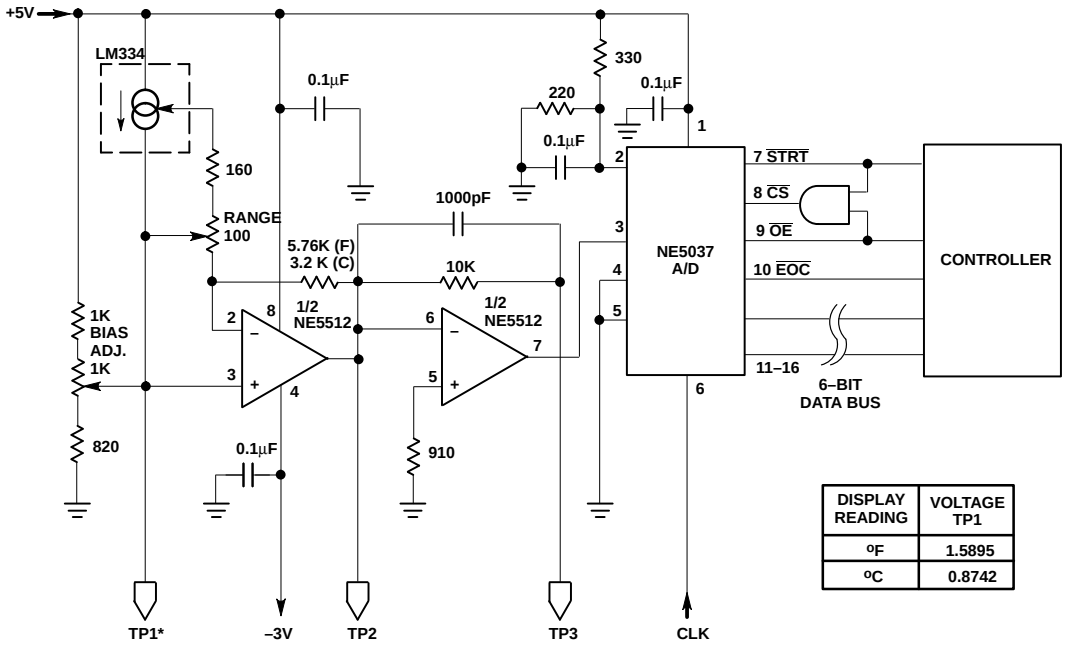
Propagation Delay Time t_P (DATA) and T_P (3-state)



Data Output High

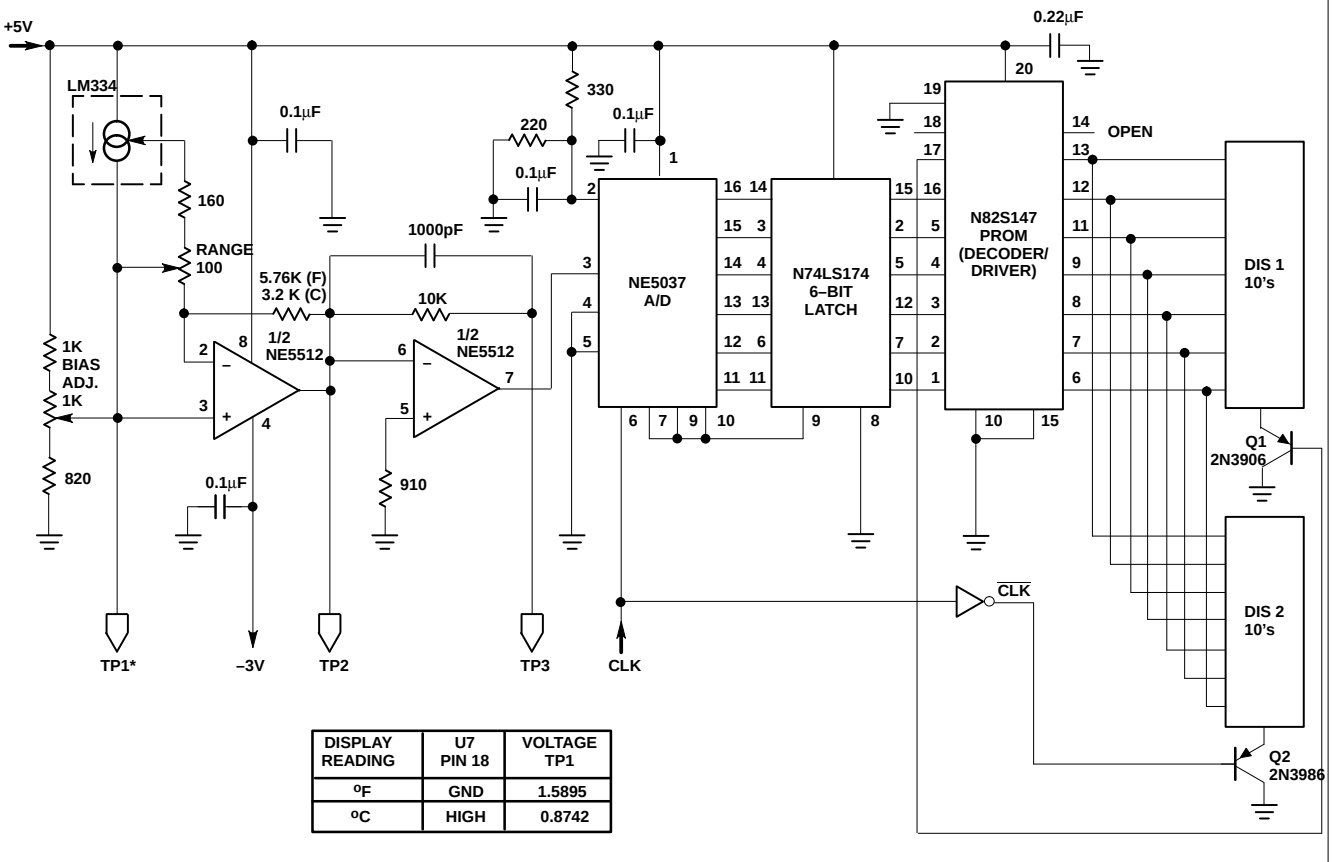


Propagation Delay Time EOC $t_{P(EOC)}$



DISPLAY READING	VOLTAGE TP1
°F	1.5895
°C	0.8742

a. Temperature Sensor



DISPLAY READING	U7 PIN 18	VOLTAGE TP1
°F	GND	1.5895
°C	HIGH	0.8742

b. Digital Thermometer

Figure 3.

6-Bit A/D converter (parallel outputs) NE5037

APPLICATION

- 0 to 63°C Temperature Sensor

CIRCUIT DESCRIPTION

The temperature sensor of Figure 3 provides an input to Pin 3 of the NE5037 of 32mV/°C. This 32mV is the value of one LSB for the NE5037. The LM334 is a three-terminal temperature sensor and provides a current of 1µA for each °Kelvin. The first section of the dual op amp is connected as a trans-impedance amplifier to convert the current from the LM334 to a voltage, which is amplified and inverted by the section amplifier. Note that the first amplifier requires different values of feedback resistance for °C and °F. The NE5512 was chosen for its low temperature coefficient of input bias current as excessive I_{OS} tempco would degrade temperature tracking.

To read temperature, conversion is started by sending a momentary low signal to Pin 7 of the NE5037. When Pin 10 of the NE5037 goes low, conversion is complete and a low is applied to Pin 9 of the NE5037 to read data on Pins 11 through 16. Note that this temperature data is in straight binary format.

The controller can be a microprocessor in a temperature control application, or discrete circuitry in a simple temperature reporting application. A temperature reporting (digital thermometer) circuit is shown in Figure 3b. The NE5037 A/D converter is connected in a continuous conversion mode by connecting together Pins 7, 9, and 10. Should this pin be momentarily shorted to any relatively low impedance point, conversion will stop. Conversion will resume upon interruption and restoration of the power. These pins are also connected to the latch enable of a 6-bit latch because the data at the converter output is available for only a short time when the converter is in the continuous conversion mode. The (P)ROM) must have the correct code for converting the data from the NE5037 (used as address for the (P)ROMs) to the appropriate segment drive codes. Note that the circuit of Figure 3b shows a circuit which can be used to display either Fahrenheit or Centigrade temperatures.

The displayed output could easily be converted to degrees Fahrenheit (°F) by the controller of Figure 3a or through the (P)ROMs of Figure 3b. When doing this, a third (hundreds) digit (P)ROM and display will be needed for displaying temperatures above 99°F.

An inexpensive clock can be made from NAND gates or inverters, as shown in Figure 3c.

CIRCUIT ADJUSTMENT

The circuit should be at a known ambient temperature for a few minutes before making adjustments.

14. Adjust bias adjust potentiometer for the voltage indicated in the chart in Figure 3b.
15. With the circuit (or sensor U3, if it is remotely located) at a known temperature for 2 to 3 minutes, adjust range control for a correct reading on the displays.

This should provide an accuracy of ±3 counts (3° F or C). Higher accuracy may require NE5037 reference voltage regulation.