Voltage comparator

NE527

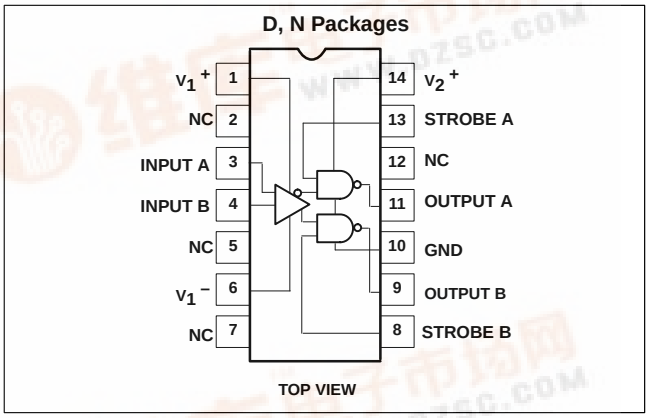
DESCRIPTION

The NE527 is a high-speed analog voltage comparator which, for the first time, mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed TTL gates with a precision linear amplifier on a single monolithic chip. The NE527 is similar in design to the Philips Semiconductors NE529 voltage comparator except that it incorporates an “Emitter-Follower” input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

FEATURES

- 15ns propagation delay
- Complementary output gates
- TTL or ECL compatible outputs
- Wide common-mode and differential voltage range
- Typical gain of 5000

PIN CONFIGURATIONS



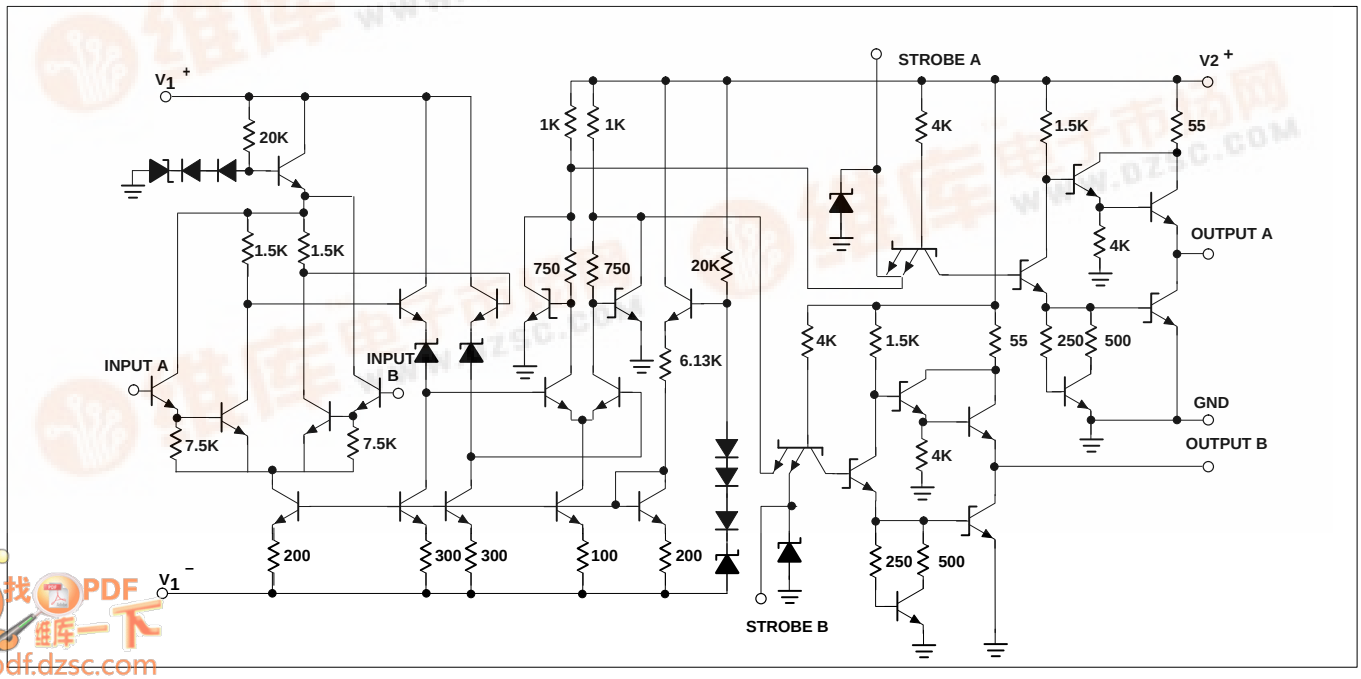
APPLICATIONS

- A/D conversion
- ECL-to-TTL interface
- TTL-to-ECL interface
- Memory sensing
- Optical data coupling

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
14-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE527N	0405B
14-Pin Small Outline (SO) Package	0 to +70°C	NE527D	0175D

EQUIVALENT SCHEMATIC

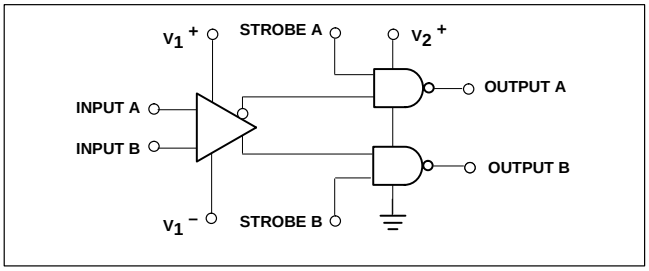


ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_1+	Positive supply voltage	+15	V
V_1-	Negative supply voltage	-15	V
V_2+	Gate supply voltage	+7	V
V_{OUT}	Output voltage	+7	V
V_{IN}	Differential input voltage	±5	V
V_{CM}	Input common mode voltage	±6	V
P_D	Max power dissipation[1] 25°C ambient (still air)		
	N package	1420	mW
	D package	1040	mW
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:
1. Derate above 25°C, at the following rates:
   N package 11.4mW/°C
   D package 8.3mW/°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V1+=10V, V1-=-10V, V2+=+5.0V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	NE527			UNIT
			Min	Typ	Max	
Input characteristics						
V_{OS}	Input offset voltage @ 25°C				6	mV
	over temperature range				10	
I_{BIAS}	Input bias current @ 25°C				2	µA
	over temperature range				4	
I_{OS}	Input offset current @ 25°C				0.75	µA
	over temperature range	V_{IN}=0V			1	µA
V_{CM}	Common-mode voltage range		-5		+5	V
Gate characteristics						
V_{OUT}	Output Voltage					
	"1" State	V_2+=4.75V, I_{SOURCE}=-1mA	2.7	3.3		V
	"0" State	V_2+=4.75V, I_{SINK}=10mA			0.5	V
	Strobe inputs					
	"0" Input current[1]	V_2+=5.25V, V_{STROBE}=0.5V			-2	mA
	"1" Input current @ 25°C[1]	V_2+=5.25V, V_{STROBE}=2.7V			100	µA
	Over temperature range	V_2+=5.25V, V_{STROBE}=2.7V			200	µA
	"0" Input voltage	V_2+=4.75V			0.8	V
	"1" Input voltage	V_2+=4.75V	2.0			V
I_{SC}	Short-circuit output current	V_2+=5.25V, V_{OUT}=0V	-18		-70	mA
Power supply requirements						
	Supply voltage					
V_1+			5		10	V
V_1-			-6		-10	V
V_2+			4.75	5	5.25	V
	Supply current	V_1+=10V, V_1-=-10V				
		V_2+=5.25V				
I_1+		Over temp.			5	mA
I_1-		Over temp.			10	mA
I_2+		Over temp.			20	mA

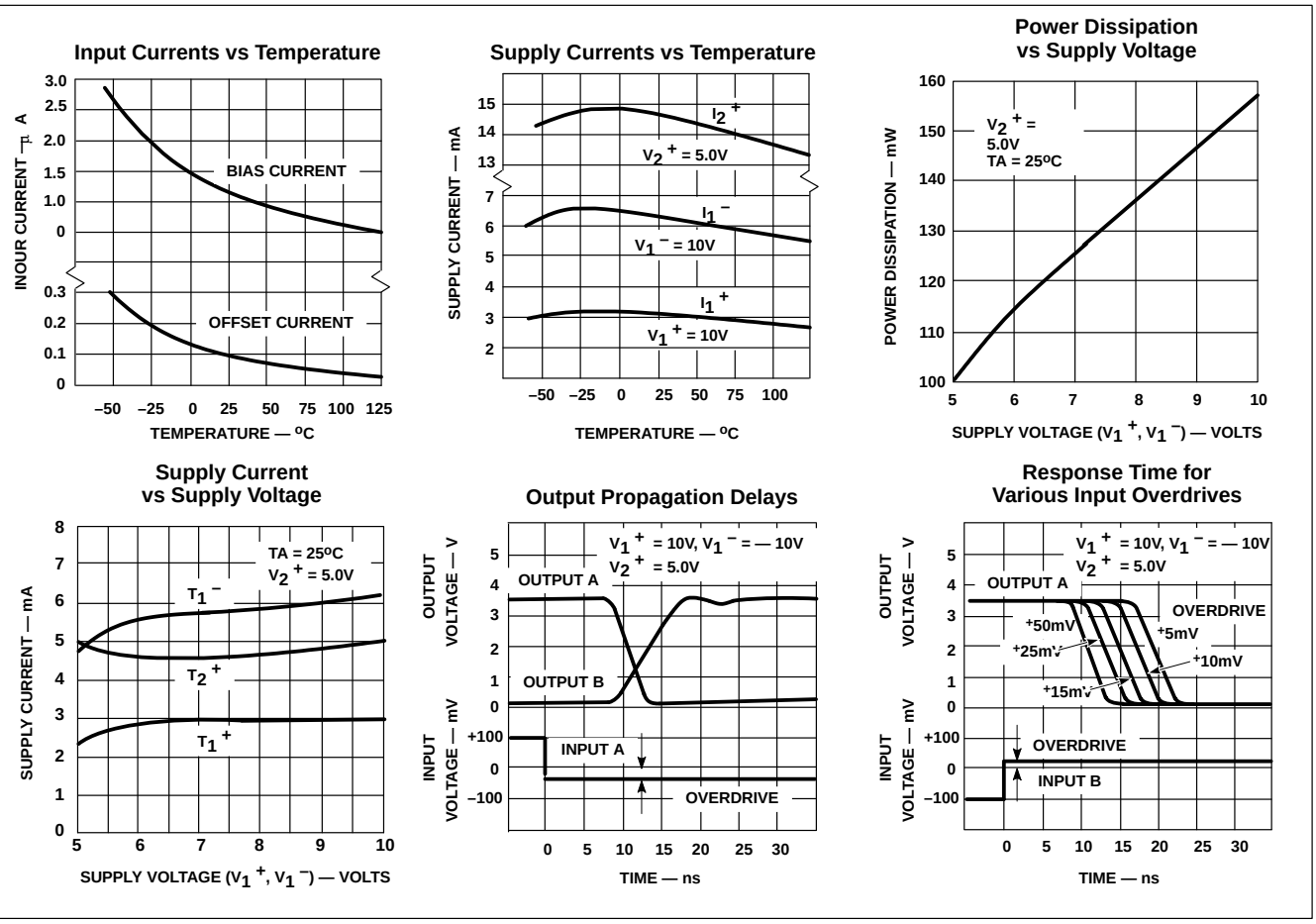
NOTES:
1. See Logic Function Table.

AC ELECTRICAL CHARACTERISTICS

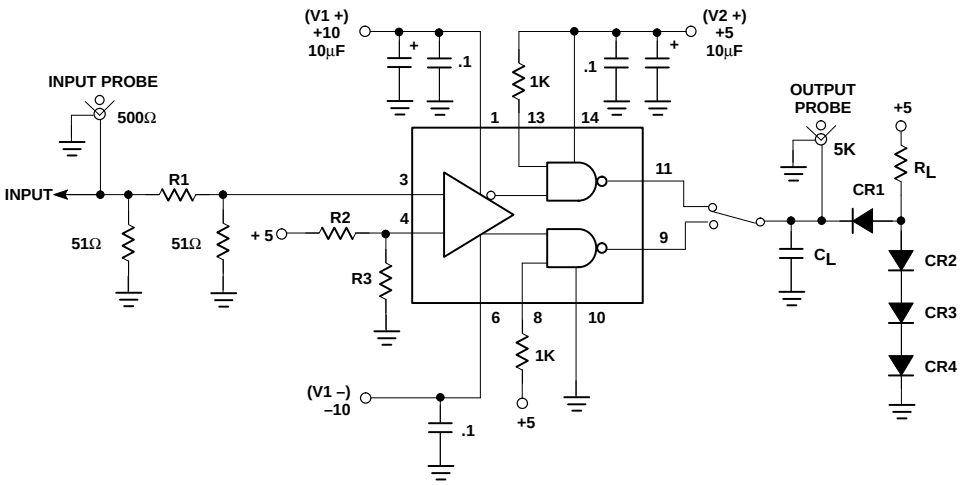
T_A=25°C, unless otherwise specified. (See AC test circuit)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Transient response propagation delay time					
t_{PLH}	Low-to-High	V_{IN}=±100mV step		16	26	ns
t_{PHL}	High-to-Low			14	24	ns
	Delay between output A and B			2	5	ns
	Strobe delay time					
t_{ON}	Turn-on time			6		ns
t_{OFF}	Turn-off time			6		ns

TYPICAL PERFORMANCE CHARACTERISTICS



RESPONSE TIME TEST CIRCUIT



NOTES:
CR1 — CR4 = IN914
R1 selected for 15.1 divider
R2, 3 selected for 100mV at Pin 4

Input
PRR = 1MHz
P_W = 50ns
$T_r = T_f$ = 2ns
Amplitude = 3.00V

Output
R_L = 390Ω
C_L = 25pF (including stray capacitance

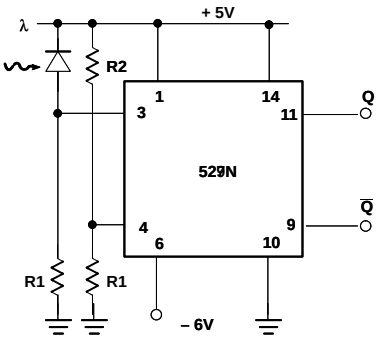
APPLICATIONS

One of the main features of the device is that supply voltages (V_1+, V_1-) need not be balanced, as in the following diagrams. For proper operation, however, negative supply (V_1-) should always be at least 6V more than the ground terminal (Pin 6). Input common-mode range should be limited to values of 2V less than the supply voltages (V_1+ and V_1-) up to a maximum of ±5V as supply voltages are increased. It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

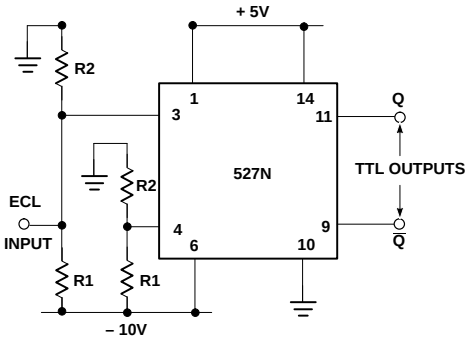
LOGIC FUNCTION

V_{ID} (A^+, B^-)	STROBE A	STROBE B	OUTPUT A	OUTPUT B	COMMENT
$V_{ID} \leq -V_{OS}$	H	X	L	H	Read I_{IHA}, I_{ILB}
$-V_{OS} < V_{ID} < V_{OS}$	H	H	Undefined	Undefined	
$V_{ID} \geq V_{OS}$	X	H	H	L	Read I_{ILA}, I_{IHB}
X	L	L	H	H	

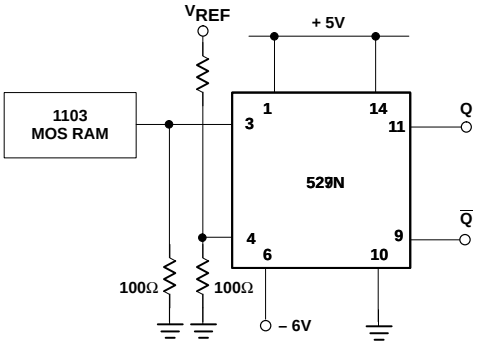
TYPICAL APPLICATIONS



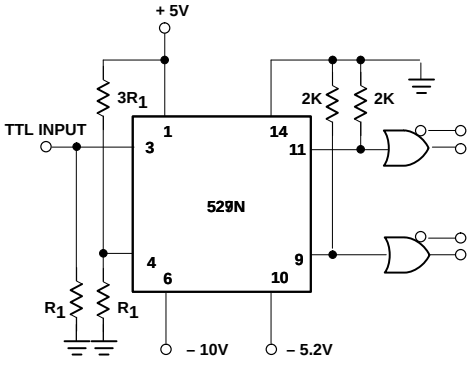
Photodiode Detector



ECL–to–TTL Interface



MOS Memory Sense AMP



TTL–to–ECL Interface