NIS6201

Product Preview

Floating, Regulated Charge Pump

The NIS6201 charge pump is designed to provide economical, low level power to circuits above ground level potential, such as the drive for ORing diodes. It is a very cost−effective replacement for a small, isolated, switching power supply.

It contains an internal linear regulator, and a versatile charge pump to allow bias voltage supplies to be transferred from a ground referenced source to a higher potential. The design of the charge pump allows for any isolation voltage required, as the high voltage components are external to the pump and can be sized accordingly.

Features

- Integrated Linear Regulator and Charge Pump
- Thermal Limit Protection
- Adjustable Voltage Output
- High Voltage Isolation

Applications

- ORing Diodes
- Floating Supervisory Circuits
- LED Driver

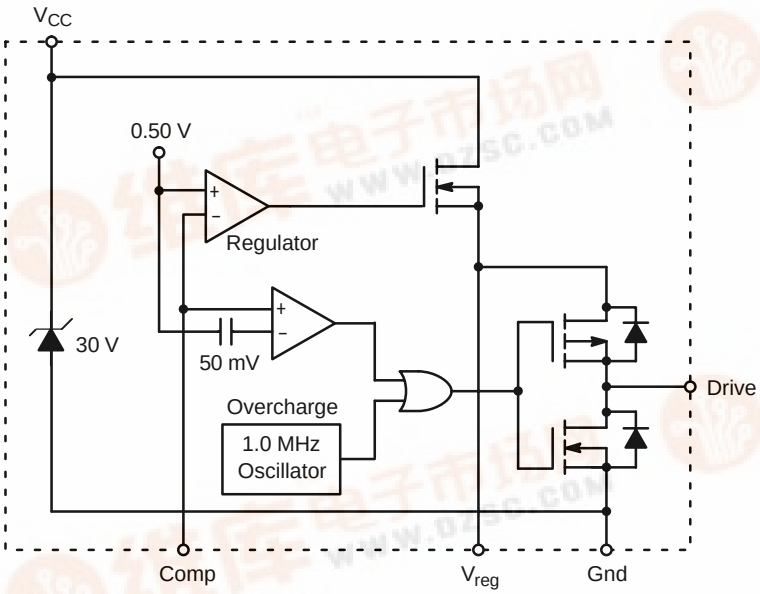

Figure 1. Charge Pump Block Diagram

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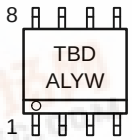
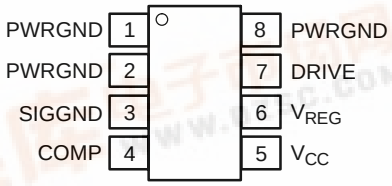
MARKING DIAGRAM

SOIC−8 NB
CASE 751



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
TBD	SOIC−8	TBD

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1, 2, 8	PWRGND	Ground reference pin for driver current.
3	SIGGND	Ground reference pin for control circuits. This should be connected to power ground on the PCB.
4	COMP	The feedback and compensation network of the linear regulator are connected to this pin.
5	V_{CC}	Input power to chip. There is an internal clamp at 30 V to allow for a shunt regulator circuit on this pin for high voltage inputs.
6	V_{REG}	This is the regulated output of the internal linear regulator.
7	DRIVE	Output drive of oscillator, that drives external diode/capacitor network.

MAXIMUM RATINGS (Maximum ratings are those, that, if exceeded, may cause damage to the device. Electrical Characteristics are not guaranteed over this range.)

Rating	Symbol	Value	Unit
Input Voltage, Operating	V_{CC}	−0.3 to 18	V
Drive Current, Peak	I_{Dpk}	3.0	A
Drive Current, Average	I_{Davg}	0.05	A
Thermal Resistance, Junction−to−Air 0.1 in^2 Copper 0.5 in^2 Copper	Q_{JA}	 − −	°C/W
Thermal Resistance, Junction−to−Lead (Pin 1)[2]	Q_{JL}	−	°C/W
Power Dissipation @ T_A = 25°C SO−8 Leadless	P_{max}	−	W
Energy Rating SO−8 Leadless	E_{max}	−	J
Operating Temperature Range	T_j	−40 to 125	°C
Non−operating Temperature Range	T_j	−55 to 150	°C
Lead Temperature, Soldering (?? Sec)	T_L	−	°C

ELECTRICAL CHARACTERISTICS (Unless otherwise noted: V_{CC} = 15 V, V_{reg} = 12 V, T_j = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
OSCILLATOR					
Frequency	f_{osc}	0.9	1.0	1.1	MHz
DRIVER					
On Resistance, High Side FET	$R_{DSon(hi)}$	−	20	−	Ω
On Resistance, Low Side FET	$R_{DSon(low)}$	−	20	−	Ω
LINEAR REGULATOR					
Reference Voltage	V_{ref}	490	500	510	mV
Temperature Coefficient	−	−	−	−	−
Headroom (V_{CC}–V_{reg})	V_{head}	−	0	−	V
Sink Current (Vpin? ≤ 300 mV, Low Z State)	I_{Low}	−	5.0	−	mA
Leakage Current (Vpin? = 18 V, High Z State)	I_{Leak}	−	20	−	μA
TOTAL DEVICE					
Minimum Operational Input Voltage	V_{min}	7.0	−	−	V
Bias Current (Operational)	I_{Bias}	−	2.0	−	mA

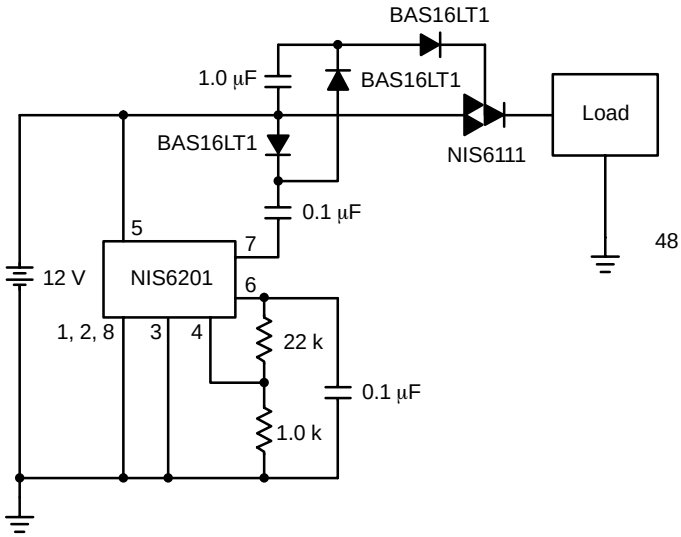


Figure 2. Application Circuit with Better ORing Diode

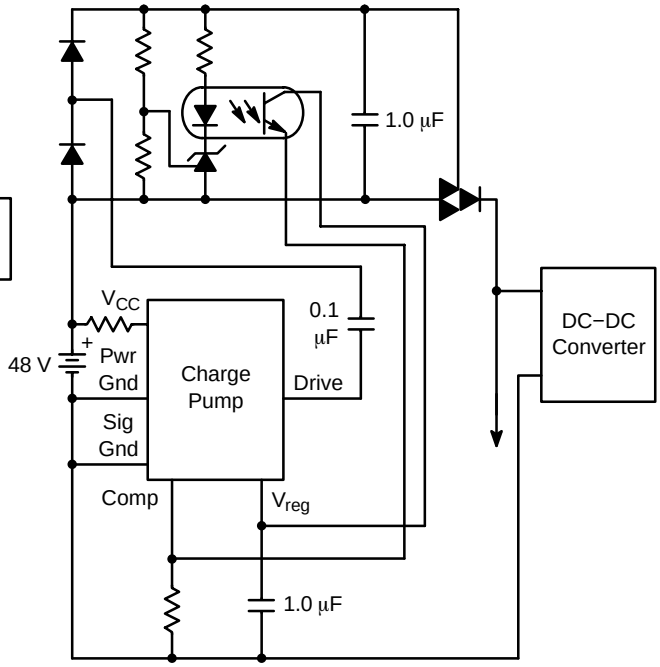


Figure 3. Application Circuit for Improved Regulation and Transient Response

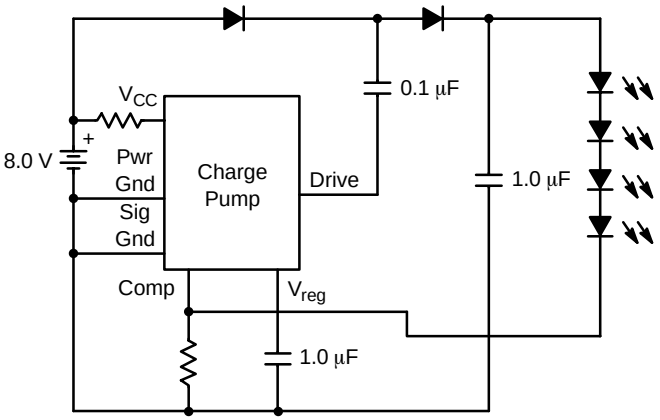
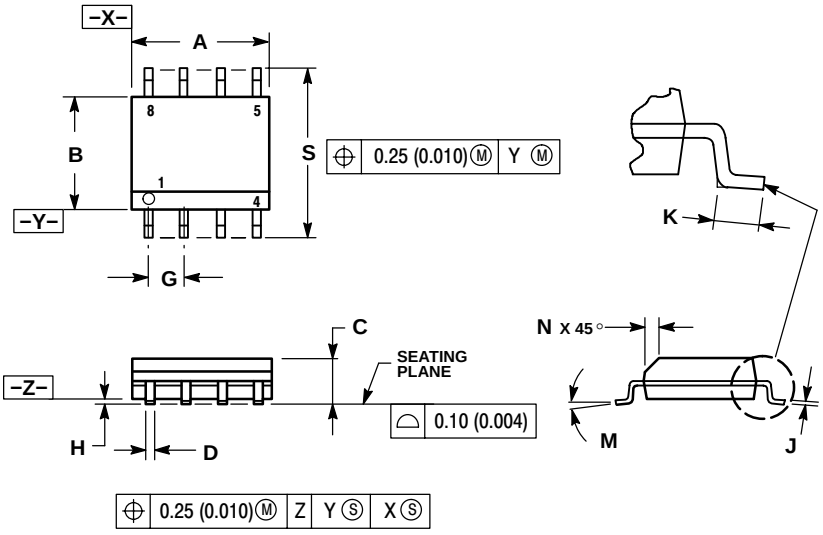


Figure 4. Current Regulated, Voltage Doubler

NIS6201

PACKAGE DIMENSIONS

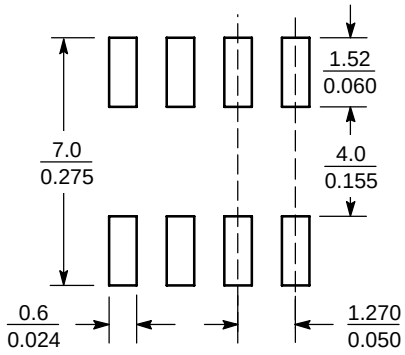
SOIC−8 NB
CASE 751−07
ISSUE AB



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
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