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# NJ8811

## CONTROL CIRCUIT FOR FREQUENCY SYNTHESIS

The NJ8811 is an N-channel MOS integrated circuit that provides all the decoding and controlling circuitry for frequency synthesisers. It is intended to be used in conjunction with a 4-modulus prescaler such as the SP8901 or SP8906 to produce a universal binary coded synthesiser for mobile radio applications.

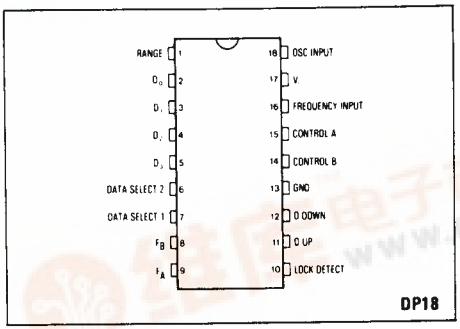


*Fig.1 Pin connections*

### FEATURES

- High Frequency Range
- Low Pin Count
- Direct Interface to ROM or PROMS
- Preset Channel Spacings 40, 50, 60 kHz and Sub-multiples.
- High Comparison Frequency.
- Low Level Sinewave Crystal Oscillator Input up to 10 MHz.
- Systems Clock Available — Constant Data Select Frequency of 1.2 kHz. (Reference Oscillator = 4.8 MHz)
- Microprocessor Compatible.

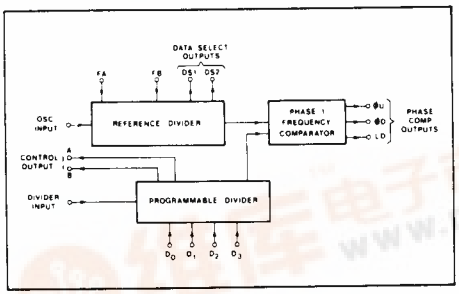


*Fig.2 NJ8811 block diagram*

### GENERAL DESCRIPTION

The NJ8811 can be described by 3 system blocks: the reference divider, the programmable divider and the phase/frequency comparator, as shown in Fig.2. All control inputs and outputs are TTL compatible.

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_S$: 5.0V ±0.25V
Temperature range: -30°C to +70°C

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min | Typ. | Max | | |
| Oscillator input | 50 | | 200 | mV RMS | 4.8 MHz reference oscillator AC coupled sinewave FA, FB O/C. |
| Max. oscillator input frequency | 10 | | | MHz | 200 mV RMS sinewave. |
| Supply current | | 8.0 | 12 | mA | All data inputs O/C. |
| Max. counter input frequency | 2.5 | | | MHz | Input TTL compatible. |
| DS1/DS2 Output High Level | 2.4 | | | V | Outputs TTL compatible. |
| Low Level | | | 0.4 | V | |
| Phase comparator output current sink | 1 | | | mA | $Ø_U Ø_D$ 0.5V max. |

**The Reference Divider**

The reference divider is driven externally from a 4.8MHz crystal oscillator and can be externally preset to one of sixteen division ratios. These division ratios enable all commonly used reference frequencies to be applied to the phase/frequency comparator. Selection is accomplished using the two pins FA and FB. These pins may be connected to ground (logic '0') or left open circuit (logic '1'), connected to Data Select 1 output or to Data Select 2 output. On-chip decoding enables the latter two states to be recognised as independent states. All sixteen selections may be latched on-chip by grounding the Data Select 2 output. Table 1 gives reference frequencies that can be preset using a 4.8MHz crystal oscillator.

The data select outputs (crystal oscillator frequency ÷4096) are independent of the preset reference frequency.

**Programmable Divider**

The programmable division section of the NJ8811 consists of two 4-bit programmable dividers and an 8-bit programmable divider. The 4-bit dividers control the modulus of the external prescaler and the 8-bit counter determines the total count period. The SP8906/NJ8811 combination is capable of dividing by all integer values between 3840 and 69,375. When the Range pin on the NJ8811 is grounded the programme range is shifted to between 36,608 and 102,143.

The programming data is multiplexed as 4 words of 4 bits, completing a 16 bit binary number. This input data may be stored on-chip by grounding the Data Select 2 output after internal data transfer has occurred (See Fig.4). All on-chip multiplexing may then be inhibited, if desired, by grounding Data Select 1 output.

**Phase/Frequency Comparator**

The outputs of the fixed and variable dividers on the NJ8811 are internally connected to a phase/frequency comparator. The comparator provides three open drain outputs. The logic diagram is shown in Fig.3.

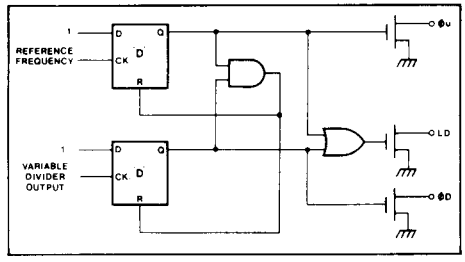


*Fig.3 Logic diagram of phase frequency comparator*

**Data Selection**

To programme the synthesiser the following information is required:

1. The reference comparison frequency—equal to the channel spacing when using the SP8906, or half when using the SP8901.
2. The frequency of the VCO.

The frequency programme information is presented to the device in multiplexed form of 4 word of 4 bits. The reading of this data by the device is controlled by the two data select outputs from the device. This sequence is shown in Fig.4.

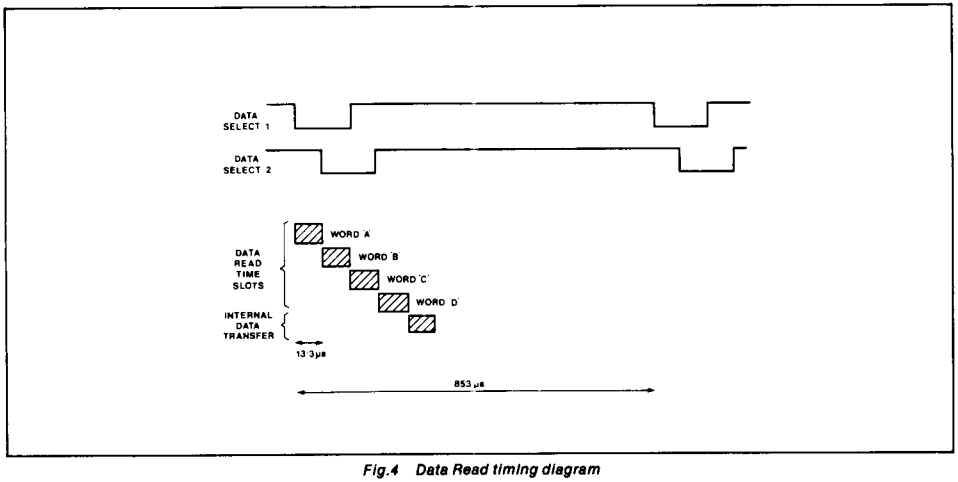


*Fig.4 Data Read timing diagram*

| FA / FB | GND | O/C | DS1 | DS2 |
|---|---|---|---|---|
| Gnd | 20 | 10 | 5 | 2.5 |
| O/C | 25 | 12.5 | 6.25 | 3.125 |
| DS1 | 30 | 15 | 7.5 | 3.75 |
| DS2 | 37.5 | 18.75 | 9.375 | 4.6875 |

*Table 1 Reference frequency selection (all frequencies in kHz)*

Table 2 shows the VCO frequency programme range that can be obtained using NJ8811 and SP8901.

| Channel Spacing | 40kHz | 50kHz | 60kHz |
|---|---|---|---|
| Low Range (MHz) | 153.6—(1000) | 192.0—(1000) | 230.4—(1000) |
| High Range (MHz) | | | |

| Channel Spacing | 20kHz | 25kHz | 30kHz |
|---|---|---|---|
| Low Range (MHz) | 76.8—(1000) | 96.0—(1000) | 115.2—(1000) |
| High Range (MHz) | 732.2—(1000) | 915.2—(1000) | |

| Channel Spacing | 10kHz | 12.5kHz | 15kHz |
|---|---|---|---|
| Low Range (MHz) | 38.4— 693.8 | 48.0— 867.2 | 57.6—(1000) |
| High Range (MHz) | 366.2—(1000) | 457.6—(1000) | 549.2—(1000) |

| Channel Spacing | 5kHz | 6.25kHz | 7.5kHz |
|---|---|---|---|
| Low Range (MHz) | 19.2— 347.0 | 24.0— 433.6 | 28.8— 520.6 |
| High Range (MHz) | 183.0— 510.8 | 228.8— 638.4 | 274.6— 766 |

*Table 2 Frequency programme range for SP8901 (with 4.800MHz crystal)*

Table 3 shows the VCO frequency programme range that can be obtained using NJ8811 and SP8906.

| Channel Spacing | 20kHz | 25kHz | 30kHz |
|---|---|---|---|
| Low Range (MHz) | 76.8—(500) | 96.0—(500) | 115.2—(500) |
| High Range (MHz) | | | |

| Channel Spacing | 10kHz | 12.5kHz | 15kHz |
|---|---|---|---|
| Low Range (MHz) | 38.4—(500) | 48.0—(500) | 57.6—(500) |
| High Range (MHz) | 366.1—(500) | 457.6—(500) | |

| Channel Spacing | 5kHz | 6.25kHz | 7.5kHz |
|---|---|---|---|
| Low Range (MHz) | 19.2—346.9 | 24.0—433.6 | 28.8—(500) |
| High Range (MHz) | 183.1—(500) | 228.8—(500) | 274.6—(500) |

| Channel Spacing | 2.5kHz | 3.125kHz | 3.75kHz |
|---|---|---|---|
| Low Range (MHz) | 9.6—173.5 | 12.0—216.8 | 14.4—260.2 |
| High Range (MHz) | 91.5—255.4 | 114.4—319.2 | 137.3—383.0 |

*Table 3 Frequency programme range for SP8906 (with 4.800MHz crystal)*

To calculate the Programme number for a given VCO frequency and channel spacing the following equation is used:

$$\text{Programme Number } N = \frac{1000 \times f}{C} - R$$

where f = VCO frequency in MHz
C = channel spacing in kHz
R = range number (R = 3840 range = 1)
(R = 36608 range = 0)

The programme number is converted to a 16 bit binary number and is segregated as 4 words of 4 bits.

The least significant word is first entered during the Data Read 1 time slot via the inputs $D_3$, $D_2$, $D_1$ and $D_0$ and the most significant last (Data Read 4 time slot).

For example, with a VCO frequency of 437MHz and channel spacing of 12.5kHz

f = 437
C = 12.5
R = 3840
N = 31120

Conversion to a 16 bit binary number is performed as follows:

| | Result |
|---|---|
| 1. Divide by 4096 | 7.5977 |
| 2. Write down the number before decimal place (WORD 'D') | 7 |
| 3. Subtract this number | 0.5977 |
| 4. Multiply by 16 | 9.5625 |
| 5. Write down the number before decimal place (WORD 'C') | 9 |
| 6. Subtract this number | 0.5625 |
| 7. Multiply by 16 | 9.0000 |
| 8. Write down the number before decimal place (WORD 'B') | 9 |
| 9. Subtract this number | 0 |
| 10. Multiply by 16 | 0 |
| 11. Write down nearest whole number (WORD 'A') | 0 |

The four decimal numbers obtained may now be directly converted to binary, and these are presented to the data inputs as shown in Table 4.

| DS1 | DS2 | $D_3$ | $D_2$ | $D_1$ | $D_0$ | |
|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 0 | 0 | WORD 'A' |
| 0 | 0 | 1 | 0 | 0 | 1 | WORD 'B' |
| 1 | 0 | 1 | 0 | 0 | 1 | WORD 'C' |
| 1 | 1 | 0 | 1 | 1 | 1 | WORD 'D' |

*Table 4*

The data may be latched internally by grounding the DS2 output. This is useful when interfacing to a microprocessor. The NJ8811 is also compatible with most types of PROM and ROM for data coding applications.

**APPLICATION NOTES**

The NJ8811 is designed for use in phase locked loop frequency synthesisers. In these synthesisers, the voltage controlled oscillator (VCO) operates at the output frequency and the output frequency is divided down to a reference frequency. Another signal at this reference frequency is derived from the crystal controlled reference oscillator, and the divided VCO signal is compared at this frequency with the reference signal in a phase and frequency comparator. The output signal derived from this comparison consists of short pulses whose mark-space ratio is such that when the pulses are integrated, a DC level is obtained, which, when applied to the VCO, locks the loop by maintaining the VCO on frequency.

Simple division to the reference frequency in a fully programmable divider is limited to frequencies of about 50MHz and below, because of the difficulty of producing fully programmable dividers.

One answer to this is to use a prescaler as in Fig.5.

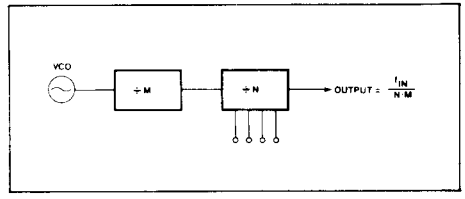


*Fig.5 Use of prescaler*

However, for any step in frequency Δf at the VCO, the change at the phase detector is Δf/N.M; if this step is caused by a change of M to M+1 then Δf must become Δf/N.(M+1) at the phase detector. Since the reference frequency is constant, the step at the VCO is therefore N times the reference frequency; this places limitations on the reference frequency value. For ease of filtering it is necessary to use as high a reference frequency as possible, preferably equal to the channel spacing.

To avoid the difficulties in simple prescaling two-modulus division may be used. In this system, the prescaler division ratio is altered from N to N+1: and while this is a very powerful method of achieving the necessary division, it is limited where very wide frequency ranges are required. This technique however may be applied by using four-modulus division as in Fig.6.

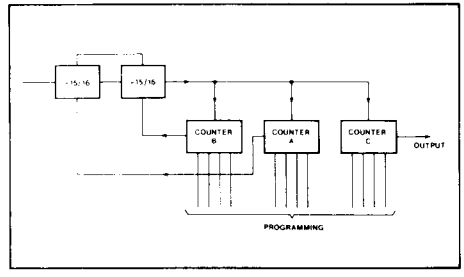


*Fig.6 Use of four-modulus divider*

In this system, the four-modulus counter can have a division ratio of 256, 255, 240 or 239. If the 'A' counter is programmed to a lower number than the 'B' counter, the system works as follows.

The 4 modulus prescaler divides by 239 'A' times, then by 240 until the 'B' counter is full and then by 256 until the 'C' counter is full. Thus the ratio is:

$$239A + 240(B - A) + 256(C - B)$$

If the 'A' counter is programmed to a higher number than the 'B' counter, then the system operation is:

Divide by 239 until the 'B' counter is full (i.e. 'B' times) then by 255 until the 'A' counter is full, then by 256 until the 'C' counter is full. The ratio is then:

$$239B + 255(A - B) + 256(C - A)$$

Both of these expressions simplify to:

$$256C - 16B - A$$

The limits are C = 16, B = 15, A = 16

and C = 271, B = 0, A = 1

Thus the minimum and maximum counts are 3840 and 69375. When the Range input is used on the NJ8811, this is modified such that the count is from 36,608 to 102,143.

A four-modulus-divider for use to 500MHz is the SP8906, which interfaces directly with the NJ8811. The SP8901 has a ÷2 prescaler preceding the four-modulus divider, which thus enables direct synthesis at frequencies up to 1GHz to be attained.

**Phase Detector**

In the NJ8811, this circuit function is implemented by the use of two D type flip-flops. These drive 'open drain' output FETs, and if these are taken to $V_S$ via resistors, waveforms as shown in Fig.7 may be expected.

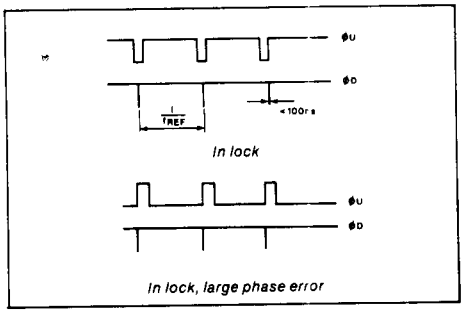


*Fig.7 Phase detector waveforms*

When out of lock, $Ø_D$ and $Ø_U$ have no definite phase relationship. These outputs, may be combined in a suitable circuit, as shown in Fig.8.

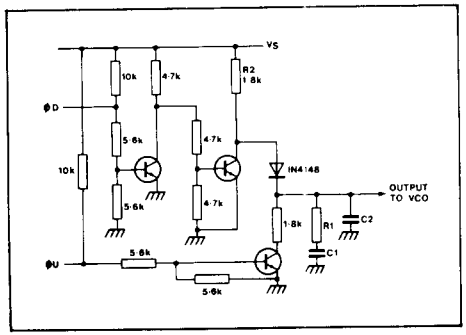


*Fig.8 Circuit for combining $Ø_D$ and $Ø_U$*

**Loop Filter Design**

A simple approach will provide a workable, but not necessarily optimum system. For more detailed methods, reference to one of the many textbooks is recommended. The following method provides a simple design.

1. Choose the loop natural frequency $\omega_n$. This frequency affects the settling time of the loop, and this settling time is, to a first order approximation, $10/\omega_n$, where $\omega_n$ is in radians per second.
2. Choose a value of damping factor to give adequate loop stability without excessive overshoot. A satisfactory value is 1.0, giving an overshoot of approximately 10%.
3. **Determine:**
   KV = VCO Gain in rads/Volt-sec
   = 2π x Hz/V
   where Hz/V is the deviation in Hz for 1 volt change on the control line.
   N = VCO frequency/Reference Frequency.
4. Choose $R_2$. For convenience, $4.7k\Omega > R_2 > 470\Omega$
   $C_1 = \frac{KV}{2\pi N \omega_n^2 R_2}$
5. $R_1 = D/\omega_n C_1$ where D is the damping factor.
6. $C_2 = \frac{1}{15\omega_n R_1}$

**Reference Oscillator Requirements**

Because the frequency synthesiser effectively multiplies the reference oscillator to the working frequency, any variations or inaccuracies in the reference oscillator appear at the output. For this reason, the accuracy of the reference oscillator must be no worse than that of the signal which it is required to synthesise, while the signal-to-noise ratio must be as high as possible. Incidental FM must be minimised.

**VCO Requirements**

The VCO should cover the frequency range desired with a suitable control line voltage swing. In addition, its power level and Q should be such as to maintain phase noise sidebands as low as is required. It is frequently found that the high impedance control line is very susceptible to picking up stray signals; screening and careful decoupling of the VCO and its supplies is often necessary. Buffering between the VCO and the prescaler is required to prevent VCO modulation from this source, and dual gate MOSFETS are very useful in this position.

**A Typical Synthesiser**

Fig.10 shows a frequency synthesiser using the SP8906 and NJ8811. In this form, it is suitable for use up to 500MHz, although the MOSFET buffer stage could be improved at frequencies above 300MHz. For use up to 1GHz, the SP8906 should be replaced with the SP8901, the MOSFET buffer replaced and the reference frequency set to half the channel spacing.

Care should be taken to ensure that the screening, filtering and buffering of the VCO is adequate, otherwise it may be found that spurious sidebands exist at the output of the VCO.

Programming is achieved by using the Frequency Synthesiser Binary Programming Circuit as in Fig. 9, or a suitable ROM, PROM or microprocessor.

The RF Choke feeding pins 1 and 2 of the SP8906 ensures stability under conditions of dynamic modulus change. This synthesiser has been demonstrated operating under 25kHz channelling at 156MHz with reference frequency sidebands more than 90dB down. For this level of performance careful construction is required to avoid spurious pick-up. The LED (pin 10) lights to indicate an out of lock condition.

For further applications information see AN1006.

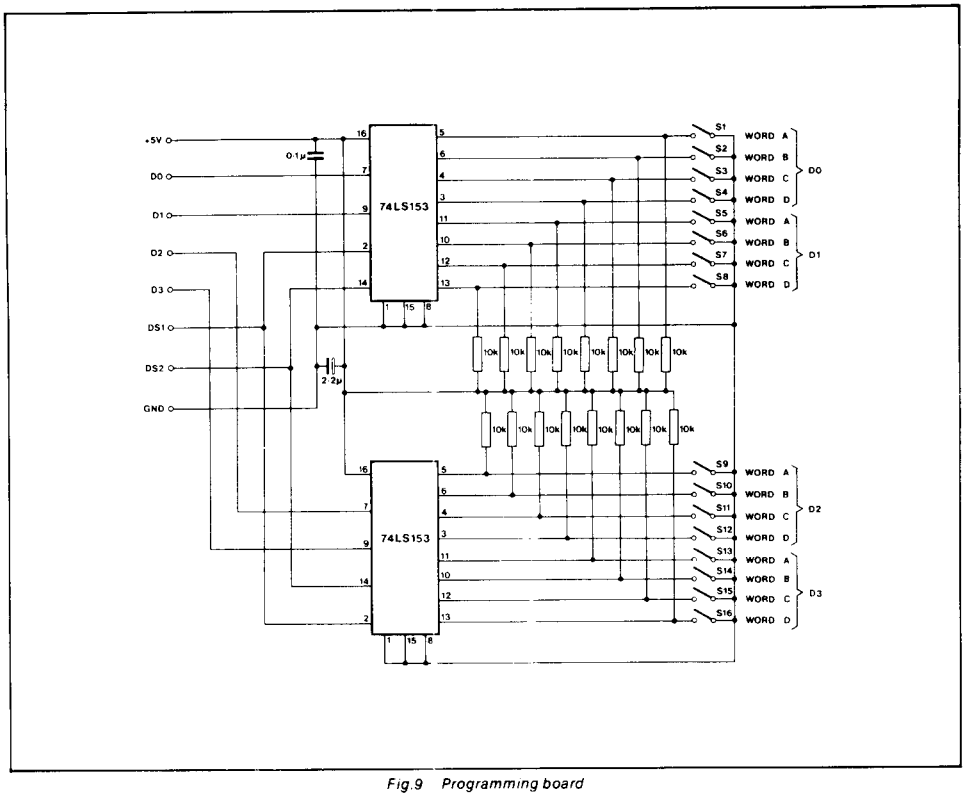


*Fig.9 Programming board*

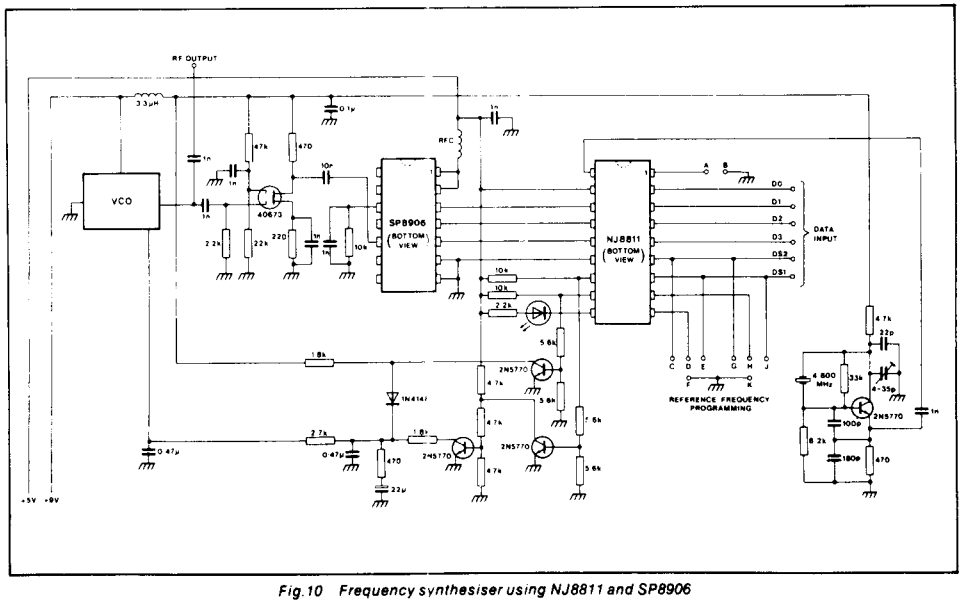


*Fig.10 Frequency synthesiser using NJ8811 and SP8906*