

## SYSTEM RESET IC

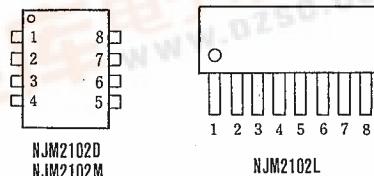
### ■ GENERAL DESCRIPTION

The NJM2102 Possesses two functions. One is to detect a voltage which decays from the desired voltage and generate a warning signal. And also, the NJM2102 holds the warning signal for a certain term after the specified voltage is obtained or recovered. The other one (Watch Dog Timer) is to identify missing clocks of microprocessors. Therefore, it should be said that the NJM2102 is ideal to protect any microprocessors from the fales operations induced by undesired condition.

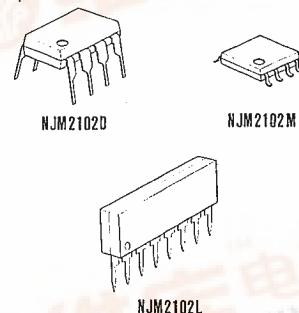
### ■ FEATURES

- Internal Watch Dog Timer
- Precise Detection of Supply Voltage Down ( $4.2V \pm 2.5\%$ )
- Package Outline DIP8, DMP8, SIP8
- Bipolar Technology

### ■ PIN CONFIGURATION



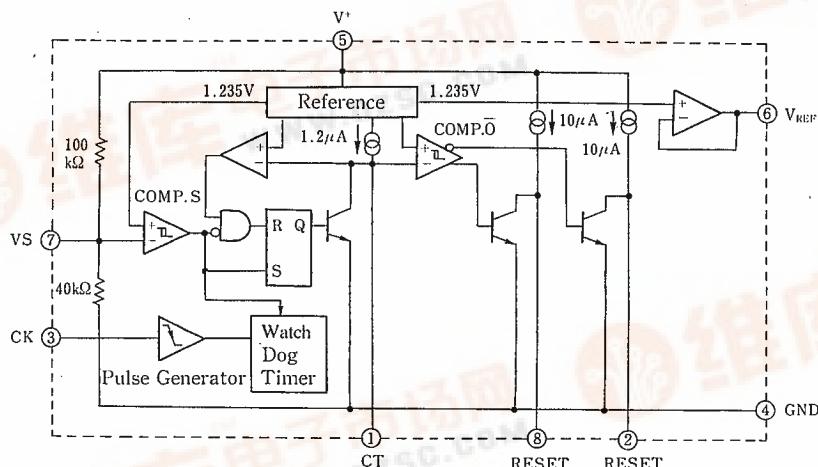
### ■ PACKAGE OUTLINE



### PIN FUNCTION

1. CT
2. RESET
3. CK
4. GND
5. V<sup>+</sup>
6. V<sub>REF</sub>
7. V<sub>S</sub>
8. RESET

### ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sup>+</sup>	13.5	V
Input Voltage	V <sub>S</sub>	V <sup>+</sup> +0.3(<20)	V
Input Voltage	V <sub>CK</sub>	20	V
Power Dissipation	P <sub>D</sub>	(DIP8) 500 (SIP8) 600 (DMP8) 300	mW
Operating Temperature Range	T <sub>opr</sub>	-40~+85	°C
Storage Temperature Range	T <sub>stg</sub>	-40~+125	°C

## ■ ELECTRICAL CHARACTERISTICS

(V<sup>+</sup>=5V, Ta=25°C)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current	I <sub>cc</sub>	Full Function	—	0.65	1.00	mA
Threshold Voltage 1	V <sub>SL</sub>	Falling Down Input	4.10	4.20	4.30	V
Threshold Voltage 2	V <sub>SH</sub>	Rising Up Input	4.20	4.30	4.40	V
Hysteresis Width	V <sub>HYS</sub>	V <sub>SL</sub> -V <sub>SH</sub>	50	100	150	mV
Reference Voltage	V <sub>RFF</sub>		1.217	1.235	1.253	V
Operating Voltage Regulation	ΔV <sub>REF1</sub>	V <sub>CC</sub> =3.5V~18V	-10	+3	+10	mV
Load Regulation	ΔV <sub>REF2</sub>	I <sub>OUT</sub> =-200μA~-+5μA	-5	—	+5	mV
CK Input Threshold Voltage	V <sub>TH</sub>		0.70	1.24	1.90	V
CK Input Current 1	I <sub>IH</sub>	V <sub>CK</sub> =5.0V	—	0	1.0	μA
CK Input Current 2	I <sub>IL</sub>	V <sub>CK</sub> =0.0V	-1.0	-0.1	—	μA
C <sub>T</sub> Charge Current 1	I <sub>CTC1</sub>	(Note 1)	20	50	110	μA
C <sub>T</sub> Charge Current 2	I <sub>CTC2</sub>	V <sub>CK</sub> =0.0V	0.6	1.4	3.0	μA
Capacitor Discharge Current 1	I <sub>CTD1</sub>	(Note 1)	6	9	13	μA
Capacitor Discharge Current 2	I <sub>CTD2</sub>	V <sub>CK</sub> =0.0V	100	600	—	μA
Output Voltage (High) 1	V <sub>OH1</sub>	V <sub>S</sub> =Open, I <sub>RESET</sub> =-5μA	4.5	4.9	—	V
Output Voltage (High) 2	V <sub>OH2</sub>	V <sub>S</sub> =0V, I <sub>RESET</sub> =-5μA	4.5	4.9	—	V
Output Voltage (Low) 1	V <sub>OL1</sub>	V <sub>S</sub> =0V, I <sub>RESET</sub> =3mA	—	0.2	0.4	V
Output Voltage (Low) 2	V <sub>OL2</sub>	V <sub>S</sub> =0V, I <sub>RESET</sub> =10mA	—	0.3	0.5	V
Output Voltage (Low) 3	V <sub>OL3</sub>	V <sub>S</sub> =Open, I <sub>RESET</sub> =3mA	—	0.2	0.4	V
Output Voltage (Low) 4	V <sub>OL4</sub>	V <sub>S</sub> =Open, I <sub>RESET</sub> =10mA	—	0.3	0.5	V
Output Sink Current 1	I <sub>OL1</sub>	V <sub>S</sub> =0V V <sub>RESET</sub> =1.0V	20	70	—	mA
Output Sink Current 2	I <sub>OL2</sub>	V <sub>S</sub> =Open, V <sub>RESET</sub> =1.0V	20	70	—	mA
Minimum Operating Voltage 1	V <sub>CCLI</sub>	V <sub>RESET</sub> =0.4V, I <sub>RESET</sub> =0.2mA	—	0.8	1.2	V
Minimum Operating Voltage 2	V <sub>CCL2</sub>	V <sub>RESET</sub> =V <sup>+</sup> -0.1V, R <sub>L</sub> =1MΩ	—	0.8	1.2	V

## AC CHARACTERISTICS

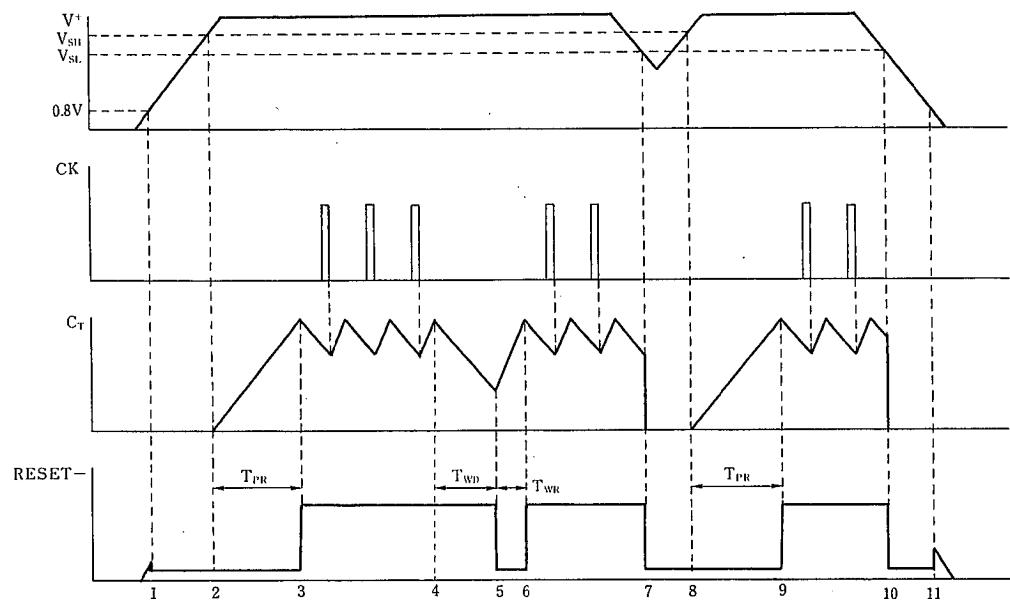
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	
V <sup>+</sup> Input Pulse Width	T <sub>PI</sub>	V <sub>CC</sub> 5V 4V	(Note 2)	—	10	—	μS
CK Input Pulse Width	T <sub>CKW</sub>	CK □ or □	(Note 2)	—	1.8	—	μS
CK Input Period	T <sub>CK</sub>		(Note 2)	—	12	—	μS
Watch Dog Timer	T <sub>WD</sub>	C <sub>T</sub> =0.1μF	—	—	10	—	μS
Warning Threshold Time							
Watch Dog Timer Reset Pulse Width	T <sub>WR</sub>	C <sub>T</sub> =0.1μF	—	—	2	—	μS
Reset Signal Hold Time	T <sub>PR</sub>	C <sub>T</sub> =0.1μF	—	—	100	—	μS
Propagation Delay (RESET Terminal)	T <sub>PD1</sub>	R <sub>L</sub> =2.2kΩ, C <sub>L</sub> =100pF	—	—	2	—	μS
(SET Terminal)	T <sub>PD2</sub>	R <sub>L</sub> =2.2kΩ, C <sub>L</sub> =100pF	—	—	3	—	μS
Output Rise Time	t <sub>R</sub>	R <sub>L</sub> =2.2kΩ, C <sub>L</sub> =100pF	—	—	1.0	—	μS
Output Fall Time	t <sub>F</sub>	R <sub>L</sub> =2.2kΩ, C <sub>L</sub> =100pF	—	—	0.1	—	μS

(Note1) : The specified pulses (Refer to AC Characteristics) are applied to CK-pin.

(Note2) : This characteristics is guaranteed within the design.

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## ■ TIMING CHART

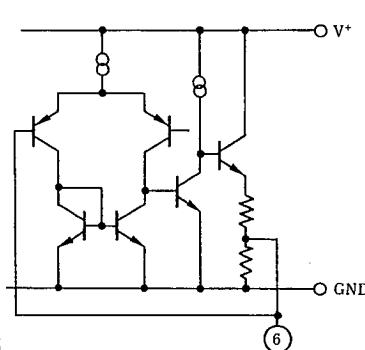
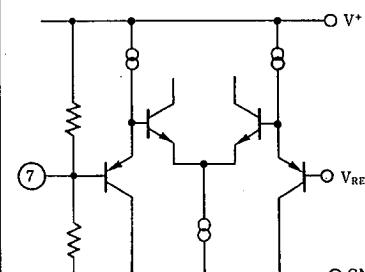
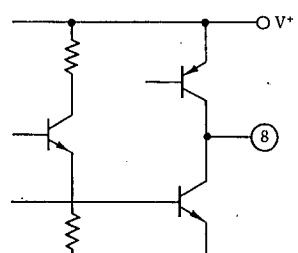


**■ TERMINAL FUNCTION**

PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
1	$C_T$	Pin Connection to Capacitor, Set the reset holding time	 The circuit diagram for Pin 1 shows a reference voltage source $V_{REF}$ connected to one terminal of a capacitor. The other terminal of the capacitor is connected to the base of a PNP transistor. The collector of this transistor is connected to the base of another PNP transistor. The collector of the second PNP transistor is connected to ground (GND). The base of the second PNP transistor is also connected to the collector of the first PNP transistor. A resistor is connected between the collector of the second PNP transistor and $V_{REF}$ . The entire circuit is powered by $V_{CC}$ .
2	RESET	Reset Output	 The circuit diagram for Pin 2 shows a reset output stage. It consists of two NPN transistors. The base of the first NPN transistor is connected to a resistor and ground. The collector of the first NPN transistor is connected to the base of the second NPN transistor. The collector of the second NPN transistor is connected to $V^+$ and ground. The entire circuit is powered by $V^+$ .
3	CK	Clock Input	 The circuit diagram for Pin 3 shows a clock input stage. It consists of three NPN transistors. The base of the first NPN transistor is connected to a resistor and ground. The collector of the first NPN transistor is connected to the base of the second NPN transistor. The collector of the second NPN transistor is connected to the base of the third NPN transistor. The collector of the third NPN transistor is connected to $V^+$ and ground. The entire circuit is powered by $V^+$ . A 'Delay Circuit' is indicated between the collector of the second NPN transistor and the collector of the third NPN transistor.

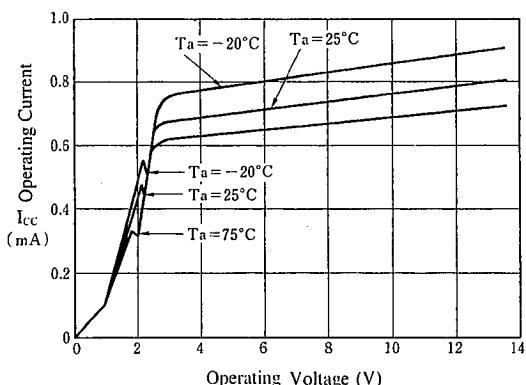
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## ■ TERMINAL FUNCTION

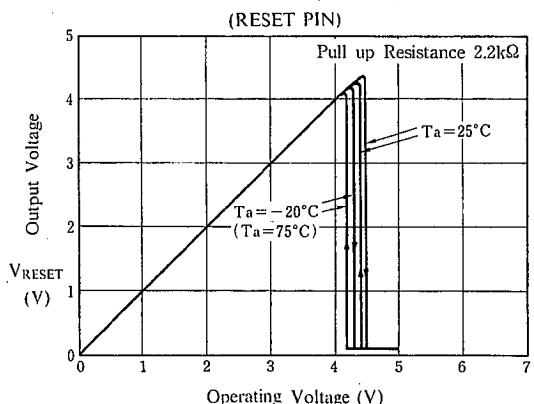
PIN NO.	SYMBOL	FUNCTION	INSIDE EQUIVALENT CIRCUIT
4	GND	Ground	
5	V <sup>+</sup>	Operating Voltage	
6	V <sub>REF</sub>	Ref Amp Output	
7	V <sub>s</sub>	Comparator S Input	
8	RESET	Reset Output Internal pull up resistor	

## ■ TYPICAL CHARACTERISTICS

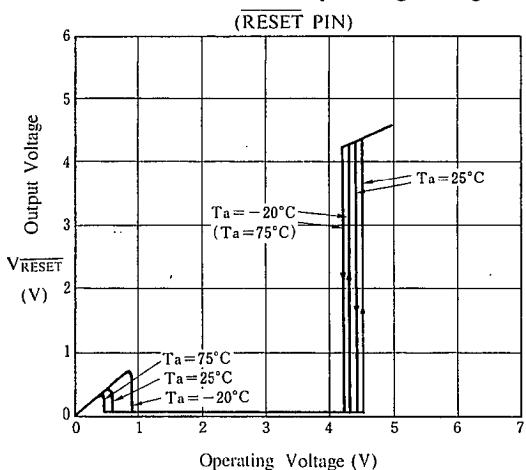
### Operating Current vs. Operating Voltage



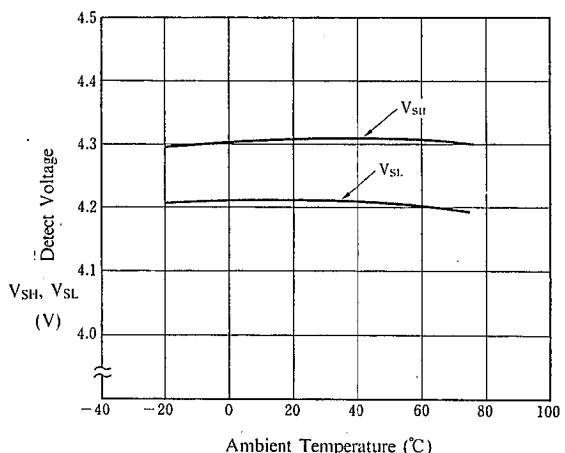
### Output Voltage vs. Operating Voltage



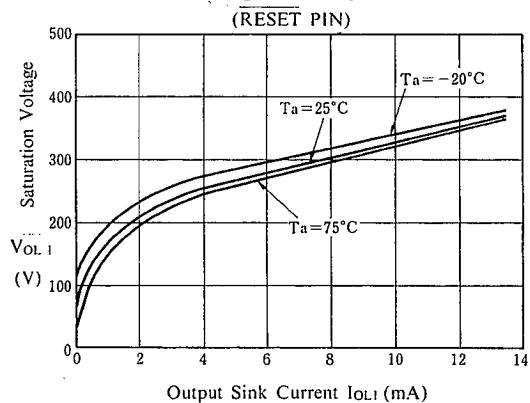
### Output Voltage vs. Operating Voltage (RESET PIN)



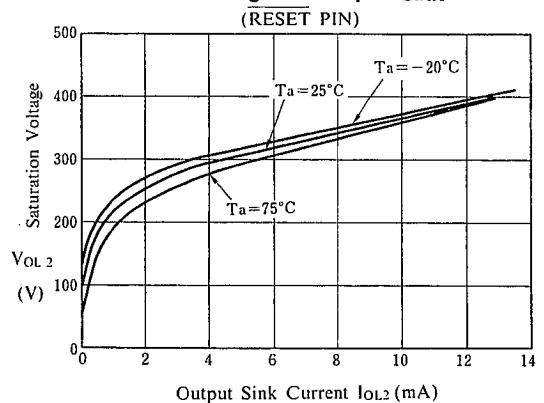
### Detect Voltage vs. Ambient Temperature



### Saturation Voltage vs. Output Sink Current (RESET PIN)

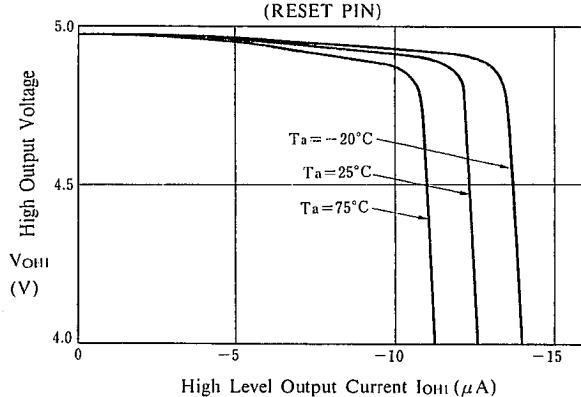


### Saturation Voltage vs. Output Sink Current (RESET PIN)

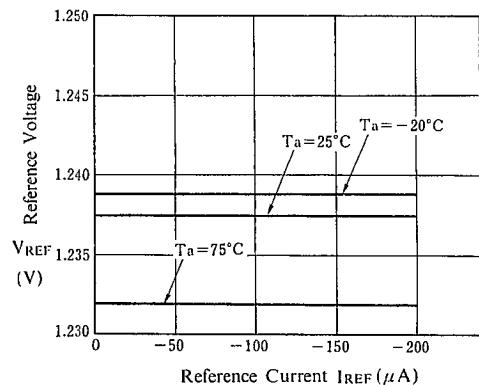


## ■ TYPICAL CHARACTERISTICS

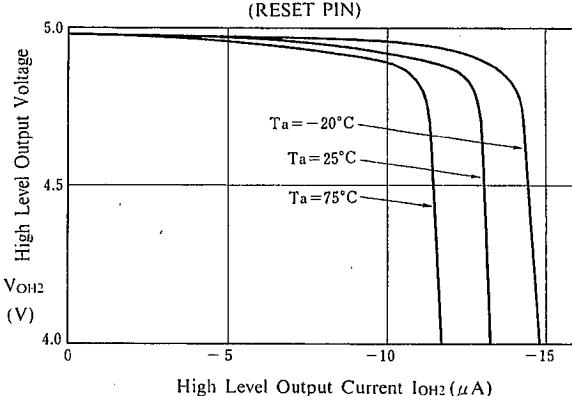
**High Level Output Voltage  
vs. High Level Output Current  
(RESET PIN)**



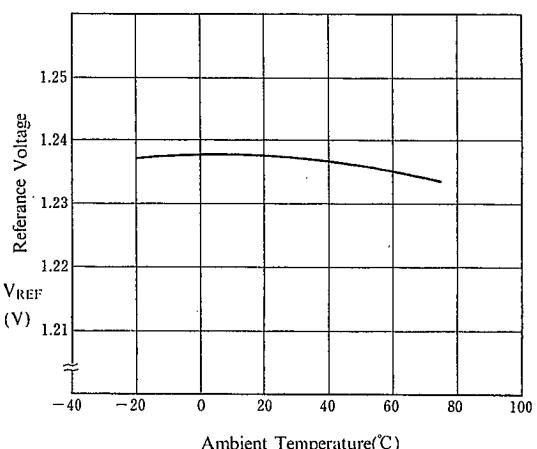
**Reference Voltage vs. Reference Current**



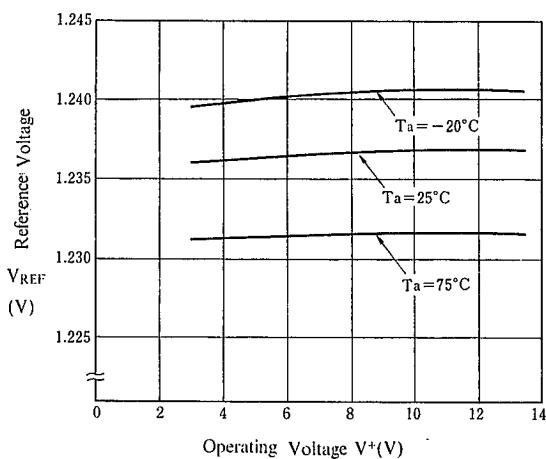
**High Output Voltage  
vs. High Level Output Current  
(RESET PIN)**

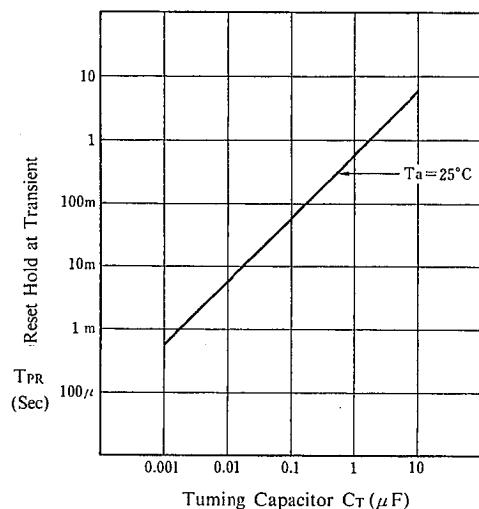
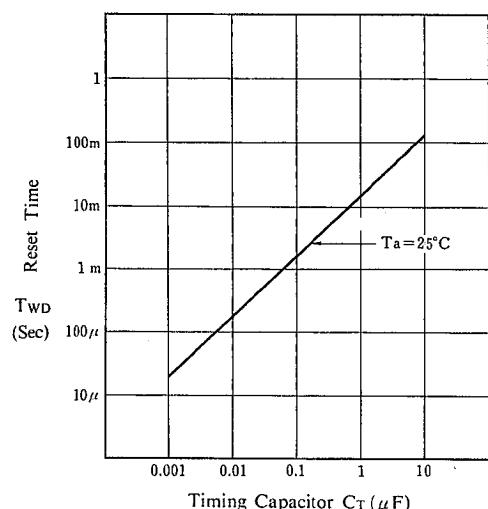
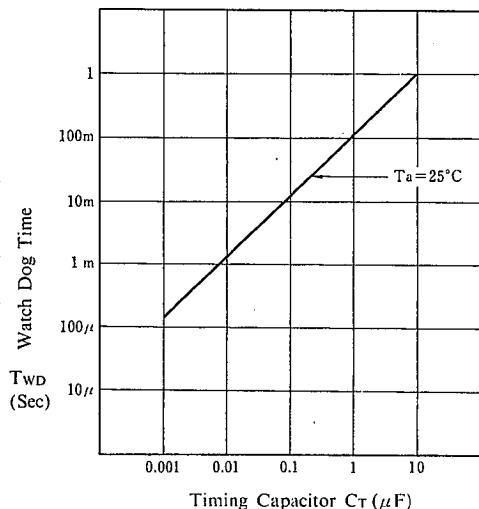
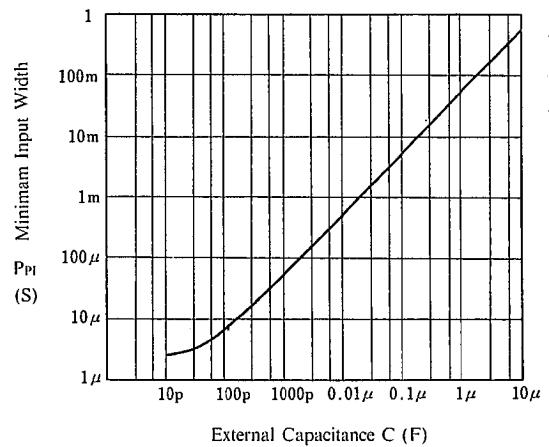


**Reference Voltage vs. Ambient Temperature**



**Reference Voltage vs. Operating Voltage**

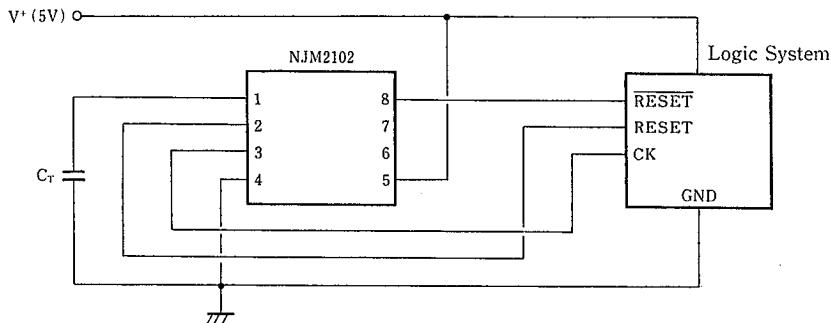


**■ TYPICAL CHARACTERISTICS****Reset Hold Time at Transient****Reset Time****Watch Dog Timer observation time****Minimum Input Pulse Width vs. CT**

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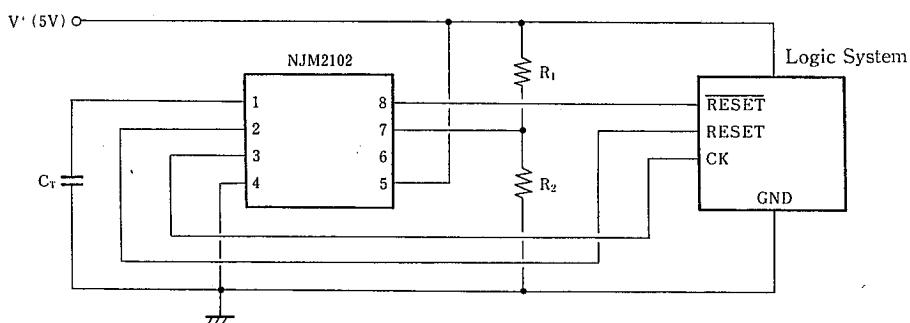
## ■ APPLICATION CIRCUIT

### 1. 5V Supply Voltage Supervisory and Watch-dog-timer



- Voltage Supply is detected through Vs. Detected Voltage is V<sub>SH</sub>, V<sub>SL</sub>.

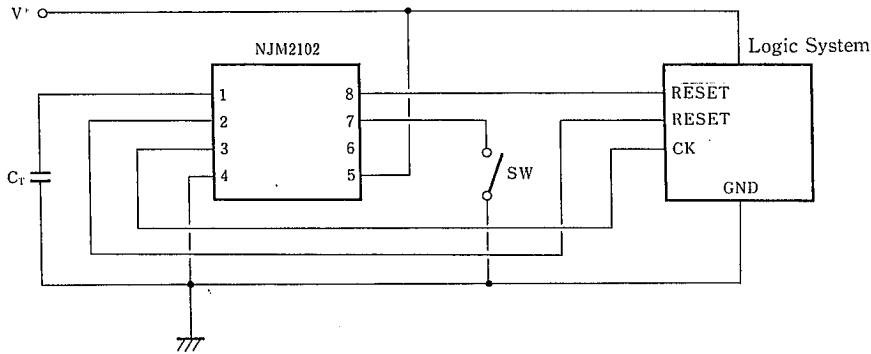
### 2. 5V Supply Voltage Supervisory (Externally fine tuning type)



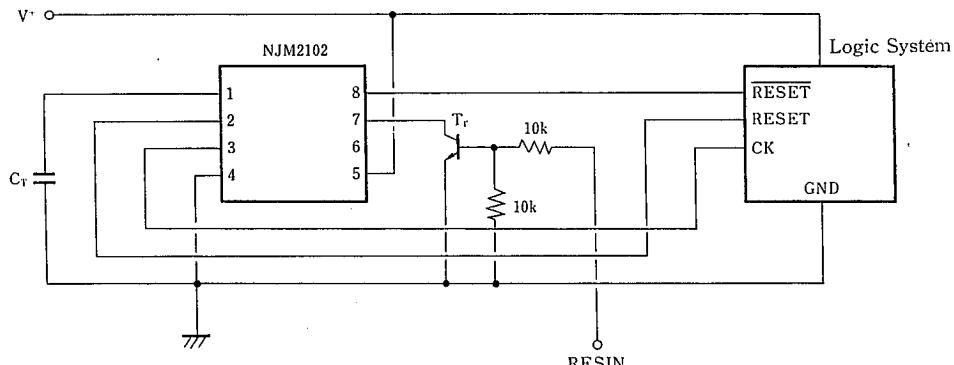
- Vs detecting Voltage can be externally adjusted.
  - Detecting Voltage can be decided by divider resistor of IC inside.  
Detecting Voltage can be set by external R<sub>1</sub>, R<sub>2</sub>.
- The external resistor R<sub>1</sub>, R<sub>2</sub> are required to be set in value less than 1/10 in comparing to divideing resistor of IC inside.  
Please refere to following Table.

R <sub>1</sub> (kΩ)	R <sub>2</sub> (kΩ)	Detecting Voltage : V <sub>Si</sub> (V)	Detecting Voltage : V <sub>Sh</sub> (V)
10	3.9	4.34	4.44
9.1	3.9	4.08	4.18

3. Compulsory Resetting attached (Reset Hold attached)



- \*Pin 7 to be grounded when SW. ON. RESET(8pin) become Low:  
RESET(pin2) become HIGH.



- By putting signal in the RESET pin, and Tr switch ON RESET pin become LOW and RESET pin High.

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## MEMO

[CAUTION]  
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