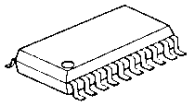
Digital Audio Delay

■ General Description

The NJU26902 is a digital audio delay. The NJU26902 provides delay-time adjustment function and digital audio interface.

■ **Package**



NJU26902VM1

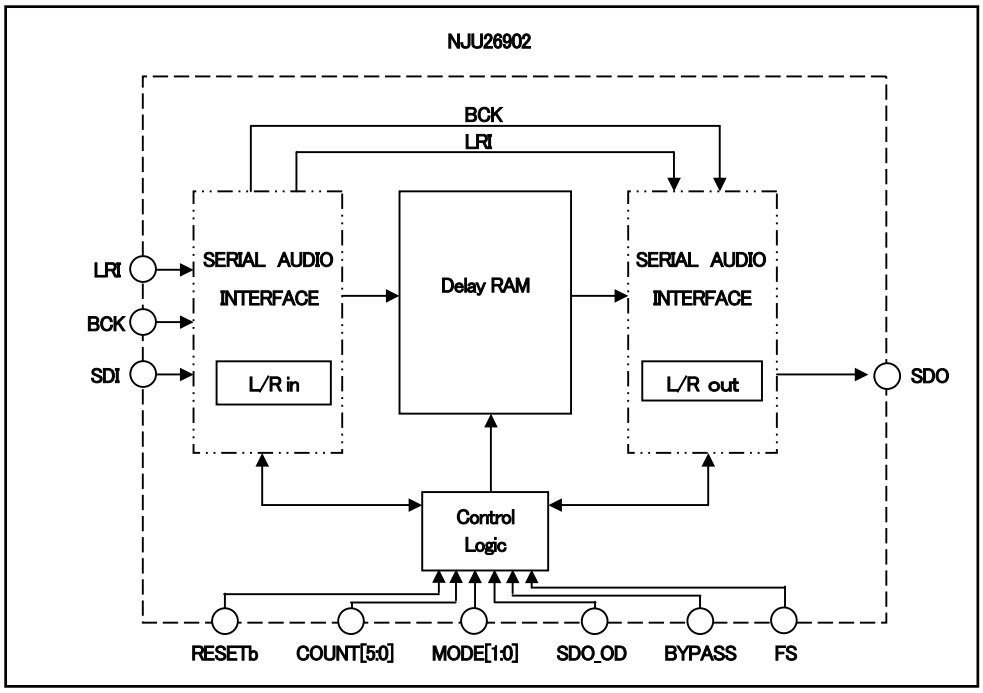
■ FEATURES

- 2-Channel Audio Delay (24 bits data width).
  Delay Time 85msec at fs = 48kHz (128msec at fs = 32kHz , 43msec at fs = 96kHz)
- To make long delay time, the NJU26902 can be connected serially.
- Non-audio-signal data can be delayed by the NJU26902.

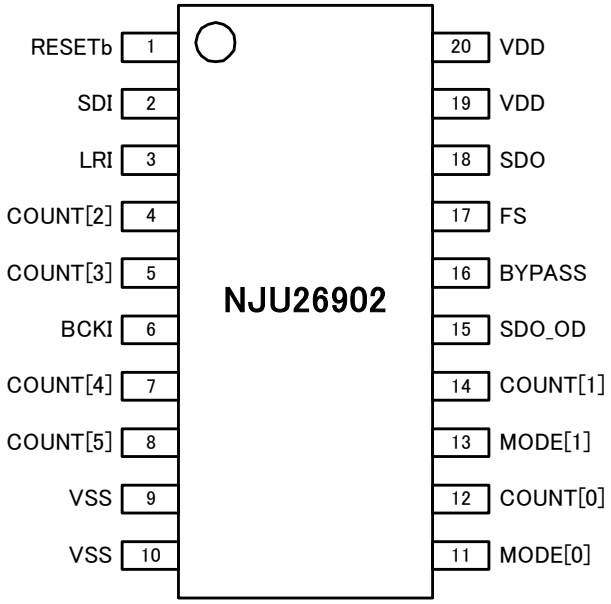
■ Hardware Specification

- Digital Audio Interface : 1 Input port, 1 Output port
- Digital Audio Format : LJ / RJ / I^2S 24bit BCK : 64fs / 32fs, Slave Mode
- Audio Bit Clock (BCK) Frequency : 13MHz Max (approximate fs=200KHz)
- Package : SSOP20-M1 Pb-Free
- Power Supply : 2.5V (+3.3V input tolerant)

■ Function Block Diagram



■ Pin Assignment



■ Pin Description

No.	Symbol	I/O	Description
1	RESETb	I△	Reset (Active low)
2	SDI	I	Audio Data Input
3	LRI	I	LR Clock Input
4	COUNT[2]	I△	Delay Time Control 2
5	COUNT[3]	I△	Delay Time Control 3
6	BCKI	I	Bit Clock Input
7	COUNT[4]	I△	Delay Time Control 4
8	COUNT[5]	I△	Delay Time Control 5
9	VSS	-	GND
10	VSS	-	GND
11	MODE[0]	I▼	Digital Audio Interface Format Select
12	COUNT[0]	I△	Delay Time Control 0
13	MODE[1]	I△	Digital Audio Interface Format Select
14	COUNT[1]	I△	Delay Time Control 1
15	SDO_OD	I▼	SDO pin Open Drain Select
16	BYPASS	I▼	SDO pin BYPASS Control
17	FS	I△	BCK fs Select
18	SDO	O	Audio Data Output (CMOS Output / Open Drain Output)
19	VDD	-	Power Supply +2.5V
20	VDD	-	Power Supply +2.5V

I : Input, I△ : Input(internal pull-up), I▼ : Input(internal pull-down), O : Output, P: +Power, G : GND

1. Electric Characteristics

1.1 Absolute Maximum Ratings

Table1-1 Absolute Maximum Ratings (V_{SS}=0V, Ta=25°C)

Parameter	Symbol	Rating	Units
Power Supply Voltage	V_{DD}	-0.3 to +3.0	V
Input Pin Voltage	$V_{X(IN)}$	-0.3 to +3.6	V
SDO Pin Voltage *1 (CMOS Output)	$V_{X(O)}$	-0.3 to V_{DD}+0.3	V
SDO Pin Voltage *2 (Open Drain Output)	$V_{X(OD)}$	-0.3 to +3.6	V
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-40 to +125	°C

*1 This specification is applied to $V_{X(O)}$ at the SDO pin. in case of SDO_OD= "Low".

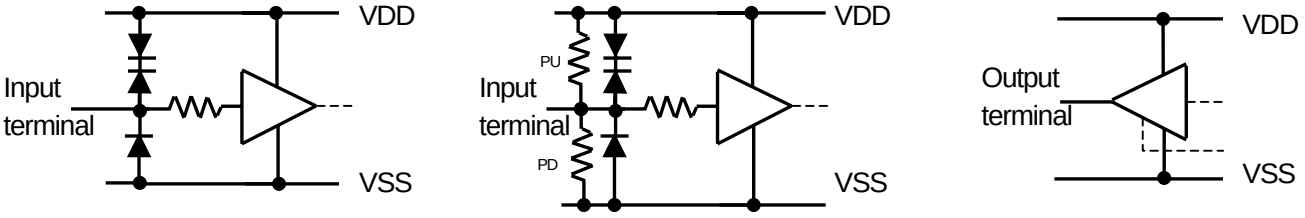
*2 This specification is applied to $V_{X(OD)}$ at the SDO pin. in case of SDO_OD= "High".

1.2 Electric Characteristics

Table1-2 Electric Characteristics (V_{DD}=2.5V, V_{SS}=0V, Ta=25℃)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Operating V_{DD} Voltage	V_{DD}		2.25	2.5	2.75	V
Operating Current	I_{DD}	BCKI:13MHz SDO:C_L=25pF	-	1.0	-	mA
Operating Temperature	T_{OPR}		-40	25	85	℃
High Level Input Voltage	V_{IH}		2.0	-	3.3	V
Low Level Input Voltage	V_{IL}		-	-	0.5	V
High Level Output Voltage (SDO_OD="Low")	V_{OH}	I_{OH}= -2mA I_{OH}= -100uA	V_{DD}-0.4 V_{DD}-0.1	- -	V_{DD} V_{DD}	V
Low Level Output Voltage	V_{OL}	I_{OL}= 2mA I_{OL}= 100uA	0 0	- -	0.4 0.1	V
Open Drain Output Current (SDO_OD="High")	I_{OD}	V_{IN}= 3.3V	-15	-	+15	
Input Current	I_{IN}	V_{IN}= V_{SS} to 3.3V	-15	-	+15	uA
Input Current (Internal Pull-up Pin)	$I_{IN(PU)}$	V_{IN}= V_{SS} to 3.3V	-100	-	+15	uA
Input Current (Internal Pull-down Pin)	$I_{IN(PD)}$	V_{IN}= V_{SS} to 3.3V	-15	-	+200	uA
Input Capacitance	C_{IN}		-	10	-	pF
Input Rise/Fall transition Time	t_r / t_f		-	-	100	ns

■ Equivalent Circuit



Input Pin
（SDI, LRI, BCKI）

Input Pin
（Internal Pull-up (PU) :
RESETb, MODE[1], FS,
COUNT[5], COUNT[4], COUNT[3],
COUNT[2], COUNT[1], COUNT[0],
Internal Pull-down (PD) :
MODE[0], SDO_OD,BYPASS）

Output Pin
（SDO）

Fig. 1-1 I/O Equivalent Circuits

2. Serial Audio Data Transmitting Diagram

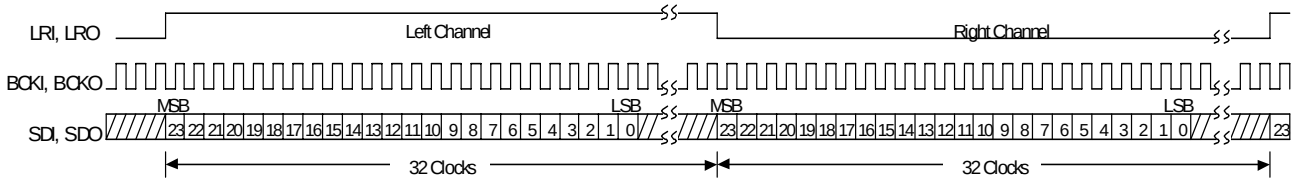


Fig. 2-1 Left-Justified Data Format 64fs, 24bit Data

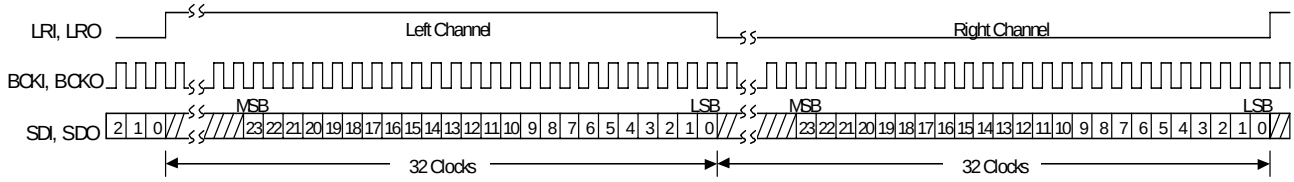


Fig. 2-2 Right-Justified Data Format 64fs, 24bit Data

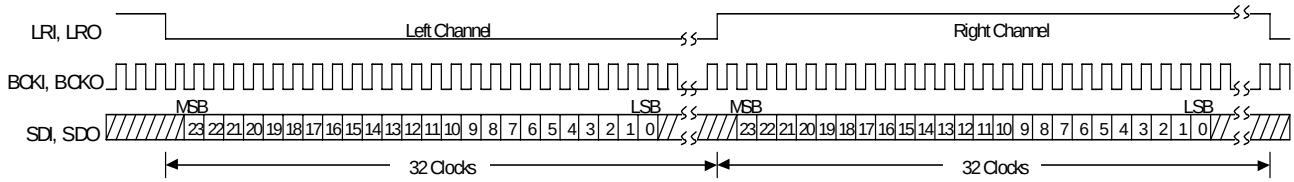


Fig. 2-3 I^2S Data Format 64fs, 24bit Data

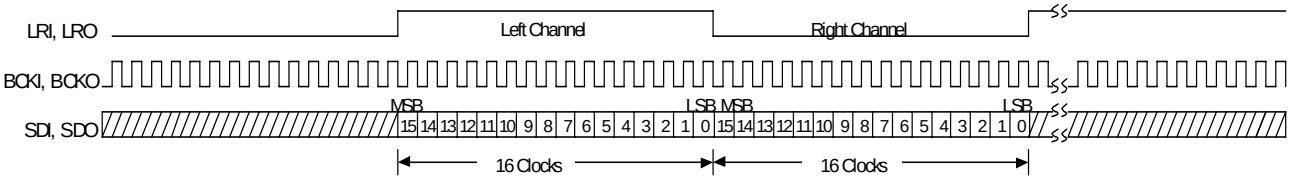


Fig. 2-4 Left-Justified Data Format 32fs, 16bit Data

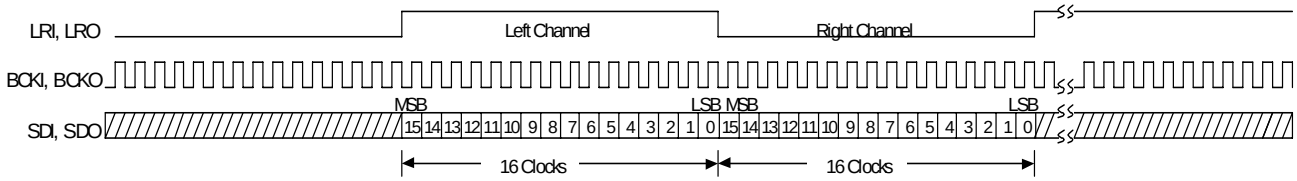


Fig. 2-5 Right-Justified Data Format 32fs, 16bit Data

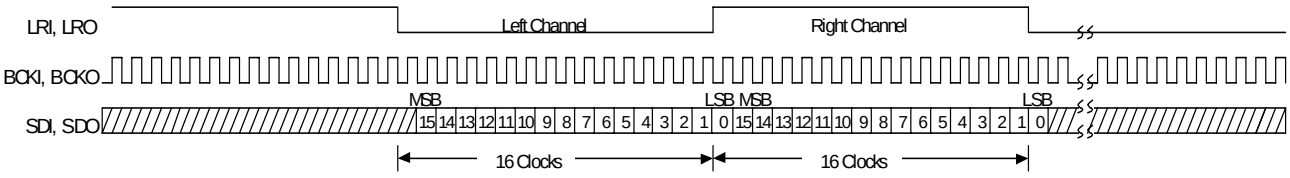


Fig. 2-6 I^2S Data Format 32fs, 16bit Data

2.1 Serial Audio Timing

Table 2-1 Serial Audio Input Timing Parameters

Parameter	Symbol	Test Condition	Min	Typ.	Max	Units
BCKI Frequency	f_{BCK}		-	-	13	MHz
BCKI Period L Pulse Width H Pulse Width	 t_{SIL} t_{SIH}		 35 35	-	-	ns
BCKI to LRI Time	T_{SLI}		15	-	-	ns
LRI to BCKI Time	t_{LSI}		15	-	-	ns
Data Setup Time	t_{DS}		15	-	-	ns
Data Hold Time	t_{DH}		15	-	-	ns
Data Output Delay	t_{DOD}	SDO:C_L=25pF SDO_OD="Low"		-	15	ns

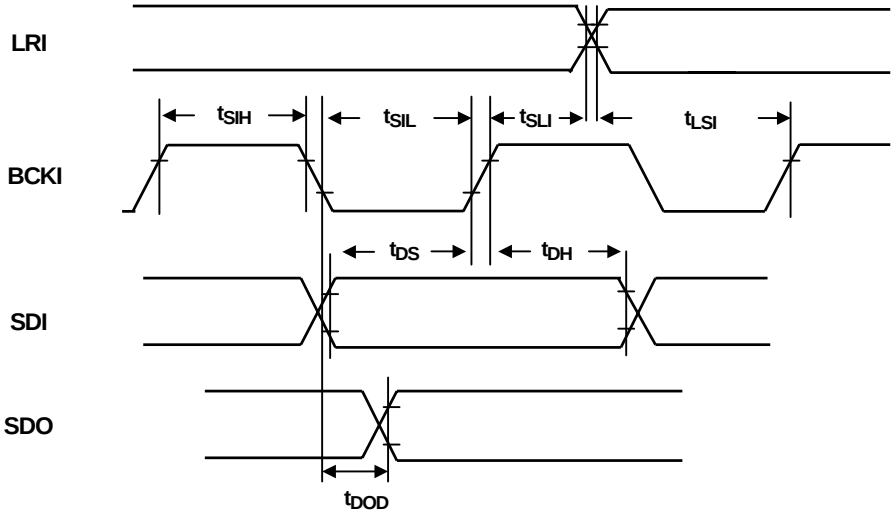


Fig. 2-7 Serial Audio Input / Output Timing

3. Function Description

- SDI(#2) is a serial audio input pin. The input audio signal should be connected to this pin.
- LRI(#3) is a LR clock input pin. This LR clock frequency is the same frequency of the input audio signal. In case of I2S format, LRI="Low" shows SDI and SDO data are left channel data, and LRI="High" shows SDI and SDO data are right channel data.
- BCKI(#6) is bit clock input pin. This BCKI clock frequency is 32 times (32fs) or 64 times (64fs) as large as the pin input audio signal. A bit length is 16bit precision in 32fs mode, and a bit length is 24bit precision in 64fs mode.
- MODE [1:0](#13,#11) and FS(#17) pins select serial audio format. Refer to Table3-1"Mode pin, FS pin Setup".
- SDO(#18) is serial audio output pin. The delayed audio data come out through this pin.
- SDO is 2.5V CMOS output in case of SDO_OD(#15)= "Low". SDO is open drain output in case of SDO_OD= "High", SDO can be pulled up to 3.3V. In case of SDO_OD= "Low" & BYPASS= "High", the bypass mode is selected.
- The next combination is reserved. Do not use this combination. SDO_OD= "High" & BYPASS= "High". Refer to Table3-2 "SDO_OD pin, BYPASS pin Setup".
- COUNT [5:0](#8, #7, #5, #4, #14, #12) pins select delay time. When the setup is changed, SDO outputs a "Low" level (mute) during the period selected by COUNT [5:0]. Refer to 4. Delay Time.
- When RESETb is "Low", the NJU26902 is initialized on the rise edge of BCKI. SDO outputs a "Low" level (mute) during the period selected by COUNT [5:0].
- In case of not using RESETb, connect RESETb to VDD.
- VDD is a power supply pin. Connect VDD to the power supply 2.5V. VSS is a GND pin. The decoupling capacitor is necessary between VDD and VSS.
- The input pins can interface to 3.3V ICs. Refer to Table 1-2"Electric Characteristics".
- After Power supply or serial audio format changing, there is possibility the NJU26902 generates random data for the delay time period set by COUNT[5:1] pins. If necessary, the mute circuit should be added or reset NJU26902.

Table 3-1 Mode pin, FS pin Setup

FS (17pin)	MODE[1] (13pin)	MODE[0] (11pin)	Setup
0	0	0	RJ 16bit 32fs
0	0	1	LJ 16bit 32fs
0	1	0	I^2S 16bit 32fs
1	0	0	RJ 24bit 64fs
1	0	1	LJ 24bit 64fs
1	1	0	I^2S 24bit 64fs
Other			Reserved *1

* : 0=Low, 1=High

*1 : Do not use.

Table 3-2 SDO_OD pin, BYPASS pin Setup

SDO_OD (15pin)	BYPASS (16pin)	NJU26902 Function
0	0	Delay Operation, SDO=CMOS Output
0	1	Bypass Operation, SDO=CMOS Output
1	0	Delay Operation, SDO=Open Drain Output
1	1	Reserved *1

* : 0=Low, 1=High

*1 : Do not use.

4. Delay Time

- The NJU26902 provides maximum 4097 samples delay and slave-mode audio interface. The delay time depends on sampling frequency.
- The next formula shows how to calculate the delay time. Refer to Table 4-1"Delaty Sample Number Setup Example".
- Total delay sample number =
  COUNT[0]*2048+COUNT[1]*1024+COUNT[2]*512+COUNT[3]*256+COUNT[4]*128+COUNT[5]*64+64+1

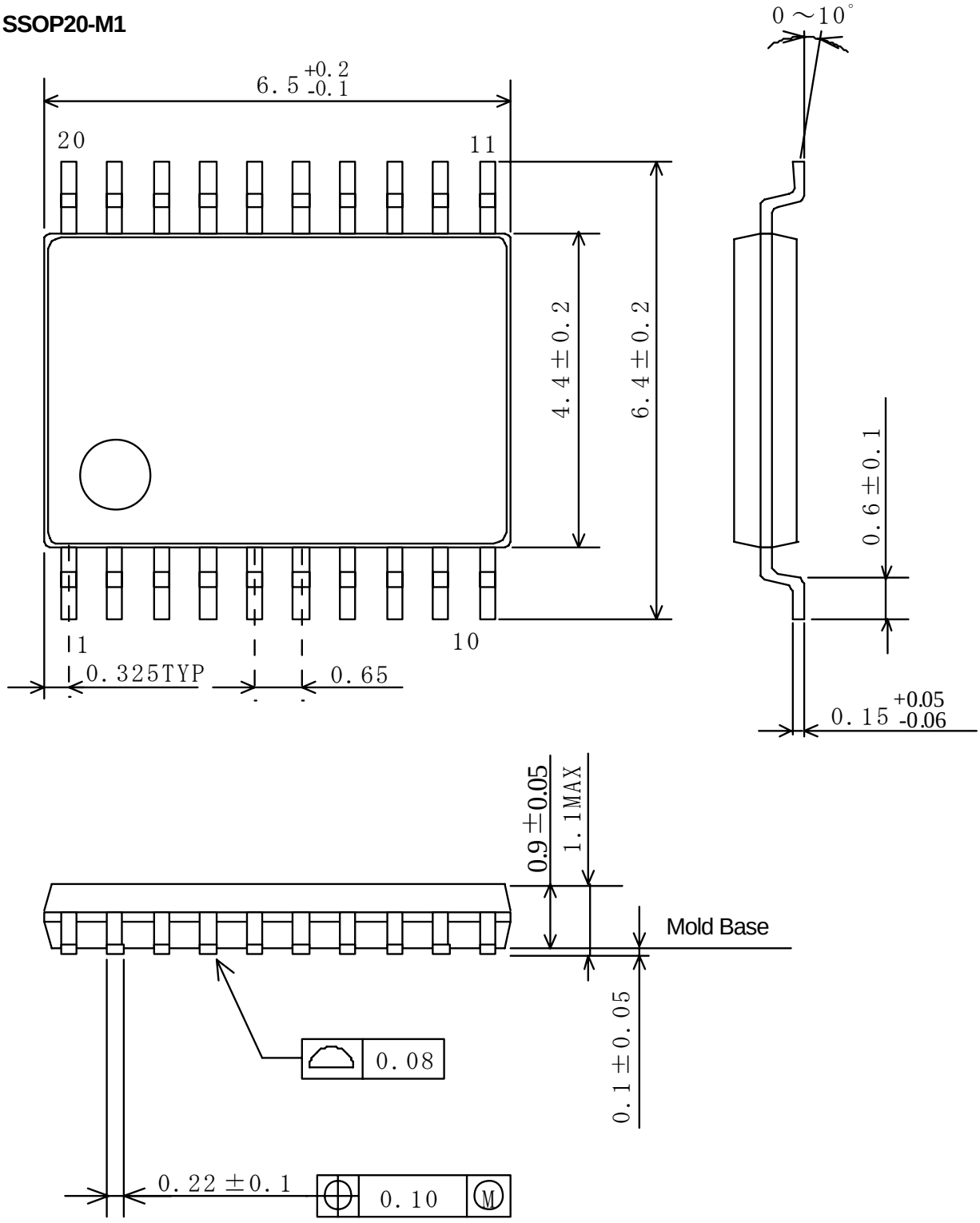
Table 4-1 Delay Sample Number Setup Example

COUNT[0] (12pin)	COUNT[1] (14pin)	COUNT[2] (4pin)	COUNT[3] (5pin)	COUNT[4] (7pin)	COUNT[5] (8pin)	Total Delay Sample Number
0	0	0	0	0	0	65 (minimum)
0	1	1	0	0	0	1601
1	1	0	0	0	1	3201
1	1	1	1	1	1	4097 (maximum)

* : 0=Low, 1=High

5. Package Dimensions

SSOP20-M1



UNIT : mm

Version V0.4

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