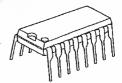
DUAL AUDIO POWER AMPLIFIER

■ GENERAL DESCRIPTION

The NJW1105 is a dual audio amplifier which supplies 2.4W (1.2W/channel) to 8Ω loads at 5V. Its features are wide operating voltage range from 4V to 12V and low consumption output by Bi-MOS technology.

The NJW1105 is suitable for speaker amplifier required high output power, such as personal computers, camcorders, and others. It includes thermally protected and mute on/off circuit.

PACKAGE OUTLINE



NJW1105D

■ FEATURES

●Operating Voltage (V*=4V~12V)

•Output Power (1.2W/ch at $V^{+}=5V$, $R_{L}=8\Omega$)

Supply Current (35mA MAX.)
 Supply Current on Mute (3.5mA MAX.)

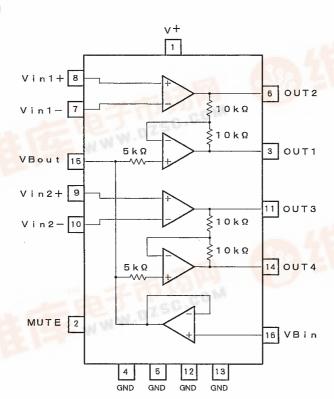
●Bi-MOS Technology

Package Outline DIP16, SDMP30



NJW1105M

BLOCK DIAGRAM





\blacksquare ABSOLUTE MAXIMUM RATINGS (T a = 25 °C)

PARAMETER	SYMBOL	RATINGS	UNIT	
Supply Voltage	V +	15	v	
Operating Current	l o	1	Α	
Mute Terminal Current	l m	1.0	m A	
Power Dissipation	Po	(DIP16) 1.9 (SDMP30) 1.8 (note 1)	W	
Operating Temperature Range	Торг	-40~+85	ొ	
Storage Temperature Range	Тетв	-40~+150	ဇ	

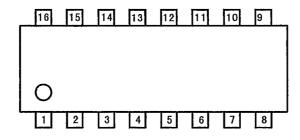
(note 1) At on PC board.

■ ELECTRICAL CHARACTERISTICS ($V^+=5V$, $Ta=25^{\circ}C$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
[ALL]			_			
Operating Supply Voltage Range	V ⁺		4	5	12	V
Mute OFF Current Dissipation	l cc 1	V _M =4. 2V, V _{1N} =2. 5V	-	20	35	m A
Mute ON Current Dissipation	1 cc 2	V _M =0V, V _{1N} =2. 5V	_	2	3. 5	m A
[POWER AMPLIFIER]						
Output Offset Voltage	Δ۷。	R _L =8Ω	-50	-	50	m V
Input Bias Current	1 в		-	-	300	n A
Output Power	P _o 1	THD=10%, f=1kHz, R∟=8Ω	-	1. 2	-	w
	P ₀ 2	THD=10%, f=1kHz, RL=8Ω V*=7V	-	2. 5	_	W
Total Harmonic Distortion	THD	R _L =8Ω, Po=800mW, f=1kHz	-	0. 35	-	96
Power Supply Rejection Ratio	PSRR	f=1kHz	-	45	-	dB
Voltage Gain	Av	AMP2, AMP3, R∟=2kΩ,	35	50	-	d B
<u> </u>		V 1 N=2. 5V				
[BUFFER AMPLIFIER]						
Input Output Potential Difference	V _{BO}		-30	0	30	m V
Input Voltage Range	V _{B1}		1.5	2. 5	3. 5	V
Output Voltage Range	Δ٧вο	1 = -5mA	-	-	-50	m V
		I.=+5mA				
[MUTING]						
Mute OFF Voltage	V MH		3. 5	4. 2	-	V
Mute ON Voltage	VML		-	0. 8	1. 0	V
Mute Sink Current	1 м	V _M =5V	70	100	130	μΑ

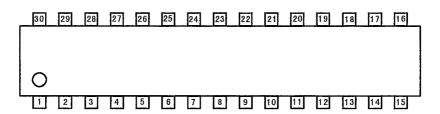
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PIN CONFIGRATION



D | P-16

```
1 : V +
                9: Vin2 (+)
2:MUTE
               10: Vin2 (-)
3:0UT1
               11:0UT3
4 : GND
               12: GND
5 : GND
               13:GND
6:OUT2
               14:OUT4
7: Vin1 (-)
              15: VBout
8: Vin1 (+)
              16: VBin
```



SDMP-30

```
1 : GND
                16:GND
 2 : GND
                17:GND
 3: OUT4
                18: OUT2
 4 : NC
                19:NC
 5 : NC
                20:NC
                21:Vin1(-)
 6: VBout
 7: VBin
                22: Vin1(+)
 8 : NC
                23:NC
 9 : V *
                24: Vin2 (+)
10: MUTE
                25: Vin2 (-)
11:NC
                26:NC
12:NC
                27:NC
13:0UT1
                28: OUT3
14: GND
                29:GND
15:GND
                30:GND
```

■ TERMINAL EXPLANATION

PIN NO.		PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT	
DIP - 1 6	SDMP — 3 O	I CIV IVAME	1 0001100	MOIDE ENGLYNEEN CHOOLI	
4 5 12 13	1 2 14 15 16 17 29 30	GND	Recommend expand- ing the island in order to heat ra- diation proper- ties.		
1 4	3	OUT4	Output terminal of AMP. 4. OUT4 signal is opposite phase against OUT3.	10k Ω OUT4 5k Ω VBout GND	
_	4 5 8 1 1 1 2 1 9 2 0 2 3 2 6 2 7	N C	Non-connection terminal. Recommend connect- ing to GND.		

PIN NO.				
DIP	SDMP	PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
— 16	-30 -30			
15	6	VBout	An buffer amplifier output.	VBout O 400 \Q
16	7	VBin	An buffer amplifi- er input.	VBin Φ V+ GND
1	9	Vcc	Supply Voltage.	
2	10	МИТЕ	An mute input. Pulldown by 50kΩ (TYP) resistor.	MUTE O → V+ 50k Ω GND

■ TERMINAL EXPLANATION

PIN NO.		PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
DIP - 1 6	SDMP — 3 O	1 111 WALL	1 0001100	THOISE EGGLYNEETH OTHOOTT
3	13	OUT1	Output terminal of AMP. 1. OUT1 signal is opposite phase against OUT2.	10k Ω
6	18	OUT2	Output terminal of AMP. 2.	10k Ω 10k Ω 10k Ω 10k Ω AMP 5k Ω VBout
7	2 1	V i n1(-)	Inverting input terminal of AMP.2.	Vin1 (-) 0 Ω Ψ AMP
8	22	V i n1(+)	Non-inverting in- put terminal of AMP. 2.	Vin1(+) Ο W

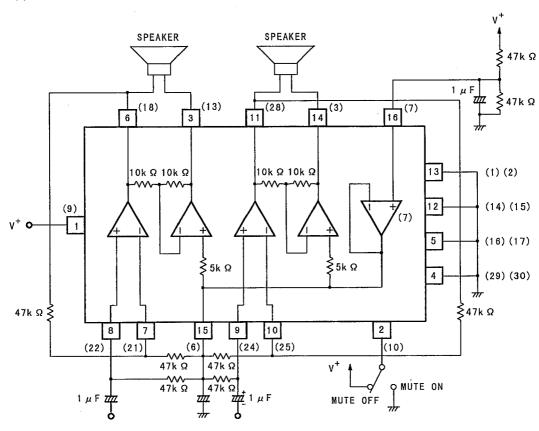
■ TERMINAL EXPLANATION

PIN NO.		PIN NAME	FUNCTION	INSIDE EQUIVALENT CIRCUIT
DIP - 16	SDMP -30	FIN NAME	TONOTTON	INSTITE ENGINALENT CINCUIT
9	24	V i n2(+)	Inverting input terminal of AMP.3.	400Ω Vin2(-) Q —√√√
•				
10	25	V i n2(-)	Non-inverting in- put terminal of AMP.3.	Vin2 (+) 0 - VVV
11	28	оитз	Output terminal of AMP. 3.	
				10kΩ 10kΩ AMP 5kΩ VBout GND

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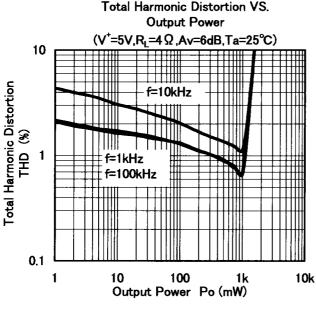
APPLICATION CIRCUIT

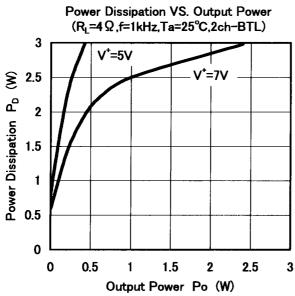
(1) BTL

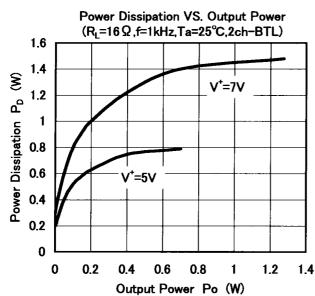


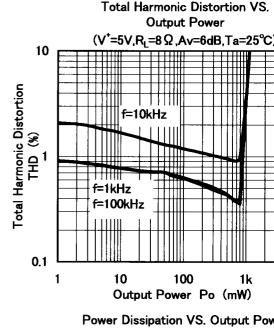
(The number in '()' indicates a pin number of SDMP.)

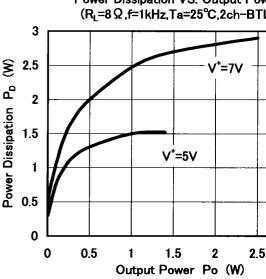
TIPICAL CHARACTERISTICS

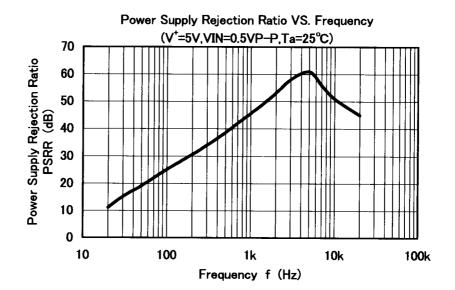


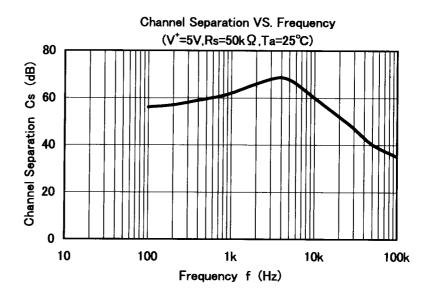












NJW1105

MEMO

[CAUTION]
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