

# NL17SZ74

## Single D Flip Flop

The NL17SZ74 is a high performance, full function Edge triggered D Flip Flop, with all the features of a standard logic device such as the 74LCX74.

- Extremely High Speed:  $t_{PD}$  2.6 ns (typical) at  $V_{CC} = 5$  V
- Designed for 1.65 V to 5.5 V  $V_{CC}$  Operation
- 5 V Tolerant Inputs – Interface Capability with 5 V TTL Logic
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10  $\mu$ A) Substantially Reduces System Power Requirements
- Replacement for NC7SZ74
- Tiny Ultra Small Package Only 2.1 X 3.0 mm
- High ESD Ratings: 2000 V Human Body Model  
200 V Machine Model
- Chip Complexity: FET = 64

### TRUTH TABLE

Inputs				Outputs		Operating Mode
PR	CLR	CP	D	Q	$\bar{Q}$	
L	H	X	X	H	L	Asynchronous Set Asynchronous Clear Undetermined
H	L	X	X	L	H	
L	L	X	X	H	H	
H	H	$\uparrow$	h	H	L	Load and Read Register
H	H	$\uparrow$	l	L	H	
H	H	$\uparrow$	X	NC	NC	Hold

- H = High Voltage Level
- h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
- L = Low Voltage Level
- l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
- NC = No Change
- X = High or Low Voltage Level and Transitions are Acceptable
- $\uparrow$  = Low-to-High Transition
- $\uparrow$  = Not a Low-to-High Transition

For  $I_{CC}$  reasons, DO NOT FLOAT Inputs



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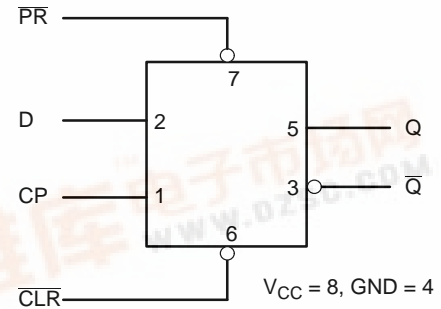
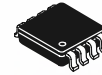
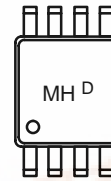


Figure 1. Logic Diagram



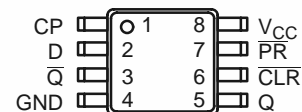
US8  
CASE 493  
US SUFFIX

### MARKING DIAGRAM



MH = Specific Device Code  
D = Date Code

### PINOUT



### ORDERING INFORMATION

Device	Package	Shipping
NL17SZ74US	US8	3000/Tape & Reel



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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>I</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>O</sub>	DC Output Voltage – Output in High or Low State (Note 1)	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	DC Input Diode Current V <sub>I</sub> < GND	-50	mA
I <sub>OK</sub>	DC Output Diode Current V <sub>O</sub> < GND	-50	mA
I <sub>O</sub>	DC Output Sink Current	±50	mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100	mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 2)	250	°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V <sub>ESD</sub>	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 N/A	V

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

1. I<sub>O</sub> absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm X 1 inch, 2 ounce copper trace with no air flow.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V <sub>I</sub>	Input Voltage (Note 6)	0	5.5	V
V <sub>O</sub>	Output Voltage (HIGH or LOW State)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Free-Air Temperature	-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate V <sub>CC</sub> = 2.5 V ±0.2 V V <sub>CC</sub> = 3.0 V ±0.3 V V <sub>CC</sub> = 5.0 V ±0.5 V	0 0 0	20 10 5.0	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			-40°C ≤ T <sub>A</sub> ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High-Level Input Voltage		1.65	0.75 V <sub>CC</sub>			0.75 V <sub>CC</sub>		V
			2.3 to 5.5	0.7 V <sub>CC</sub>			0.7 V <sub>CC</sub>		
V <sub>IL</sub>	Low-Level Input Voltage		1.65			0.25 V <sub>CC</sub>		0.25 V <sub>CC</sub>	V
			2.3 to 5.5			0.3 V <sub>CC</sub>		0.3 V <sub>CC</sub>	
V <sub>OH</sub>	High-Level Output Voltage V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub>	I <sub>OH</sub> = 100 μA	1.65 to 5.5	V <sub>CC</sub> - 0.1	V <sub>CC</sub>		V <sub>CC</sub> - 0.1		V
		I <sub>OH</sub> = -3 mA	1.65	1.29	1.52		1.29		
		I <sub>OH</sub> = -8 mA	2.3	1.9	2.1		1.9		
		I <sub>OH</sub> = -12 mA	2.7	2.2	2.4		2.2		
		I <sub>OH</sub> = -16 mA	3.0	2.4	2.7		2.4		
		I <sub>OH</sub> = -24 mA	3.0	2.3	2.5		2.3		
		I <sub>OH</sub> = -32 mA	4.5	3.8	4.0		3.8		
V <sub>OL</sub>	Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub>	I <sub>OL</sub> = 100 μA	1.65 to 5.5		0.008	0.1		0.1	V
		I <sub>OL</sub> = 3 mA	1.65		0.10	0.24		0.24	
		I <sub>OL</sub> = 8 mA	2.3		0.12	0.3		0.3	
		I <sub>OL</sub> = 12 mA	2.7		0.15	0.4		0.4	
		I <sub>OL</sub> = 16 mA	3.0		0.19	0.4		0.4	
		I <sub>OL</sub> = 24 mA	3.0		0.30	0.55		0.55	
		I <sub>OL</sub> = 32 mA	4.5		0.30	0.55		0.55	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			±0.1		±1.0	μA
I <sub>OFF</sub>	Power off Input Leakage Current	5.5V or V <sub>IN</sub> = GND	0			1.0		10	μA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			1.0		10	μA

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## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	V <sub>CC</sub> (V)	Test Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency (50% Duty Cycle) (Waveform 1)	1.8 ± 0.15	C <sub>L</sub> = 15 pF R <sub>D</sub> = 1 MΩ S <sub>1</sub> = Open	75			75		MHz
		2.5 ± 0.2		150			150		
		3.3 ± 0.3		200			200		
		5.0 ± 0.5		250			250		
		3.3 ± 0.3	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open	175			175		
		5.0 ± 0.5		200			200		
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, CP to Q or Q̄ (Waveform 1)	1.8 ± 0.15	C <sub>L</sub> = 15 pF R <sub>D</sub> = 1 MΩ S <sub>1</sub> = Open	2.5	6.5	12.5	2.5	13	ns
		2.5 ± 0.2		1.5	3.8	7.5	1.5	8.0	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5		0.8	2.2	4.5	0.8	5.0	
		3.3 ± 0.3	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, PR or CLR to Q or Q̄ (Waveform 2)	1.8 ± 0.15	C <sub>L</sub> = 15 pF R <sub>D</sub> = 1 MΩ S <sub>1</sub> = Open	2.5	6.5	14	2.5	14.5	ns
		2.5 ± 0.2		1.5	3.8	9.0	1.5	9.5	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5		0.8	2.2	5.0	0.8	5.5	
		3.3 ± 0.3	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t <sub>S</sub>	Setup Time, D to CP (Waveform 1)	1.8 ± 0.15	C <sub>L</sub> = 15 pF R <sub>D</sub> = 1 MΩ S <sub>1</sub> = Open	6.5			6.5		ns
		2.5 ± 0.2		3.5			3.5		
		3.3 ± 0.3		2.0			2.0		
		5.0 ± 0.5		1.5			1.5		
		3.3 ± 0.3	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open	2.0			2.0		
		5.0 ± 0.5		1.5			1.5		
t <sub>H</sub>	Hold Time, D to CP (Waveform 1)	1.8 ± 0.15	C <sub>L</sub> = 15 pF R <sub>D</sub> = 1 MΩ S <sub>1</sub> = Open	0.5			0.5		ns
		2.5 ± 0.2		0.5			0.5		
		3.3 ± 0.3		0.5			0.5		
		5.0 ± 0.5		0.5			0.5		
		3.3 ± 0.3	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open	0.5			0.5		
		5.0 ± 0.5		0.5			0.5		
t <sub>W</sub>	Pulse Width, CP, CLR, PR (Waveform 3)	1.8 ± 0.15	C <sub>L</sub> = 15 pF R <sub>D</sub> = 1 MΩ S <sub>1</sub> = Open	6.0			6.0		ns
		2.5 ± 0.2		4.0			4.0		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5		2.0			2.0		
		3.3 ± 0.3	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open	3.0			3.0		
		5.0 ± 0.5		2.0			2.0		
t <sub>REC</sub>	Recover Time PR; CLR to CP (Waveform 3)	1.8 ± 0.15	C <sub>L</sub> = 15 pF R <sub>D</sub> = 1 MΩ S <sub>1</sub> = Open	8.0			8.0		MHz
		2.5 ± 0.2		4.5			4.5		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5		3.0			3.0		
		3.3 ± 0.3	C <sub>L</sub> = 50 pF, R <sub>D</sub> = 500 Ω, S <sub>1</sub> = Open	3.0			3.0		
		5.0 ± 0.5		3.0			3.0		

7. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/2 (per flip-flop). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

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### CAPACITANCE (Note 8)

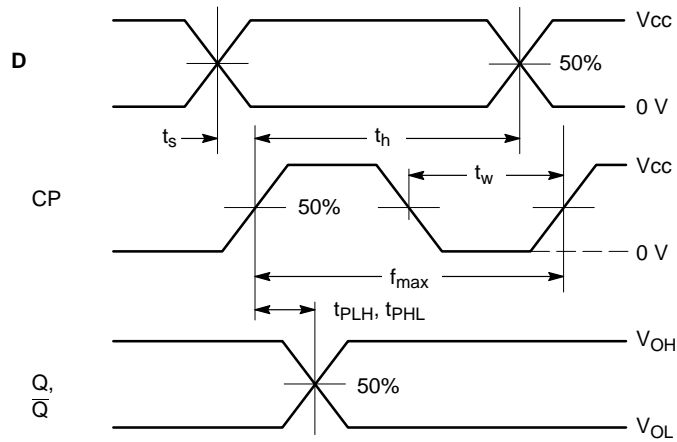
Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 5.5 V	7.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 5.5 V	7.0	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 9) Frequency = 10 MHz	V <sub>CC</sub> = 3.3 V	16	pF
		V <sub>CC</sub> = 5.0 V	21	

8. T<sub>A</sub> = +25°C, f = 1 MHz

9. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I<sub>CCD</sub>) at no output loading and operating at 50% duty cycle. (See Figure 2) C<sub>PD</sub> is related to I<sub>CCD</sub> dynamic operating current by the expression:

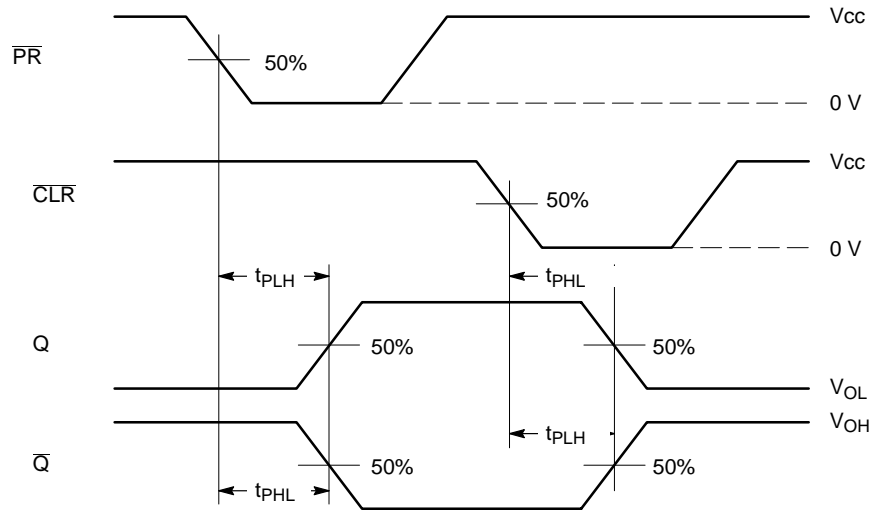
$$I_{CCD} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC(static)}$$

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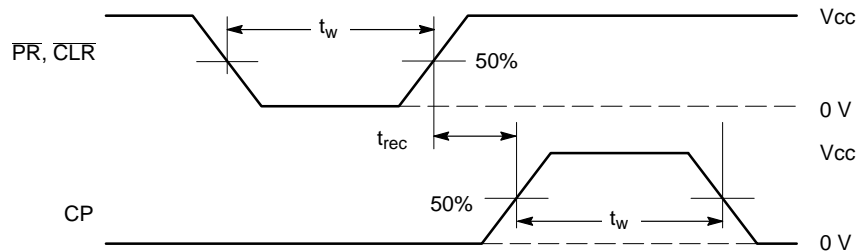
**WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES**

$t_R = t_F = 3.0$  ns, 10% to 90%;  $f = 1$  MHz;  $t_w = 500$  ns



**WAVEFORM 2 – PROPAGATION DELAYS**

$t_R = t_F = 3.0$  ns, 10% to 90%;  $f = 1$  MHz;  $t_w = 500$  ns



**WAVEFORM 3 – RECOVERY TIME**

$t_R = t_F = 3.0$  ns from 10% to 90%;  $f = 1$  MHz;  $t_w = 500$  ns  
Output Reg:  $V_{OL} \leq 0.8$  V,  $V_{OH} \geq 2.0$  V

**Figure 2. AC Waveforms**

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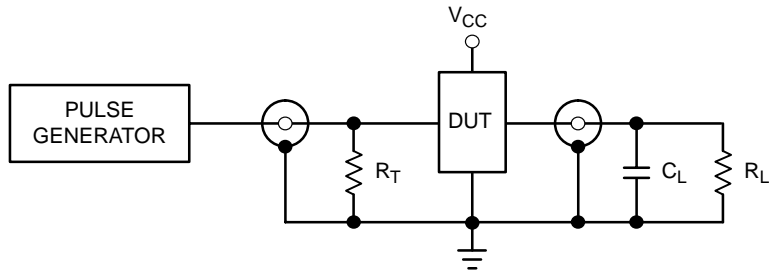


Figure 3. Test Circuit

## DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix		
NL17SZ74US	NL	1	7	SZ	74	US	US8	178 mm, 3000 Unit

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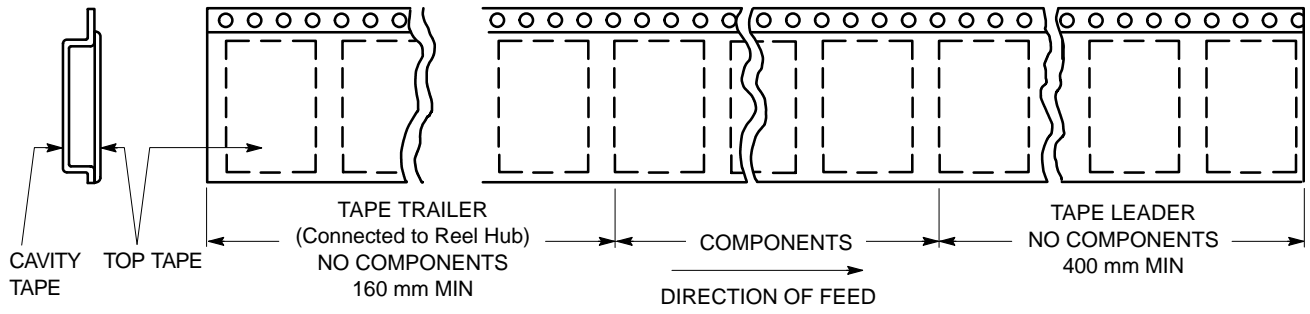


Figure 4. Tape Ends for Finished Goods

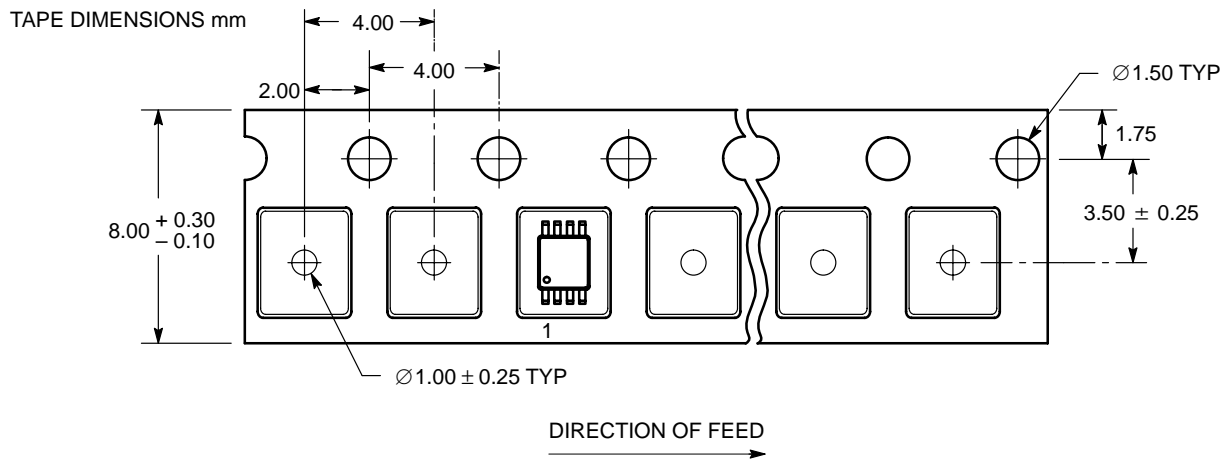


Figure 5. US8 Reel Configuration/Orientation



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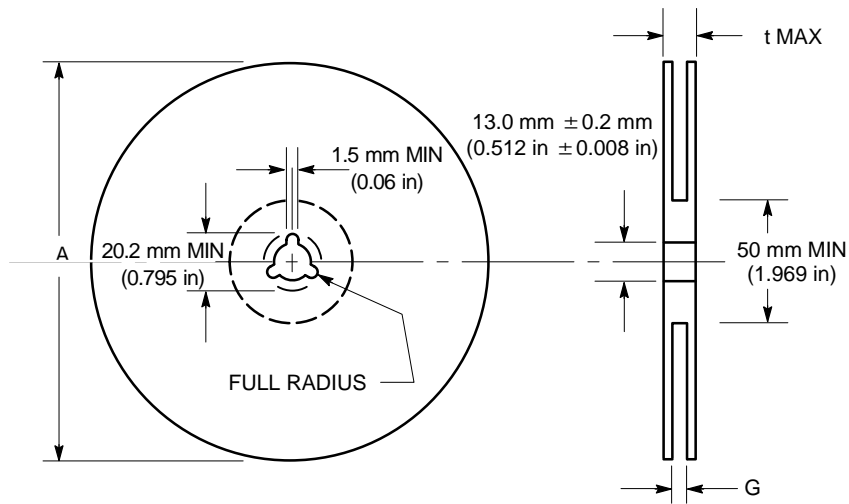


Figure 6. Reel Dimensions

## REEL DIMENSIONS

Tape Size	T and R Suffix	A Max	G	t Max
8 mm	US	178 mm (7 in)	8.4 mm, + 1.5 mm, -0.0 (0.33 in + 0.059 in, -0.00)	14.4 mm (0.56 in)

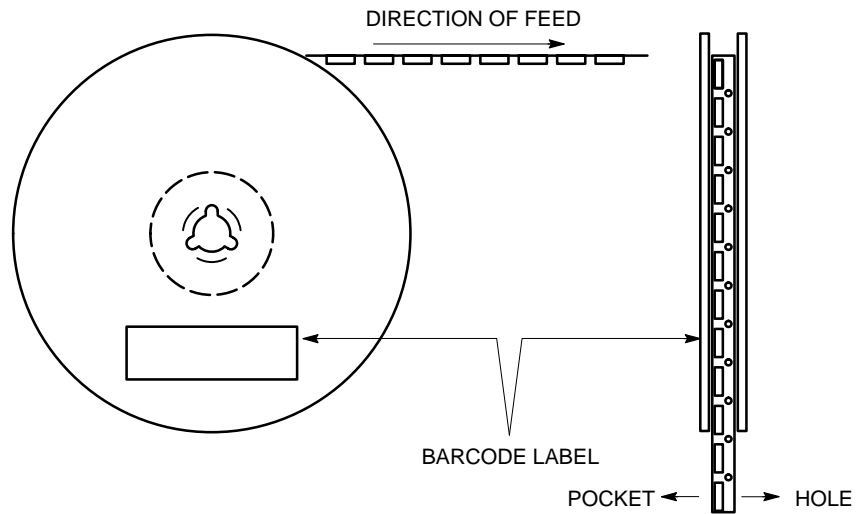
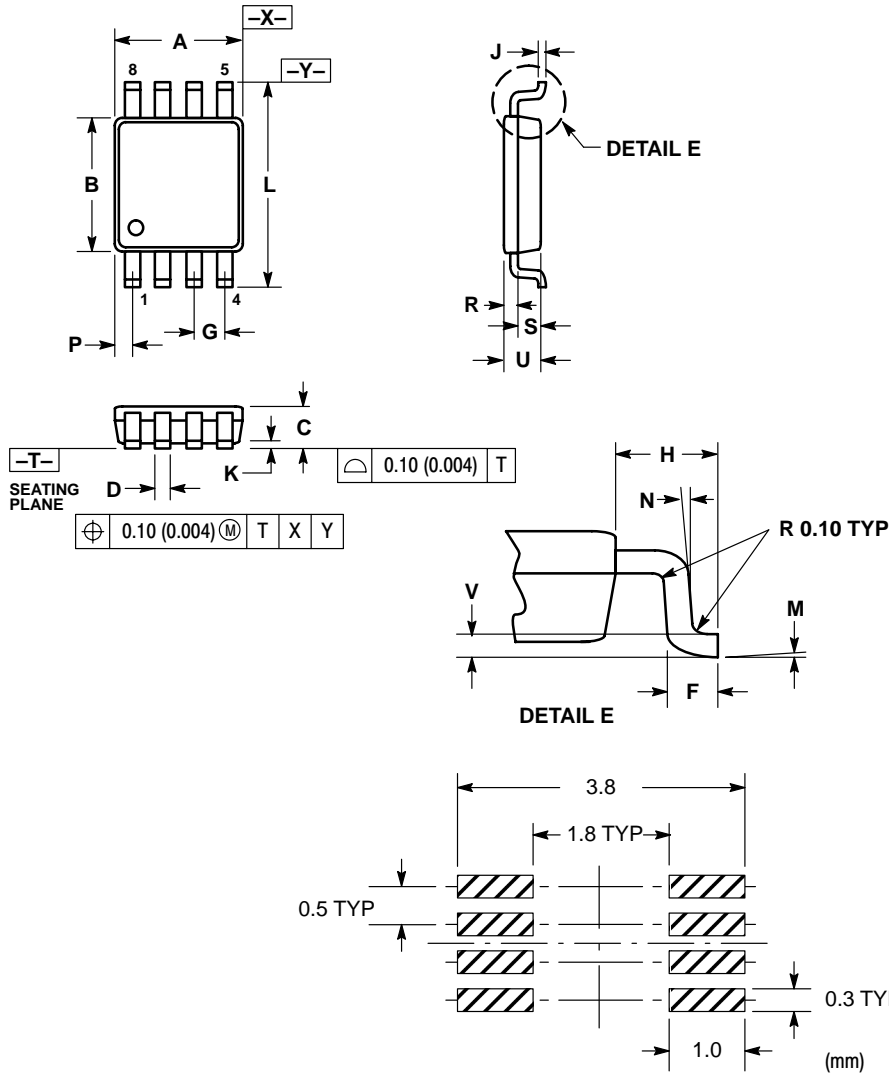


Figure 7. Reel Winding Direction

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## PACKAGE DIMENSIONS

US8  
US SUFFIX  
CASE 493-01  
ISSUE O




### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 mINCH).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED  $\pm 0.0508$  (0.0002").

NL17SZ74

**Notes**

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