NL17SZ86

Single 2-Input Exclusive-OR Gate

The NL17SZ86 is a high performance single 2–input Exclusive–OR Gate operating from a 2.3 V to 5.5 V supply.

Features

- Extremely High Speed: t_{PD} 2.4 ns (typical) at V_{CC} = 5.0 V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Over Voltage Tolerant Inputs
- L_{VTTL} Compatible – Interface Capability with 5.0 V TTL Logic with V_{CC} = 3 V
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current Substantially Reduces System Power Requirements
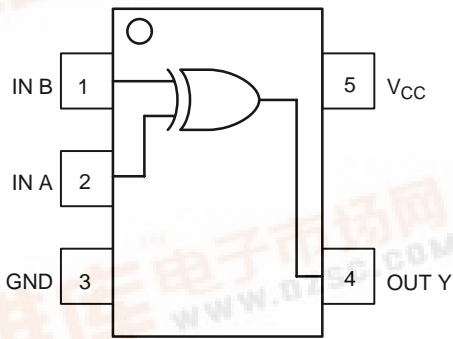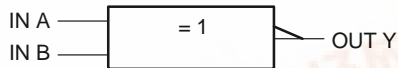- Replacement for NC7SZ86
- Pb–Free Package is Available

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

5

1

SC70–5/SC–88A/SOT–353
DF SUFFIX
CASE 419A

L8^d

Pin 1

d = Date Code
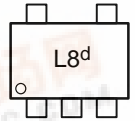
PIN ASSIGNMENT

1	IN B
2	IN A
3	GND
4	OUT Y
5	V_{CC}

Figure 1. Pinout (Top View)

Figure 2. Logic Symbol

FUNCTION TABLE

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		-0.5 to $+7.0$	V
V_I	DC Input Voltage		$-0.5\ V \leq V_I \leq +7.0\ V$	V
V_O	DC Output Voltage, Output in High or Low State (Note 1)		$-0.5\ V$ to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	$V_I < GND$	-50	mA
I_{OK}	DC Output Diode Current	$V_O < GND$	-50	mA
I_O	DC Output Sink Current		± 50	mA
I_{CC}	DC Supply Current per Supply Pin		± 100	mA
I_{GND}	DC Ground Current per Ground Pin		± 100	mA
T_{STG}	Storage Temperature Range		-65 to $+150$	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		$+150$	°C
θ_{JA}	Thermal Resistance	(Note 2)	350	°C/W
P_D	Power Dissipation in Still Air at 85°C		150	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in	
$I_{Latchup}$	Latchup Performance	Above V_{CC} and Below GND @ 85°C (Note 3)	± 500	mA
ESD	ESD Classification	Human Body Model (Note 4) Machine Model (Note 5) Charge Device Model (Note 6)	Class 1B Class B N/A	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm–by–1 inch, 2–ounce copper trace with no air flow.
3. Tested to EIA/JESD78
4. Tested to EIA/JESD22–A114–A, rated to EIA/JESD22–A114–B.
5. Tested to EIA/JESD22–A115–A, rated to EIA/JESD22–A115–B.
6. Tested to JESD22–C101–A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V_I	Input Voltage	(Note 7)	0	5.5	V
V_O	Output Voltage	(HIGH or LOW State)	0	5.5	V
T_A	Operating Free–Air Temperature		-40	$+85$	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	$V_{CC} = 2.5\ V \pm 0.2\ V$ $V_{CC} = 3.0\ V \pm 0.3\ V$ $V_{CC} = 5.0\ V \pm 0.5\ V$	0 0 0	20 10 5	ns/V

7. Unused inputs may not be left open. All inputs must be tied to a high– or low–logic input voltage level.

NL17SZ86

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V$_{CC}$ (V)	T$_A$ = 25°C			−40°C ≤ T$_A$ ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V$_{IH}$	High−Level Input Voltage		1.65 to 1.95 2.3 to 5.5	0.75 V$_{CC}$ 0.7 V$_{CC}$			0.75 V$_{CC}$ 0.7 V$_{CC}$		V
V$_{IL}$	Low−Level Input Voltage		1.65 to 1.95 2.3 to 5.5			0.25 V$_{CC}$ 0.3 V$_{CC}$		0.25 V$_{CC}$ 0.3 V$_{CC}$	V
V$_{OH}$	High−Level Output Voltage V$_{IN}$ = V$_{IL}$ or V$_{IL}$	I$_{OH}$ = 100 μA I$_{OH}$ = −3 mA I$_{OH}$ = −8 mA I$_{OH}$ = −12 mA I$_{OH}$ = −16 mA I$_{OH}$ = −24 mA I$_{OH}$ = −32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5	V$_{CC}$ − 0.1 1.29 1.9 2.2 2.4 2.3 3.8	V$_{CC}$ 1.8 2.1 2.4 2.7 2.5 4.0		V$_{CC}$ − 0.1 1.29 1.9 2.2 2.4 2.3 3.8		V
V$_{OL}$	Low−Level Output Voltage V$_{IN}$ = V$_{IH}$	I$_{OL}$ = 100 μA I$_{OL}$ = 3 mA I$_{OL}$ = 8 mA I$_{OL}$ = 12 mA I$_{OL}$ = 16 mA I$_{OL}$ = 24 mA I$_{OL}$ = 32 mA	1.65 to 5.5 1.65 2.3 2.7 3.0 3.0 4.5		0.08 0.20 0.22 0.28 0.38 0.42	0.1 0.24 0.3 0.4 0.4 0.55 0.55		0.1 0.24 0.3 0.4 0.4 0.55 0.55	V
I$_{IN}$	Input Leakage Current	V$_{IN}$ = V$_{CC}$ or GND	0 to 5.5			± 0.1		± 1.0	μA
I$_{CC}$	Quiescent Supply Current	V$_{IN}$ = V$_{CC}$ or GND	5.5			1		10	μA

AC ELECTRICAL CHARACTERISTICS t$_R$ = t$_F$ = 3.0 ns

Symbol	Parameter	Condition	V$_{CC}$ (V)	T$_A$ = 25°C			−40°C ≤ T$_A$ ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
t$_{PLH}$ t$_{PHL}$	Propagation Delay (Figure 3 and 4)	R$_L$ = 1 MΩ, C$_L$ = 15 pF	1.65	2.0	6.9	13.8	2.0	14.5	ns
		R$_L$ = 1 MΩ, C$_L$ = 15 pF	1.8	2.0	5.7	11.5	2.0	12	
		R$_L$ = 1 MΩ, C$_L$ = 15 pF	2.5 ± 0.2	1.2	4.1	7.0	1.2	7.5	
		R$_L$ = 1 MΩ, C$_L$ = 15 pF R$_L$ = 500 Ω, C$_L$ = 50 pF	3.3 ± 0.3	0.8 1.2	3.0 3.8	4.8 5.4	0.8 1.2	5.2 5.9	
		R$_L$ = 1 MΩ, C$_L$ = 15 pF R$_L$ = 500 Ω, C$_L$ = 50 pF	5.0 ± 0.5	0.5 0.8	2.2 2.9	3.5 4.2	0.5 1.0	3.8 4.6	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C$_{IN}$	Input Capacitance	V$_{CC}$ = 5.5 V, V$_I$ = 0 V or V$_{CC}$	7.0	pF
C$_{PD}$	Power Dissipation Capacitance (Note 8)	10 MHz, V$_{CC}$ = 3.3 V, V$_I$ = 0 V or V$_{CC}$ 10 MHz, V$_{CC}$ = 5.5 V, V$_I$ = 0 V or V$_{CC}$	9 11	pF

8. C$_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I$_{CC(OPR)}$ = C$_{PD}$ • V$_{CC}$ • f$_{in}$ + I$_{CC}$. C$_{PD}$ is used to determine the no−load dynamic power consumption; P$_D$ = C$_{PD}$ • V$_{CC}^2$ • f$_{in}$ + I$_{CC}$ • V$_{CC}$.
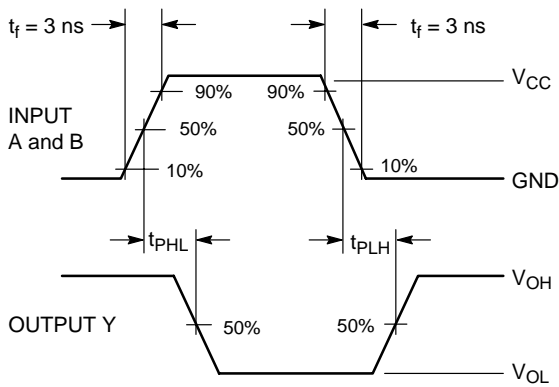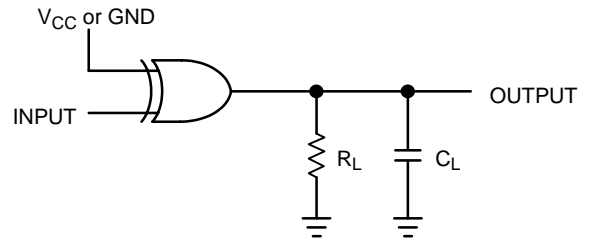
NL17SZ86

Figure 3. Switching Waveform

A 1–MHz square input wave is recommended for propagation delay tests.

**Figure 4. Test Circuit**

DEVICE ORDERING INFORMATION

| Device Order Number | Device Nomenclature | | | | | | | Package Type | Tape and Reel Size† |
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix	Tape and Reel Suffix		
NL17SZ86DFT2	NL	1	7	SZ	86	DF	T2	SC70–5/ SC–88A/ SOT–353	178 mm, 3000 Unit
NL17SZ86DFT2G	NL	1	7	SZ	86	DF	T2	SC70–5/ SC–88A/ SOT–353 (Pb–Free)	178 mm, 3000 Unit

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NL17SZ86

PACKAGE DIMENSIONS

SOT–353
DF SUFFIX
5–LEAD PACKAGE
CASE 419A–02
ISSUE G
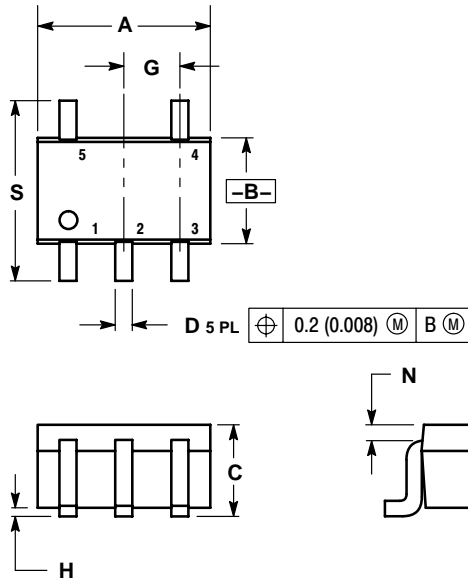
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A–01 OBSOLETE. NEW STANDARD 419A–02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

D 5 PL | ⊕ | 0.2 (0.008) Ⓜ | B Ⓜ

SOLDERING FOOTPRINT*

$\frac{0.50}{0.0197}$

$\frac{0.65}{0.025}$

$\frac{0.65}{0.025}$

$\frac{0.40}{0.0157}$

$\frac{1.9}{0.0748}$

SCALE 20:1 $\left(\frac{mm}{inches}\right)$
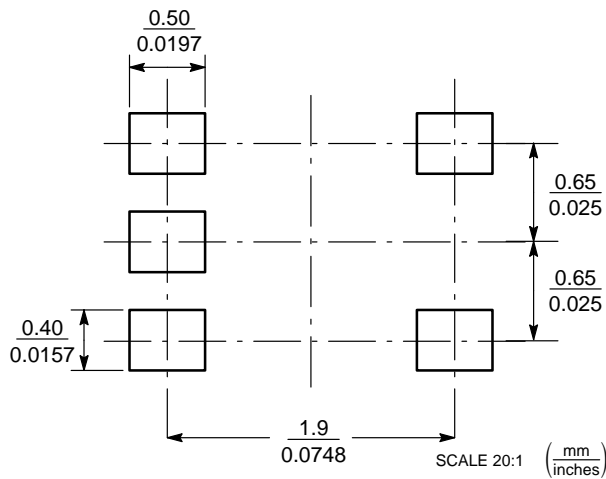
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NL17SZ86