National Semiconductor

September 1996

NM93C06LZ/C46LZ/C56LZ/C66LZ 256-/1024-/2048-/4096-Bit Serial EEPROM with Zero Power and Extended Voltage (2.7V to 5.5V) (MICROWIRE™ Bus Interface)

General Description

The NM93C06LZ/C46LZ/C56LZ/C66LZ devices are 256/1024/2048/4096 bits respectively, of CMOS non-volatile electrically erasable memory divided into 16/64/128/256 16-bit registers. They are fabricated using National Semiconductor's floating-gate CMOS process for high reliability and low power consumption. These memory devices are available in both SO and TSSOP packages for small space considerations.

The serial interface that operates these EEPROMs is MICROWIRE compatible for simple interface to standard microcontrollers and microprocessors. There are 7 instructions that control these devices: Read, Erase/Write Enable, Erase, Erase All, Write, Write All, and Erase/Write Disable. The ready/busy status is available on the DO pin to indicate the completion of a programming cycle.

Features

- Less than 1.0 μA standby current
- 2.7V–5.5V operation in all modes
- Typical active current of 100 μA
- Direct write: no erase before program
- Reliable CMOS floating gate technology
- MICROWIRE compatible serial I/O
- Self-timed programming cycle
- Device status indication during programming mode
- 40 years data retention
- Endurance: 10^6 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP
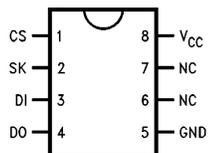
Block Diagram
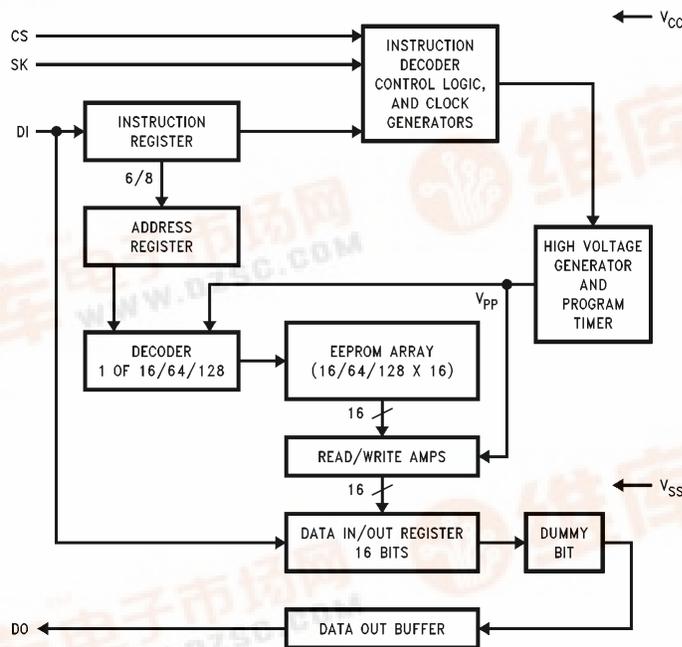
TL/D/11778–1

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MICROWIRE™ is a trademark of National Semiconductor Corporation.

Connection Diagram

Dual-in-Line Package (N)
8-Pin SO (M8) and 8-Pin TSSOP (MT8)

```
        ┌───┬───────┐
 CS  ───┤ 1     8 ├─── V_CC
 SK  ───┤ 2     7 ├─── NC
 DI  ───┤ 3     6 ├─── NC
 DO  ───┤ 4     5 ├─── GND
        └───────────┘
```

TL/D/11778–2

Top View

**See NS Package Number
N08E and M08A**

Pin Names

Pin	Description
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply

Ordering Information

Commercial Temperature Range (0°C to $+70$°C)

Order Number
NM93C06LZN/NM93C46LZN
NM93C56LZN/NM93C66LZN
NM93C06LZM8/NM93C46LZM8
NM93C56LZM8/NM93C66LZM8
NM93C06LZMT8/NM93C46LZMT8
NM93C56LZMT8/NM93C66LZMT8

Extended Temperature Range (-40°C to $+85$°C)

Order Number
NM93C06LZEN/NM93C46LZEN
NM93C56LZEN/NM93C66LZEN
NM93C06LZEM8/NM93C46LZEM8
NM93C56LZEM8/NM93C66LZEM8
NM93C06LZEMT8/NM93C46LZEMT8
NM93C56LZEMT8/NM93C66LZEMT8

Automotive Temperature Range (-40°C to $+125$°C)

Order Number
NM93C06LZVN/NM93C46LZVN
NM93C56LZVN/NM93C66LZVN
NM93C06LZVM8/NM93C46LZVM8
NM93C56LZVM8/NM93C66LZVM8
NM93C06LZVMT8/NM93C46LZVMT8
NM93C56LZVMT8/NM93C66LZVMT8

LOW VOLTAGE (2.7V ≤ 4.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	−65°C to +150°C
All Input or Output Voltage with Respect to Ground	V_{CC} + 1 to −0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature
NM93C06LZ/46LZ/56LZ/66LZ	0°C to +70°C
NM93C06LZE/46LZE/56LZE/66LZE	−40°C to +85°C
NM93C06LZV/46LZV/56LZV/66LZV	−40°C to +125°C
Power Supply (V_{CC}) Range	2.7V to 4.5V

DC and AC Electrical Characteristics

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	CS = V_{IH}, SK = 250 kHz		1 1	mA
I_{CC3}	Standby Current	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	CS = 0V		1 1	μA
I_{IL}	Input Leakage	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	V_{IN} = 0V to V_{CC}	−100	+100	nA
I_{OL}	Output Leakage	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	V_{IN} = 0V to V_{CC}	−100	+100	nA
V_{IL2}	Input Low Voltage		2V ≤ V_{CC} ≤ 4.5V	−0.1	0.15 V_{CC}	V
V_{IH2}	Input High Voltage		2V ≤ V_{CC} ≤ 4.5V	0.8 V_{CC}	V_{CC} + 1	V
V_{OL2}	Output Low Voltage		I_{OL} = 10 μA		0.2	V
V_{OH2}	Output High Voltage		I_{OH} = −10 μA	0.9 V_{CC}		V
f_{SK}	SK Clock Frequency	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V		0 0	250 250	kHz
t_{SKH}	SK High Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	(Note 2)	1 1		μs
t_{SKL}	SK Low Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	(Note 2)	1 1		μs
t_{SKS}	SK Setup Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	Relative to CS	50 50		μs
t_{CS}	Minimum CS Low Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	(Note 3)	1 1		μs
t_{CSS}	CS Setup Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	Relative to SK	0.2 0.2		μs
t_{DH}	DO Hold Time		Relative to SK	70		ns
t_{DIS}	DI Setup Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	Relative to SK	0.4 0.4		μs
t_{CSH}	CS Hold Time		Relative to SK	0		μs
t_{DIH}	DI Hold Time		Relative to SK	0.4		μs
t_{PD1}	Output Delay to "1"	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	AC Test		2 2	μs
t_{PD0}	Output Delay to "0"	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	AC Test		2 2	μs
t_{SV}	CS to Status Valid	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	AC Test		1 1	μs
t_{DF}	CS to DO in TRI-STATE®	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	AC Test CS = V_{IL}		0.4 0.4	μs
t_{WP}	Write Cycle Time	NM93C06/46/56/66LZ	V_{CC} = 2.7V		15	ms

STANDARD VOLTAGE (4.5V $\leq$ V$_{CC}$ $\leq$ 5.5V) SPECIFICATIONS

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Ambient Storage Temperature	$-65°C$ to $+150°C$
All Input or Output Voltage with Respect to Ground	V$_{CC}$ + 1 to -0.3V
Lead Temperature (Soldering, 10 sec.)	$+300°C$
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature

NM93C06LZ/46LZ/56LZ/66LZ	0°C to $+70°C$
NM93C06LZE/46LZE/56LZE/66LZE	$-40°C$ to $+85°C$
NM93C06LZV/46LZV/56LZV/66LZV	$-40°C$ to $+125°C$
Power Supply (V$_{CC}$) Range	4.5V to 5.5V

DC and AC Electrical Characteristics: 4.5V $\leq$ V$_{CC}$ $\leq$ 5.5V

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
I$_{CC1}$	Operating Current CMOS Input Levels	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	CS = V$_{IH}$, SK = 1 MHz SK = 1 MHz		2 2	mA
I$_{CC2}$	Operating Current TTL Input Levels	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	CS = V$_{IH}$, SK = 1 MHz		3 3	mA
I$_{CC3}$	Standby Current	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	CS = 0V		50 50	μA
I$_{IL}$	Input Leakage	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	V$_{IN}$ = 0V to V$_{CC}$	-2.5 -10	2.5 10	nA
I$_{OL}$	Output Leakage	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	V$_{IN}$ = 0V to V$_{CC}$	-2.5 -10	2.5 10	nA
V$_{IL}$	Input Low Voltage			-0.1	0.8	V
V$_{IH}$	Input High Voltage			2	V$_{CC}$ + 1	V
V$_{OL1}$	Output Low Voltage	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	I$_{OL}$ = 2.1 mA I$_{OH}$ = 2.1 mA		0.4 0.4	V
V$_{OH1}$	Output High Voltage		I$_{OL}$ = -400 μA	2.4		V
V$_{OL2}$	Output Low Voltage	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	I$_{OL}$ = 10 μA		0.2	V
V$_{OH2}$	Output High Voltage		I$_{OH}$ = -10 μA	0.9 V$_{CC}$		V
f$_{SK}$	SK Clock Frequency	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V		0 0	1 1	MHz
t$_{SKH}$	SK High Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V		250 300		ns
t$_{SKL}$	SK Low Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V		250 250		ns
t$_{CS}$	Minimum CS Low Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	(Note 3)	250 250		ns
t$_{CSS}$	CS Setup Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	Relative to SK	50 50		ns
t$_{DH}$	DO Hold Time		Relative to SK	70		ns

STANDARD VOLTAGE (4.5V ≤ V_{CC} ≤ 5.5V) SPECIFICATIONS (Continued)

DC and AC Electrical Characteristics V_{CC} = 5.0V ±10% unless otherwise specified (Continued)

Symbol	Parameter	Part Number	Conditions	Min	Max	Units
t_{DIS}	DI Setup Time	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	Relative to SK	100 200		ns
t_{CSH}	CS Hold Time		Relative to SK	0		ns
t_{DIH}	DI Hold Time		Relative to SK	20		ns
t_{PD1}	Output Delay to "1"	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	AC Test		500 500	ns
t_{PD0}	Output Delay to "0"	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	AC Test		500 500	ns
t_{SV}	CS to Status Valid	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	AC Test		500 500	ns
t_{DF}	CS to DO in TRI-STATE	NM93C06/46/56/66LZ NM93C06/46/56/66LZE/V	AC Test CS = V_{IL}		100 100	ns
t_{WP}	Write Cycle Time				10	ms

AC Test Conditions

Output Load: 1 TTL Gate and C_L = 100 pF	
V_{CC} Range	**AC Test Conditions**
4.5V < V_{CC} < 5.5V	Input Pulse Levels 0.8V and 2.0V Timing Measurement Level (V_{IL}/V_{IH}) 0.9V and 1.9V Timing Measurement Level (V_{OL}/V_{OH}) 0.8V and 2.0V (TTL Load Condition: I_{OL} = 2.1 mA, I_{OH} = −0.4 mA)
2.7V < V_{CC} < 4.5V	Input Pulse Levels 0.3V and 0.8 V_{CC} Timing Measurement Level (V_{IL}/V_{IH}) 0.4V and 1.6V Timing Measurement Level (V_{OL}/V_{OH}) 0.8V and 1.6V (CMOS Load Condition: I_{OL} = 10 μA, I_{OH} = −10 μA)

Capacitance T_A = 25°C, f = 1 MHz

Symbol	Test	Max	Units
C_{OUT}	Output Capacitance	5	pF
C_{IN}	Input Capacitance	5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Minimum V_{CC} requirements: All functional modes are guaranteed to full operation at V_{CC} ≥ 2V except the bulk programming op-codes ERAL and WRAL. These are regarded as test mode commands and are only guaranteed to V_{CC} ≥ 2.5V.

Note 3: CS must be brought low for a minimum of 1 t_{CS} between consecutive instruction cycles.

Functional Description

The NM93C06/C46/C56/C66LZ devices have 7 instructions as described below. Note that the MSB of any instruction is a ''1'' and is viewed as a start bit in the interface sequence. For the C06LZ and C46LZ the next 8 bits carry the op code and the 6-bit address for register selection. For the C56LZ and C66LZ the next 10 bits carry the op code and the 8-bit address for register selection.

Read (READ): The READ instruction outputs serial data on the DO pin. After the READ instruction is received, the instruction and address are decoded, followed by data transfer from the selected memory register into a serial-out shift register. A dummy bit (logical 0) precedes the 16-bit data output string. Output data changes are initiated by a low to high transition of the SK clock.

Erase/Write Enable (EWEN): When V_{CC} is applied to the part, it powers up in the Erase/Write Disable (EWDS) state. Therefore, all programming modes must be preceded by an Erase/Write Enable (EWEN) instruction. Once an Erase/Write Enable instruction is executed, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or until V_{CC} is removed from the part.

Erase (ERASE): The ERASE instruction will program all bits in the specified register to the logical ''1'' state. CS is brought low following the loading of the last address bit. This falling edge of the CS pin initiates the self-timed programming cycle.

The DO pin indicates the READY/BUSY status of the chip. DO = logical ''0'' indicates that programming is still in progress. DO = logical ''1'' indicates that the register, at the address specified in the instruction, has been erased, and the part is ready for another instruction.

Write (WRITE): The WRITE instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the data-in (DI) pin, CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. The DO pin indicates the READY/BUSY status of the chip if CS is brought high after a minimum of 250 ns (t_{CS}). DO = logical 0 indicates that programming is still in progress. DO = 1 indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction.

Erase All (ERAL): The ERAL instruction will simultaneously program all registers in the memory array and set each bit to the logical ''1'' state. The Erase All cycle is identical to the ERASE cycle except for the different op code. As in the ERASE mode, the DO pin indicates the READY/BUSY status of the chip. The ERASE ALL instruction is not required, see note below.

Write All (WRAL): The WRAL instruction will simultaneously program all registers with the data pattern specified in the instruction. As in the WRITE mode, the DO pin indicates the READY/BUSY status of the chip.

Erase/Write Disable (EWDS): To protect against accidental data disturb, the (EWDS) instruction disables all programming modes and should follow all programming operations. Execution of a READ instruction is independent of both the EWEN and EWDS instructions.

Note: The NM93C06/C46/C56/C66LZ devices do not require an ''ERASE'' or ''ERASE ALL'' prior to the ''WRITE'' or ''WRITE ALL'' instructions.

## Instruction Set for the NM93C06LZ and NM93C46LZ

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5–A0		Read data stored in memory, at specified address
EWEN	1	00	11XXXX		Write enable must precede all programming modes
EWDS	1	11	A5–A0		Erase register A5, A4, A3, A2, A1, A0
WRITE	1	01	A5–A0	D15–D0	Writes register
ERAL	1	00	10XXXX		Erases all registers
WRAL	1	00	01XXXX	D15–D0	Writes all registers
EWDS	1	00	00XXXX		Disables all programming instructions

Instruction Set for the NM93C56LZ and NM93C66LZ

| Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A7–A0		Read data stored in memory, at specified address
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes
EWDS	1	11	A7–A0		Erase selected register
ERAL	1	00	10XXXXXX		Erases all registers
WRITE	1	01	A7–A0	D15–D0	Write register if address is unprotected
WRAL	1	00	01XXXXXX	D15–D0	Writes all registers
EWDS	1	00	00XXXXXX		Disables all programming instructions

Timing Diagrams

Synchronous Data Timing
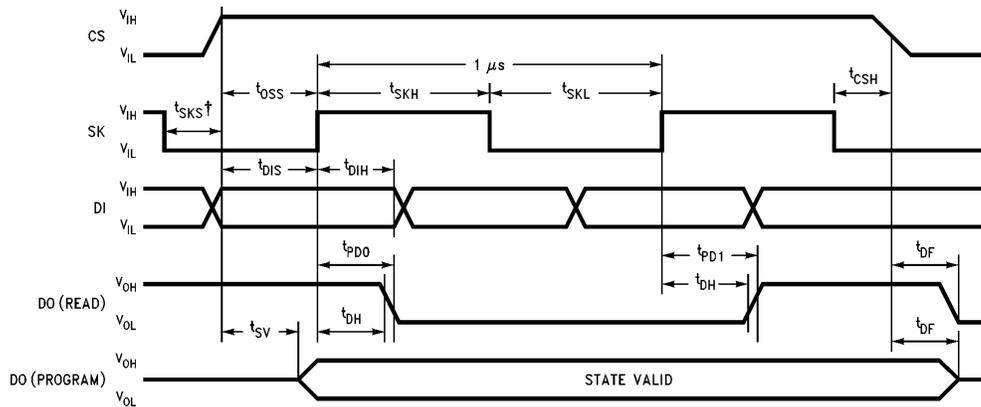
TL/D/11778–3

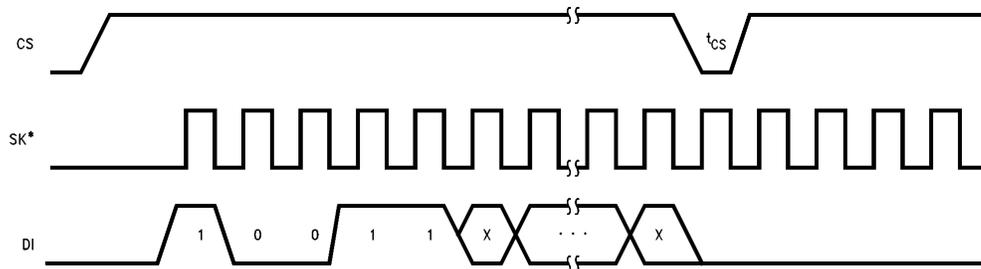†t_{SKS} is not needed if DI = V_{IL} when CS is going active (HIGH).

READ
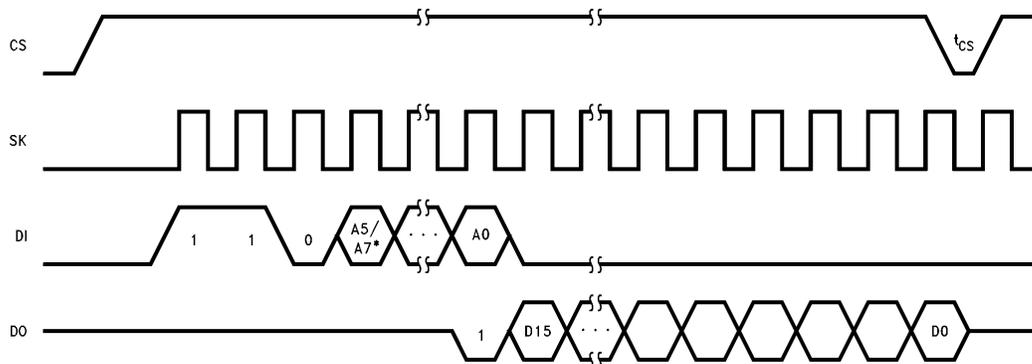
TL/D/11778–4

*Address bits A5 and A4 become "don't care" for NM93C06LZ.
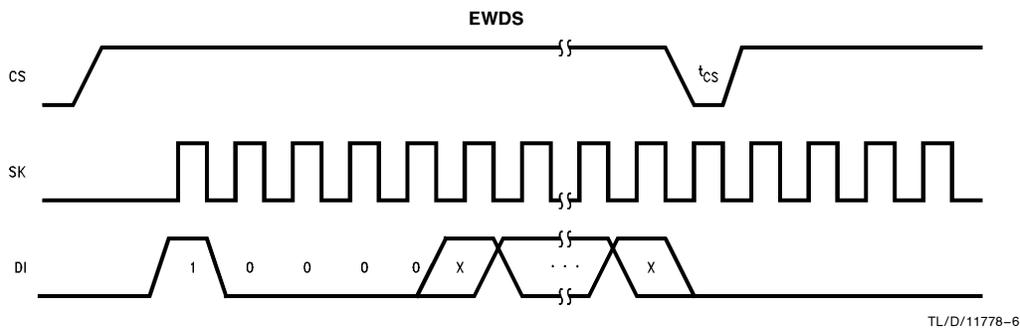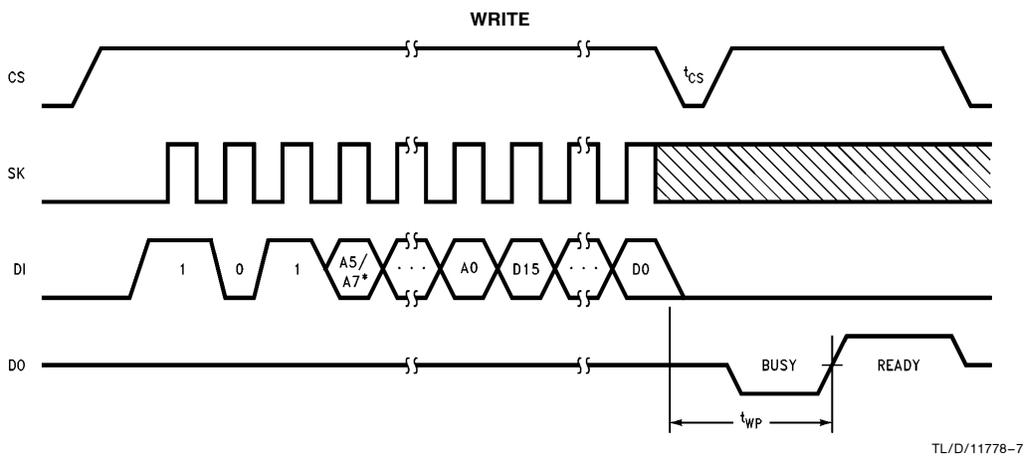 Address bit A7 becomes a "don't care" for NM93C56LZ.

EWEN

TL/D/11778–5

*The NM93C56LZ and NM93C66LZ require a minimum of 11 clock cycles. The NM93C06LZ and NM93C46LZ require a minimum of 9 clock cycles.
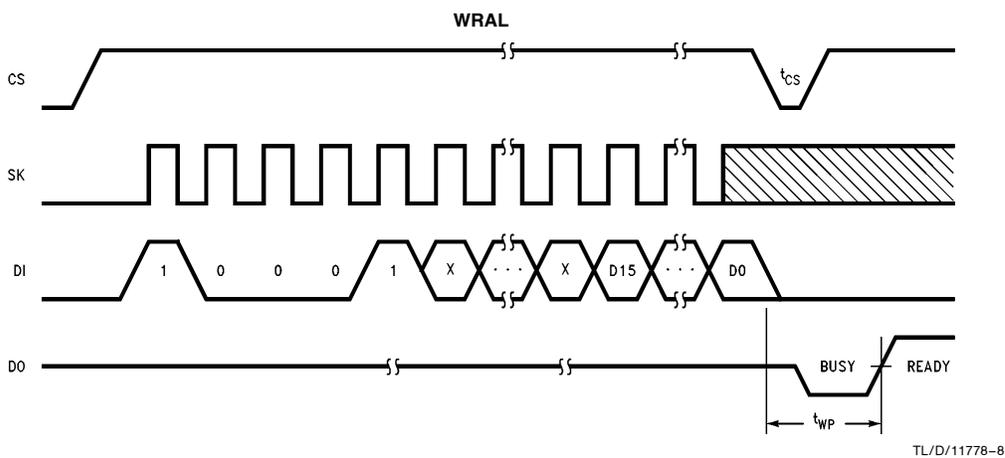
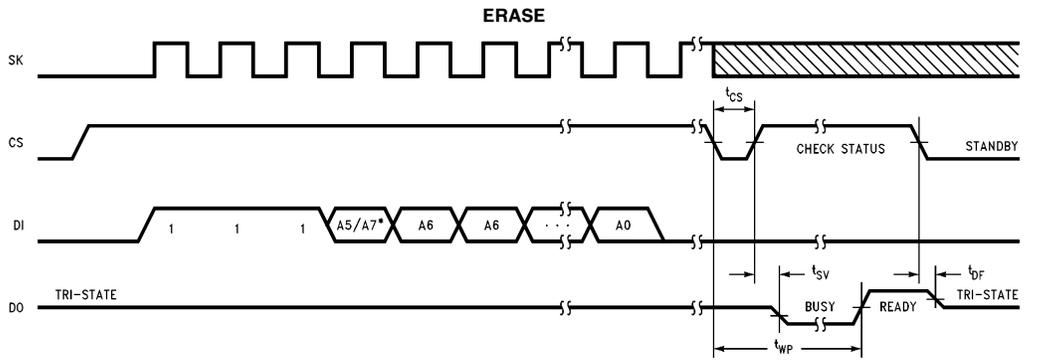http://www.national.com

Timing Diagrams (Continued)

EWDS

TL/D/11778–6

*The NM93C56LZ and NM93C66LZ require a minimum of 11 clock cycles. The NM93C06LZ and NM93C46LZ require a minimum of 9 clock cycles.

WRITE

TL/D/11778–7

*Address bits A5 and A4 become ''don't care'' for NM93C06LZ.
 Address bit A7 becomes a ''don't care'' for NM93C56LZ.

WRAL

TL/D/11778–8

Timing Diagrams (Continued)

ERASE

*Address bits A5 and A4 become "don't care" for NM93C06LZ.
 Address bit A7 becomes a "don't care" for NM93C56LZ.

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ERAL

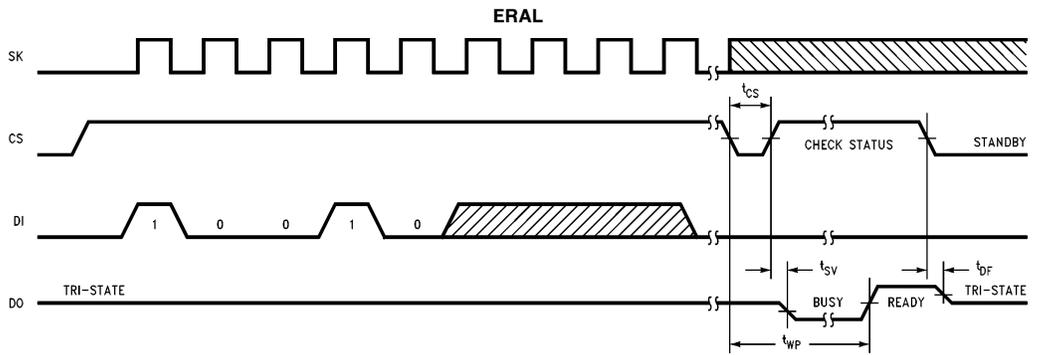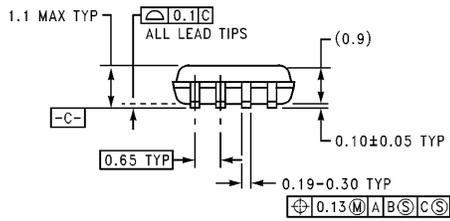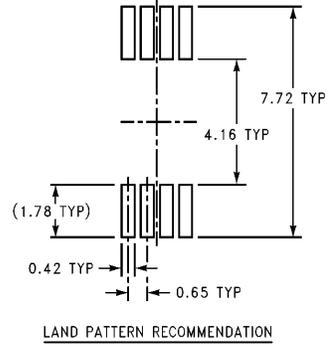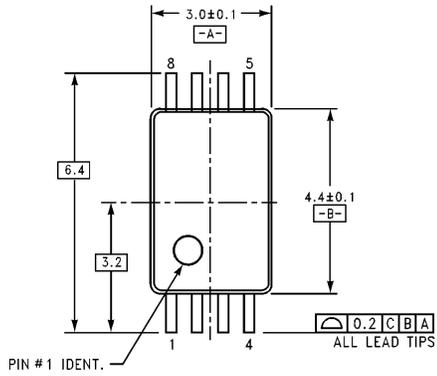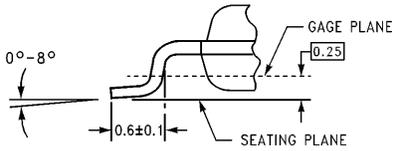TL/D/11778–10

Physical Dimensions inches (millimeters) unless otherwise noted

0.189 − 0.197
(4.800 − 5.004)

8 7 6 5

0.228 − 0.244
(5.791 − 6.198)

0.010 MAX
(0.254)

LEAD NO. 1
IDENT

1 2 3 4

30°
TYP

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008 TYP
(0.203)

0.014 − 0.020 TYP
(0.356 − 0.508)

M08A (REV H)

Molded Small Out-Line Package (M8)
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

3.0±0.1
-A-

8   5

6.4

4.4±0.1
-B-

3.2

PIN #1 IDENT.

| ⌒ | 0.2 | C | B | A |

ALL LEAD TIPS

1   4

7.72 TYP

4.16 TYP

(1.78 TYP)

0.42 TYP

0.65 TYP

LAND PATTERN RECOMMENDATION

1.1 MAX TYP

| ⌒ | 0.1 | C |

ALL LEAD TIPS

(0.9)

-C-

0.10±0.05 TYP

0.65 TYP

0.19-0.30 TYP

| ⊕ | 0.13 Ⓜ | A | BⓈ | CⓈ |

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.09-0.20 TYP

0°-8°
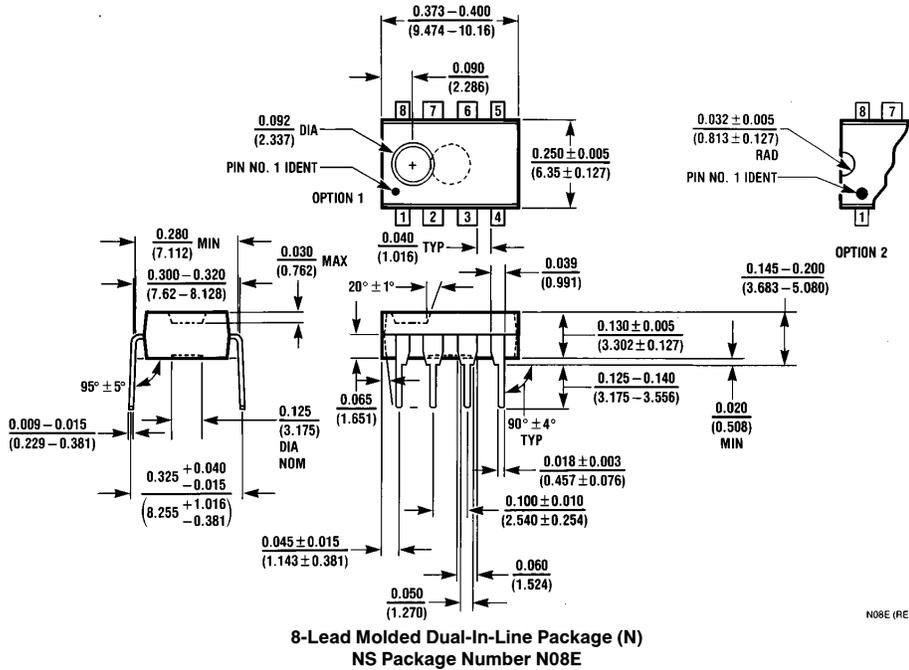
GAGE PLANE

0.25

0.6±0.1

SEATING PLANE
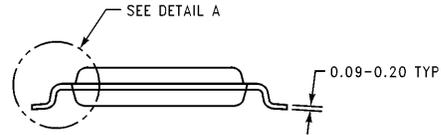
DETAIL A
TYPICAL, SCALE : 40X

MTC08 (REV A)

Note: Unless otherwise specified
1. Reference JEDEC Registration M0-153, Variation AA, Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
NS Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.373 – 0.400
(9.474 – 10.16)

0.090
(2.286)

0.092
(2.337) DIA

PIN NO. 1 IDENT

OPTION 1

0.250 ± 0.005
(6.35 ± 0.127)

0.032 ± 0.005
(0.813 ± 0.127) RAD

PIN NO. 1 IDENT

OPTION 2

0.280
(7.112) MIN

0.300 – 0.320
(7.62 – 8.128)

0.030
(0.762) MAX

0.040
(1.016) TYP

0.039
(0.991)

0.145 – 0.200
(3.683 – 5.080)

20° ± 1°

0.130 ± 0.005
(3.302 ± 0.127)

95° ± 5°

0.009 – 0.015
(0.229 – 0.381)

0.125
(3.175) DIA NOM

0.065
(1.651)

0.125 – 0.140
(3.175 – 3.556)

0.020
(0.508) MIN

90° ± 4° TYP

0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

0.018 ± 0.003
(0.457 ± 0.076)

0.100 ± 0.010
(2.540 ± 0.254)

0.045 ± 0.015
(1.143 ± 0.381)

0.050
(1.270)

0.060
(1.524)

N08E (REV F)

8-Lead Molded Dual-In-Line Package (N)
NS Package Number N08E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.