

Single chip 868 MHz Transmitter

nRF902

FEATURES

- True single chip FSK/ASK transmitter in a small 8-pin package
- Adjustable output power up to +10dBm
- FSK data rate up to 50kbits/s
- Very few external components
- On-chip frequency synthesiser gives improved frequency stability compared to SAW solutions
- Wide power supply range: 2.4 to 3.6 V
- Low supply current, typical 9mA
 @ -10dBm output power
- Power Down and Clock modes makes power saving easy
- Reference Clock output pin for microcontroller

APPLICATIONS

- Automatic Meter Reading
- Keyless entry
- Wireless data communication
- Alarm and security systems
- Home Automation
- Remote control
- Surveillance
- Automotive
- Telemetry
- Toys

GENERAL DESCRIPTION

nRF902 is a single-chip transmitter for the 868 MHz ISM band, designed to comply with the ETSI specification I-ETS 300 220. Using nRF902 both FSK and ASK modulation is possible. The transmitter consists of a fully integrated frequency synthesiser, a power amplifier, a crystal oscillator and a modulator. Few external components are required: a 13.567 MHz crystal, two resistors and some decoupling capacitors. Due to the use of the crystal-oscillator stabilised frequency synthesiser, frequency drift is much lower than in comparable SAW-resonator based solutions. Output power is easily programmable by use of an external resistor. Current consumption is very low, only 9 mA at an output power of –10dBm. Built-in Clock and Power Down modes makes power saving and duty-cycling easily realisable.

OUICK REFERENCE DATA

Value	Unit
2.4	V
10	dBm
50	kbit/s
10	kbit/s
9	mA
200	μΑ
<10	nA
	2.4 10 50 10 9

Table 1. nRF902 quick reference data

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BLOCK DIAGRAM

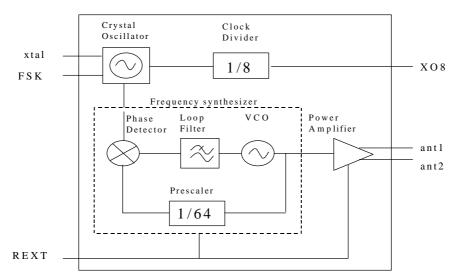


Figure 1. nRF902 block diagram

PIN FUNCTIONS

Pin	Name	Pin function	Description
1	xtal	Input	Crystal pin / Power Up
2	REXT	Input	Power adjust / Clock Mode / ASK modulation digital input
3	XO8	Output	Reference Clock Output (Crystal Frequency / 8)
4	VDD	Input	Positive Supply (2.4 - 3.6V)
5	FSK	Input	Digital Data Input
6	ant2	Power/Output	Antenna output 1
7	ant1	Power/Output	Antenna output 2
8	VSS	Power	Ground (0V)

Table 2. nRF902 pin functions

PIN ASSIGNMENT

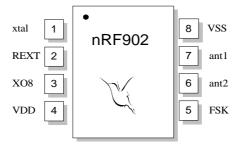


Figure 2. nRF902 pin assignment

ELECTRICAL SPECIFICATIONS

Conditions: VDD = +3V, VSS = 0V, $T_A = -40$ °C to +85°C

Symbol	Parameter (condition)	Notes	Min.	Тур.	Max.	Units
	Operating conditions	1				
f_{TX}	Transmit frequency	1)	868		870	MHz
f_{XTAL}	Crystal frequency	1)	13.563		13.593	MHz
$V_{ m DD}$	Supply voltage		2.4		3.6	V
Tamb	Operating temperature		- 40		+ 85	°C
P_{RF}	Maximum Output Power	3)			10	dBm
I_{DD}	Supply current CLOCK Mode	2)		200	300	μΑ
I_{DD}	Supply current POWER DOWN Mode			10	100	nA
	FSK modulation	Т				
Δf	Frequency deviation		10	20	30	kHz
R_{FSK}	FSK data rate				50	kbit/s
I_{DD}	Supply current @ 10dBm output power	3)		30	37	mA
I_{DD}	Supply current @ -10dBm output power	3)		9	17	mA
	ASK modulation					
R _{ASK}	ASK data rate		0		10	kbit/s
P _{RF1}	Transmitted power at data = '1'				10	dBm
P_{RF0}	Transmitted power at data = '0'				-50	dBm
I_{DD}	Supply current @ 10dBm output power	3)		30	37	mA
I_{DD}	Supply current @ -50dBm output power	3)		200	300	uA
	FSK input pin					
V _{IH}	HIGH level input voltage		V _{DD} - 0.5		V_{DD}	V
$V_{\rm IL}$	LOW level input voltage		Vss		0.3	V
V _{OH}	HIGH level output voltage		V _{DD} - 0.5		V_{DD}	V
V _{OL}	LOW level output voltage		Vss		0.3	V

NOTES:

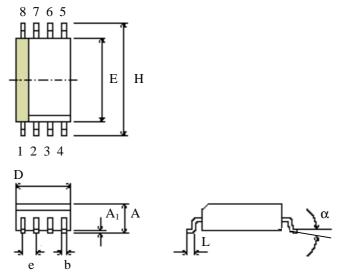
- The crystal frequency may be altered to produce any desired frequency within the 868MHz to 870MHz band.
 Measured with no load on XO8 output pin.
- 3) Antenna load impedance = 400Ω .

Table 3. nRF902 electrical specifications



PACKAGE OUTLINE

nRF902, uses the SOIC 8 package. Dimensions are in mm.



Package Type		D	E	Н	A	$\mathbf{A_1}$	e	b	L	Copl.	α
SOIC 8	Min	4.80	3.81	5.84	1.55	0.127	1.27	0.35	0.41		0°
	Max	4.98	3.99	6.20	1.73	0.250	1.27	0.49	0.89	0.25	8°

Figure 3. Package outline.

Absolute Maximum Ratings

Supply voltages	Total Power Dissipation
VDD 0.3V to + 6V	$P_D(T_A=85^{\circ}C)220mW$
VSS0V	
Input voltage V_1 0.3V to VDD + 0.3V	Temperatures Operating Temperature 40°C to + 85°C Storage Temperature 40°C to + 125°C
Output voltage	
V_0 0.3V to VDD + 0.3V	

Note: Stress exceeding one or more of the limiting values may cause permanent damage to the device.

ATTENTION!

Electrostatic Sensitive Device Observe Precaution for handling.



IMPORTANT TIMING DATA

Timing information

The timing information for the different operations is summarised in Table 4. (TX is Transmit mode, Clk is Clock mode, Pwr_Dn is Power Down Mode.)

Change of Mode	Max Delay
Pwr_Dn → TX	2ms
Clk → TX	30us

Table 4 Switching times for nRF902

Switching between Power Down Mode and Transmit-mode.

The maximum time from Power Down mode until the synthesised frequency is stable and data can be transmitted is seen in Figure 4.

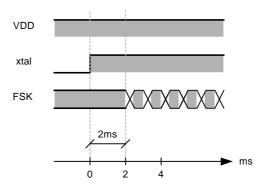


Figure 4. Timing diagram when going from Power Down mode to Transmit-mode

Switching between Clock Mode and Transmit-mode.

The maximum time from Clock mode until the synthesised frequency is stable and data can be transmitted is seen in Figure 5.

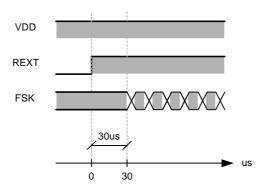


Figure 5. Timing diagram when going from Clock mode to Transmit-mode

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APPLICATION INFORMATION

FSK Transmit mode

FSK modulation is realised by feeding the modulating data to the digital FSK input pin (see Figure 6).

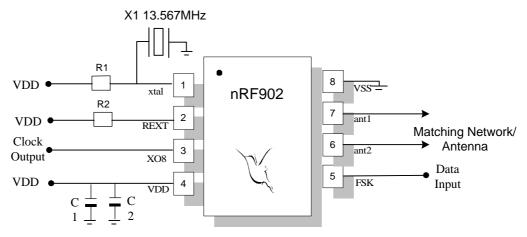


Figure 6. FSK transmitter in FSK Transmit mode

In applications where high data rate and low spectrum bandwidth is required an external varactor may be used to modulate the crystal. For optimum bandwidth usage a low pass filter should be used to shape the input bit stream, (see Figure 7).

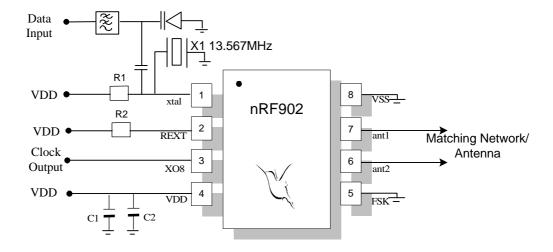


Figure 7. FSK transmitter in FSK Transmit mode for low spectral bandwidth



ASK modulation.

ASK modulation can be realised by using the REXT pin (see Figure 8). When R2 is connected to VDD, the chip transmits a carrier. When the bias resistor is connected to VSS then the internal output power amplifier is turned off. These two situations represent logic '1' and logic '0' in an ASK system. When ASK modulation is used, the FSK pin must be connected to VDD.

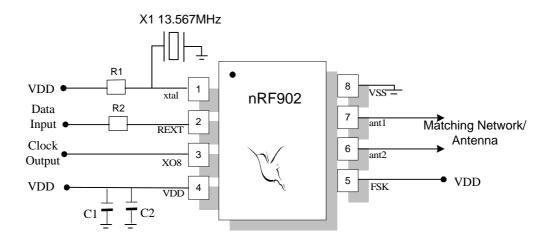


Figure 8. FSK transmitter in ASK Transmit mode

Antenna output

The "ant" output pins provide a balanced RF output to the antenna. The pins must have a DC path to V_{DD} , either via a RF choke or via the centre point in a loop antenna. The load impedance seen between the ant1/ant2 outputs should be in the range 200-700 Ω . A load impedance of 400 Ω is recommended if maximum output power (10dBm) is needed. Lower load impedance (for instance 50 Ω) can be obtained by fitting a simple matching network or a RF transformer (balun). The 50 Ω load can also be connected directly between the ant1/ant2 pins, but this will result in higher current consumption for a given output power to the antenna.

Note: Application notes of antenna layout solutions with matching networks will soon be available on our website: http://www.nvlsi.no.

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Power Down mode

Power Down mode is used to achieve very low current consumption. Effectively the chip is disabled with minimal leakage current consumption, typically less than 10nA. Operating in this mode when not transmitting data, i.e. low duty cycle systems can significantly increase battery lifetime.

The resistor R1 connected from the crystal pin towards VDD supplies the crystal oscillator with bias current (see Figure 9). When this resistor is connected to VSS or left open, the chip enters Power Down mode. As shown in Figure 9 the resistor R1 is connected to the "Power Down" terminal, this can be controlled by a micro-controller, hence eliminating the need to switch off the power supply to the chip when not transmitting. Start-up time when switching from Power Down mode to Transmit mode is approximately 2 ms.

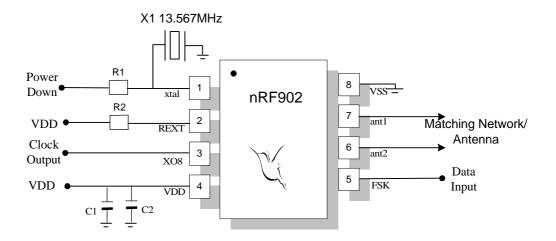


Figure 9. FSK transmitter in Power Down mode

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Clock mode

Clock mode is available so that an external microprocessor may have a reference signal without the cost of a second crystal. In Clock mode, the crystal oscillator and reference clock outputs are operating, while the rest of the transmitter is disabled. The reference signal from the internal crystal oscillator is divided by 8 by use of a prescaler, this signal is available at the XO8 pin.

Clock mode may be set by connecting the power adjusting resistor R2 to ground or by leaving it open (see Figure 10). Current consumption in Clock mode is typically 200 μ A when no load is applied at the XO8 clock output pin. If a capacitive load is applied at the XO8 output, then current consumption in Clock mode will increase. Start-up time when switching between Clock mode and Transmit mode is extremely fast, typically 30 μ s.

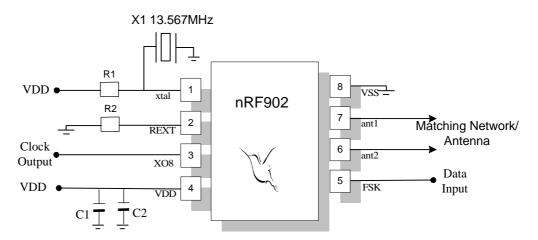


Figure 10. FSK transmitter in Clock mode

XO8 Clock Output Pin Capacitance

The frequency of the clock signal is 1/8th of the crystal frequency i.e. a crystal frequency of 13.567 MHz will result in an output clock frequency of 1.695 MHz. The XO8 output signal will be present in Transmit mode and Clock mode. In Power Down mode the XO8 signal will be a logic "0".

The capacitive load at the XO8 pin will affect current consumption in Clock mode. If the pin is left open the current consumption will typically be 200uA. Adding a capacitive load, such as microcontroller load [C_{ML}] to the XO8 pin will result in an increase in the current consumption, the increase ΔI is given as:

$$\Delta I = f_{XO8} \cdot VDD \cdot C_{ML}$$

Example

With a capacitive load of $C_{ML} = 5pF$, using VDD=3.0 V and a 13.567 MHz crystal, the current increase ΔI becomes :

$$\Delta I = f_{XO8} \cdot VDD \cdot C_{ML} = ((13.567 \text{ MHz}) / 8) \cdot 3.0 \text{ V} \cdot 5 \text{ pF} = 25 \text{ uA}.$$

The typical current consumption will increase to 225uA when adding $C_{ML}=5$ pF.



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Crystal Specification

Modulation is achieved by pulling of the crystal capacitance. As such to achieve correct frequency deviation (20kHz) and frequency of operation as specified in Table 3 the crystal must meet the following specification:

 $Co \le 3 pF$ Crystal parallel equivalent capacitor $ESR \leq 50 \ ohm$. Crystal equivalent series resistor

 $C_{T} = 12 \, pF$ Crystal load capacitor

Output Power adjustment

A bias resistor R2 (see Figure 6) should be connected from the REXT pin to the positive power supply VDD. The value of this resistor determines the output power level. See table 5 for choice of R2 value.

Power setting resistor R2	RF output power	DC current consumption
$22\mathrm{k}\Omega$	10dBm	30mA
82kΩ	0dBm	15mA
180kΩ	-10dBm	9mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27°C, Load impedance = 400 Ω .

Table 5. RF output power setting for the nRF902.

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DEFINITIONS

Data sheet status		
Objective product specification	This datasheet contains target specifications for product development.	
Preliminary product	This datasheet contains preliminary data; supplementary data may be	
specification	published from Nordic VLSI ASA later.	
Product specification	This datasheet contains final product specifications. Nordic VLSI ASA	
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Limiting values		
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application information		
Where application information is given, it is advisory and does not form part of the specification.		

Table 6. Definitions.

Nordic VLSI ASA reserves the right to make changes without further notice to the product to improve reliability, function or design. Nordic VLSI does not assume any liability arising out of the application or use of any product or circuits described herein.

LIFE SUPPORT APPLICATIONS

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Preliminary specification: Revision Date: 06/04/2000.

Datasheet order code: 060400-nRF902.

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YOUR NOTES

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Revision 1.0 April 2000