NT7181 Specification

V 2.1

NOVATEK MICROELECTRONICS CORP.

1 Features

- 28:4 Data Channel Compression at up to 297 Megabytes per Second Throughput
- Suited for VGA, SVGA, XGA and Dual pixel SXGA, UXGA Display Data Transmission From Controller to Display With Very Low EMI
- 28 Data Channels and Clock-In Low-Voltage TTL and 4 Data Channels and Clock-Out Low-Voltage Differential
- Operates From a Single 3.3V Supply With 250mW (Typ)
- Low profile 56 Lead TSSOP Package
- Clock edge Programmable for Transmitter
- Wide Phase-Lock Input Frequency Range: 25 MHz To 85 MHz
- Supports Spread Spectrum Clock Generator
- Suggests to use for LCD monitor only
- No External Components Required for PLL

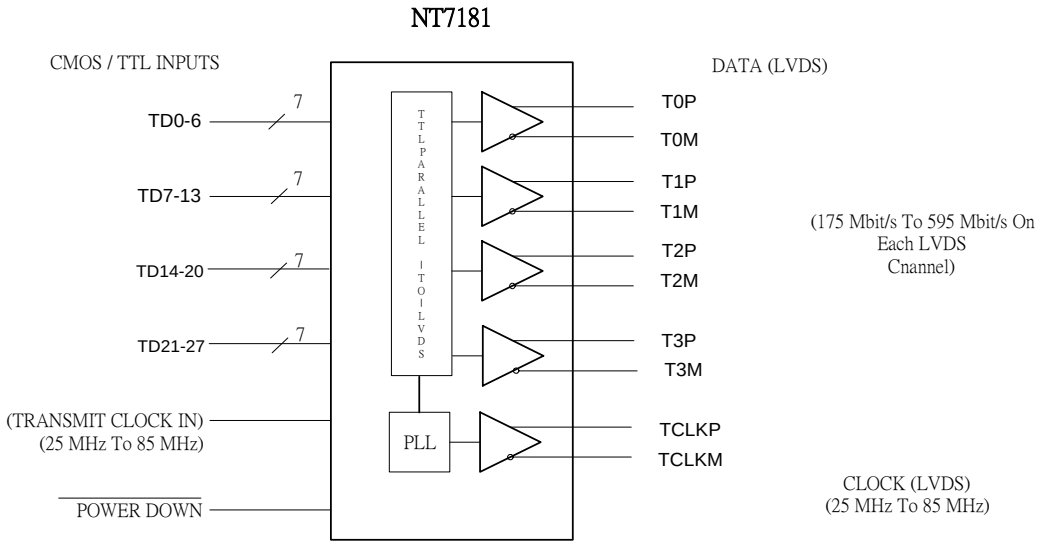
2 General Description

The NT7181 transmitter contains four 7-bit parallel-load serial-out registers, a 7x clock synthesizer, and five low-voltage differential (LVDS) line in a single integrated circuit. These functions allow 28 bits of single-ended low-voltage TTL (LVTTL) data to be synchronously transmitted over four balanced-pair conductors for receipt by a compatible receiver, such as the DS90CF386 or THC63LVDF84A.The NT7181 transmitter is offered with programmable edge data strobes for convenient interface with a variety of graphic controllers. The NT7181 transmitter can be programmed for rising edge strobe(RFB=1) or falling edge strobe(RFB=0) through the RFB pin. When transmitting, data bits D0 - D27 are each loaded into registers of the NT7181 on the rising edge or falling edge of the input clock signal (CLKIN). The frequency of CLKIN is multiplied seven times and then used to unload the data registers in 7-bit slices and serially. The four serial streams and a phase-locked clock (TCLK) are then output to LVDS output drivers. The frequency of TCLK is the same as the input clock, CLKIN.

The NT7181 requires no external components and little or no control. The data bus appears the same at the input to the transmitting and output of the receiver with the data transmission transparent to the user. The only user intervention is the possible use of the shutdown/clear ($\overline{\text{PWDN}}$) active-low input to inhibit the clock and shut off the LVDS output drivers for lower power consumption. A low level on this signal clears all internal registers to a low level.

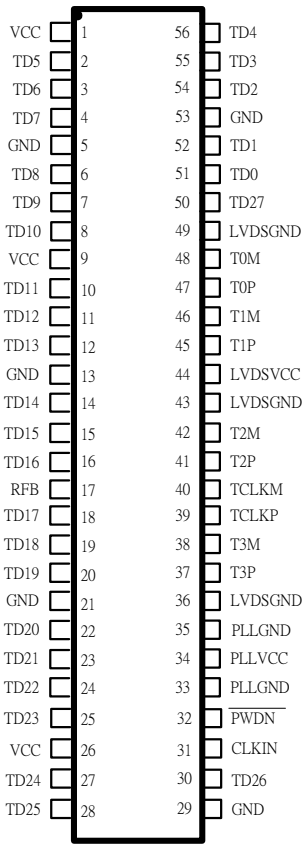
The NT7181 are characterized for operation over free-air temperature ranges of 0°C to 70°C.

2.1 Block Diagrams



3 Pin Configuration

NT7181



4 Absolute Maximum Ratings

Supply voltage range, V_{CC} (see Note1)……..-0.3V to 4V
Output voltage range, V_O……-0.3V to Vcc +0.3V
Input voltage range, V_I……-0.3V to Vcc +0.3V
Storage temperature range, Tstg……-65°C to 150°C
Lead temperature 1, 6 mm (1/16 inch) from case for 10 seconds……260°C
Junction Temperature……150°C

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

4.1 Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit
VCC	Supply voltage	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
Z_L	Differential load impedance	90	100	110	Ω
T_A	Operating free-air temperature	0		70	°C

4.2 Timing requirements

Symbol	Parameter	Min.	Nom.	Max.	Unit
T_C	Cycle time, input clock	11.8		40	ns
t_W	Pulse duration, high-level input clock	$0.4t_C$		$0.6t_C$	ns
t_T	Transition,			5	ns
t_{su}	Setup time, data, TD0 - TD27 valid before CLKIN ↑ or CLKIN ↓ (See Figure 1)	5			ns
t_h	Hold time, data, , TD0 - TD27 valid after CLKIN ↑ or CLKIN ↓ (See Figure 1)	2.5			ns

Note: t_h is measured under the conditions of input clock jitter of 1.9ns at 65MHz.

5 Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$\|V_{OD}\|$	Differential Steady-state Output Voltage Magnitude	240		490	mV	R_L = 100Ω, See Figure 2
$\triangle\|V_{OD}\|$	Change in the Steady-state Differential Output Voltage Magnitude between Opposite binary States			35	mV	
$V_{OC(SS)}$	Steady-state Common-mode Output Voltage	1.125		1.475	V	See Figure 2
$V_{OC(PP)}$	Peak-to-peak Common-mode Output Voltage		80	150	mV	
I_{IH}	High-level Input Current			20	μA	V_{IH} = VCC
I_{IL}	Low-level Input Current			±30	μA	V_{IL} = 0
I_{OS}	Short-circuit Output Current			±24	mA	$V_{O(TP)}$ = 0
				±12	mA	V_{OD} = 0
I_{OZ}	High-impedance State Output Current		±1		μA	V_O = 0 to Vcc
I_{CC}	Quiescent Supply Current		280		uA	Disables, All inputs at GND
			68	80	mA	Enables, R_L = 100Ω, Gray-scale pattern (see Figure 3), VCC = 3.3V, t_c = 15.38ns
			75	110	mA	Enabled, R_L = 100Ω, (4 places) Worst-case pattern (see Figure 4), t_c = 15.38ns

*All typical values are at VCC = 3.3V, T_A = 25°C

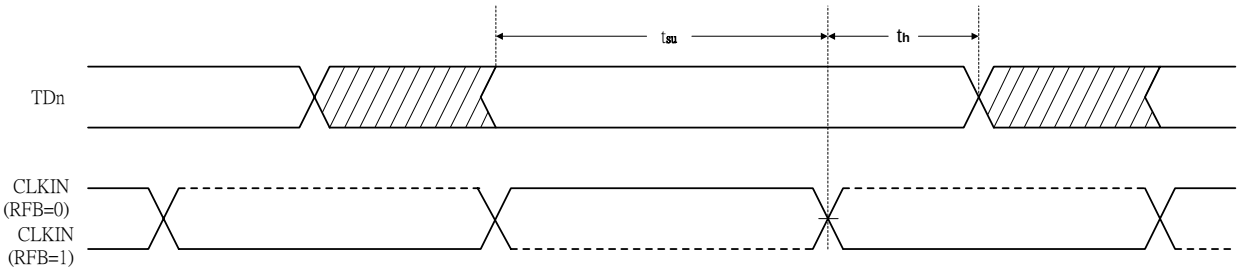
6 Swing Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.*	Max.	Unit	Conditions
t_{d0}	Delay Time, TCLK↓ to Serial Bit Position 0	-0.4		0.3	ns	t_c = 15.38 ns (± 0.2%), |Input Clock Jitter| < 50 ps** See Figure 5
t_{d1}	Delay Time, TCLK↓ to Serial Bit Position 1	1.8		2.5	ns	
t_{d2}	Delay Time, TCLK↓ to Serial Bit Position 2	4.0		4.7	ns	
t_{d3}	Delay Time, TCLK↓ to Serial Bit Position 3	6.2		6.9	ns	
t_{d4}	Delay Time, TCLK↓ to Serial Bit Position 4	8.4		9.1	ns	
t_{d5}	Delay Time, TCLK↓ to Serial Bit Position 5	10.6		11.3	ns	
t_{d6}	Delay Time, TCLK↓ to Serial Bit Position 6	12.8		13.5	ns	
t_{d7}	Delay Time, CLKIN↑ or CLKIN ↓ to TCLK↑	3.0	4.2	5.5	ns	t_c = 15.38 ns (± 0.2%), |Input Clock Jitter| < 50 ps ** See Figure 5
t_w	Pulse Duration, High-Level Output Clock	0.35t_c	$\frac{4}{7}$ t_c	0.65t_c	ns	
t_t	Transition Time, Differential Output Voltage (t_r or t_f)	260	700	1500	ps	See Figure 2
t_{en}	Enable Time, $\overline{\text{PWDN}}$ ↑ to Phase Lock (TCLK Valid)			10	ms	See Figure 6
t_{dis}	Disable Time, $\overline{\text{PWDN}}$ ↓ to Off State (TCLK Low)			100	ns	See Figure 7

* All typical values are at VCC = 3.3V, T_A = 25°C

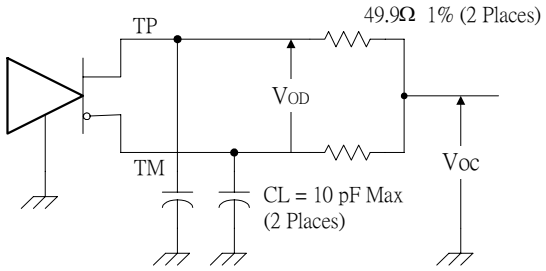
****** |Input Clock Jitter| is the magnitude of the change in the input clock period.

7 Parameter Measurement Information

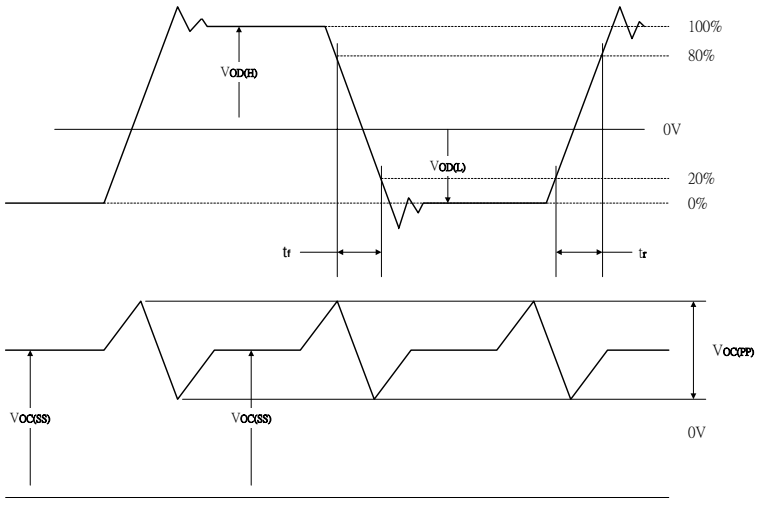


Note A: All input timing is defined at 1.4V on an input signal with a 10%-to-90% rise or fall time of less than 5ns.

Figure 1. Setup and Hold Time Definition

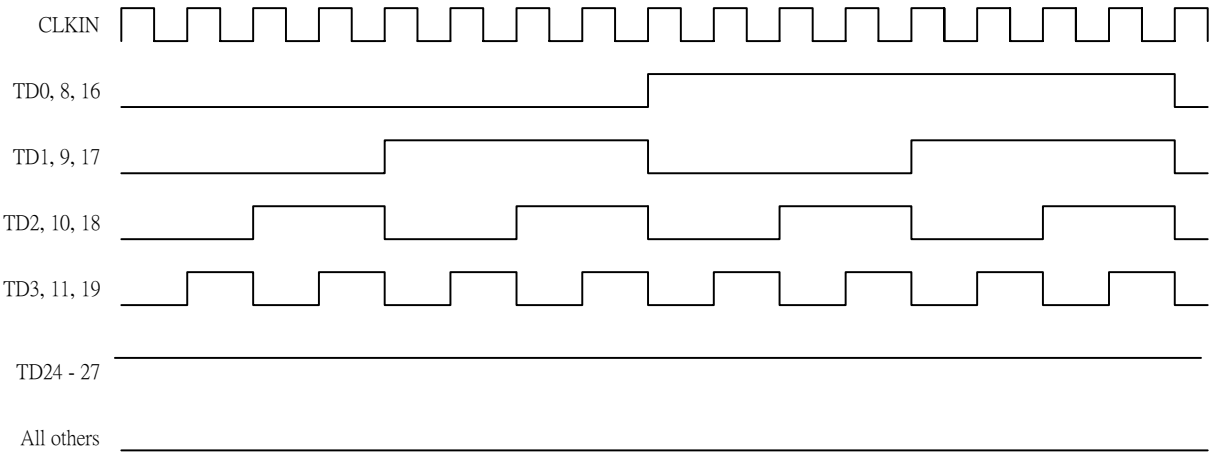


(a) SCHEMATIC



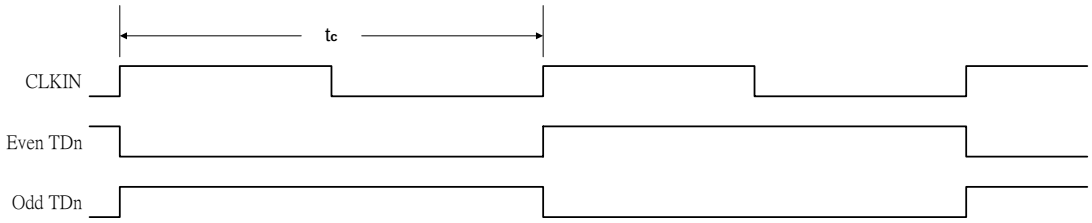
(b) WAVEFORMS

Figure 2. Test Load and Voltage Definitions for VLDS Outputs



Notes: A. The 16-grayscale test-pattern test device power consumption for a typical display pattern.
B. V**IH** = 2V and V**IL** = 0.8V.

Figure 3. 16-Grayscale Test-Pattern Waveforms



Notes: A. The worst-case test pattern produces nearly the maximum switching frequency for all of the LVDS outputs.
B. V_{IH} = 2V and V_{IL} = 0.8V.

Figure 4. Worst-Case Test-Pattern Waveforms

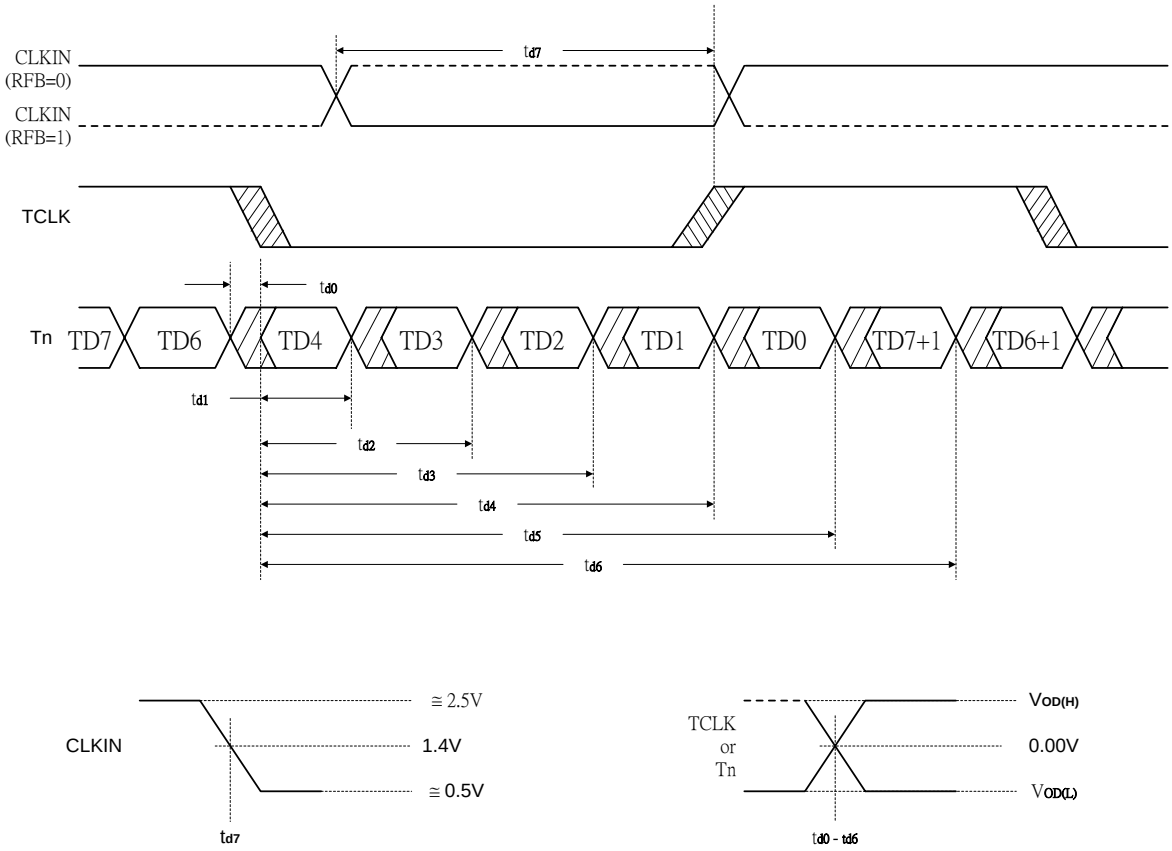


Figure 5. Timing Definitions

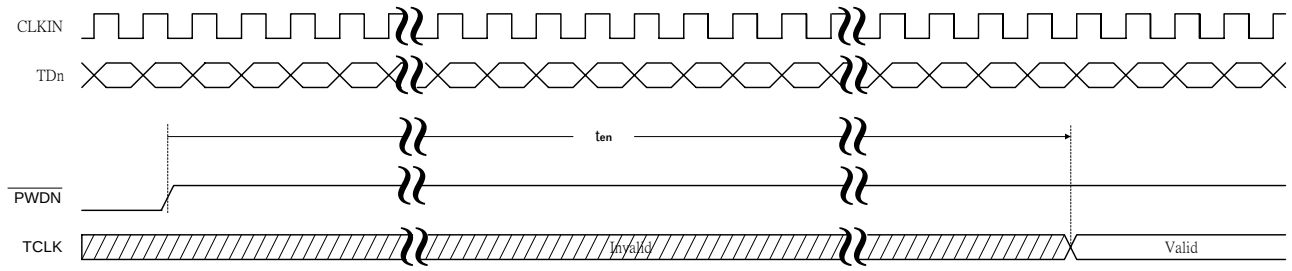


Figure 6. Enable Time Waveforms

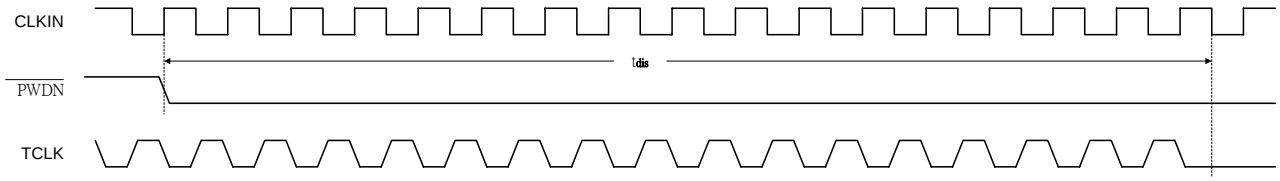


Figure 7. Disable Time Waveforms

8 Application Information

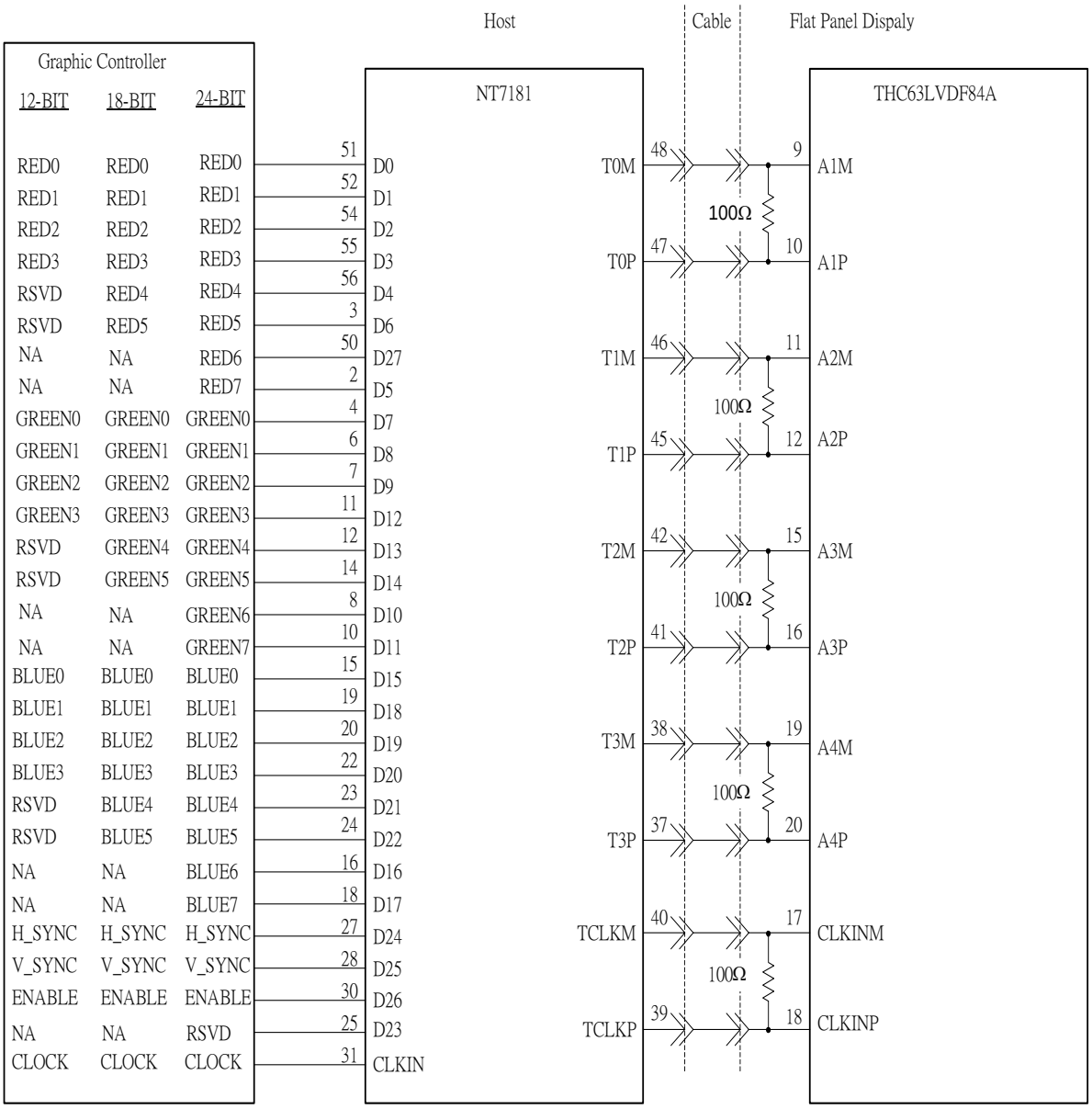


Figure 12. Color Host to LCD Panel Application

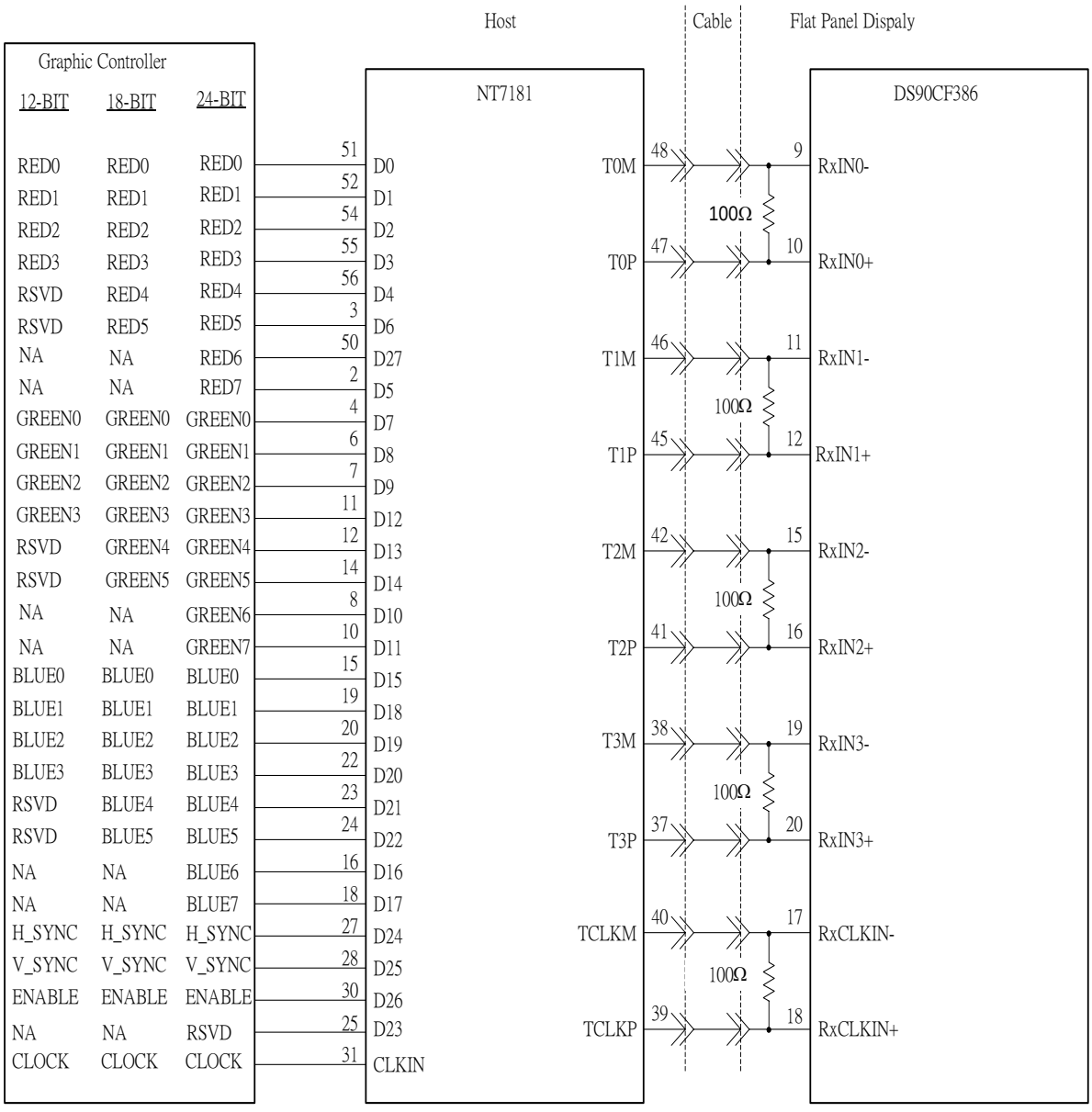


Figure 13. 18-Bit Color Host to 24-Bit LCD Display Panel Application*

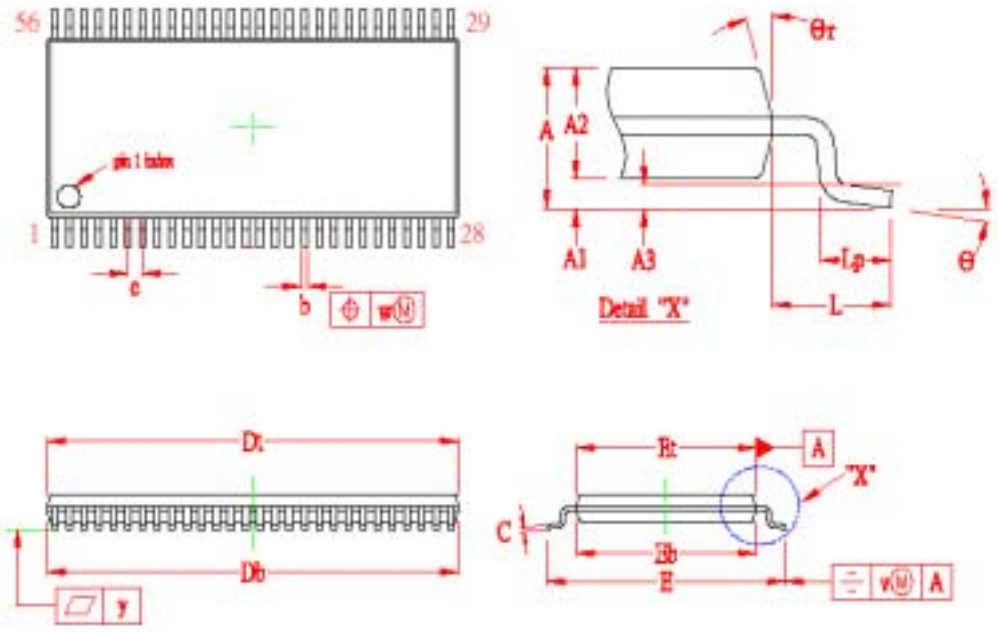
9 Ordering Information

Part No.	Package	Packing
NT7181F	56L TSSOP	Tube
NT7181FQ	56L TSSOP	Tape on reel

10 Package Information

TSSOP 56L Outline Dimensions

unit : inches/mm



ITEM	MAX.	NOM.	MIN.
A	1.10		
A1	0.15		0.05
A2	1.00		0.80
A3	0.25		
b	0.25		0.15
c	0.20		0.10
Dt	14.00		13.80
Db	14.10		13.90
e		0.50	
Et	6.10		5.90
Eb	6.20		6.00
E	8.20		8.00
L		1.00	
Lp	0.70		0.50
v	0.20		
w	0.08		
y	0.08		
θ	5°		1°
θt	13°		11°