Power MOSFET

-60 V, -18.5 A, P-Channel, D²PAK

Features

- Designed for Low R_{DS(on)}
- Withstands High Energy in Avalanche and Commutation Modes

Applications

- Power Supplies
- PWM Motor Control
- Converters
- Power Management

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	-60	V
Gate-to-Source Voltage			V _{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T _A = 25°C	I _D	-18.5	Α
Power Dissipation (Note 1)	Steady State	T _A = 25°C	P _D	88	W
Pulsed Drain Current	t _p = 10 μs		I _{DM}	-55	Α
Operating Junction and Storage Temperature			T _J , T _{STG}	-55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy (V _{DD} = 25 V, V _{GS} = 5.0 V, I _{PK} = 15 A, L = 3.0 mH, R _G = 25 Ω)			E _{AS}	338	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		5 Gr	260	°C	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) - Steady State	$R_{\theta JC}$	1.7	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1" pad size (Cu Area 1.127 in²).

2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu Area 0.41 in²).

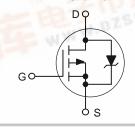


ON Semiconductor®

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V _{(BR)DSS}	R _{DS(on)} TYP	I _D MAX		
-60 V	120 mΩ @ -5.0 V	–18.5 A		

P-Channel





D²PAK CASE 418B STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



NTB5605P = Device Code Y = Year WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping [†]		
NTB5605P	D ² PAK	50 Units/Rail		
NTB5605PT4	D ² PAK	800/Tape & Reel		

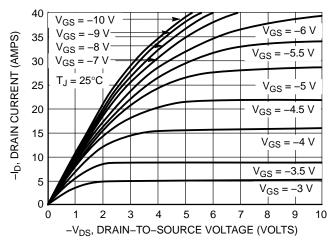
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS		-					
Drain-to-Source Breakdown Voltage	V _{(Br)DSS}	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$		-60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(Br)DSS} /T _J				-64		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	$T_J = 25^{\circ}C$			-1.0	μΑ
		$V_{DS} = -60 \text{ V}$	T _J = 125°C			-10	1
Gate-to-Source Leakage Current	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$				±100	nA
ON CHARACTERISTICS (Note 3)		-					
Gate Threshold Voltage	V _{GS(th)}	$V_{GS} = V_{DS}, I_{D}$	₀ = -250 μA	-1.0	-1.5	-2.0	V
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = -5.0 \text{ V},$ $V_{GS} = -5.0 \text{ V},$	$V_{GS} = -5.0 \text{ V}, I_D = -8.5 \text{ A}$ $V_{GS} = -5.0 \text{ V}, I_D = -17 \text{ A}$		120 140	140	mΩ
Forward Transconductance	9FS	$V_{DS} = -10 \text{ V},$	I _D = -8.5 A		12		S
Drain-to-Source On Voltage	V _{DS(on)}	$V_{GS} = -5.0 \text{ V},$	I _D = -8.5 A			-1.3	V
CHARGES, CAPACITANCES AND GATE	RESISTANCE					-	
Input Capacitance	C _{iss}				730	1190	
Output Capacitance	C _{oss}	$V_{GS} = 0 \text{ V, f} = 1.0 \text{ MHz,}$ $V_{DS} = -25 \text{ V}$			211	300	pF
Reverse Transfer Capacitance	C _{rss}				67	120	
Total Gate Charge	Q _{G(TOT)}				13	22	
Gate-to-Source Charge	Q _{GS}	$V_{GS} = -5.0 \text{ V}, V_{DS} = -48 \text{ V},$ $I_{D} = -17 \text{ A}$			4.0		nC
Gate-to-Drain Charge	Q_{GD}				7.0		
SWITCHING CHARACTERISTICS (Note	4)					-	
Turn-On Delay Time	t _{d(on)}				12.5	25	
Rise Time	t _r	$V_{GS} = -5.0 \text{ V}, V_{DD} = -30 \text{ V},$ $I_{D} = -17 \text{ A}, R_{G} = 9.1 \Omega$			122	183	1
Turn-Off Delay Time	t _{d(off)}	$I_D = -17 \text{ A, F}$	$R_{\rm G} = 9.1 \Omega$		29	58	ns
Fall Time	t _f	1			75	150	1
DRAIN-SOURCE DIODE CHARACTERIS	STICS	•			•		•
Forward Diode Voltage	V _{SD}	V _{GS} = 0 V	$T_J = 25^{\circ}C$		-1.55	-2.5	V
		$I_S = -17 \text{ A}$ $T_J = 125^{\circ}\text{C}$ -1.4					
Reverse Recovery Time	t _{rr}	$V_{GS} = 0 \text{ V, dI}_{S}/dt = 100 \text{ A/}\mu\text{s,}$ $I_{S} = -17 \text{ A}$			60		
Charge Time	t _a				39		ns
Discharge Time	t _b				21		1
Reverse Recovery Charge	Q _{RR}				0.14		nC

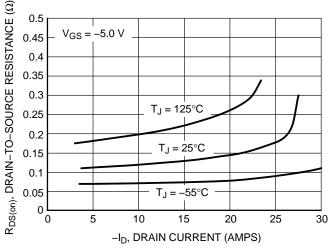
Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
 Switching characteristics are independent of operating junction temperatures.



40 V_{DS} = -10 V T_J = -55°C T_J = 125°C T

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



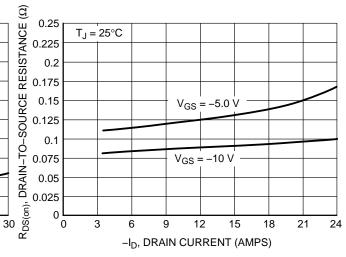
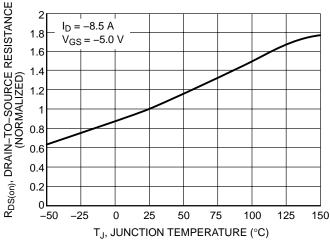


Figure 3. On–Resistance vs. Drain Current and Temperature

Figure 4. On–Resistance vs. Drain Current and Gate Voltage



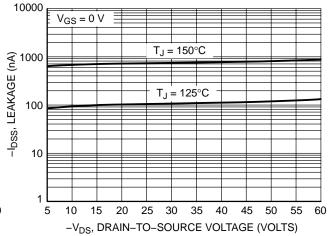


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

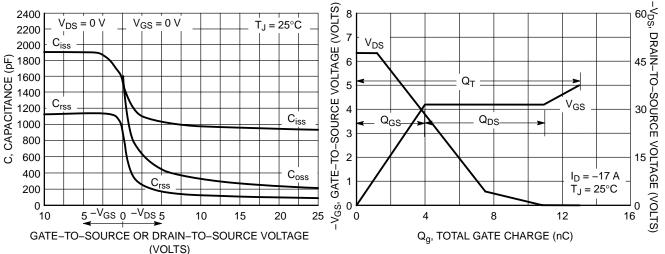


Figure 7. Capacitance Variation

Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

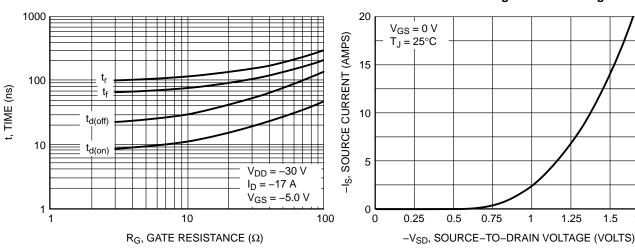


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current

1.75

150

 $I_D = -15 A$

125

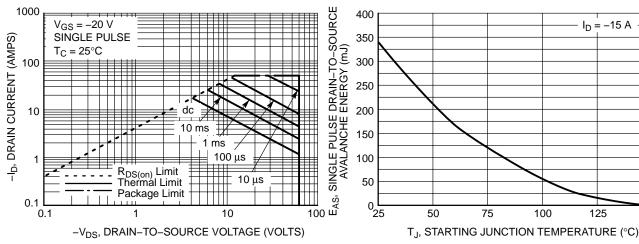


Figure 11. Maximum Rated Forward Biased Safe Operating Area

Figure 12. Maximum Avalanche Energy vs. **Starting Junction Temperature**

100

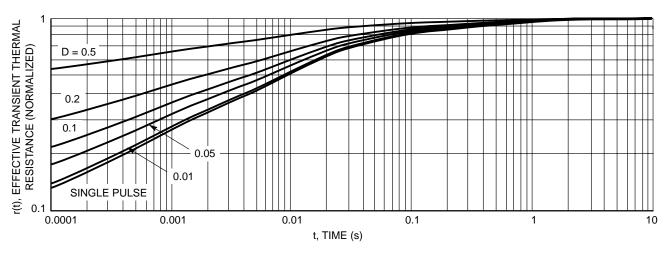


Figure 13. Thermal Response

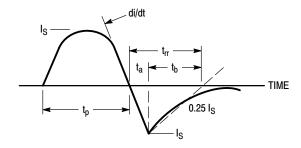
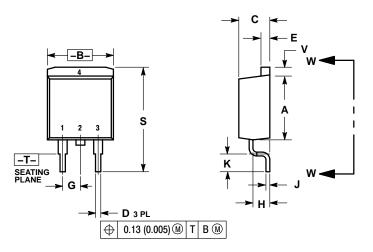
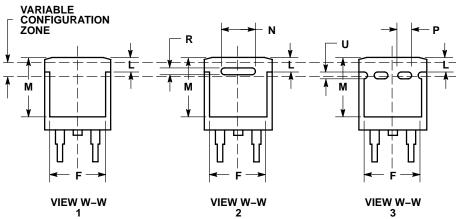


Figure 14. Diode Reverse Recovery Waveform

PACKAGE DIMENSIONS

D²PAK CASE 418B-04 ISSUE H



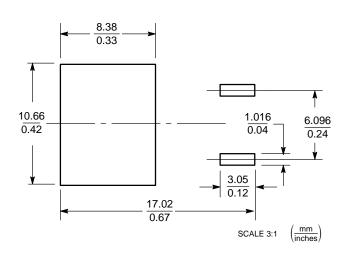


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX		
Α	0.340	0.380	8.64	9.65		
В	0.380	0.405	9.65	10.29		
С	0.160	0.190	4.06	4.83		
D	0.020	0.035	0.51	0.89		
Е	0.045	0.055	1.14	1.40		
F	0.310	0.350	7.87	8.89		
G	0.100 BSC		2.54 BSC			
Н	0.080	0.110	2.03	2.79		
J	0.018	0.025	0.46	0.64		
K	0.090	0.110	2.29	2.79		
L	0.052	0.072	1.32	1.83		
M	0.280	0.320	7.11	8.13		
N	0.197	0.197 REF		0 REF		
Р	0.079 REF		2.00 REF			
R	0.039	REF	0.99 REF			
S	0.575	0.625	14.60	15.88		
V	0.045	0.055	1.14	1.40		

- STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

SOLDERING FOOTPRINT



Notes

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