捷多邦,专业PCB打样工厂,24小时加急出货

NTB65N02R, NTP65N02R

Product Preview Power MOSFET 65 A, 24 V N-Channel TO-220, D²PAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low R_{DSon} to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Fast Switching

MAXIMUM RATINGS (T_J = 25°C Unless otherwise specified)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V _{DSS}	24	V _{dc}		
Gate-to-Source Voltage Continuous	V _{GS}	±20	V _{dc}		
Drain Current (Continuous @ $T_A = 25^{\circ}C$ (Note 3) Single Pulse (tp = 10 μ s)	I _D I _{DM}	65 160	A A		
Total Power Dissipation @ T _A = 25°C	PD	78	W		
Operating and Storage Temperature	T _J and T _{stg}	–55 to 150	°C		
Single Pulse Drain–to Source Avalanche Energy – Starting $T_J=25^{\circ}C$ ($V_{DD} = 50 V_{dc}, V_{GS} = 5 V_{dc}, I_L = A_{pk}, L = 1 mH, R_G = 25 \Omega$)	E _{AS}	TBD	mJ		
Thermal Resistance Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$\begin{array}{c} R_{\theta JC} \\ R_{\theta JA} \\ R_{\theta JA} \end{array}$	1.6 67 120	°C/W		
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds	ΤL	260	°C		

1. When surface mounted to an FR4 board using 1 inch pad size, (Cu Area 1.127 in²).

 When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).

3. Chip current capability limited by package.

PIN ASSIGNMENT

f.dzsc.com

PIN	FUNCTION
1	Gate
2	Drain
3	Source
4	Drain

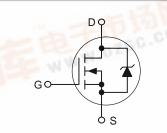
This document contains information on a product under development. ON Semiconductor

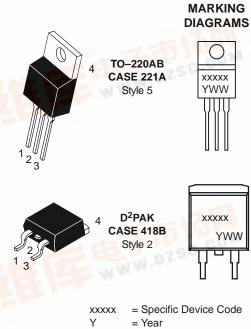


ON Semiconductor®

http://onsemi.com

65 A, 24 V R_{DS(on)} = 8.3 mΩ (TYP)





WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTB65N02R	D ² PAK	50 Units/Rail
NTB65N02RT4	D ² PAK	800 Tape & Reel
NTP65N02R	TO-220AB	50 Units/Rail

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless otherwise specified)

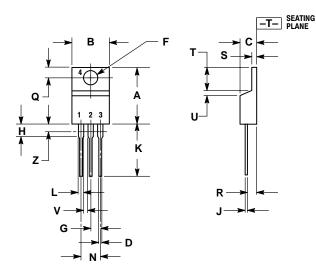
Characteristics			Min	Тур	Мах	Unit
OFF CHARACTERISTICS			-		-	
Drain-to-Source Breakdown Voltage (Note 4) ($V_{GS} = 0 V_{dc}$, $I_D = 250 \mu A_{dc}$) Temperature Coefficient (Positive)			24 -	27.5 25.5		V _{dc} mV/°C
Zero Gate Voltage Drain Current $(V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc})$ $(V_{DS} = 20 V_{dc}, V_{GS} = 0 V_{dc}, T_J = 150^{\circ}C)$					1.5 15	μA _{dc}
$ \begin{array}{l} \mbox{Gate-Body Leakage Current} \\ \mbox{(V}_{GS} = \pm 20 \ V_{dc}, \ V_{DS} = 0 \ V_{dc}) \end{array} $			-	-	±100	nA _{dc}
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage (Note 4) ($V_{DS} = V_{GS}$, $I_D = 250 \ \mu A_{dc}$) Threshold Temperature Coefficient (Negative)			1.0 _	1.5 4.1	2.0	V _{dc} mV/°C
$ Static Drain-to-Source On-Resistance (Note 4) \\ (V_{GS} = 4.5 V_{dc}, I_D = 15 A_{dc}) \\ (V_{GS} = 10 V_{dc}, I_D = 20 A_{dc}) \\ (V_{GS} = 10 V_{dc}, I_D = 30 A_{dc}) \\ (V_{GS} = 10 V_{dc}, I_D = 30 A_{dc}) $			_ _ _	10.5 8.3 9.5	12.5 10.5 -	mΩ
Forward Transconductance (Note 4) $(V_{DS} = 10 V_{dc}, I_D = 15 A_{dc})$			_	20	_	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance		C _{iss}	_	1050	1470	pF
Output Capacitance	$(V_{DS} = 24 V_{dc}, V_{GS} = 0 V f = 1 MHz)$	C _{oss}	_	394	550	
Transfer Capacitance		C _{rss}	_	88	120	
SWITCHING CHARACTERISTICS (N	ote 5)	-	_		-	-
Turn–On Delay Time		t _d (on)	_	11.2	20	ns
Rise Time	$(V_{GS} = 5 V_{dc}, V_{DD} = 10 V_{dc}, I_D = 30 A_{dc}, R_G = 3 \Omega)$	t _r	-	52	100	
Turn–Off Delay Time	$I_{\rm D} = 30 \text{ A}_{\rm dc}, \text{ R}_{\rm G} = 3 \Omega)$	t _d (off)	-	10	20	
Fall Time		tf	-	4	10	
Gate Charge		Q _T	_	8.4	12	nC
	$(V_{GS} = 4.5 V_{dc}, I_D = 30 A_{dc}, V_{DS} = 10 V_{dc})$ (Note 4)	Q ₁	-	3.7	_	
		Q ₂	_	4.04	_	
SOURCE-DRAIN DIODE CHARACTE	RISTICS					
Forward On–Voltage		V _{SD}	_ _ _	0.88 1.10 0.80	1.2 - -	V _{dc}
Reverse Recovery Time	$(I_{S} = 20 A_{dc}, V_{GS} = 0 V_{dc},$	t _{rr}	-	15.5	-	ns
		ta	-	12.6	-	
	$dI_S/dt = 100 A/\mu s)$ (Note 4)	t _b	_	2.6	-	
Reverse Recovery Stored Charge	1	Q _{RR}	_	0.005	-	μC

5. Switching characteristics are independent of operating junction temperatures.

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PACKAGE DIMENSIONS



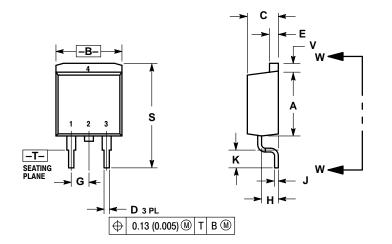


- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Η	0.110	0.155	2.80	3.93
ſ	0.018	0.025	0.46	0.64
Κ	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
Ν	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
۷	0.045		1.15	
Ζ		0.080		2.04

STYLE 5: PIN 1. GATE 2. DRAIN SOURCE
DRAIN

D²PAK CASE 418B-04 ISSUE G



NOTES:

VOIES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. 4188–01 THRU 4188–03 OBSOLETE, NEW STANDARD 4188–04.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.340	0.380	8.64	9.65
В	0.380	0.405	9.65	10.29
С	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
Е	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
Н	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
М	0.280	0.320	7.11	8.13
Ν	0.197 REF		5.00	REF
Ρ	0.079 REF		2.00	REF
R	0.039	0.039 REF		REF
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

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