

NTMD6N02R2

Power MOSFET 6.0 Amps, 20 Volts

N-Channel Enhancement Mode Dual SO-8 Package

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual SO-8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SO-8 Mounting Information Provided

Applications

- DC-DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery-Powered Products, for example, Computers, Printers, Cellular and Cordless Telephones and PCMCIA Cards

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	20	V
Drain-to-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	20	V
Gate-to-Source Voltage - Continuous	V_{GS}	± 12	V
Thermal Resistance - Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.0	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	6.5	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	5.5	A
Pulsed Drain Current (Note 4)	I_{DM}	50	A
Thermal Resistance - Junction-to-Ambient (Note 2)	$R_{\theta JA}$	102	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.22	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	5.07	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	4.07	A
Pulsed Drain Current (Note 4)	I_{DM}	40	A
Thermal Resistance - Junction-to-Ambient (Note 3)	$R_{\theta JA}$	172	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.73	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	3.92	A
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	3.14	A
Pulsed Drain Current (Note 4)	I_{DM}	30	A

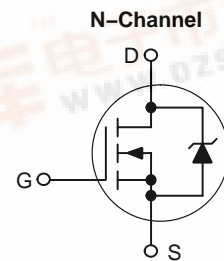
1. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz. Cu 0.06" thick single sided), $t < 10$ seconds.
2. Mounted onto a 2" square FR-4 Board (1" sq. 2 oz. Cu 0.06" thick single sided), $t =$ steady state.
3. Minimum FR-4 or G-10 PCB, $t =$ steady state.
4. Pulse Test: Pulse Width = 10 μs , Duty Cycle = 2%.



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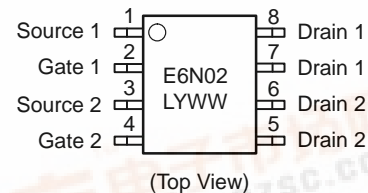
<http://onsemi.com>

V_{DSS}	$R_{DS(on)}$ TYP	I_D MAX
20 V	35 m Ω @ $V_{GS} = 4.5\text{ V}$	6.0 A



SO-8
CASE 751
STYLE 11

MARKING DIAGRAM & PIN ASSIGNMENT



E6N02 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTMD6N02R2	SO-8	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) (continued)

Rating	Symbol	Value	Unit
Operating and Storage Temperature Range	T _J , T _{stg}	–55 to +150	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T _J = 25°C (V _{DD} = 20 Vdc, V _{GS} = 5.0 Vdc, Peak I _L = 6.0 Apk, L = 20 mH, R _G = 25 Ω)	E _{AS}	360	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T _L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted) (Note 5)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	20 –	– 19.2	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 25°C) (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 125°C)	I _{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = +12 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	100	nAdc
Gate-Body Leakage Current (V _{GS} = –12 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	–100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = –250 μAdc) Temperature Coefficient (Negative)	V _{GS(th)}	0.6 –	0.9 –3.0	1.2 –	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V _{GS} = 4.5 Vdc, I _D = 6.0 Adc) (V _{GS} = 4.5 Vdc, I _D = 4.0 Adc) (V _{GS} = 2.7 Vdc, I _D = 2.0 Adc) (V _{GS} = 2.5 Vdc, I _D = 3.0 Adc)	R _{DS(on)}	– – – –	0.028 0.028 0.033 0.035	0.035 0.043 0.048 0.049	Ω
Forward Transconductance (V _{DS} = 12 Vdc, I _D = 3.0 Adc)	g _{FS}	–	10	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 16 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	785	1100	pF
Output Capacitance		C _{oss}	–	260	450	
Reverse Transfer Capacitance		C _{rss}	–	75	180	

SWITCHING CHARACTERISTICS (Notes 6 and 7)

Turn-On Delay Time	(V _{DD} = 16 Vdc, I _D = 6.0 Adc, V _{GS} = 4.5 Vdc, R _G = 6.0 Ω)	t _{d(on)}	–	12	20	ns
Rise Time		t _r	–	50	90	
Turn-Off Delay Time		t _{d(off)}	–	45	75	
Fall Time		t _f	–	80	130	
Turn-On Delay Time	(V _{DD} = 16 Vdc, I _D = 4.0 Adc, V _{GS} = 4.5 Vdc, R _G = 6.0 Ω)	t _{d(on)}	–	11	18	ns
Rise Time		t _r	–	35	65	
Turn-Off Delay Time		t _{d(off)}	–	45	75	
Fall Time		t _f	–	60	110	
Total Gate Charge	(V _{DS} = 16 Vdc, V _{GS} = 4.5 Vdc, I _D = 6.0 Adc)	Q _{tot}	–	12	20	nC
Gate-Source Charge		Q _{gs}	–	1.5	–	
Gate-Drain Charge		Q _{gd}	–	4.0	–	

5. Handling precautions to protect against electrostatic discharge is mandatory

6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

7. Switching characteristics are independent of operating junction temperature.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued) (Note 8)

Characteristic	Symbol	Min	Typ	Max	Unit
BODY-DRAIN DIODE RATINGS (Note 9)					
Diode Forward On-Voltage	V_{SD}	–	0.83	1.1	Vdc
		–	0.88	1.2	
		–	0.75	–	
Reverse Recovery Time	t_{rr}	–	30	–	ns
		–	15	–	
		–	15	–	
Reverse Recovery Stored Charge	Q_{RR}	–	0.02	–	μC

8. Handling precautions to protect against electrostatic discharge is mandatory.

9. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.

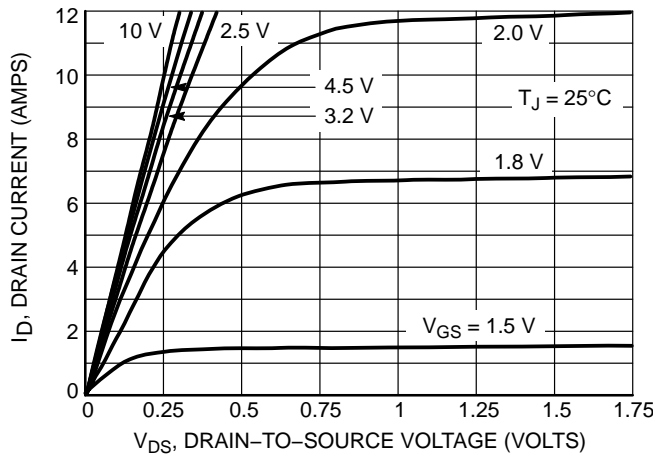


Figure 1. On-Region Characteristics

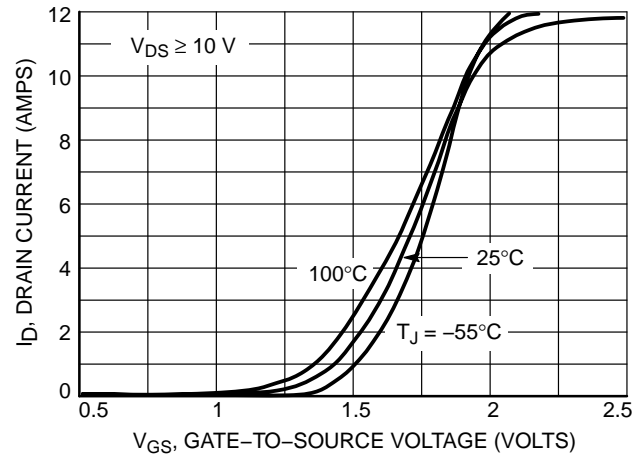


Figure 2. Transfer Characteristics

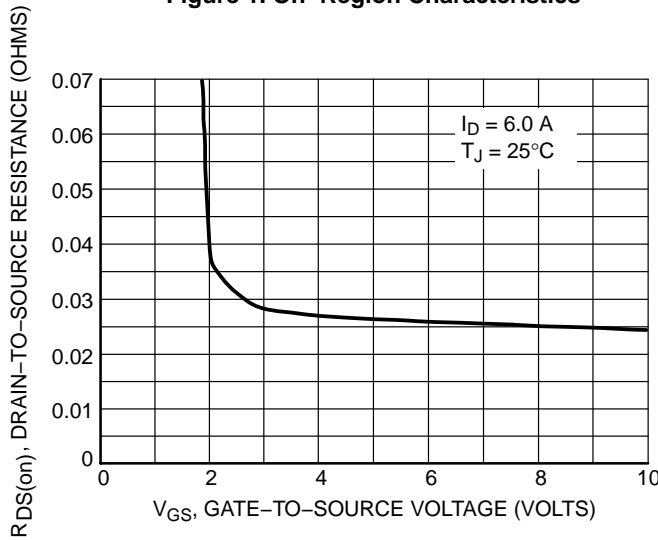


Figure 3. On-Resistance versus Gate-To-Source Voltage

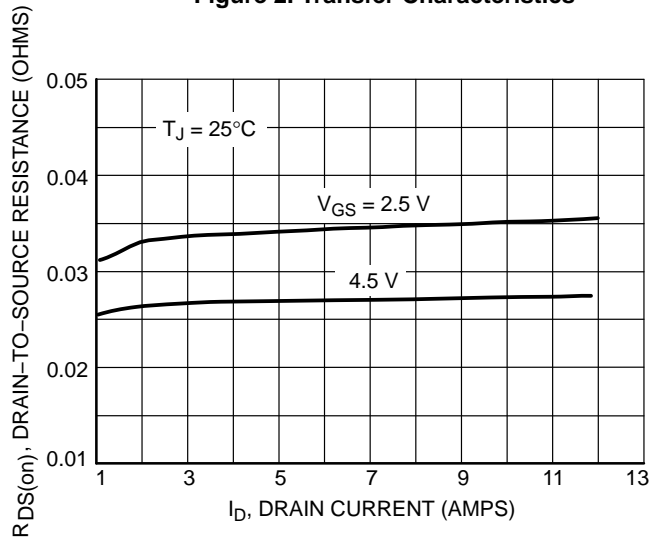


Figure 4. On-Resistance versus Drain Current and Gate Voltage

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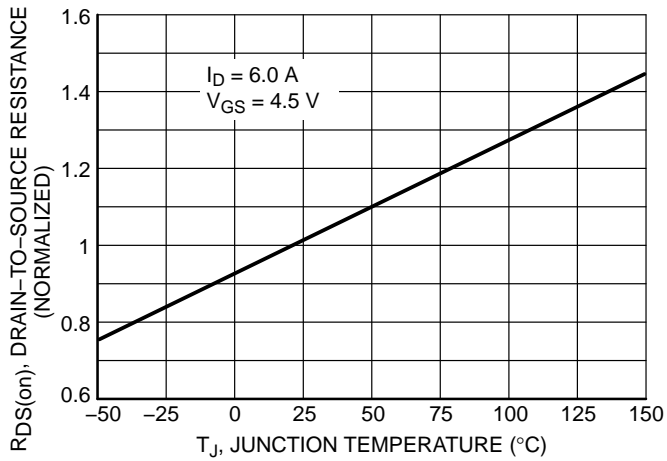


Figure 5. On-Resistance Variation with Temperature

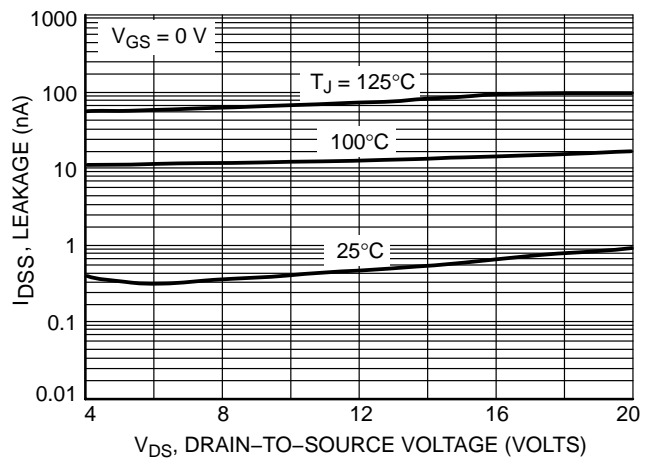


Figure 6. Drain-To-Source Leakage Current versus Voltage

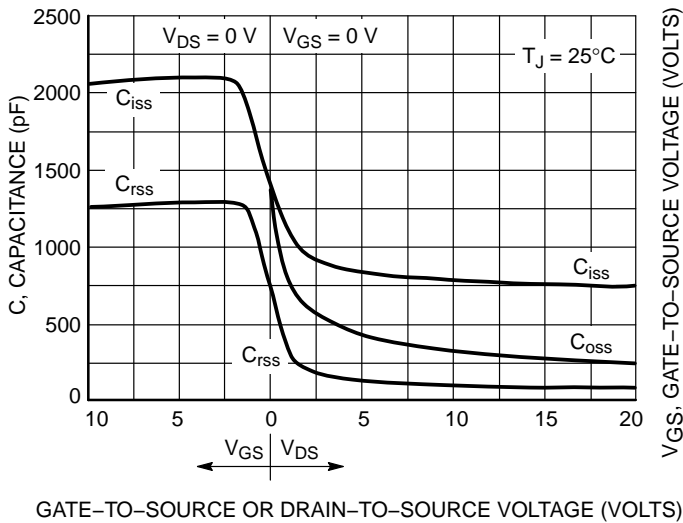


Figure 7. Capacitance Variation

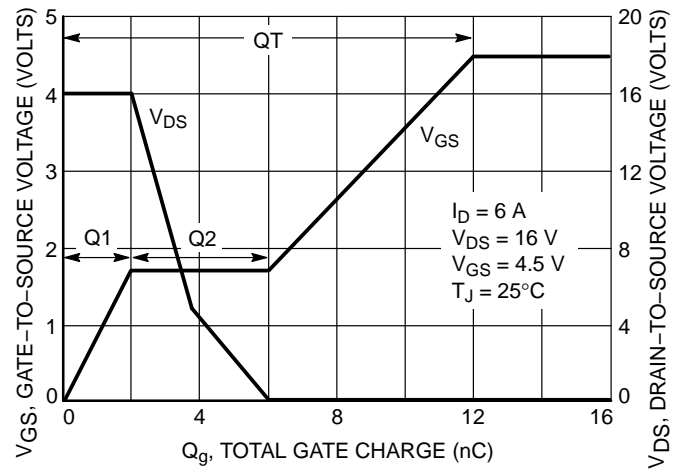


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

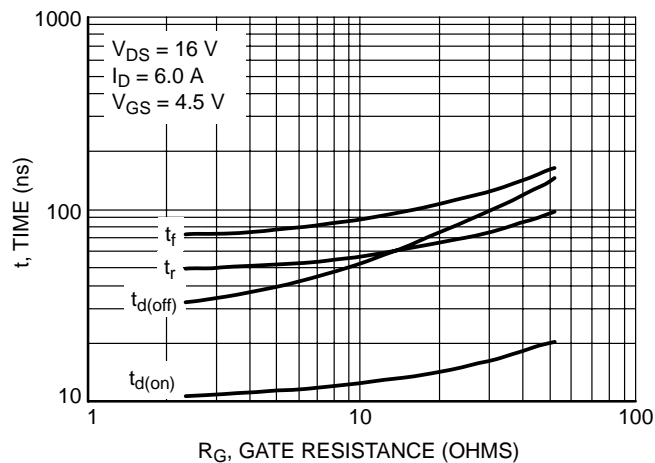


Figure 9. Resistive Switching Time Variation versus Gate Resistance

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DRAIN-TO-SOURCE DIODE CHARACTERISTICS

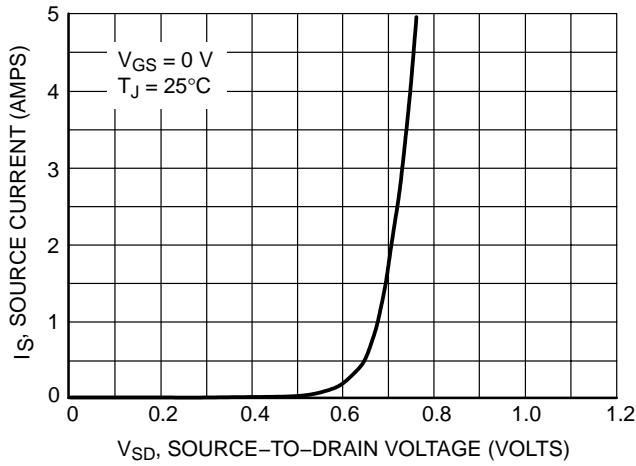


Figure 10. Diode Forward Voltage versus Current

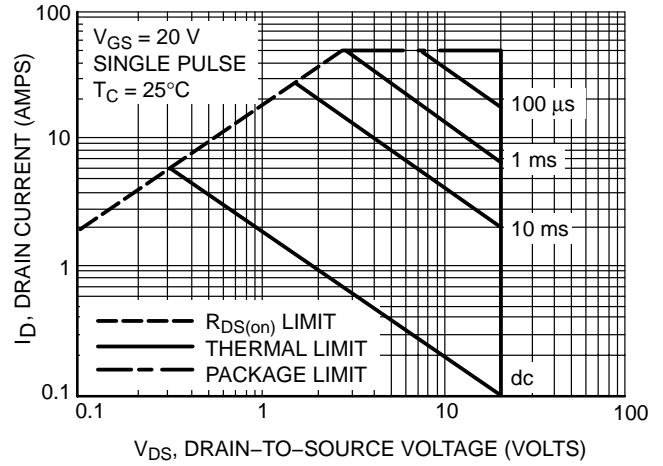


Figure 11. Maximum Rated Forward Biased Safe Operating Area

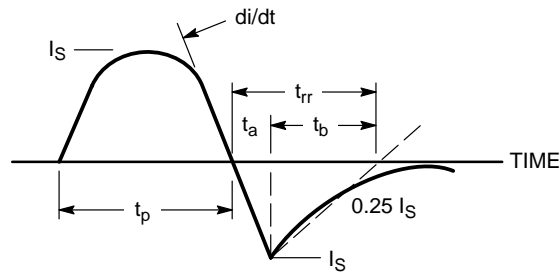


Figure 12. Diode Reverse Recovery Waveform

TYPICAL ELECTRICAL CHARACTERISTICS

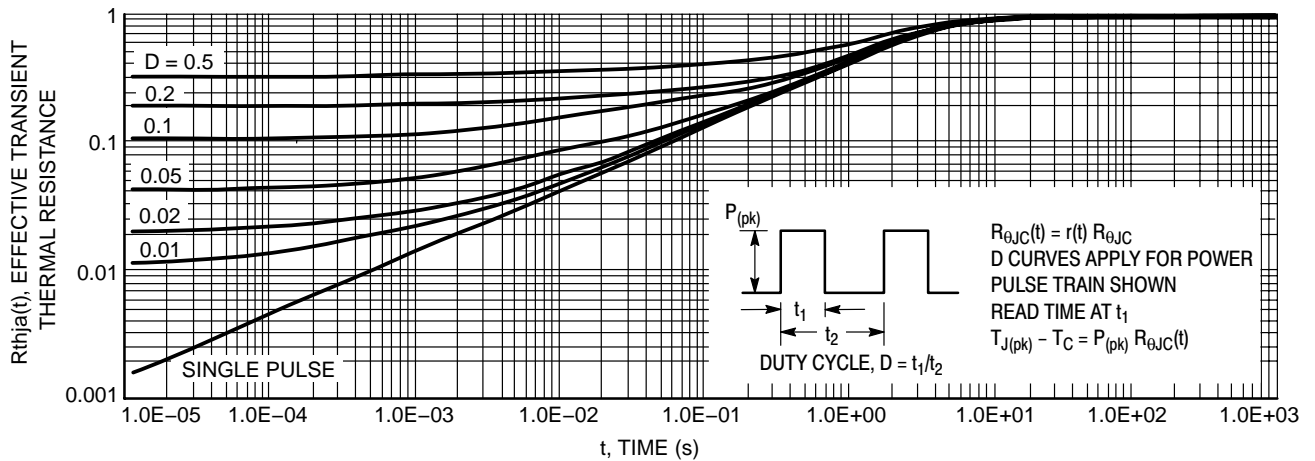
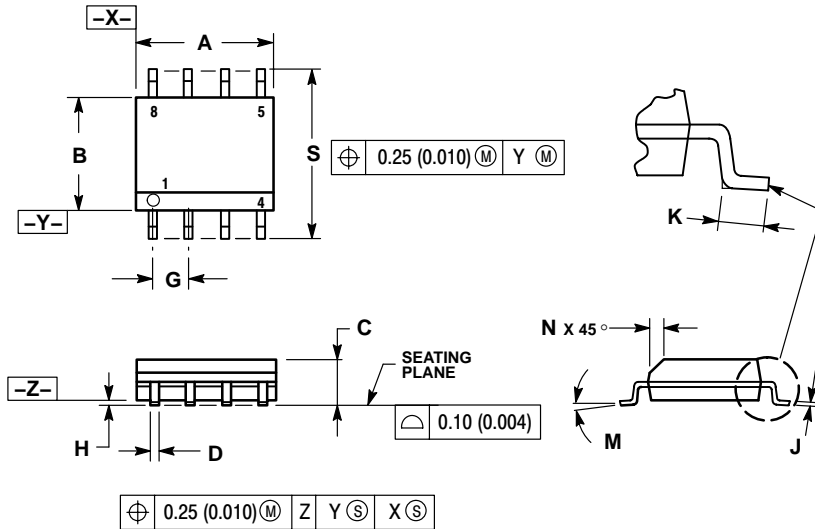


Figure 13. Thermal Response

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PACKAGE DIMENSIONS

SO-8
CASE 751-07
ISSUE AB



NOTES:

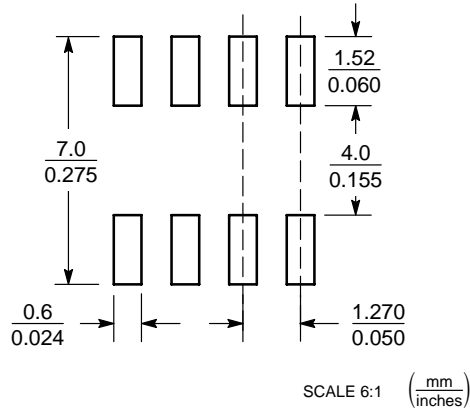
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 11:

- PIN 1: SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1

SOLDERING FOOTPRINT*



SCALE 6:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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