15 MHz Rail-to-Rail Operational Amplifiers

OP162/OP262/OP462

FEATURES

Wide Bandwidth: 15 MHz
Low Offset Voltage: 325 µV max
Low Noise: 9.5 nV/√Hz @ 1 kHz
Single-Supply Operation: +2.7 V to +12 V
Rail-to-Rail Output Swing
Low TCV_{OS}: 1 µV/°C typ
High Slew Rate: 13 V/µs
No Phase Inversion
Unity Gain Stable

APPLICATIONS

Portable Instrumentation
Sampling ADC Amplifier
Wireless LANs
Direct Access Arrangement
Office Automation

GENERAL DESCRIPTION

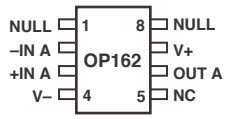
The OP162 (single), OP262 (dual), OP462 (quad) rail-to-rail 15 MHz amplifiers feature the extra speed new designs require, with the benefits of precision and low power operation. With their incredibly low offset voltage of 45 µV (typ) and low noise, they are perfectly suited for precision filter applications and instrumentation. The low supply current of 500 µA (typ) is critical for portable or densely packed designs. In addition, the rail-to-rail output swing provides greater dynamic range and control than standard video amplifiers provide.

These products operate from single supplies as low as +2.7 V to dual supplies of ±6 V. The fast settling times and wide output swings recommend them for buffers to sampling A/D converters. The output drive of 30 mA (sink and source) is needed for many audio and display applications; more output current can be supplied for limited durations.

The OP162 family is specified over the extended industrial temperature range (–40°C to +125°C). The single OP162 and dual OP262 are available in 8-lead SOIC and TSSOP packages. The quad OP462 is available in 14-lead narrow-body SOIC and TSSOP packages.

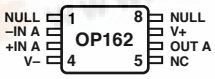
PIN CONFIGURATIONS

8-Lead Narrow-Body SO
(S Suffix)



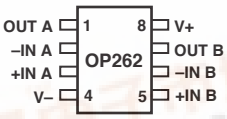
NC = NO CONNECT

8-Lead TSSOP
(RU Suffix)

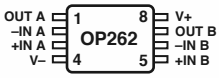


NC = NO CONNECT

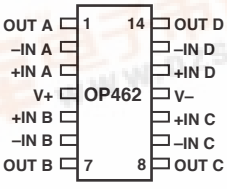
8-Lead Narrow-Body SO
(S Suffix)



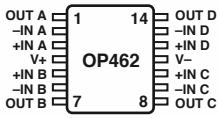
8-Lead TSSOP
(RU Suffix)



14-Lead Narrow-Body SO
(S Suffix)



14-Lead TSSOP
(RU Suffix)



REV. D

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OP162/OP262/OP462–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = +5.0 V, V_{CM} = 0 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP162G, OP262G, OP462G,		45	325	µV
		–40°C ≤ T_A ≤ +125°C			800	µV
		H Grade, –40°C ≤ T_A ≤ +125°C			1	mV
		D Grade, –40°C ≤ T_A ≤ +125°C		0.8	3	mV
					5	mV
Input Bias Current	I_B			360	600	nA
		–40°C ≤ T_A ≤ +125°C			650	nA
Input Offset Current	I_{OS}			±2.5	±25	nA
		–40°C ≤ T_A ≤ +125°C			±40	nA
Input Voltage Range	V_{CM}		0		+4	V
Common-Mode Rejection	CMRR	0 V ≤ V_{CM} ≤ +4.0 V,				
		–40°C ≤ T_A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 ≤ V_{OUT} ≤ 4.5 V		30		V/mV
		R_L = 10 kΩ, 0.5 ≤ V_{OUT} ≤ 4.5 V	65	88		V/mV
		R_L = 10 kΩ, –40°C ≤ T_A ≤ +125°C	40			V/mV
Long-Term Offset Voltage	V_{OS}	G Grade[1]			600	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2		1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			250		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA, –40°C ≤ T_A ≤ +125°C	4.95	4.99		V
		I_L = 5 mA	4.85	4.94		V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA, –40°C ≤ T_A ≤ +125°C		14	50	mV
		I_L = 5 mA		65	150	mV
Short Circuit Current	I_{SC}	Short to Ground		±80		mA
Maximum Output Current	I_{OUT}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.7 V to +7 V		120		dB
		–40°C ≤ T_A ≤ +125°C	90			dB
Supply Current/Amplifier	I_{SY}	OP162, V_{OUT} = 2.5 V		600	750	µA
		–40°C ≤ T_A ≤ +125°C			1	mA
		OP262, OP462, V_{OUT} = 2.5 V		500	700	µA
		–40°C ≤ T_A ≤ +125°C			850	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	1 V < V_{OUT} < 4 V, R_L = 10 kΩ		10		V/µs
Settling Time	t_S	To 0.1%, A_V = –1, V_O = 2 V Step		540		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	ϕ_m			61		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		9.5		nV/$\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz		0.4		pA/$\sqrt{Hz}$

NOTES

[1]Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.

[2]Offset voltage drift is the average of the –40°C to +25°C delta and the +25°C to +125°C delta.

Specifications subj]ect to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = +3.0 V, V_{CM} = 0 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP162G, OP262G, OP462G		50	325	µV
		H Grade, –40°C ≤ T_A ≤ +125°C			1	mV
		D Grade, –40°C ≤ T_A ≤ +125°C		0.8	3	mV
					5	mV
Input Bias Current	I_B			360	600	nA
Input Offset Current	I_{OS}			±2.5	±25	nA
Input Voltage Range	V_{CM}		0		+2	V
Common-Mode Rejection	CMRR	0 V ≤ V_{CM} ≤ +2.0 V,				
		–40°C ≤ T_A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, 0.5 V ≤ V_{OUT} ≤ 2.5 V		20		V/mV
		R_L = 10 kΩ, 0.5 V ≤ V_{OUT} ≤ 2.5 V	20	30		V/mV
Long-Term Offset Voltage	V_{OS}	G Grade[1]			600	µV
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA	2.95	2.99		V
		I_L = 5 mA	2.85	2.93		V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA		14	50	mV
		I_L = 5 mA		66	150	mV
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +2.7 V to +7 V,				
		–40°C ≤ T_A ≤ +125°C	60	110		dB
Supply Current/Amplifier	I_{SY}	OP162, V_{OUT} = 1.5 V		600	700	µA
		–40°C ≤ T_A ≤ +125°C			1	mA
		OP262, OP462, V_{OUT} = 1.5 V		500	650	µA
		–40°C ≤ T_A ≤ +125°C			850	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		10		V/µs
Settling Time	t_S	To 0.1%, A_V = –1, V_O = 2 V Step		575		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	ϕ_m			59		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		9.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4		pA/√Hz

NOTES

[1]Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125°C, with an LTPD of 1.3.

Specifications subject to change without notice.

OP162/OP262/OP462–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±5.0 V, V_{CM} = 0 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	OP162G, OP262G, OP462G		25	325	µV
		–40°C ≤ T_A ≤ +125°C			800	µV
		H Grade, –40°C ≤ T_A ≤ +125°C			1	mV
		D Grade, –40°C ≤ T_A ≤ +125°C		0.8	3	mV
					5	mV
Input Bias Current	I_B			260	500	nA
		–40°C ≤ T_A ≤ +125°C			650	nA
Input Offset Current	I_{OS}			±2.5	±25	nA
		–40°C ≤ T_A ≤ +125°C			±40	nA
Input Voltage Range	V_{CM}		–5		+4	V
Common-Mode Rejection	CMRR	–4.9 V ≤ V_{CM} ≤ +4.0 V,				
		–40°C ≤ T_A ≤ +125°C	70	110		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, –4.5 V ≤ V_{OUT} ≤ 4.5 V		35		V/mV
		R_L = 10 kΩ, –4.5 V ≤ V_{OUT} ≤ 4.5 V	75	120		V/mV
		–40°C ≤ T_A ≤ +125°C	25			V/mV
Long-Term Offset Voltage	V_{OS}	G Grade[1]			600	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	Note 2		1		µV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			250		pA/°C
OUTPUT CHARACTERISTICS						
Output Voltage Swing High	V_{OH}	I_L = 250 µA, –40°C ≤ T_A ≤ +125°C	4.95	4.99		V
		I_L = 5 mA	4.85	4.94		V
Output Voltage Swing Low	V_{OL}	I_L = 250 µA, –40°C ≤ T_A ≤ +125°C		–4.99	–4.95	V
		I_L = 5 mA		–4.94	–4.85	V
Short Circuit Current	I_{SC}	Short to Ground		±80		mA
Maximum Output Current	I_{OUT}			±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±1.35 V to ±6 V,				
		–40°C ≤ T_A ≤ +125°C	60	110		dB
Supply Current/Amplifier	I_{SY}	OP162, V_{OUT} = 0 V		650	800	µA
		–40°C ≤ T_A ≤ +125°C			1.15	mA
		OP262, OP462, V_{OUT} = 0 V		550	775	µA
		–40°C ≤ T_A ≤ +125°C			1	mA
Supply Voltage Range	V_S		+3.0 (±1.5)		+12 (±6)	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	–4 V < V_{OUT} < 4 V, R_L = 10 kΩ		13		V/µs
Settling Time	t_S	To 0.1%, A_V = –1, V_O = 2 V Step		475		ns
Gain Bandwidth Product	GBP			15		MHz
Phase Margin	ϕ_m			64		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		9.5		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.4		pA/√Hz

NOTES

[1]Long-term offset voltage is guaranteed by a 1000 hour life test performed on three independent lots at +125 °C, with an LTPD of 1.3.

[2]Offset voltage drift is the average of the –40°C to +25°C delta and the +25°C to +125°C delta.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±6 V
Input Voltage[1] . . . . . ±6 V
Differential Input Voltage[2] . . . . . ±0.6 V
Internal Power Dissipation
  SOIC (S) . . . . . Observe Derating Curves
  TSSOP (RU) . . . . . Observe Derating Curves
Output Short-Circuit Duration . . . . Observe Derating Curves
Storage Temperature Range . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +125°C
Junction Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . . . +300°C

Package Type	θ_{JA}[3]	θ_{JC}	Units
8-Lead SOIC (S)	158	43	°C/W
8-Lead TSSOP (RU)	240	43	°C/W
14-Lead SOIC (S)	120	36	°C/W
14-Lead TSSOP (RU)	180	35	°C/W

NOTES
[1]For supply voltages greater than 6 volts, the input voltage is limited to less than or equal to the supply voltage.
[2]For differential input voltages greater than 0.6 volts the input current should be limited to less than 5 mA to prevent degradation or destruction of the input devices.
[3]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for SOIC and TSSOP packages.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
OP162GS	–40°C to +125°C	8-Lead SOIC	RN-8
OP162DRU	–40°C to +125°C	8-Lead TSSOP	RU-8
OP162HRU	–40°C to +125°C	8-Lead TSSOP	RU-8
OP262DRU	–40°C to +125°C	8-Lead TSSOP	RU-8
OP262GS	–40°C to +125°C	8-Lead SOIC	RN-8
OP262HRU	–40°C to +125°C	8-Lead TSSOP	RU-8
OP462DRU	–40°C to +125°C	14-Lead TSSOP	RU-14
OP462DS	–40°C to +125°C	14-Lead SOIC	RN-14
OP462GS	–40°C to +125°C	14-Lead SOIC	RN-14
OP462HRU	–40°C to +125°C	14-Lead TSSOP	RU-14

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP162/OP262/OP462 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OP162/OP262/OP462–Typical Performance Characteristics

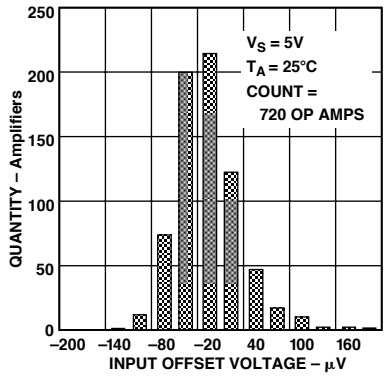


Figure 1. OP462 Input Offset Voltage Distribution

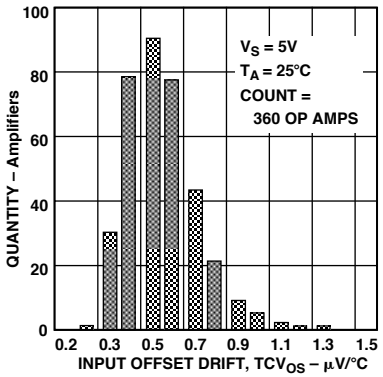


Figure 2. OP462 Input Offset Voltage Drift (TCV_{OS})

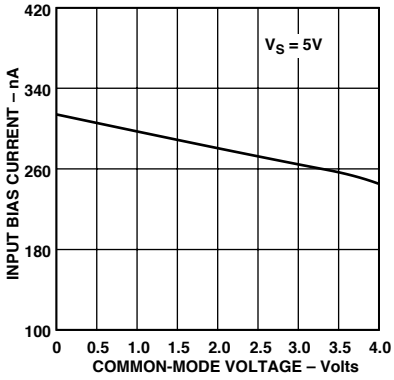


Figure 3. OP462 Input Bias Current vs. Common-Mode Voltage

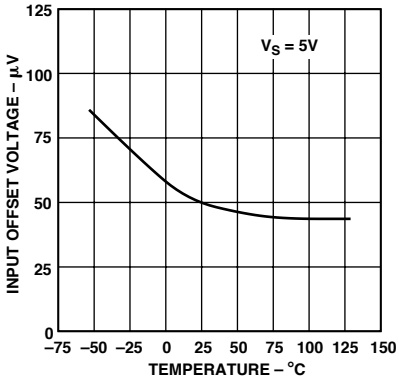


Figure 4. OP462 Input Offset Voltage vs. Temperature

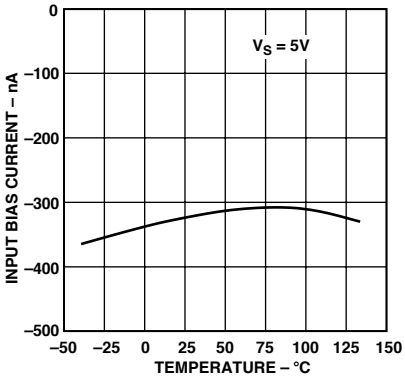


Figure 5. OP462 Input Bias Current vs. Temperature

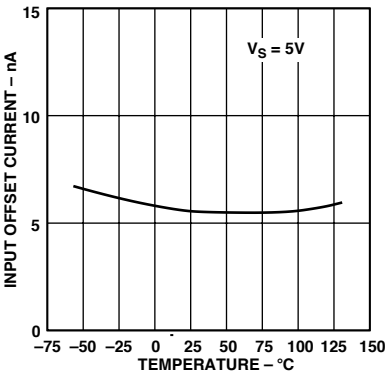


Figure 6. OP462 Input Offset Current vs. Temperature

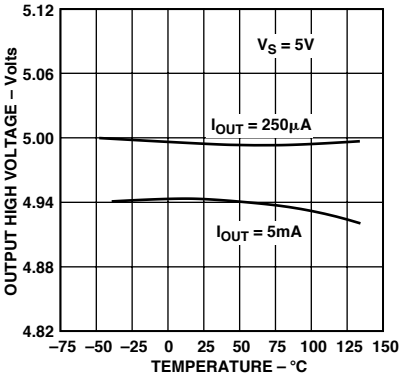


Figure 7. OP462 Output High Voltage vs. Temperature

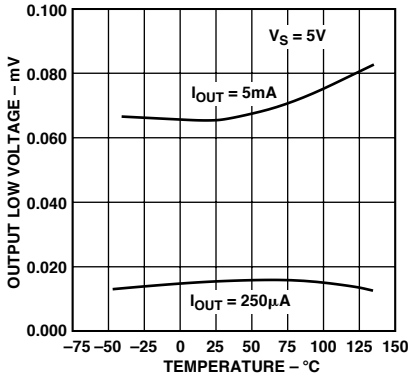


Figure 8. OP462 Output Low Voltage vs. Temperature

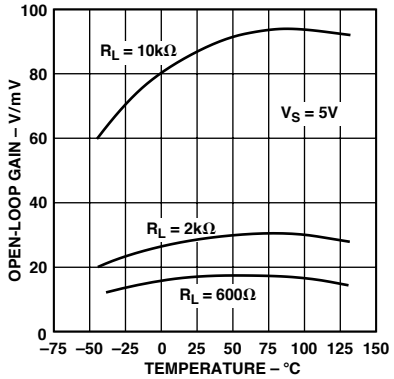


Figure 9. OP462 Open-Loop Gain vs. Temperature

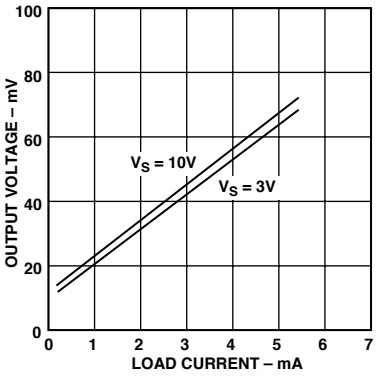


Figure 10. Output Low Voltage to Supply Rail vs. Load Current

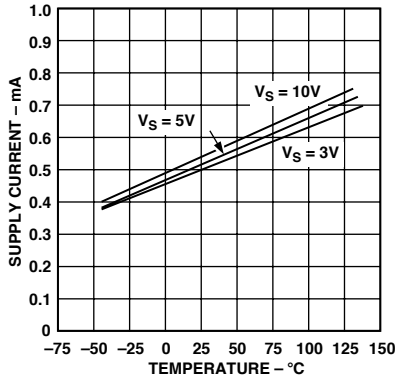


Figure 11. Supply Current/Amplifier vs. Temperature

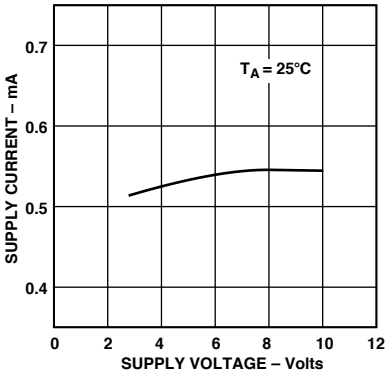


Figure 12. OP462 Supply Current/ Amplifier vs. Supply Voltage

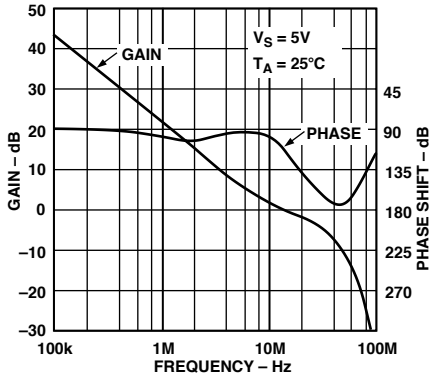


Figure 13. Open-Loop Gain and Phase vs. Frequency (No Load)

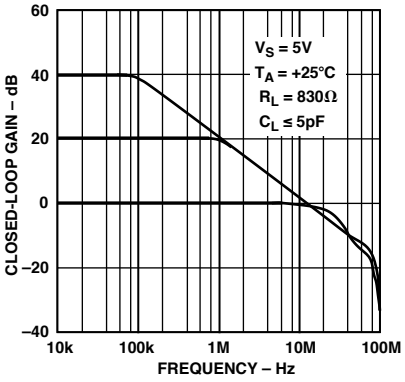


Figure 14. Closed-Loop Gain vs. Frequency

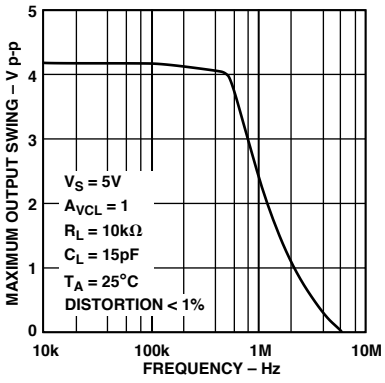


Figure 15. Maximum Output Swing vs. Frequency

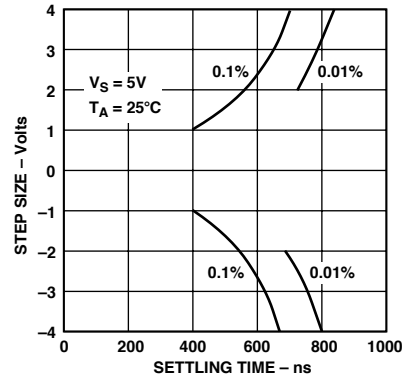


Figure 16. Settling Time vs. Step Size

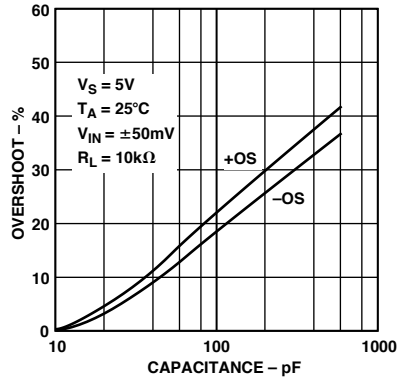


Figure 17. Small-Signal Overshoot vs. Capacitance

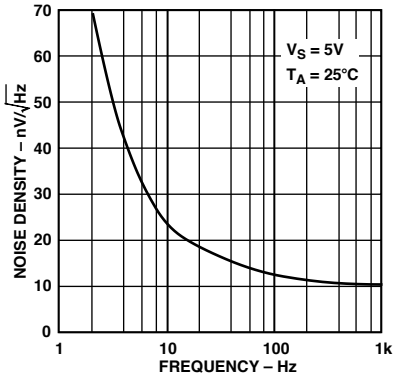


Figure 18. Voltage Noise Density vs. Frequency

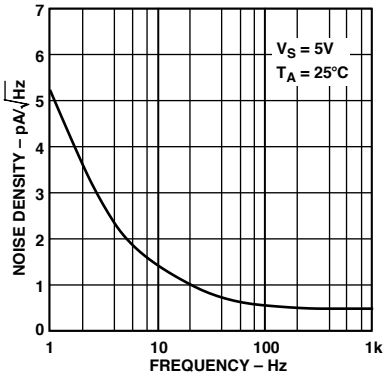


Figure 19. Current Noise Density vs. Frequency

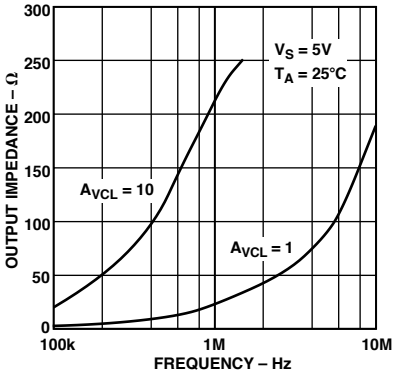


Figure 20. Output Impedance vs. Frequency

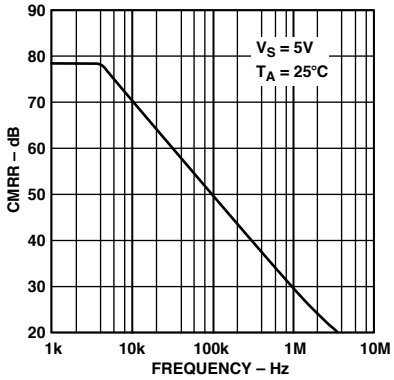


Figure 21. CMRR vs. Frequency

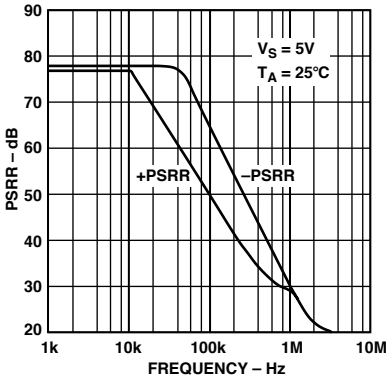


Figure 22. PSRR vs. Frequency

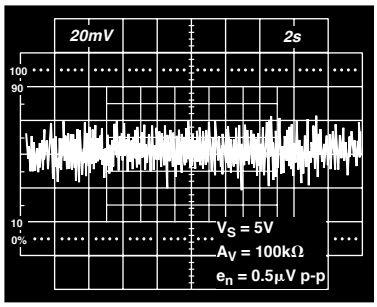


Figure 23. 0.1 Hz to 10 Hz Noise

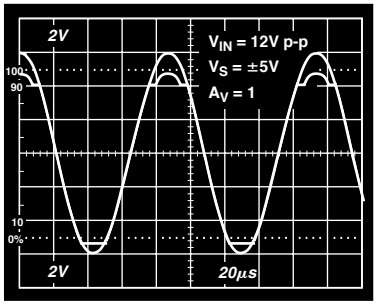


Figure 24. No Phase Reversal; [V_{IN} = 12 V p-p, V_S = ±5 V, A_V = 1]

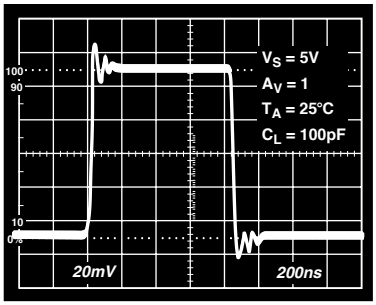


Figure 25. Small Signal Transient Response

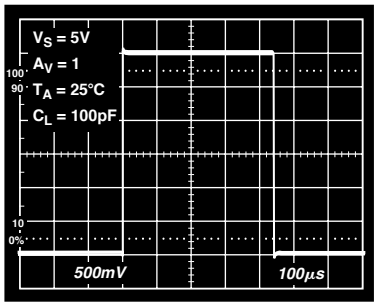


Figure 26. Large Signal Transient Response

APPLICATIONS SECTION

Functional Description

The OPx62 family is fabricated using Analog Devices' high speed complementary bipolar process, also called XFCB. The process includes trench isolating each transistor to lower parasitic capacitances thereby allowing high speed performance. This high speed process has been implemented without trading off the excellent transistor matching and overall dc performance characteristic of Analog Devices' complementary bipolar process. This makes the OPx62 family an excellent choice as an extremely fast and accurate low voltage op amp.

Figure 27 shows a simplified equivalent schematic for the OP162. A PNP differential pair is used at the input of the device. The cross connecting of the emitters is used to lower the transconductance of the input stage, which improves the slew rate of the device. Lowering the transconductance through cross connecting the emitters has another advantage in that it provides a lower noise factor than if emitter degeneration resistors were used. The input stage can function with the base voltages taken all the way to the negative power supply, or up to within 1 V of the positive power supply.

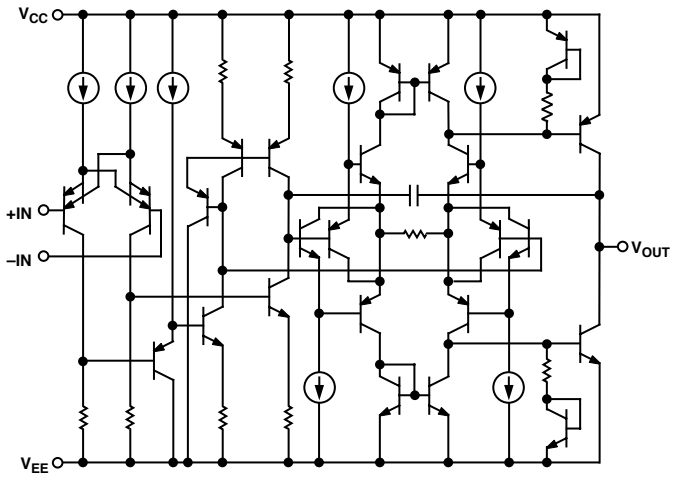


Figure 27. Simplified Schematic

Two complementary transistors in a common-emitter configuration are used for the output stage. This allows the output of the device to swing to within 50 mV of either supply rail at load currents less than 1 mA. As load current increases, the maximum voltage swing of the output will decrease. This is due to the collector-to-emitter saturation voltages of the output transistors increasing. The gain of the output stage, and consequently the open-loop gain of the amplifier, is dependent on the load resistance connected at the output. And because the dominant pole frequency is inversely proportional to the open-loop gain, the unity-gain bandwidth of the device is not affected by the load resistance. This is typically the case in rail-to-rail output devices.

Offset Adjustment

Because the OP162/OP262/OP462 has such an exceptionally low typical offset voltage, adjustment to correct offset voltage may not be needed. However, the OP162 does have pinouts where a nulling resistor can be attached. Figure 28 shows how the OP162 offset voltage can be adjusted by connecting a potentiometer between Pins 1 and 8, and connecting the wiper to V_{CC}. It is important to avoid accidentally connecting the wiper to V_{EE}, as this will damage the device. The recommended value for the potentiometer is 20 kΩ.

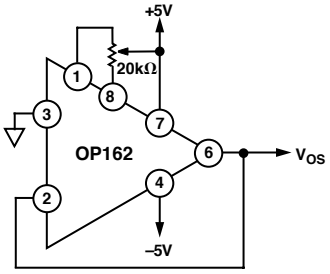


Figure 28. Schematic Showing Offset Adjustment

Rail-to-Rail Output

The OP162/OP262/OP462 has a wide output voltage range that extends to within 60 mV of each supply rail with a load current of 5 mA. Decreasing the load current will extend the output voltage range even closer to the supply rails. The common-mode input range extends from ground to within 1 V of the positive supply. It is recommended that there be some minimal amount of gain when a rail-to-rail output swing is desired. The minimum gain required is based on the supply voltage and can be found as:

$$A_{V,\min} = \frac{V_S}{V_S - 1}$$

where V_S is the positive supply voltage. With a single supply voltage of +5 V, the minimum gain to achieve rail-to-rail output should be 1.25.

Output Short-Circuit Protection

To achieve a wide bandwidth and high slew rate, the output of the OP162/OP262/OP462 is not short-circuit protected. Shorting the output directly to ground or to a supply rail may destroy the device. The typical maximum safe output current is ±30 mA. Steps should be taken to ensure the output of the device will not be forced to source or sink more than 30 mA.

In applications where some output current protection is needed, but not at the expense of reduced output voltage headroom, a low value resistor in series with the output can be used. This is shown in Figure 29. The resistor is connected within the feedback loop of the amplifier so that if V_{OUT} is shorted to ground and V_{IN} swings up to +5 V, the output current will not exceed 30 mA.

For single +5 V supply applications, resistors less than 169 Ω are not recommended.

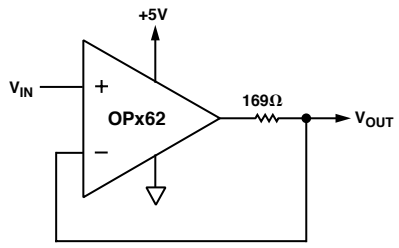


Figure 29. Output Short-Circuit Protection

Input Overvoltage Protection

The input voltage should be limited to ±6 V or damage to the device can occur. Electrostatic protection diodes placed in the input stage of the device help protect the amplifier from static discharge. Diodes are connected between each input as well as from each input to both supply pins as shown in the simplified equivalent circuit in Figure 27. If an input voltage exceeds either supply voltage by more than 0.6 V, or if the differential input voltage is greater than 0.6 V, these diodes begin to energize and overvoltage damage could occur. The input current should be limited to less than 5 mA to prevent degradation or destruction of the device.

This can be done by placing an external resistor in series with the input that could be overdriven. The size of the resistor can be calculated by dividing the maximum input voltage by 5 mA. For example, if the differential input voltage could reach 5 V, the external resistor should be 5 V/5 mA = 1 kΩ. In practice, this resistance should be placed in series with both inputs to balance any offset voltages created by the input bias current.

Output Phase Reversal

The OP162/OP262/OP462 is immune to phase reversal as long as the input voltage is limited to ±6 V. Figure 24 shows a photo of the output of the device with the input voltage driven beyond the supply voltages. Although the device's output will not change phase, large currents due to input overvoltage could result, damaging the device. In applications where the possibility of an input voltage exceeding the supply voltage exists, overvoltage protection should be used, as described in the previous section.

Power Dissipation

The maximum power that can be safely dissipated by the OP162/OP262/OP462 is limited by the associated rise in junction temperature. The maximum safe junction temperature is 150°C, and should not be exceeded or device performance could suffer. If this maximum is momentarily exceeded, proper circuit operation will be restored as soon as the die temperature is reduced. Leaving the device in an "overheated" condition for an extended period can result in permanent damage to the device.

To calculate the internal junction temperature of the OPx62, the following formula can be used:

$$T_J = P_{DISS} \times \theta_{JA} + T_A$$

where: T_J = OPx62 junction temperature;

P_{DISS} = OPx62 power dissipation;

θ_{JA} = OPx62 package thermal resistance, junction-to-ambient; and

T_A = Ambient temperature of the circuit.

The power dissipated by the device can be calculated as:

$$P_{DISS} = I_{LOAD} \times (V_S - V_{OUT})$$

where: I_{LOAD} is the OPx62 output load current;

V_S is the OPx62 supply voltage; and

V_{OUT} is the OPx62 output voltage.

Figures 30 and 31 provide a convenient way to see if the device is being overheated. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature around the package. By using the previous equation, it is a simple matter to see if P_{DISS} exceeds the device's power derating curve. To ensure proper operation, it is important to observe the recommended derating curves shown in Figures 30 and 31.

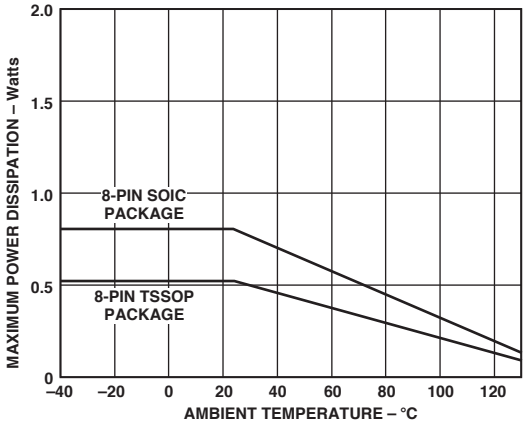


Figure 30. Maximum Power Dissipation vs. Temperature for 8-Pin Package Types

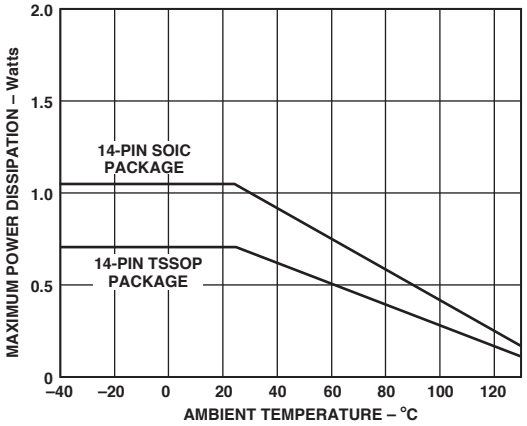


Figure 31. Maximum Power Dissipation vs. Temperature for 14-Pin Package Types

Unused Amplifiers

It is recommended that any unused amplifiers in a dual or a quad package be configured as a unity gain follower with a 1 kΩ feedback resistor connected from the inverting input to the output and the noninverting input tied to the ground plane.

Power On Settling Time

The time it takes for the output of an op amp to settle after a supply voltage is delivered can be an important consideration in some power-up sensitive applications. An example of this would be in an A/D converter where the time until valid data can be produced after power-up is important.

The OPx62 family has a rapid settling time after power-up. Figure 32 shows the OP462 output settling times for a single supply voltage of V_S = +5 V. The test circuit in Figure 33 was used to find the power on settling times for the device.

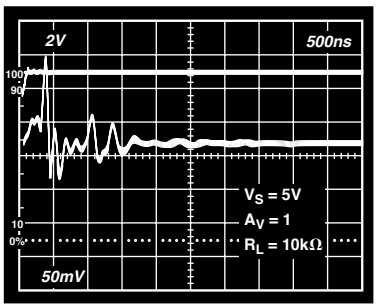


Figure 32. Oscilloscope Photo of V_S and V_{OUT}

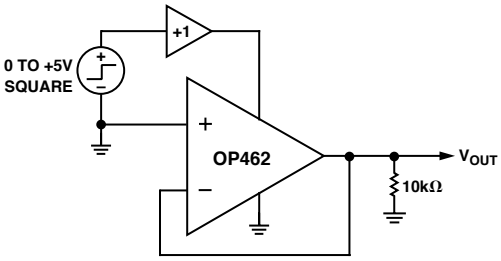


Figure 33. Test Circuit for Power On Settling Time

Capacitive Load Drive

The OP162/OP262/OP462 is a high speed, extremely accurate device and can tolerate some capacitive loading at its output. As load capacitance increases, however, the unity-gain bandwidth of the device will decrease. There will also be an increase in overshoot and settling time for the output. Figure 35 shows an example of this with the device configured for unity gain and driving a 10 kΩ resistor and 300 pF capacitor placed in parallel.

By connecting a series R-C network, commonly called a "snubber" network, from the output of the device to ground, this ringing can be eliminated and overshoot can be significantly reduced. Figure 34 shows how to set up the snubber network, and Figure 36 shows the improvement in output response with the network added.

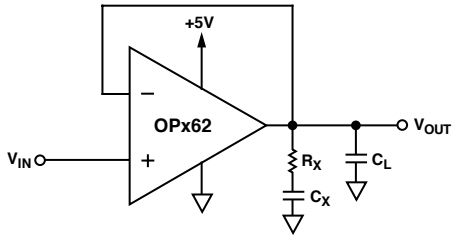


Figure 34. Snubber Network Compensation for Capacitive Loads

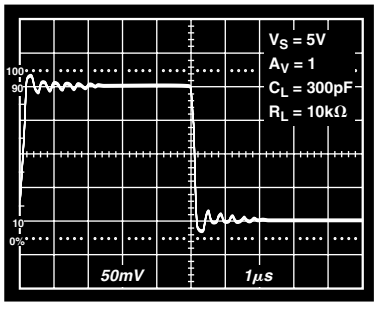


Figure 35. A Photo of a Ringing Square Wave

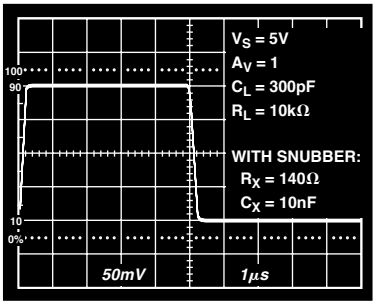


Figure 36. A Photo of a Nice Square Wave at the Output

The network operates in parallel with the load capacitor, C_L, and provides compensation for the added phase lag. The actual values of the network resistor and capacitor are determined empirically to minimize overshoot while maximizing unity-gain bandwidth. Table I shows a few sample snubber networks for large load capacitors:

Table I. Snubber Networks for Large Capacitive Loads

C_{LOAD}	R_X	C_X
<300 pF	140 Ω	10 nF
500 pF	100 Ω	10 nF
1 nF	80 Ω	10 nF
10 nF	10 Ω	47 nF

Obviously, higher load capacitance will also reduce the unity-gain bandwidth of the device. Figure 37 shows a plot of unity-gain bandwidth versus capacitive load. The snubber network will not provide any increase in bandwidth, but it will substantially reduce ringing and overshoot, as shown in the difference between Figures 35 and 36.

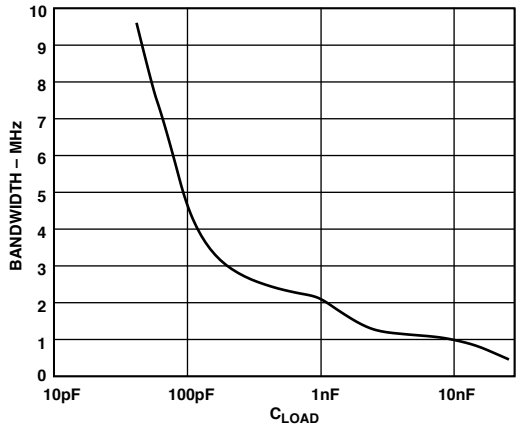


Figure 37. Unity Gain Bandwidth vs. C_{LOAD}

Total Harmonic Distortion and Crosstalk

The OPx62 device family offers low total harmonic distortion. This makes it an excellent device choice for audio applications. Figure 38 shows a graph of THD plus noise figures at 0.001% for the OP462.

Figure 39 shows a graph of the worst case crosstalk between two amplifiers in the OP462 device. A 1 V rms signal is applied to one amplifier while measuring the output of an adjacent amplifier. Both amplifiers are configured for unity gain and supplied with ±2.5 V.

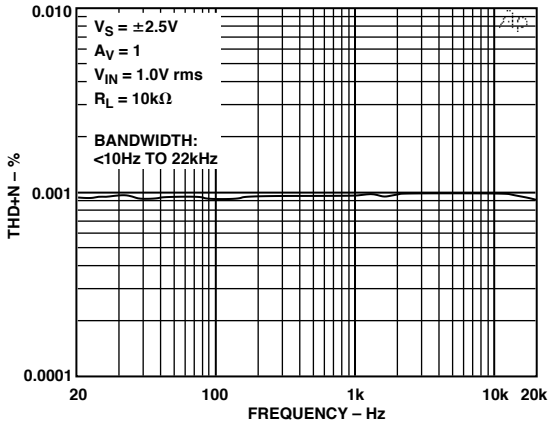


Figure 38. THD+N vs. Frequency Graph

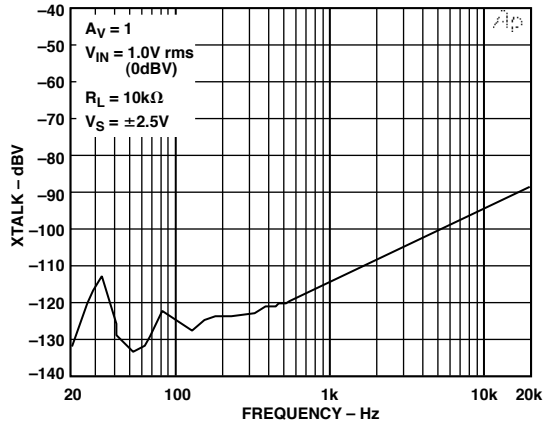


Figure 39. Crosstalk vs. Frequency Graph

PCB Layout Considerations

Because the OP162/OP262/OP462 can provide gain at high frequency, careful attention to board layout and component selection is recommended. As with any high speed application, a good ground plane is essential to achieve the optimum performance. This can significantly reduce the undesirable effects of ground loops and I×R losses by providing a low impedance reference point. Best results are obtained with a multilayer board design with one layer assigned to ground plane.

Chip capacitors should be used for supply bypassing, with one end of the capacitor connected to the ground plane and the other end connected within 1/8 inch of each power pin. An additional large tantalum electrolytic capacitor (4.7 µF–10 µF) should be connected in parallel. This capacitor does not need to be placed as close to the supply pins, as it is to provide current for fast large-signal changes at the device's output.

APPLICATION CIRCUITS

Single Supply Stereo Headphone Driver

Figure 40 shows a stereo headphone output amplifier that can be run from a single +5 V supply. The reference voltage is derived by dividing the supply voltage down with two 100 kΩ resistors. A 10 µF capacitor prevents power supply noise from contaminating the audio signal and establishes an ac ground for the volume control potentiometers.

The audio signal is ac coupled to each noninverting input through a 10 µF capacitor. The gain of the amplifier is controlled by the feedback resistors and is: (R2/R1) + 1. For this example, the gain is 6. By removing R1 altogether, the amplifier would have unity gain. A 169 Ω resistor is placed at the output in the feedback network to short-circuit protect the output of the device. This would prevent any damage to the device from occurring if the headphone output became shorted. A 270 µF capacitor is used at the output to couple the amplifier to the headphone. This value is much larger than that used for the input because of the low impedance of headphones, which can range from 32 Ω to 600 Ω or more.

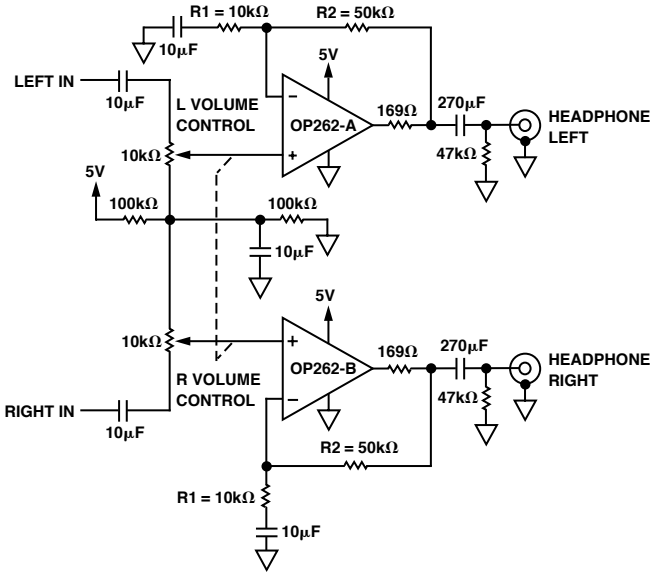


Figure 40. Headphone Output Amplifier

Instrumentation Amplifier

Because of its high speed, low offset voltages and low noise characteristics, the OP162/OP262/OP462 can be used in a wide variety of high speed applications, including a precision instrumentation amplifier. Figure 41 shows an example of such an application.

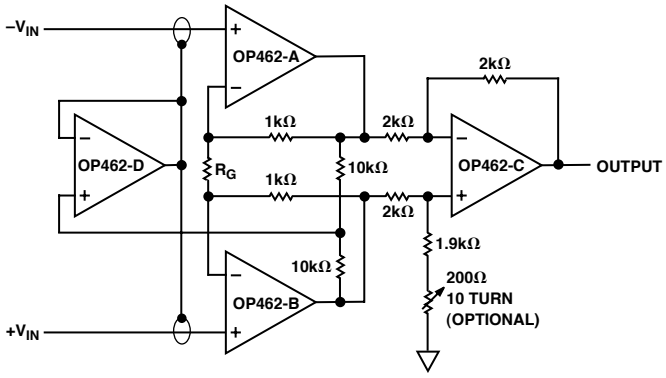


Figure 41. A High Speed Instrumentation Amplifier

The differential gain of the circuit is determined by R_G, where:

$$A_{DIFF} = 1 + \frac{2}{R_G}$$

with the R_G resistor value in kΩ. Removing R_G will set the circuit gain to unity.

The fourth op amp, OP462-D, is optional and is used to improve CMRR by reducing any input capacitance to the amplifier. By shielding the input signal leads and driving the shield with the common-mode voltage, input capacitance is eliminated at common-mode voltages. This voltage is derived from the midpoint of the outputs of OP462-A and OP462-B by using two 10 kΩ resistors followed by OP462-D as a unity gain buffer.

It is important to use 1% or better tolerance components for the 2 kΩ resistors, as the common-mode rejection is dependent on their ratios being exact. A potentiometer should also be connected in series with the OP462-C noninverting input resistor to ground to optimize common-mode rejection.

The circuit in Figure 41 was implemented to test its settling time. The instrumentation amp was powered with ±5 V, so the input step voltage went from –5 V to +4 V to keep the OP462 within its input range. Therefore, the 0.05% settling range is when the output is within 4.5 mV. Figure 42 shows the positive slope settling time to be 1.8 µs, and Figure 43 shows a settling time of 3.9 µs for the negative slope.

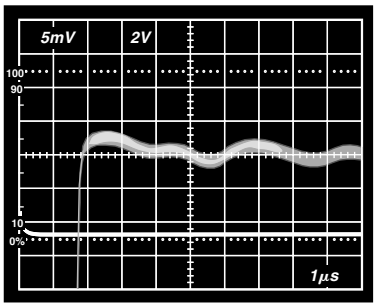


Figure 42. Positive Slope Settling Time

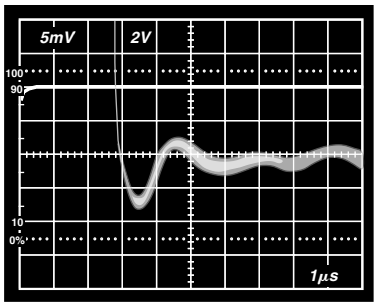


Figure 43. Negative Slope Settling Time

Direct Access Arrangement

Figure 44 shows a schematic for a +5 V single supply transmit/receive telephone line interface for 600 Ω transmission systems. It allows full duplex transmission of signals on a transformer coupled 600 Ω line. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured so as to apply the largest possible differential signal to the transformer. The largest signal available on a single +5 V supply is approximately 4.0 V p-p into a 600 Ω transmission system. Amplifier A3 is configured as a difference amplifier to extract the receive information from the transmission line for amplification by A4. A3 also prevents the transmit signal from interfering with the receive signal. The gain of A4 can be adjusted in the same manner as A1's to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (Single In-line Package) format resistor arrays. Couple this with the OP462 14-lead SOIC or TSSOP package and this circuit can offer a compact solution.

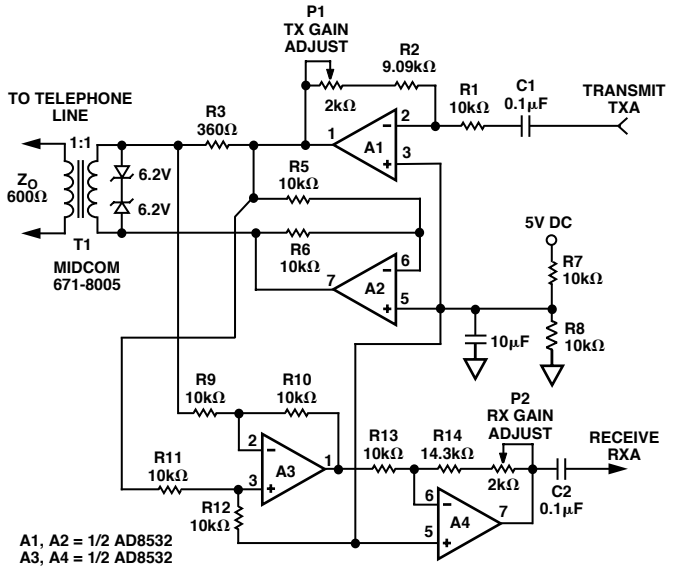


Figure 44. A Single-Supply Direct Access Arrangement for Modems

OP162/OP262/OP462

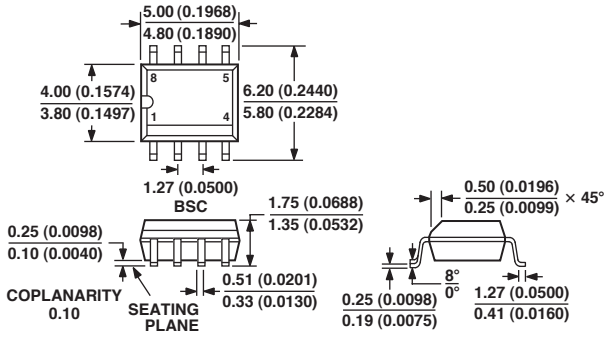
Spice Macro-Model

```
* OP162/OP262/OP462 SPICE Macro-model
* 7/96, Ver. 1
* Troy Murphy / ADSC
*
* Copyright 1996 by Analog Devices
*
* Refer to “README.DOC” file for License Statement. Use of this model
* indicates your acceptance of the terms and provisions in the License
* Statement
*
* Node Assignments
*                      noninverting input
*                      |       inverting input
*                      |       |       positive supply
*                      |       |       |       negative supply
*                      |       |       |       |       output
*                      |       |       |       |       |
.SUBCKT OP162  1       2       99      50      45
*
*INPUT STAGE
*
Q1   5    7    3    PIX 5
Q2   6    2    4    PIX 5
Ios  1    2    1.25E-9
I1   99   15   85E-6
EOS  7    1    POLY(1)  (14, 20)   45E-6 1
RC1  5    50   3.035E+3
RC2  6    50   3.035E+3
RE1  3    15   607
RE2  4    15   607
C1   5    6    600E-15
D1   3    8    DX
D2   4    9    DX
V1   99   8    DC  1
V2   99   9    DC  1
*
* 1st GAIN STAGE
*
EREF 98   0    (20, 0)   1
G1   98   10   (5, 6)    10.5
R1   10   98   1
C2   10   98   3.3E-9
*
* COMMON-MODE STAGE WITH ZERO AT 4kHz
*
ECM  13   98   POLY (2)   (1, 98)   (2, 98)   0    0.5   0.5
R2   13   14   1E+6
R3   14   98   70
C3   13   14   80E-12
*
* POLE AT 1.5MHz, ZERO AT 3MHz
*
G2   21   98   (10, 98)   .588E-6
R4   21   98   1.7E6
R5   21   22   1.7E6
C4   22   98   31.21E-15
*
* POLE AT 6MHz, ZERO AT 3MHz
*
E1   23   98   (21, 98)   2
R6   23   24   53E+3
R7   24   98   53E+3
C5   23   24   1E-12
*
* SECOND GAIN STAGE
*
G3   25   98   (24, 98)   40E-6
R8   25   98   1.65E+6
D3   25   99   DX
D4   50   25   DX
*
* OUTPUT STAGE
*
GSY  99   50   POLY (1)   (99, 50)   277.5E-6  7.5E-6
R9   99   20   100E3
R10  20   50   100E3
Q3   45   41   99   POUT   4
Q4   45   43   50   NOUT   2
EB1  99   40   POLY (1)   (98, 25)   0.70366   1
EB2  42   50   POLY (1)   (25, 98)   0.73419   1
RB1  40   41   500
RB2  42   43   500
CF   45   25   11E-12
D5   46   99   DX
D6   47   43   DX
V3   46   41   0.7
V4   47   50   0.7
.
MODEL   PIX    PNP  (Bf=117.7)
.MODEL  POUT   PNP  (BF=119, IS=2.782E-17, VAF=28,  KF=3E-7)
.MODEL  NOUT   NPN  (BF=110, IS=1.786E-17, VAF=90,  KF=3E-7)
.MODEL  DX     D()
.ENDS
```

OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(RN-8)

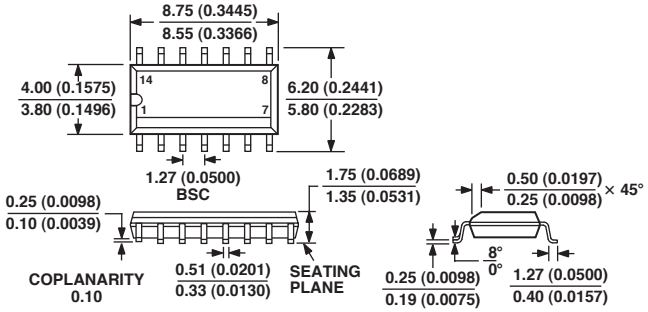
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

14-Lead Standard Small Outline Package [SOIC]
Narrow Body
(RN-14)

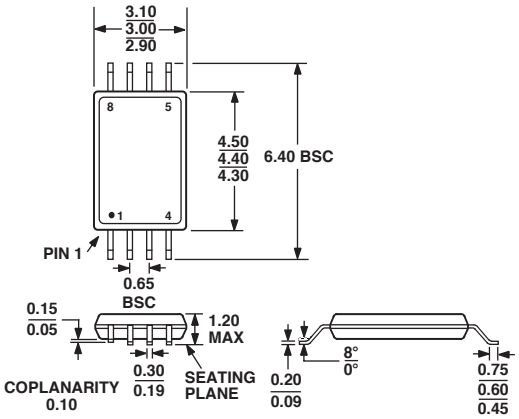
Dimensions shown in millimeters and (inches)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-8)

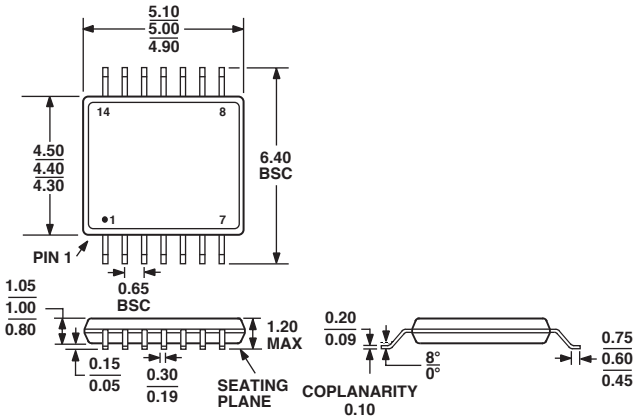
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AA

14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153AB-1

OP162/OP262/OP462

Revision History

Location	Page
10/02—Data Sheet changed from REV. C to REV. D.	
Deleted 8-Lead Plastic DIP (N-8)	Universal
Deleted 14-Lead Plastic DIP (N-14)	Universal
Edits to ORDERING GUIDE	5
Edits to Figure 30	10
Edits to Figure 31	10
Updated OUTLINE DIMENSIONS	15

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