Rail-to-Rail High Output Current Operational Amplifiers

OP179/OP279

FEATURES

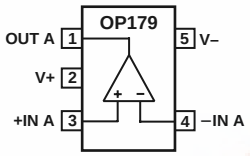
Rail-to-Rail Inputs and Outputs
High Output Current: ±60 mA
Single Supply: +5 V to +12 V
Wide Bandwidth: 5 MHz
High Slew Rate: 3 V/μs
Low Distortion: 0.01%
Unity-Gain Stable
No Phase Reversal
Short Circuit Protected
Drives Capacitive Loads: 10 nF

APPLICATIONS

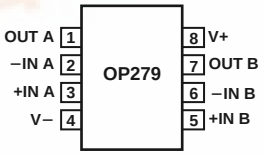
Multimedia
Telecom
DAA Transformer Driver
LCD Driver
Low Voltage Servo Control
Modems
FET Drivers

PIN CONFIGURATIONS

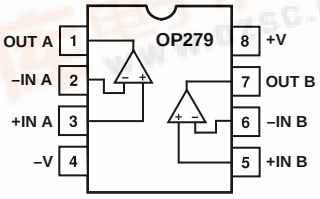
5-Lead SOT-23-5
(RT-5)



8-Lead SOIC and TSSOP
SO-8 (R) and RU-8



8-Lead Plastic DIP
(N-8)



GENERAL DESCRIPTION

The OP179 and OP279 are rail-to-rail, high output current, single-supply amplifiers. They are designed for low voltage applications that require either current or capacitive load drive capability. The OP179/OP279 can sink and source currents of ±60 mA (typical) and are stable with capacitive loads to 10 nF.

Applications that benefit from the high output current of the OP179/OP279 include driving headphones, displays, transformers and power transistors. The powerful output is combined with a unique input stage that maintains very low distortion with wide common-mode range, even in single supply designs.

The OP179/OP279 can be used as a buffer to provide much greater drive capability than can usually be provided by CMOS outputs. CMOS ASICs and DAC often have outputs that can swing to both the positive supply and ground, but cannot drive more than a few milliamps.

Bandwidth is typically 5 MHz and the slew rate is 3 V/μs, making these amplifiers well suited for single supply applications that require audio bandwidths when used in high gain configurations. Operation is guaranteed from voltages as low as 4.5 V, up to 12 V.

Very good audio performance can be attained when using the OP179/OP279 in +5 volt systems. THD is below 0.01% with a 600 Ω load, and noise is a respectable 21 nV/$\sqrt{\text{Hz}}$. Supply current is less than 3.5 mA per amplifier.

The single OP179 is available in the 5-lead SOT-23-5 package. It is specified over the industrial (–40°C to +85°C) temperature range.

The OP279 is available in 8-lead plastic DIP, TSSOP and SO-8 surface mount packages. They are specified over the industrial (–40°C to +85°C) temperature range.

REV. F

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com

OP179/OP279–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (@ V_S = +5.0 V, V_{CM} = 2.5 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage						
OP179	V_{OS}	V_{OUT} = 2.5 V			±5	mV
OP279	V_{OS}	V_{OUT} = 2.5 V			±4	mV
Input Bias Current	I_B	V_{OUT} = 2.5 V, T_A = +25°C			±300	nA
		V_{OUT} = 2.5 V			±700	nA
Input Offset Current	I_{OS}	V_{OUT} = 2.5 V, T_A = +25°C			±50	nA
		V_{OUT} = 2.5 V			±100	nA
Input Voltage Range	V_{CM}		0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	56	66		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, 0.3 V ≤ V_{OUT} ≤ 4.7 V	20			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			4		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA Source	+4.8			V
Output Voltage Low	V_{OL}	I_L = 10 mA Sink, T_A = +25°C			75	mV
		I_L = 10 mA Sink			100	mV
Short Circuit Limit	I_{SC}	T_A = +25°C	±40			mA
Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		22		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = +4.5 V to +12 V	70	88		dB
Supply Current/Amplifier	I_{SY}	V_{OUT} = 2.5 V			3.5	mA
Supply Voltage Range	V_S		+4.5		+12	V
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 kΩ, 1 nF		3		V/µs
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			60		Degrees
Capacitive Load Drive		No Oscillation		10		nF
AUDIO PERFORMANCE						
Total Harmonic Distortion	THD			0.01		%
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz

ELECTRICAL SPECIFICATIONS (@ V_S = ±5.0 V, –40°C ≤ T_A ≤ +85°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
INPUT CHARACTERISTICS						
Offset Voltage						
OP179	V_{OS}	V_{OUT} = 0			±5	mV
OP279	V_{OS}	V_{OUT} = 0			±4	mV
Input Bias Current	I_B	T_A = +25°C			±300	nA
					±700	nA
Input Offset Current	I_{OS}	T_A = +25°C			±50	nA
					±100	nA
Input Voltage Range	V_{CM}		–5		+5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –5 V to +5 V	56	66		dB
Large Signal Voltage Gain	A_{VO}	R_L = 1 kΩ, –4.7 V ≤ V_{OUT} ≤ 4.7 V	20			V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			3		µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 10 mA Source	+4.8			V
Output Voltage Low	V_{OL}	I_L = 10 mA Sink			–4.85	V
Short Circuit Limit	I_{SC}	T_A = +25°C	±50			mA
Open-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = +1		22		Ω
POWER SUPPLY						
Supply Current/Amplifier	I_{SY}	V_S = ±6 V, V_{OUT} = 0 V			3.75	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 1 kΩ, 1 nF		3		V/µs
Full-Power Bandwidth	BW_p	1% Distortion				kHz
Gain Bandwidth Product	GBP			5		MHz
Phase Margin	ϕm			69		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		22		nV/√Hz
Current Noise Density	i_n			1		pA/√Hz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . +16 V
Input Voltage . . . . . +16 V
Differential Input Voltage[1] . . . . . ±1 V
Output Short-Circuit Duration to GND . . . . . Indefinite
Storage Temperature Range
P, S, RT, RU Package . . . . . –65°C to +150°C
Operating Temperature Range
OP179G/OP279G . . . . . –40°C to +85°C
Junction Temperature Range
P, S, RT, RU Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . +300°C

Package Types	θ_{JA}[2]	θ_{JC}	Unit
5-Lead SOT-23 (RT)	256	81	°C/W
8-Lead Plastic DIP (P)	103	43	°C/W
8-Lead SOIC (S)	158	43	°C/W
8-Lead TSSOP (RU)	240	43	°C/W

NOTES
[1]The inputs are clamped with back-to-back diodes. If the differential input voltage exceeds 1 volt, the input current should be limited to 5 mA.
[2]θ_{JA} is specified for the worst case conditions, i.e., θ_{JA} is specified for device in socket for P-DIP, packages; θ_{JA} is specified for device soldered in circuit board for SOIC packages.

ORDERING GUIDE

Package	Temperature Range	Package Description	Package Option	Brand Code
OP179GRT	–40°C to +85°C	5-Lead SOT-23	RT-5	A2G
OP279GP	–40°C to +85°C	8-Lead Plastic DIP	N-8	
OP279GS	–40°C to +85°C	8-Lead SOIC	SO-8	
OP279GRU	–40°C to +85°C	8-Lead TSSOP	RU-8	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP179/OP279 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Typical Performance Graphs

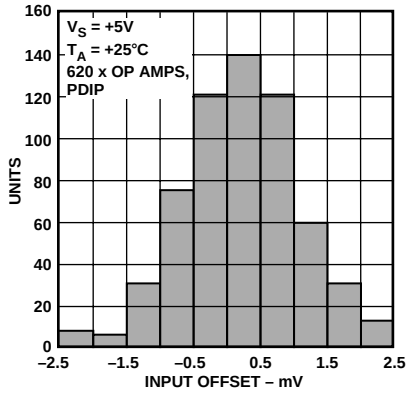


Figure 1. Input Offset Distribution

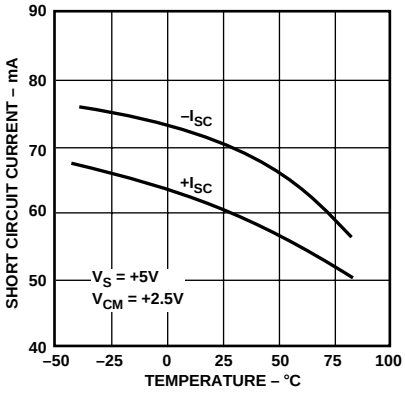


Figure 2. Short Circuit Current vs. Temperature

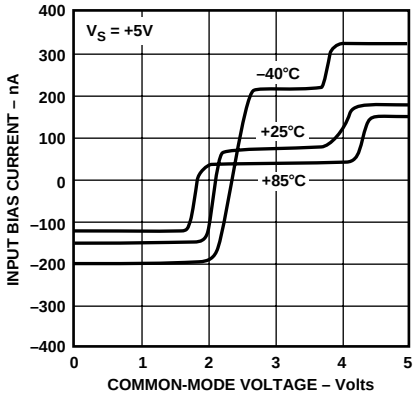


Figure 3. Input Bias Current vs. Common-Mode Voltage

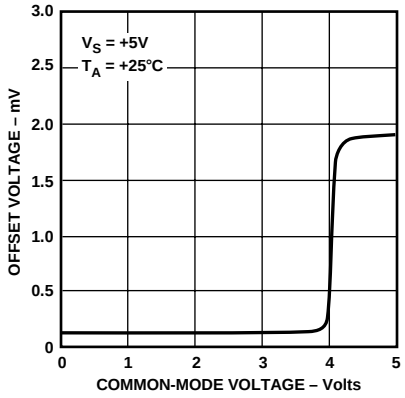


Figure 4. Offset Voltage vs. Common-Mode Voltage

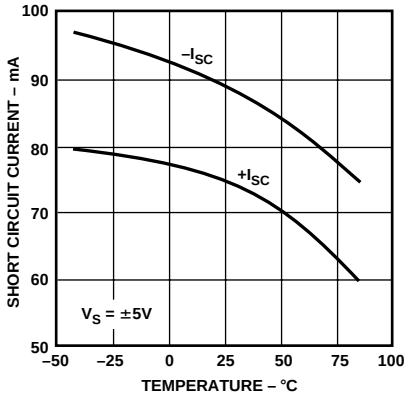


Figure 5. Short Circuit Current vs. Temperature

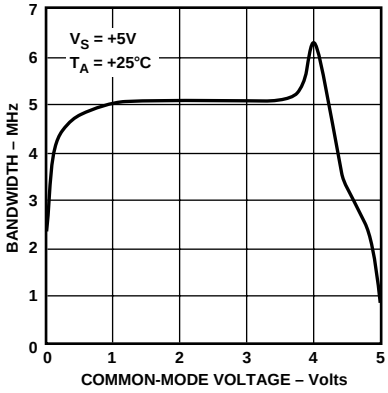


Figure 6. Bandwidth vs. Common-Mode Voltage

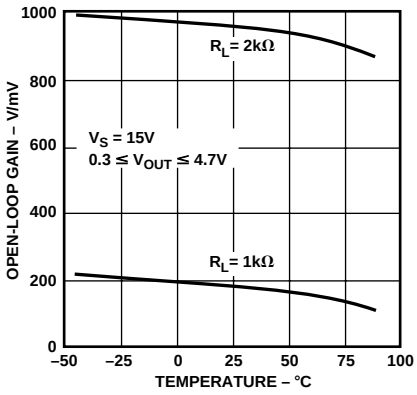


Figure 7. Open-Loop Gain vs. Temperature

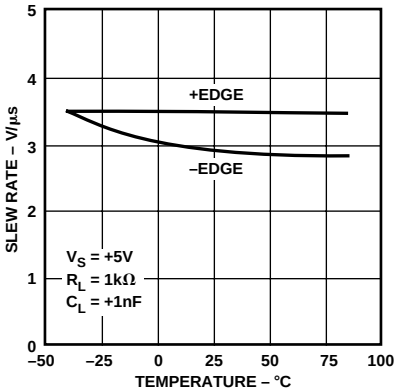


Figure 8. Slew Rate vs. Temperature

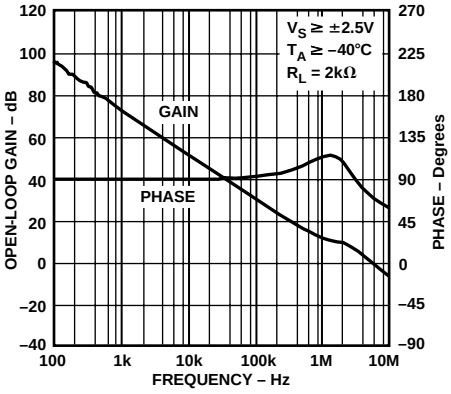


Figure 9. Open-Loop Gain and Phase vs. Frequency

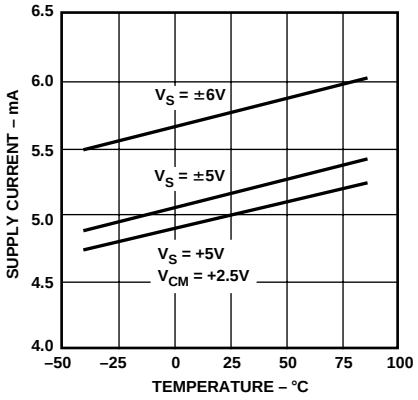


Figure 10. Supply Current vs. Temperature

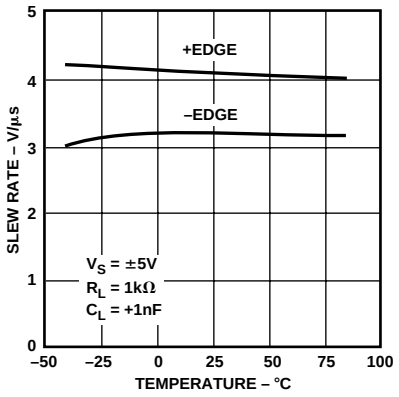


Figure 11. Slew Rate vs. Temperature

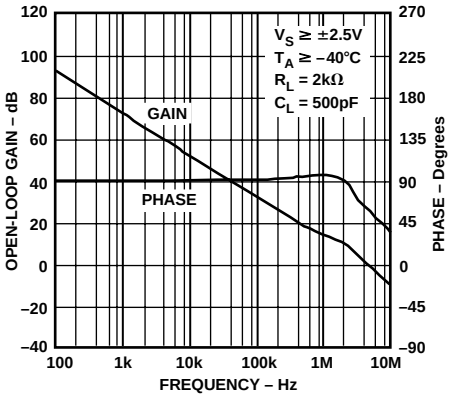


Figure 12. Open-Loop Gain and Phase vs. Frequency

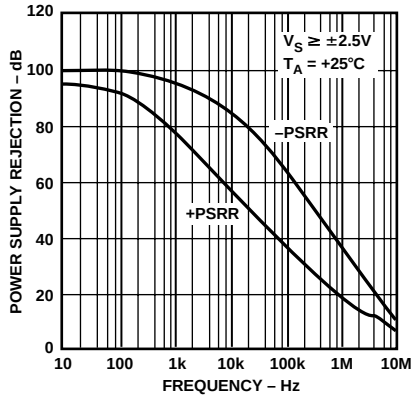


Figure 13. Power Supply Rejection vs. Frequency

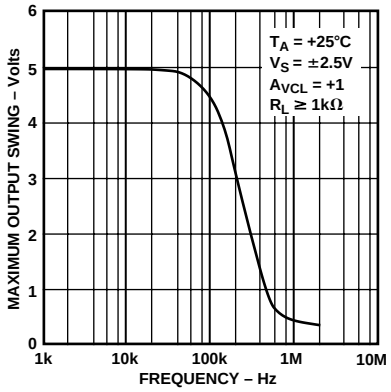


Figure 14. Maximum Output Swing vs. Frequency

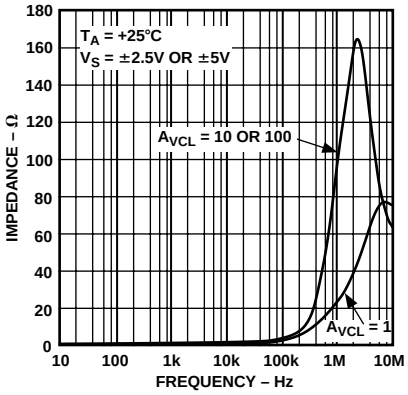


Figure 15. Closed-Loop Output Impedance vs. Frequency

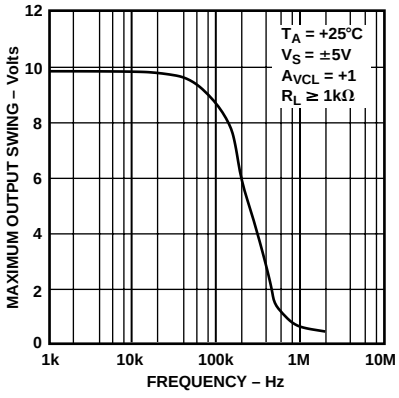


Figure 16. Maximum Output Swing vs. Frequency

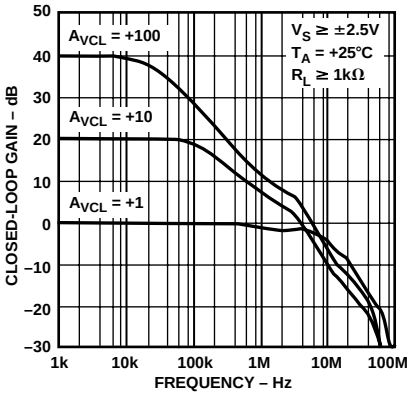


Figure 17. Closed-Loop Gain vs. Frequency

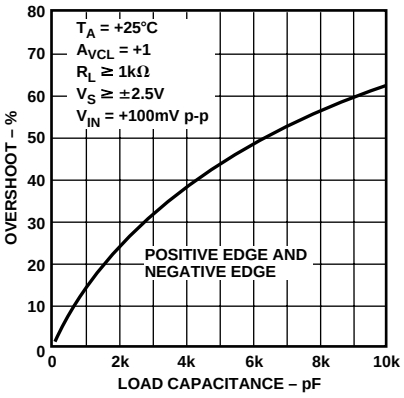


Figure 18. Small Signal Overshoot vs. Load Capacitance

Typical Performance Graphs

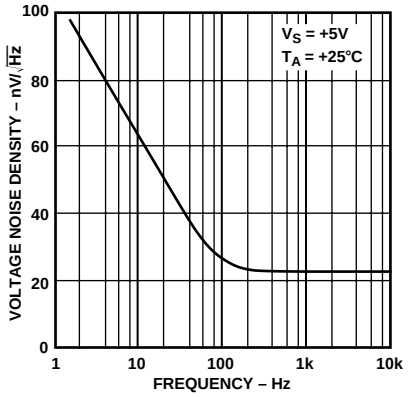


Figure 19. Voltage Noise Density vs. Frequency

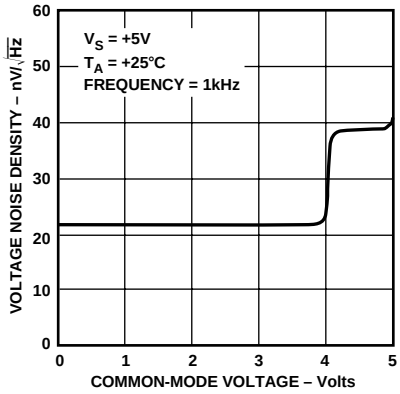


Figure 20. Voltage Noise Density vs. Common-Mode Voltage

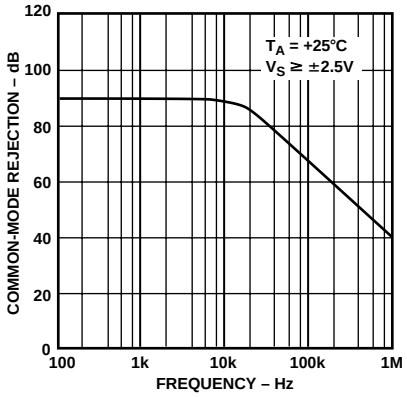


Figure 21. Common-Mode Rejection vs. Frequency

THEORY OF OPERATION

The OP179/OP279 is the latest entry in Analog Devices' expanding family of single-supply devices, designed for the multimedia and telecom marketplaces. It is a high output current drive, rail-to-rail input /output operational amplifier, powered from a single +5 V supply. It is also intended for other low supply voltage applications where low distortion and high output current drive are needed. To combine the attributes of high output current and low distortion in rail-to-rail input/output operation, novel circuit design techniques are used.

For example, Figure 1 illustrates a simplified equivalent circuit for the OP179/OP279's input stage. It is comprised of two PNP differential pairs, Q5-Q6 and Q7-Q8, operating in parallel, with diode protection networks. Diode networks D5-D6 and D7-D8 serve to clamp the applied differential input voltage to the OP179/OP279, thereby protecting the input transistors against avalanche damage. The fundamental differences between these two PNP gain stages are that the Q7-Q8 pair are normally OFF and that their inputs are buffered from the operational amplifier inputs by Q1-D1-D2 and Q9-D3-D4. Operation is best understood as a function of the applied common-mode voltage: When the inputs of the OP179/OP279 are biased midway between the supplies, the differential signal path gain is controlled by the resistively loaded (via R7, R8) Q5-Q6. As the input common-mode level is reduced toward the negative supply (V_{NEG} or GND), the input transistor current sources, I1 and I3, are forced into saturation, thereby forcing the Q1-D1-D2 and Q9-D3-D4 networks into cutoff; however, Q5-Q6 remain active, providing input stage gain. On the other hand, when the common-mode input voltage is increased toward the positive supply, Q5-Q6 are driven into cutoff, Q3 is driven into saturation, and Q4 becomes active, providing bias to the Q7-Q8 differential pair. The point at which the Q7-Q8 differential pair becomes active is approximately equal to (V_{POS} – 1 V).

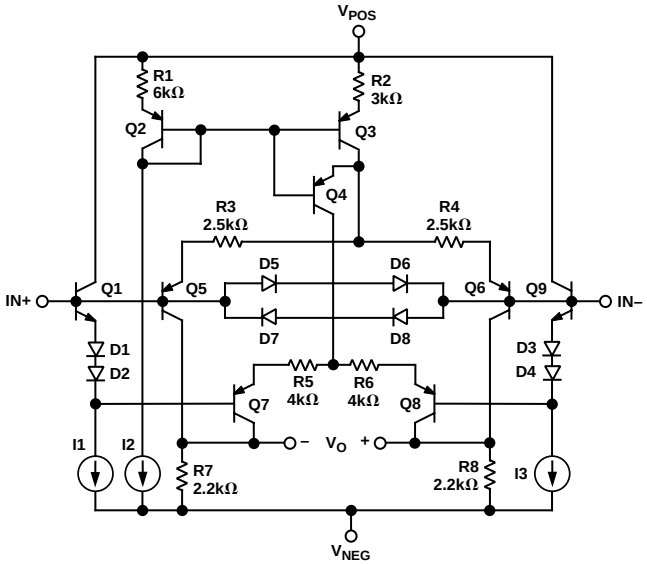


Figure 22. OP179/OP279 Equivalent Input Circuit

The key issue here is the behavior of the input bias currents in this stage. The input bias currents of the OP179/OP279 over the range of common-mode voltages from (V_{NEG} + 1 V) to (V_{POS} – 1 V) are the arithmetic sum of the base currents in Q1-Q5 and Q9-Q6. Outside of this range, the input bias currents are dominated by the base current sum of Q5-Q6 for input signals close to V_{NEG}, and of Q1-Q5 (Q9-Q6) for input signals close to V_{POS}. As a result of this design approach, the input bias currents in the OP179/OP279 not only exhibit different amplitudes, but also exhibit different polarities. This input bias current behavior is best illustrated in Figure 3. It is, therefore, of paramount importance that the effective source impedances connected to the OP179/OP279's inputs are balanced for optimum dc and ac performance.

In order to achieve rail-to-rail output behavior, the OP179/OP279 design employs a complementary common-emitter (or g_mR_L) output stage (Q15-Q16), as illustrated in Figure 23. These amplifiers provide output current until they are forced into saturation which occurs at approximately 50 mV from either supply rail. Thus, their saturation voltage is the limit on the maximum output voltage swing in the OP179/OP279. The output stage also exhibits voltage gain, by virtue of the use of common-emitter amplifiers; and, as a result, the voltage gain of the output stage (thus, the open-loop gain of the device) exhibits a strong dependence to the total load resistance at the output of the OP179/OP279 as illustrated in Figure 7.

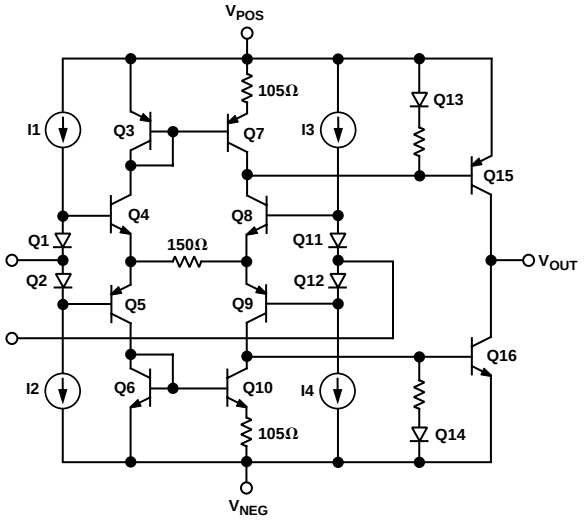


Figure 23. OP179/OP279 Equivalent Output Circuit

Input Overvoltage Protection

As with any semiconductor device, whenever the condition exists for the input to exceed either supply voltage, the device's input overvoltage characteristic must be considered. When an overvoltage occurs, the amplifier could be damaged, depending on the magnitude of the applied voltage and the magnitude of the fault current. Figure 24 illustrates the input overvoltage characteristic of the OP179/OP279. This graph was generated with the power supplies at ground and a curve tracer connected to the input. As can be seen, when the input voltage exceeds either supply by more than 0.6 V, internal pn-junctions energize, which allows current to flow from the input to the supplies. As illustrated in the simplified equivalent input circuit (Figure 22), the OP179/OP279 does not have any internal current limiting resistors, so fault currents can quickly rise to damaging levels.

This input current is not inherently damaging to the device as long as it is limited to 5 mA or less. For the OP179/OP279, once the input voltage exceeds the supply by more than 0.6 V, the input current quickly exceeds 5 mA. If this condition continues to exist, an external series resistor should be added. The size of the resistor is calculated by dividing the maximum overvoltage by 5 mA. For example, if the input voltage could reach 100 V, the external resistor should be (100 V/5 mA) = 20 kΩ. This resistance should be placed in series with either or both inputs if they are exposed to an overvoltage. Again, in order to ensure optimum dc and ac performance, it is important to balance source impedance levels. For more information on general overvoltage characteristics of amplifiers refer to the *1993 Seminar Applications Guide,* available from the Analog Devices Literature Center.

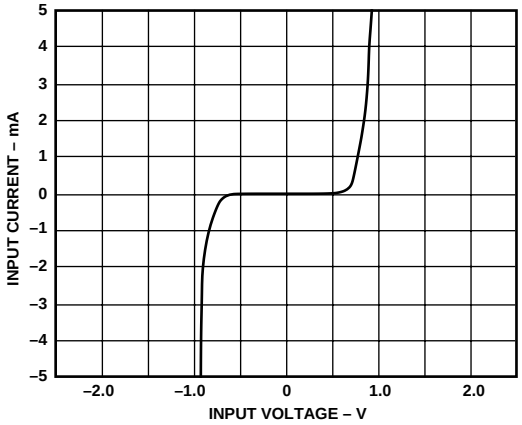


Figure 24. OP179/OP279 Input Overvoltage Characteristic

Output Phase Reversal

Some operational amplifiers designed for single supply operation exhibit an output voltage phase reversal when their inputs are driven beyond their useful common-mode range. Typically for single-supply bipolar op amps, the negative supply determines the lower limit of their common-mode range. With these devices, external clamping diodes, with the anode connected to ground and the cathode to the inputs, input signal excursions are prevented from exceeding the device's negative supply (i.e., GND), preventing a condition that could cause the output voltage to change phase. JFET input amplifiers may also exhibit phase reversal and, if so, a series input resistor is usually required to prevent it.

The OP179/OP279 is free from reasonable input voltage range restrictions provided that input voltages no greater than the supply voltages are applied. Although the device's output will not change phase, large currents can flow through the input protection diodes, shown in Figure 22. Therefore, the technique recommended in the Input Overvoltage Protection section should be applied in those applications where the likelihood of input voltages exceeding the supply voltages is possible.

Capacitive Load Drive

The OP179/OP279 has excellent capacitive load driving capabilities. It can drive up to 10 nF directly as the performance graph titled Small Signal Overshoot vs. Load Capacitance (Figure 18) shows. However, even though the device is stable, a capacitive load does not come without a penalty in bandwidth. As shown in Figure 25, the bandwidth is reduced to under 1 MHz for loads greater than 3 nF. A "snubber" network on the output won't increase the bandwidth, but it does significantly reduce the amount of overshoot for a given capacitive load. A snubber consists of a series R-C network (R_S, C_S), as shown in Figure 26, connected from the output of the device to ground. This network operates in parallel with the load capacitor, C_L, to provide phase lag compensation. The actual value of the resistor and capacitor is best determined empirically.

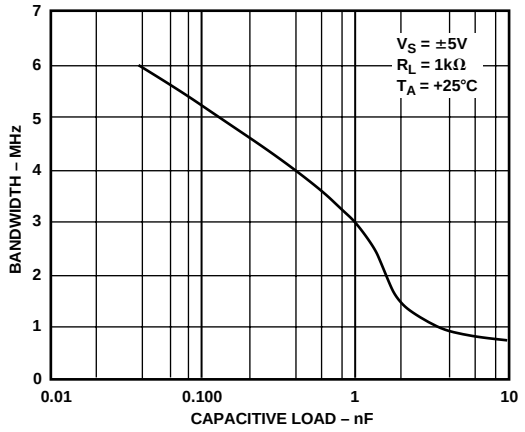


Figure 25. OP179/OP279 Bandwidth vs. Capacitive Load

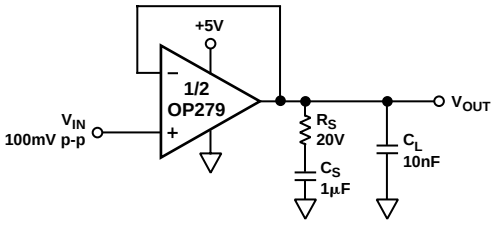


Figure 26. Snubber Network Compensates for Capacitive Load

The first step is to determine the value of the resistor, R_S. A good starting value is 100 Ω (typically, the optimum value will be less than 100 Ω). This value is reduced until the small-signal transient response is optimized. Next, C_S is determined—10 µF is a good starting point. This value is reduced to the smallest value for acceptable performance (typically, 1 µF). For the case of a 10 nF load capacitor on the OP179/OP279, the optimal snubber network is a 20 Ω in series with 1 µF. The benefit is immediately apparent as seen in the scope photo in Figure 27. The top trace was taken with a 10 nF load and the bottom trace with the 20 Ω, 1 µF snubber network in place. The amount of overshot and ringing is dramatically reduced. Table I illustrates a few sample snubber networks for large load capacitors.

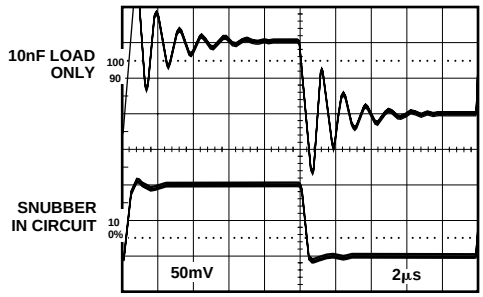


Figure 27. Overshoot and Ringing Is Reduced by Adding a "Snubber" Network in Parallel with the 10 nF Load

Table I. Snubber Networks for Large Capacitive Loads

Load Capacitance (C_L)	Snubber Network (R_S, C_S)
10 nF	20 Ω, 1 µF
100 nF	5 Ω, 10 µF
1 µF	0 Ω, 10 µF

Overload Recovery Time

Overload, or overdrive, recovery time of an operational amplifier is the time required for the output voltage to recover to its linear region from a saturated condition. This recovery time is important in applications where the amplifier must recover after a large transient event. The circuit in Figure 28 was used to evaluate the OP179/OP279's overload recovery time. The OP179/OP279 takes approximately 1 µs to recover from positive saturation and approximately 1.2 µs to recover from negative saturation.

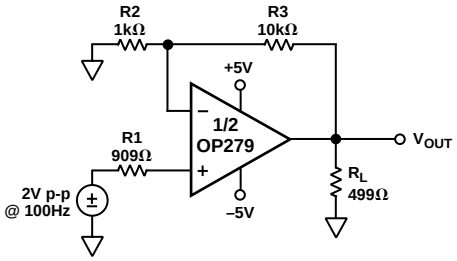


Figure 28. Overload Recovery Time Test Circuit

Output Transient Current Recovery

In many applications, operational amplifiers are used to provide moderate levels of output current to drive the inputs of ADCs, small motors, transmission lines and current sources. It is in these applications that operational amplifiers must recover quickly to step changes in the load current while maintaining steady-state load current levels. Because of its high output current capability and low closed-loop output impedance, the OP179/OP279 is an excellent choice for these types of applications. For example, when sourcing or sinking a 25 mA steady-state load current, the OP179/OP279 exhibits a recovery time of less than 500 ns to 0.1% for a 10 mA (i.e., 25 mA to 35 mA and 35 mA to 25 mA) step change in load current.

A Precision Negative Voltage Reference

In many data acquisition applications, the need for a precision negative reference is required. In general, any positive voltage reference can be converted into a negative voltage reference through the use of an operational amplifier and a pair of matched resistors in an inverting configuration. The disadvantage to that approach is that the largest single source of error in the circuit is the relative matching of the resistors used.

The circuit illustrated in Figure 29 avoids the need for tightly matched resistors with the use of an active integrator circuit. In this circuit, the output of the voltage reference provides the input drive for the integrator. The integrator, to maintain circuit equilibrium, adjusts its output to establish the proper relationship between the reference's V_{OUT} and GND. Thus, various negative output voltages can be chosen simply by substituting for the appropriate reference IC (see table). To speed up the

ON-OFF settling time of the circuit, R2 can be reduced to 50 kΩ or less. Although the integrator's time constant chosen here is 1 ms, room exists to trade-off circuit bandwidth and noise by increasing R3 and decreasing C2. The SHUTDOWN feature is maintained in the circuit with the simple addition of a PNP transistor and a 10 kΩ resistor. One caveat with this approach should be mentioned: although rail-to-rail output amplifiers work best in the application, these operational amplifiers require a finite amount (mV) of headroom when required to provide any load current. The choice for the circuit's negative supply should take this issue into account.

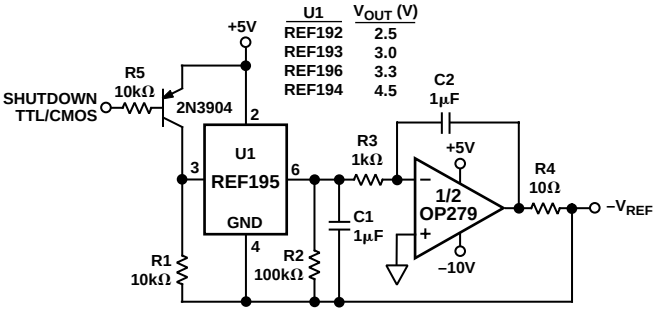


Figure 29. A Negative Precision Voltage Reference That Uses No Precision Resistors Exhibits High Output Current Drive

A High Output Current, Buffered Reference/Regulator

Many applications require stable voltage outputs relatively close in potential to an unregulated input source. This "low dropout" type of reference/regulator is readily implemented with a rail-to-rail output op amp, and is particularly useful when using a higher current device such as the OP179/OP279. A typical example is the 3.3 V or 4.5 V reference voltage developed from a 5 V system source. Generating these voltages requires a three-terminal reference, such as the REF196 (3.3 V) or the REF194 (4.5 V), both of which feature low power, with sourcing outputs of 30 mA or less. Figure 30 shows how such a reference can be outfitted with an OP179/OP279 buffer for higher currents and/or voltage levels, plus sink and source load capability.

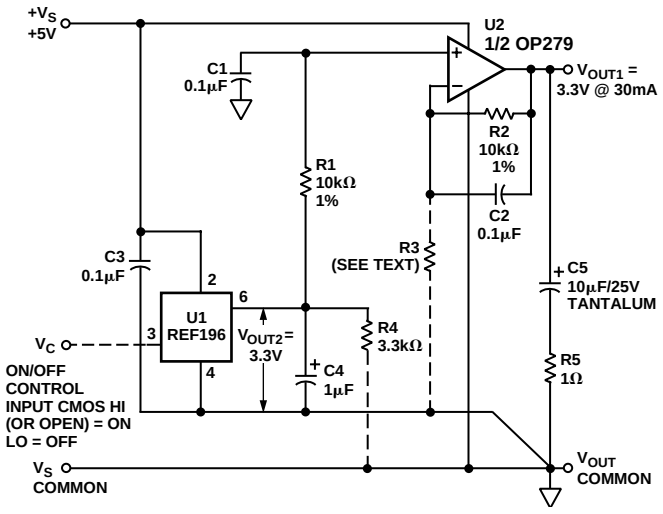


Figure 30. A High Output Current Reference/Regulator

The low dropout performance of this circuit is provided by stage U2, one-half of an OP179/OP279 connected as a follower/buffer for the basic reference voltage produced by U1. The low voltage saturation characteristic of the OP179/OP279 allows up to 30 mA of load current in the illustrated use, as a 5 V to 3.3 V converter with high dc accuracy. In fact, the dc output voltage change for a 30 mA load current delta measures less than 1 mV. This corresponds to an equivalent output impedance of < 0.03 Ω. In this application, the stable 3.3 V from U1 is applied to U2 through a noise filter, R1-C1. U2 replicates the U1 voltage within a few mV, but at a higher current output at V_{OUT1}, with the ability to both sink and source output current(s)—unlike most IC references. R2 and C2 in the feedback path of U2 provide bias compensation for lowest dc error and additional noise filtering.

Transient performance of the reference/regulator for a 10 mA step change in load current is also quite good and is determined largely by the R5-C5 output network. With values as shown, the transient is about 10 mV peak and settles to within 2 mV in 8 μs, for either polarity. Although room exists for optimizing the transient response, any changes to the R5-C5 network should be verified by experiment to preclude the possibility of excessive ringing with some capacitor types.

To scale V_{OUT2} to another (higher) output level, the optional resistor R3 (shown dotted) is added, causing the new V_{OUT1} to become:

$$V_{OUT1} = V_{OUT2} \times \left(1 + \frac{R2}{R3}\right)$$

As an example, for a V_{OUT1} = 4.5 V, and V_{OUT2} = 2.5 V from a REF192, the gain required of U2 is 1.8 times, so R2 and R3 would be chosen for a ratio of 0.8:1, or 18 kΩ:22.5 kΩ. Note that for the lowest V_{OUT1} dc error, the parallel combination of R2 and R3 should be maintained equal to R1 (as here), and the R2-R3 resistors should be stable, close tolerance metal film types.

The circuit can be used as shown as either a 5 V to 3.3 V reference/regulator, or it can be used with ON/OFF control. By driving Pin 3 of U1 with a logic control signal as noted, the output is switched ON/OFF. Note that when ON/OFF control is used, resistor R4 should be used with U1 to speed ON-OFF switching.

Direct Access Arrangement for Telephone Line Interface

Figure 31 illustrates a +5 V only transmit/receive telephone line interface for 110 Ω transmission systems. It allows full duplex transmission of signals on a transformer coupled 110 Ω line in a differential manner. Amplifier A1 provides gain that can be adjusted to meet the modem output drive requirements. Both A1 and A2 are configured to apply the largest possible signal on a single supply to the transformer. Because of the OP179/OP279's high output current drive and low dropout voltage, the largest signal available on a single +5 V supply is approximately 4.5 V p-p into a 110 Ω transmission system. Amplifier A3 is configured as a difference amplifier to extract the receive signal from the transmission line for amplification by A4. A4's gain can be adjusted in the same manner as A1's to meet the modem's input signal requirements. Standard resistor values permit the use of SIP (Single In-line Package) format resistor arrays. Couple this with the OP179/OP279's 8-lead SOIC footprint and this circuit offers a compact, cost-sensitive solution.

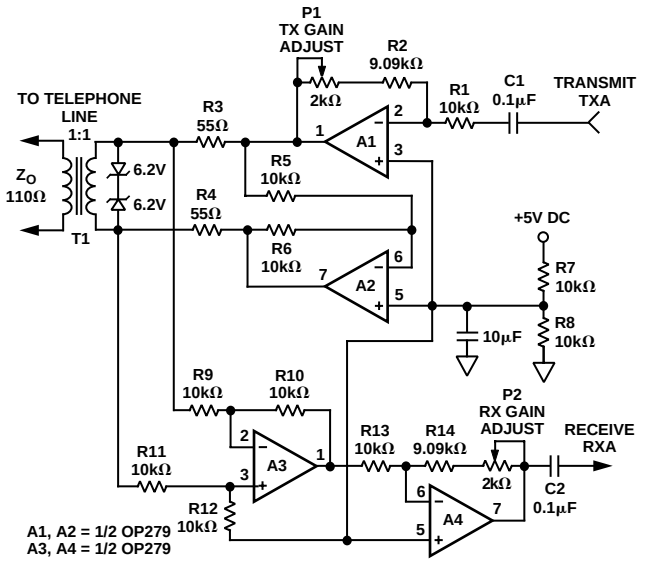


Figure 31. A Single Supply Direct Access Arrangement for Modems

A Single Supply, Remote Strain Gage Signal Conditioner

The circuit in Figure 32 illustrates a way by which the OP179/OP279 can be used in a +12 V single supply, 350 Ω strain gage signal conditioning circuit. In this circuit, the OP179/OP279 serves two functions: (1) By servoing the output of the REF43's +2.5 V output across R1, it provides a 20 mA drive to the 350 Ω strain gage. In this way, small changes in the strain gage produce large differential output voltages across the AMP04's inputs. (2) To maximize the circuit's dynamic range, the other half of the OP179/OP279 is configured as a supply-splitter connected to the AMP04's REF terminal. Thus, tension or compression in the application can be measured by the circuit.

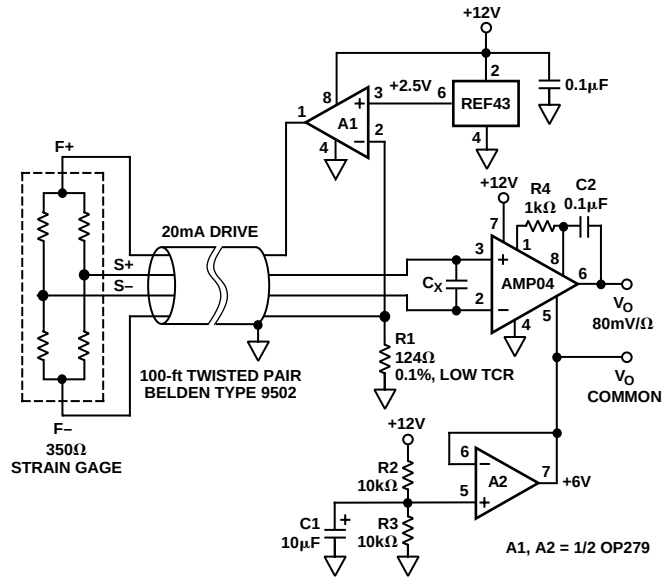


Figure 32. A Single Supply, Remote Strain Gage Signal Conditioner

The AMP04 is configured for a gain of 100, producing a circuit sensitivity of 80 mV/Ω. Capacitor C2 is used across the AMP04's Pins 8 and 6 to provide a 16-Hz noise filter. If additional noise filtering is required, an optional capacitor, C_X, can be used across the AMP04's input to provide differential-mode noise rejection.

A Single Supply, Balanced Line Driver

The circuit in Figure 33 is a unique line driver circuit topology used in professional audio applications and has been modified for automotive audio applications. On a single +12 V supply, the line driver exhibits less than 0.02% distortion into a 600 Ω load across the entire audio band (not shown). For loads greater than 600 Ω, distortion performance improves to where the circuit exhibits less than 0.002%. The design is a transformerless, balanced transmission system where output common-mode rejection of noise is of paramount importance. Like the transformer-based system, either output can be shorted to ground for unbalanced line driver applications without changing the circuit gain of 1. Other circuit gains can be set according to the equation in the diagram. This allows the design to be easily configured for noninverting, inverting, or differential operation.

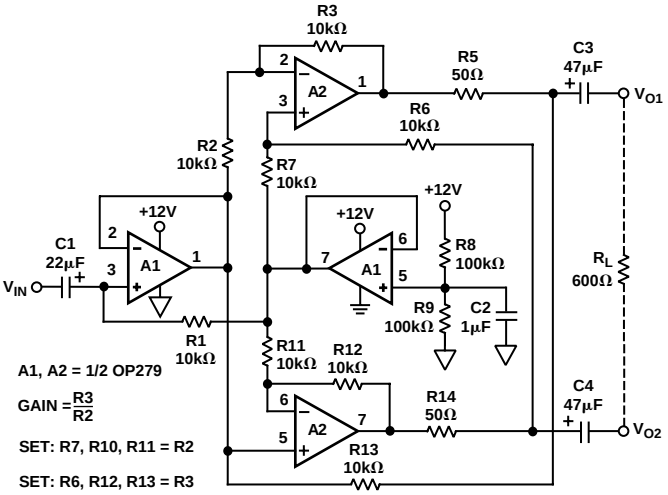


Figure 33. A Single Supply, Balanced Line Driver for Automotive Applications

A Single Supply Headphone Amplifier

Because of its high speed and large output drive, the OP179/OP279 makes for an excellent headphone driver, as illustrated in Figure 34. Its low supply operation and rail-to-rail inputs and outputs give a maximum signal swing on a single +5 V supply. To ensure maximum signal swing available to drive the headphone, the amplifier inputs are biased to V+/2, which is in this case 2.5 V. The 100 kΩ resistor to the positive supply is equally split into two 50 kΩ with their common point bypassed by 10 µF to prevent power supply noise from contaminating the audio signal.

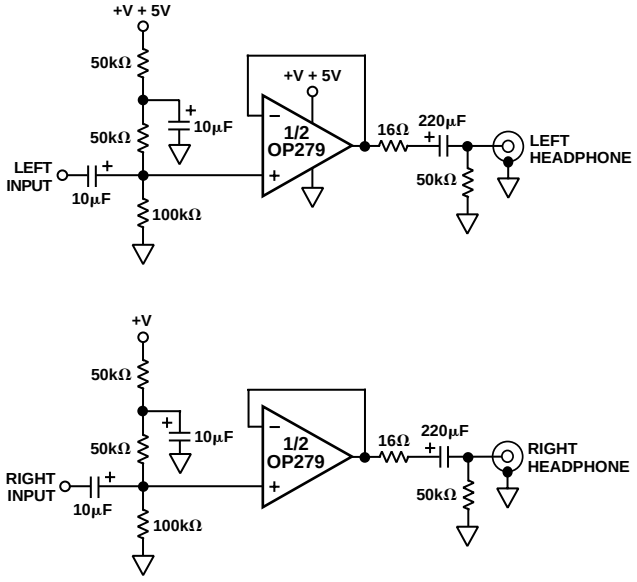


Figure 34. A Single Supply, Stereo Headphone Driver

The audio signal is then ac-coupled to each input through a 10 µF capacitor. A large value is needed to ensure that the 20 Hz audio information is not blocked. If the input already has the proper dc bias, the ac coupling and biasing resistors are not required. A 220 µF capacitor is used at the output to couple the amplifier to the headphone. This value is much larger than that used for the input because of the low impedance of the headphones, which can range from 32 Ω to 600 Ω. An additional 16 Ω resistor is used in series with the output capacitor to protect the op amp's output stage by limiting capacitor discharge current. When driving a 48 Ω load, the circuit exhibits less than 0.02% THD+N at low output drive levels (not shown). The OP179/OP279's high current output stage can drive this heavy load to 4 V p-p and maintain less than 1% THD+N.

Active Filters

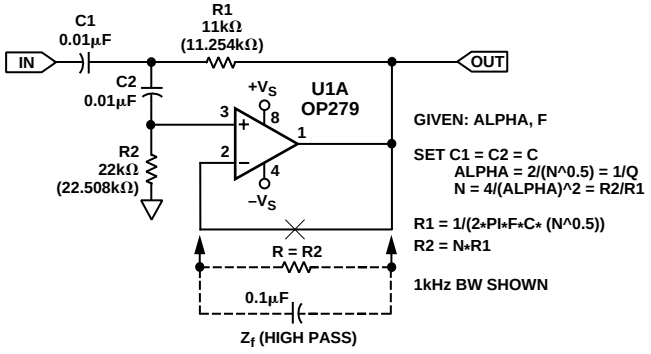
Several active filter topologies are useful with the OP179/OP279. Among these are two popular architectures, the familiar Sallen-Key (SK) voltage controlled voltage source (VCVS) and the multiple feedback (MFB) topologies. These filter types can be arranged for high pass (HP), low pass (LP), and bandpass (BP) filters. The SK filter type uses the op amp as a fixed gain voltage follower at unity or a higher gain, while the MFB structure uses it as an inverting stage. Discussed here are simplified, 2-pole forms of these filters, highly useful as system building blocks.

UNITY-GAIN, SALLEN-KEY (VCVS) FILTERS

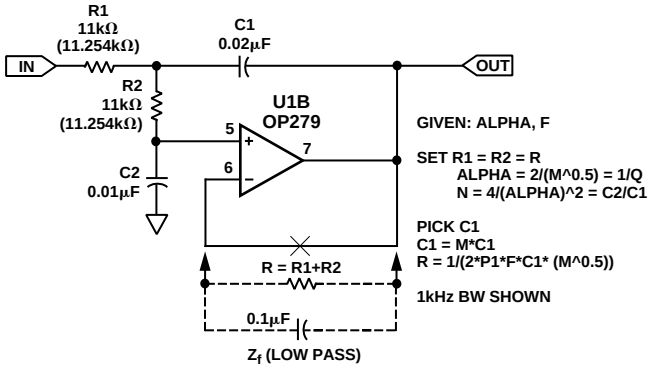
High Pass Configurations

In Figure 35a is the HP form of a unity-gain 2-pole SK filter using an OP179/OP279 section. For this filter and its LP counterpart, the gain in the passband is inherently unity, and the signal phase is noninverting due to the follower hookup. For simplicity and practicality, capacitors C1-C2 are set equal, and resistors R2-R1 are adjusted to a ratio "N," which provides the filter damping "α" as per the design expressions. A HP design is begun with selection of standard capacitor values for C1 and C2 and a calculation of N; then R1 and R2 are calculated as per the figure expressions.

In these examples, α (or 1/Q) is set equal to $\sqrt{2}$, providing a Butterworth (maximally flat) response characteristic. The filter corner frequency is normalized to 1 kHz, with resistor values shown in both rounded and (exact) form. Various other 2-pole response shapes are also possible with appropriate selection of α. For a given response type (α), frequency can be easily scaled, using proportional R or C values.



a. High Pass



b. Low Pass

Figure 35. 2-Pole Unity-Gain Sallen Key HP/LP Filters

Low Pass Configurations

In the LP SK arrangement of Figure 35b, R and C elements are interchanged, and the resistors are made equal. Here the C2/C1 ratio "M" is used to set the filter α, as noted. This design is begun with the choice of a standard capacitor value for C1 and a calculation of M, which forces a value of "M × C1" for C2. Then, the value "R" for R1 and R2 is calculated as per the expression.

For highest performance, the passive components used for tuning active filters deserve attention. Resistors should be 1%, low TC, metal film types of the RN55 or RN60 style, or similar.

Capacitors should be 1% or 2% film types preferably, such as polypropylene or polystyrene, or NPO (COG) ceramic for smaller values. Somewhat lesser performance is available with the use polyester capacitors.

Parasitic Effects in Sallen-Key Implementations

In designing these circuits, moderately low (10 kΩ or less) values for R1-R2 can be used to minimize the effects of Johnson noise when critical, with of course practical tradeoffs of capacitor size and expense. DC errors will result for larger values of resistance, unless bias current compensation is used. To add bias compensation in the HP filter of Figure 35a, a feedback compensation resistor with a value equal to R2 is used, shown optionally as Z_f. This will minimize bias induced offset, reducing it to the product of the OP179/OP279's I_{OS} and R2. Similar compensation is applied to the LP filter, using a Z_f resistance of R1 + R2. Using dc compensation and relatively low filter values, filter output dc errors using the OP179/OP279 will be dominated by V_{OS}, which is limited to 4 mV or less. A caveat here is that the additional resistors increase noise substantially—for example, an unbypassed 10 kΩ resistor generates ≈ 12 nV/$\sqrt{Hz}$ of noise. However, the resistance can be ac-bypassed to eliminate noise with a simple shunt capacitor, such as 0.1 µF.

Sallen-Key Implementations in Single Supply Applications

The hookups shown illustrate a classical dual supply op amp application, which for the OP179/OP279 would use supplies up to ±5 V. However, these filters can also use the op amp in a single-supply mode, with little if any alteration to the filter itself. To operate single-supply, the OP179/OP279 is powered from +5 V at Pin 8 with Pin 4 grounded. The input dc bias for the op amp must be supplied from a dc source equal to 1/2 supply, or 2.5 V in this case.

For the HP section, dc bias is applied to the common end of R2. R2 is simply returned to an ac ground that is a well-bypassed 2:1 divider across the 5 V source. This can be as simple as a pair of 100 kΩ resistors with a 10 µF bypass cap. The output from the stage is then ac coupled, using an appropriate coupling cap from U1A to the next stage. For the LP section dc bias is applied to the input end of R1, in common with the input signal. This dc can be taken from an unbypassed dual 100 kΩ divider across the supply, with the input signal ac coupled to the divider and R1.

Multiple Feedback Filters

MFB filters, like their SK relatives, can be used as building blocks as well. They feature LP and HP operation as well, but can also be used in a bandpass BP mode. They have the property of inverting operation in the pass band, since they are based on an inverting amplifier structure. Another useful asset is their ability to be easily configured for gain.

High Pass Configurations

Figure 36 shows an HP MFB 2-pole filter using an OP179/OP279 section. For this filter, the gain in the passband is user configurable, and the signal phase is inverting. The circuit uses one more tuning component than the SK types. For simplicity, capacitors C1 and C3 are set to equal standard values, and resistors R1-R2 are selected as per the relationships noted. Gain of this filter, H, is set by capacitors C1 and C2, and this factor limits both gain selectability and precision. Also, input capacitance C1 makes the load seen by the driving stage highly reactive, and limits overall practicality of this filter. The dire effect of C1 loading can be tempered somewhat by using a small series input resistance of about 100 Ω, but can still be an issue.

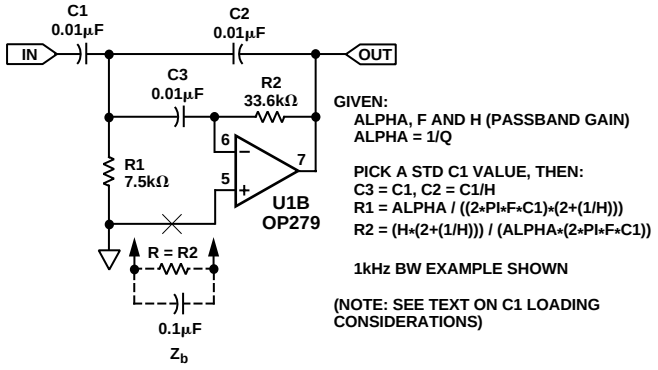


Figure 36. Two-Pole, High Pass Multiple Feedback Filters

In this example, the filter gain is set to unity, the corner frequency is 1 kHz, and the response is a Butterworth type. For applications where dc output offset is critical, bias current compensation can be used for the amplifier. This is provided by network Z_b, where R is equal to R2, and the capacitor provides a noise bypass.

Low Pass Configurations

Figure 37 is a LP MFB 2-pole filter using an OP179/OP279 section. For this filter, the gain in the pass band is user configurable over a wide range, and the pass band signal phase is inverting. Given the design parameters for α, F, and H, a simplified design process is begun by picking a standard value for C2. Then C1 and resistors R1-R3 are selected as per the relationships noted. Optional dc bias current compensation is provided by Z_b, where R is equal to the value of R3 plus the parallel equivalent value of R1 and R2.

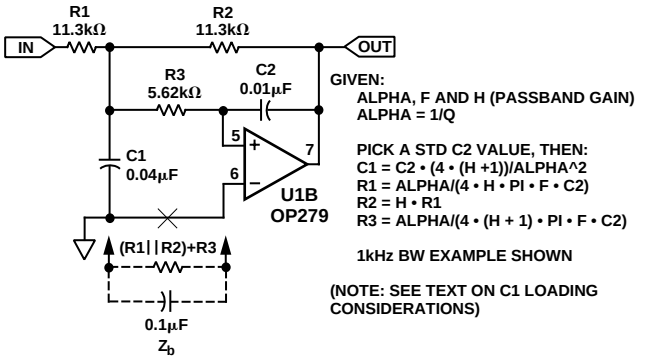


Figure 37. Two-Pole, Low-Pass Multiple Feedback Filters

Gain of this filter, H, is set here by resistors R2 and R1 (as in a standard op amp inverter), and can be just as precise as these resistors allow at low frequencies. Because of this flexible and accurate gain characteristic, plus a low range of component value spread, this filter is perhaps the most practical of all the MFB types. Capacitor ratios are best satisfied by paralleling two or more common types, as in the example, which is a 1 kHz unity gain Butterworth filter.

Bandpass Configurations

The MFB bandpass filter using an OP179/OP279 section is shown in Figure 38. This filter provides reasonably stable medium Q designs for frequencies of up to a few kHz. For best predictability and stability, operation should be restricted to applications where the OP179/OP279 has an open-loop gain in excess of $2Q^2$ at the filter center frequency.

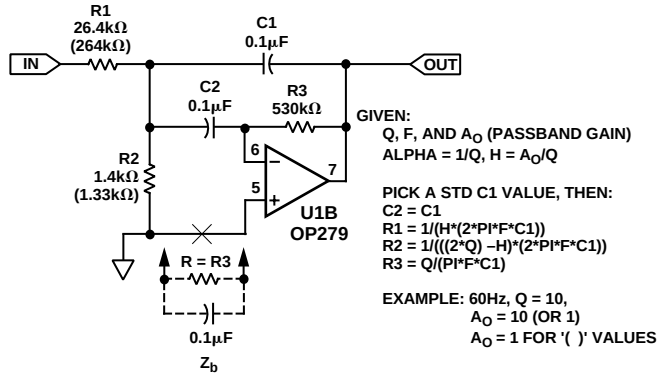


Figure 38. Two-Pole, Bandpass Multiple Feedback Filters

Given the bandpass design parameters for Q, F, and pass band gain A_O, the design process is begun by picking a standard value for C1. Then C2 and resistors R1-R3 are selected as per the relationships noted. This filter is subject to a wide range of component values by nature. Practical designs should attempt to restrict resistances to a 1 kΩ to 1 MΩ range, with capacitor values of 1 µF or less. When needed, dc bias current compensation is provided by Z_b, where R is equal to R3.

Two-Way Loudspeaker Crossover Networks

Active filters are useful in loudspeaker crossover networks for reasons of small size, relative freedom from parasitic effects, and the ease of controlling low/high channel drive, plus the controlled driver damping provided by a dedicated amplifier. Both Sallen-Key (SK) VCVS and multiple-feedback (MFB) filter architectures are useful in implementing active crossover networks (see Reference 4), and the circuit shown in Figure 39 is a two-way active crossover which combines the advantages of both filter topologies. This active crossover exhibits less than 0.01% THD+N at output levels of 1 V rms using general purpose unity gain HP/LP stages. In this two-way example, the LO signal is a dc-500 Hz LP woofer output, and the HI signal is the HP (> 500 Hz) tweeter output. U1B forms a MFB LP section at 500 Hz, while U1A provides a SK HP section, covering frequencies ≥ 500 Hz.

This crossover network is a Linkwitz-Riley type (see Reference 5), with a damping factor or α of 2 (also referred to as "Butterworth squared"). A hallmark of the Linkwitz-Riley type of filter is the fact that the summed magnitude response is flat across the pass band. A necessary condition for this to happen is the relative signal polarity of the HI output must be inverted with respect to the LOW outputs. If only SK filter sections were used, this requires that the connections to one speaker be reversed on installation. Alternately, with one inverting stage used in the LO channel, this accomplishes the same effect. In the circuit as shown, stage U1B is the MFB LP filter which provides the necessary polarity inversion. Like the SK sections, it is configured for unity gain and an α of 2. The cutoff frequency is 500 Hz, which complements the SK HP section of U4.

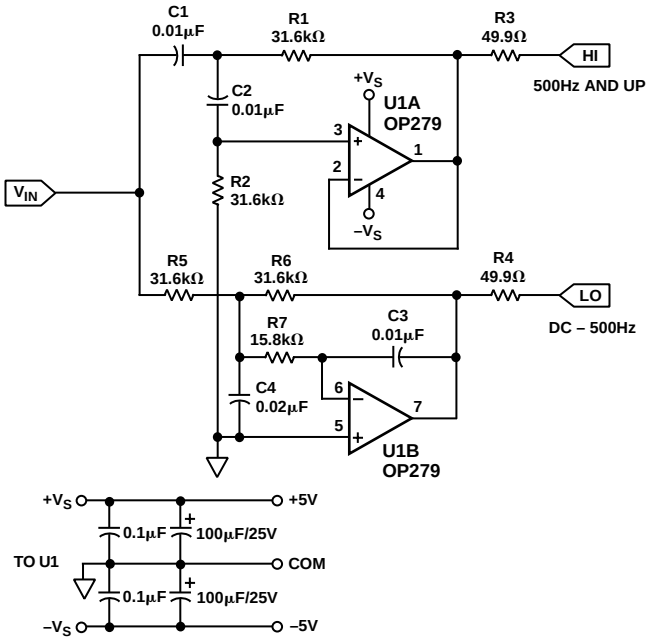


Figure 39. Two-Way Active Crossover Networks

In the filter sections, component values have been selected for good balance between reasonable physical/electrical size, and lowest noise and distortion. DC offset errors can be minimized by using dc compensation in the feedback and bias paths, ac bypassed with capacitors for low noise. Also, since the network input is reactive, it should driven from a directly coupled low impedance source at V_{IN}.

Figure 40 shows this filter architecture adapted for single supply operation from a 5 V dc source, along the lines discussed previously.

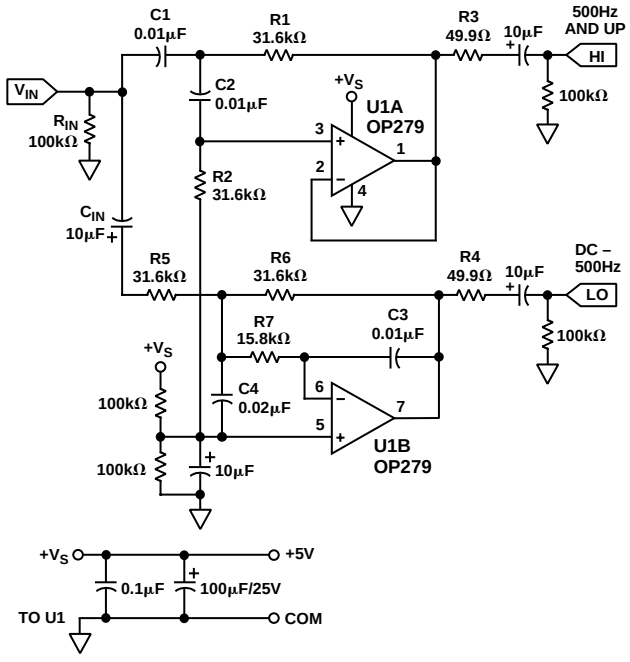


Figure 40. A Single Supply, Two-Way Active Crossover

The crossover example frequency of 500 Hz can be shifted lower or higher by frequency scaling of either resistors or capacitors. In configuring the circuit for other frequencies, complementary LP/HP action must be maintained between sections, and component values within the sections must be in the same ratio. Table II provides a design aid to adaptation, with suggested standard component values for other frequencies.

Table II. RC Component Selection for Various Crossover Frequencies

Crossover Frequency (Hz)	R1/C1 (U1A)* R5/C3 (U1B)**
100	160 kΩ/0.01 µF
200	80.6 kΩ/0.01 µF
319	49.9 kΩ/0.01 µF
500	31.6 kΩ/0.01 µF
1 k	16 kΩ/0.01 µF
2 k	8.06 kΩ/0.01 µF
5 k	3.16 kΩ/0.01 µF
10 k	1.6 kΩ/0.01 µF

Table notes (applicable for $\alpha = 2$).
* For SK stage U1A: R1 = R2, and C1 = C2, etc.
** For MFB stage U1B: R6 = R5, R7 = R5/2, and C4 = 2C3.

References on Active Filters and Active Crossover Networks

1. Sallen, R.P.; Key, E.L., "A Practical Method of Designing RC Active Filters," *IRE Transactions on Circuit Theory, vol. CT-2*, March 1955.
2. Huelsman, L.P.; Allen, P.E., *Introduction to the Theory and Design of Active Filters*, McGraw-Hill, 1980.
3. Zumbahlen, H., "Chapter 6: Passive and Active Analog Filtering," within 1992 *Analog Devices Amplifier Applications Guide*.
4. Zumbahlen, H., "Speaker Crossovers," within Chapter 8 of 1993 *Analog Devices System Applications Guide.*
5. Linkwitz, S., "Active Crossover Networks for Noncoincident Drivers," *JAES*, Vol. 24, #1, Jan/Feb 1976.

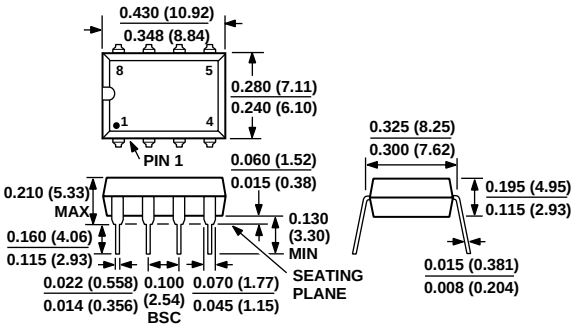
OP179/OP279 Spice Macro Model

```
* OP179/OP279 SPICE Macro-model          Rev. A, 5/94
*                                ARG / ADI
*
* Copyright 1994 by Analog Devices
*
* Refer to "README.DOC" file for License Statement. Use of
* this model indicates your acceptance of the terms and pro-
* visions in the License Statement.
*
* Node assignments
*                        noninverting input
*                        |    inverting input
*                        |    |    positive supply
*                        |    |    |    negative supply
*                        |    |    |    |    output
*                        |    |    |    |    |
.SUBCKT OP179/OP279  3    2    99   50   45
*
* INPUT STAGE AND POLE AT 6 MHz
*
I1      1       50      60.2E-6
Q1      5       2       7   QN
Q2      6       4       8   QN
D1      4       2       DX
D2      2       4       DX
R1      1       7       1.628E3
R2      1       8       1.628E3
R3      5       99      2.487E3
R4      6       99      2.487E3
C1      5       6       5.333E-12
EOS     4       3       POLY(1) (16,39) 0.25E-3 50.118
IOS     2       3       5E-9
GB1     2       98      (24,98) 100E-9
GB2     4       98      (24,98) 100E-9
CIN     2       3       1E-12
*
* GAIN STAGE AND DOMINANT POLE AT 16 Hz
*
EREF    98      0       (39,0) 1
G1      98      9       (5,6) 402.124E-6
R7      9       98      497.359E6
C2      9       98      20E-12
V1      99      10      0.58
V2      11      50      0.47
D5      9       10      DX
D6      11      9       DX
*
* COMMON-MODE STAGE WITH ZERO AT 10 kHz
*
ECM     15      98      POLY(2) (3,39) (2,39) 0 0.5 0.5
R9      15      16      1E6
R10     16      98      10
C3      15      16      15.915E-12
*
* ZERO AT 1.5 MHz
*
E1      14      98      (9,39) 1E6
R5      14      18      1E6
R6      18      98      1
C4      14      18      106.103E-15
*
* BIAS CURRENT-VS-COMMON-MODE VOLTAGE
*
EP      97      0       (99,0) 1
EN      51      0       (50,0) 1
V3      20      21      1.6
V4      22      23      2.8
R12     97      20      530
R13     23      51      1E3
D13     15      21      DX
D14     22      15      DX
FIB     98      24      POLY(2) V3 V4 0 –1 1
RIB     24      98      10E3
E3      97      25      POLY(1) (99,39) –1.63 1
E4      26      51      POLY(1) (39,50) –2.73 1
D15     24      25      DX
D16     26      24      DX
*
* POLE AT 6 MHz
*
G6      98      40      (18,39)      1E       6
R20     40      98      1E6
C10     40      98      26.526E-15
*
* OUTPUT STAGE
*
RS1     99      39      6.0345E3
RS2     39      50      6.0345E3
RO1     99      45      40
RO2     45      50      40
G7      45      99      (99,40) 25E-3
G8      50      45      (40,50) 25E-3
G9      98      60      (45,40) 25E-3
D9      60      61      DX
D10     62      60      DX
V7      61      98      DC          0
V8      98      62      DC 0
FSY     99      50      POLY(2) V7 V8 1.711E-3   1   1
D11     41      45      DZ
D12     45      42      DZ
V5      40      41      1.54
V6      42      40      1.54
.MODEL          DX      D()
.MODEL          DZ      D(IS=1E-6)
.MODEL          QN NPN(BF=300)
.ENDS
```

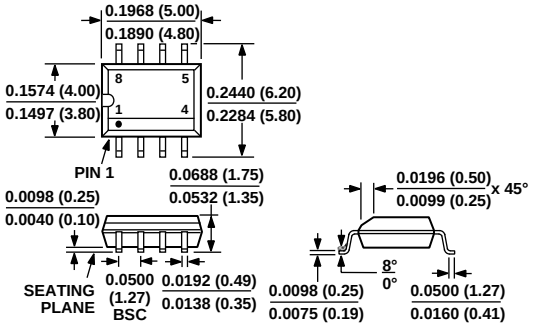
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

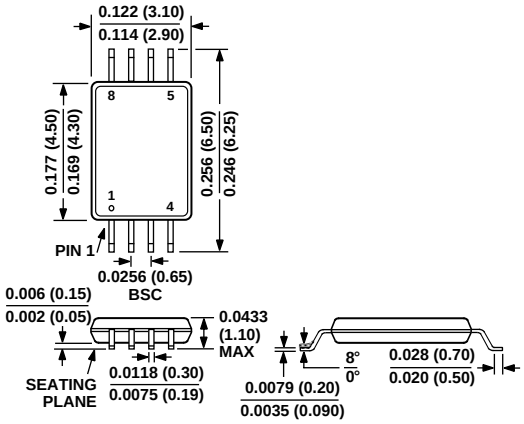
8-Lead Plastic DIP (N-8)



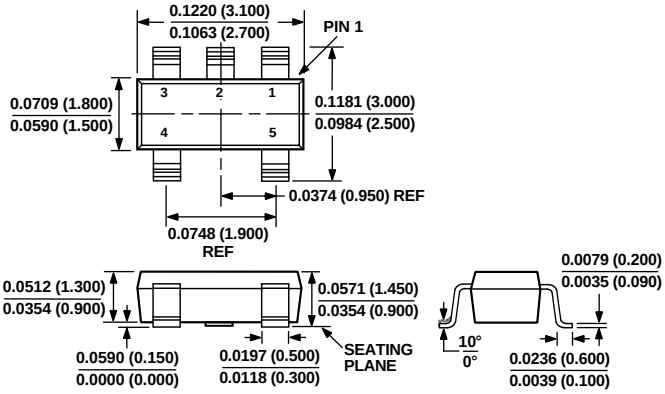
8-Lead Narrow-Body SO (SO-8)



8-Lead TSSOP (RU-8)



5-Lead SOT-23 (RT-5)



NOTE:
PACKAGE OUTLINE INCLUSIVE AS SOLDER PLATING.

C3497a–0–10/99

PRINTED IN U.S.A.