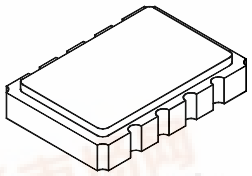
Preliminary

OP4008B

669.327 MHz Optical Timing Clock

- *Quartz SAW Stabilized and Filtered "Diff Sine" Technology*
- *Fundamental-Mode Oscillation at 669.327 MHz*
- *Voltage Tunable for Phase Lock Loop Operations*
- *Optical Timing Reference for Forward Error Correction Applications*

The output of this device is generated and filtered by narrow-band quartz SAW elements at 669.327 MHz. The configuration of this clock provides a pure signal for optical timing applications in noisy signal environments. The Q/$\overline{Q}$ differential output swing of ±1 volt about 0 Vdc has symmetry better than ±1% into loads from 40 to 70 ohms, determined by customer application. The long term frequency accuracy is set by an external reference source allowing this device to complete a Phase Lock Loop design without the usual noise and jitter problems associated with PLL's.



SMC-08

Absolute Maximum Ratings

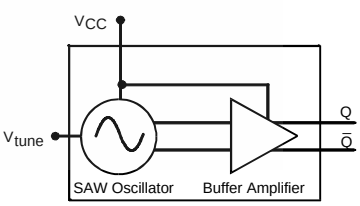
Rating	Value	Units
DC Suppy Voltage	0 to 5.5	Vdc
Tuning Voltage	0 to 6	Vdc
Case Temperature	-55 to 100	°C

Electrical Characteristics

Characteristic		Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency	Absolute Frequency	f_O	1, 9		669.327		MHz
	Tuning Range		2	±100			ppm
	Tuning Voltage		1	0		+3	V
	Tuning Linearity		1, 8		±3		%
	Tuning Sensitivity	df/dv	2,10	140		300	ppm/V
	Modulation Bandwidth			125	265		kHz
Q and $\overline{Q}$ Output	Voltage into 50 Ω (VSWR≤1.2)	V_O	1,3	0.60		1.1	V_{P-P}
	Operating Load VSWR		1,3			2:1	
	Symmetry		3, 4, 5	49		51	%
	Harmonic Spurious		3, 4, 6			-30	dBc
	Nonharmonic Spurious		3, 4, 6, 7			-60	dBc
Phase Noise	@100 Hz offset				-75		dBc/Hz
	@ 1 kHz offset				-105		dBc/Hz
	@ 10 k offset				-125		dBc/Hz
	Noise Floor				-155		dBc/Hz
Q and $\overline{Q}$ Jitter	RMS Jitter		3, 4, 6, 7		2		ps_{P-P}
	No Noise on V_{CC}		3, 4, 6, 7		12		ps_{P-P}
with 200 mV_{P-P} noise added from 1 MHz to ½ f_O			3		12		ps_{P-P}
Output DC Resistance (between Q & $\overline{Q}$)			1, 3	50			KΩ
DC Power Supply	Operating Voltage	V_{CC}	1, 3	3.13	3.3, 5.0	5.25	Vdc
	Operating Current	I_{CC}	1, 3			70	mA
Operating Case Temperature		T_C	1, 3	-40		+85	°C
Lid Symbolization (YY=Year, WW=Week)		RFM OP4008B YYWW					

CAUTION: Electrostatic Sensitive Device. Observe precautions for handling. COCOM CAUTION: Approval by the U.S. Department of Commerce is required prior to export of this device.

BLOCK DIAGRAM

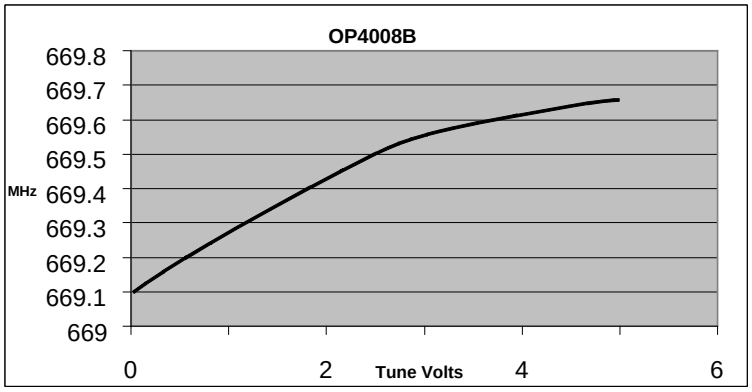


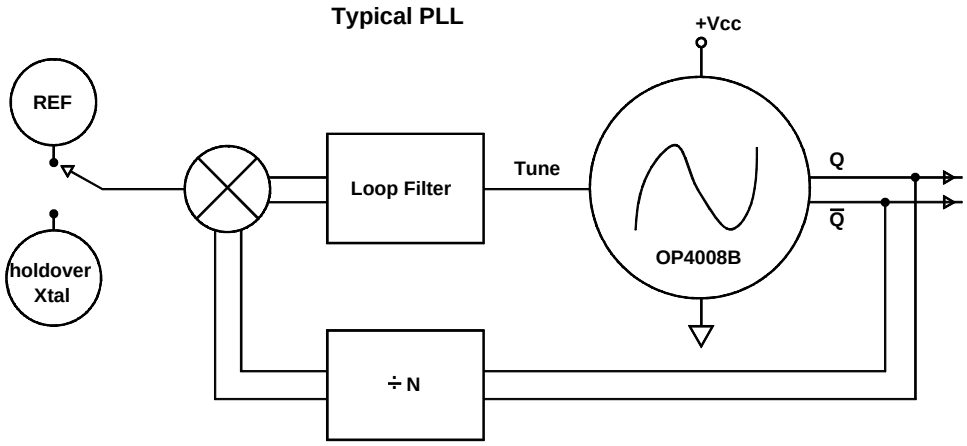
Notes:

1. Unless otherwise noted, all specifications include any combination of load VSWR, Vcc, and temperature, with Q and $\overline{Q}$ terminated into 50 ohm loads to ground (see typical test circuit).
2. Useful tuning range is in excess of what is required over temp, aging, pushing, pulling & accuracy.
3. The design, manufacturing process, and specifications of this device are subject to change without notice.
4. Only under the nominal conditions of 50 Ω load impedance with VSWR ≤ 1.2 and nominal power supply voltage.
5. Symmetry is defined as the pulse width (in percent of total period) measured at the 50% points of Q or $\overline{Q}$ (see timing definitions).
6. Jitter and other spurious outputs induced by externally generated electrical noise on V_{CC} or mechanical vibration are not included in this specification, except where noted. External voltage regulation and careful PCB layout are recommended for optimum performance.
7. Applies to period jitter of Q and $\overline{Q}$. Measurements are made with the Tektronix CSA803 signal analyzer with at least 1000 samples.
8. Linearity is a function of the percentage variation from a permitted linear deviation versus the amount of frequency tune range *(see linearity definition)*.
9. One or more of the following United States patents apply: 4,616,197; 4,670,681; 4,760,352.
10. Over the range of 669.327 MHz ±25 ppm and the conditions of Note 1.

OP4008B Tuning

The OP4008B will tune from 0 to 5 volts as shown in the adjacent plot. For normal use in a PLL, the tuning voltage will not change much from the nominal operating point. The operating point is determined by: (1) the temperature of the OP4008B case, (2) the reference frequency from the PLL, and (3) the internal characteristics of the key components used in the OP4008B part. Although the nominal operating point may be different from part to part by up to 1 volt, the locked operation of the part in a PLL will not tune more than 0.5 volts, allowing good linearity over the operating range.





RFM's OPB-series Voltage Controlled SAW Clocks are designed for use in Phase Lock Loops (PLL's) for optical timing applications. PLL operating parameters such as loop bandwidth are typically determined by optical timing requirements, and noise reduction demands in a given system. The phase noise in the OP4008B Clock is good enough to allow the loop bandwidth to be set at 100 Hz or less. Optical timing systems containing multiple or cascaded timing loops have additional considerations that apply. For example, jitter peaking is often determined by VCO linearity.

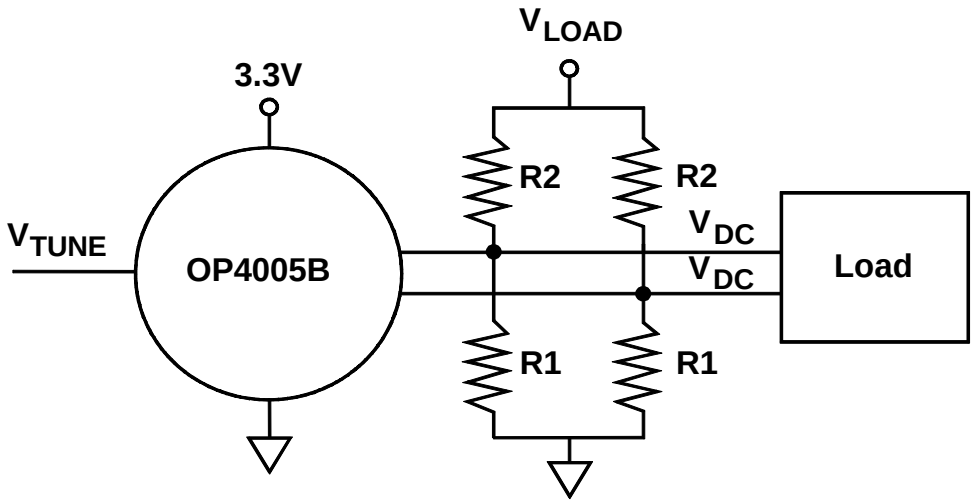
Load Recommendations for the OP4008B

The Q and $\overline{Q}$ outputs of RFM's OPB-series of SAW clocks are AC-coupled internally. This allows customers to set the DC level of the outputs with a simple resistor pair on each output to drive most any application.

$$1)\quad Vdc = \frac{V_{load} \times R1}{R1 + R2}$$

$$2)\quad \frac{1}{R1} + \frac{1}{R2} = \frac{1}{50}$$

Vdc is the DC level desired on the outputs.
$\mathbf{V_{load}}$ is the DC supply on the load resistors (typically 3.3 V).



Equations 1 & 2 describe the voltage divider created by **R1** & **R2** and the equilivent load impedence set by the parrellel combination of **R1** & **R2**.

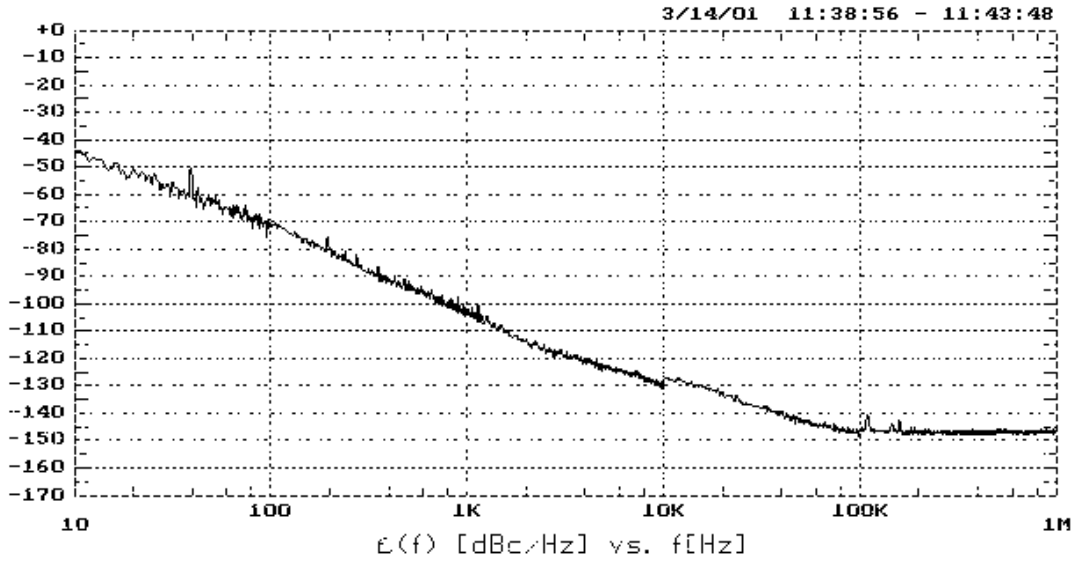
A given load type will have specifications that set **Vdc**. Choose an available V_{load} that is 2x to 3x larger than the desired **Vdc**. This will allow **R1** to be expressed in terms of **R2** as in equation 1. By substituting this result in equation 2, a value for **R2** will result. Solving equation 1 for **R1** with the known **R2** is the last step.

Table 1 has some typical values for Vdc & V_{load} for various ECL loads along with R1 & R2 values that are standard.

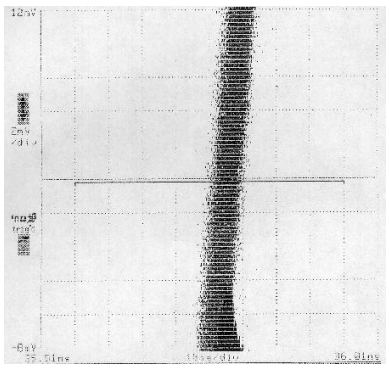
Note that the OPB parts will drive negative ECL loads by applying negative voltage to the V_{load} points in the circuit.

Load Type	Vdc	R1	R2	V_{load}
10k 3.3 V PECL	1.95	120	91	3.3 V
100k 3.3 V PECL	1.88	120	91	3.3 V
10k 5 V PECL	3.65	180	68	5.0 V
100k 5 V PECL	3.58	180	68	5.0 V
10k -5 V NECL	-1.30	240	62	-5.0 V
100k -5 V NECL	-1.42	240	62	-5.0 V

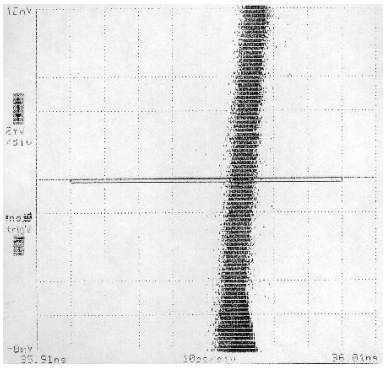
Single Sideband Phase Noise



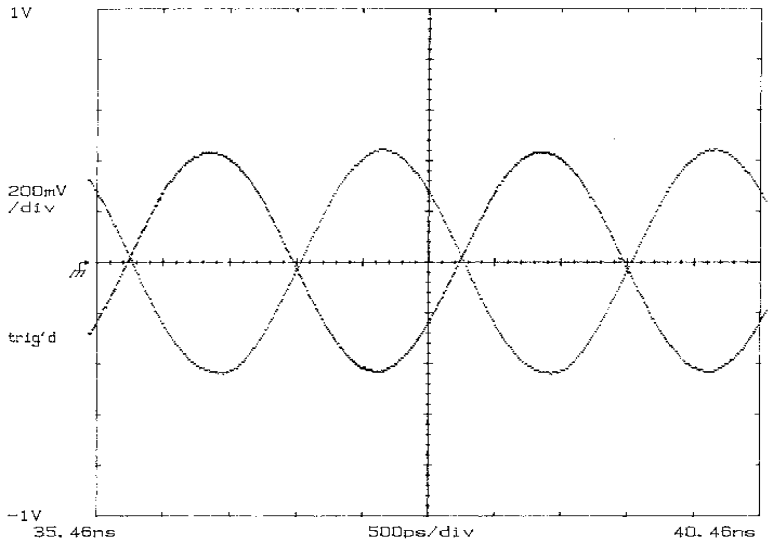
Jitter



Jitter with 200 mV of power supply noise



Symmetry



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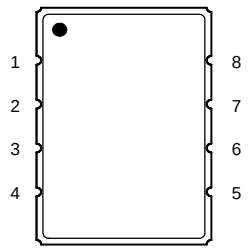
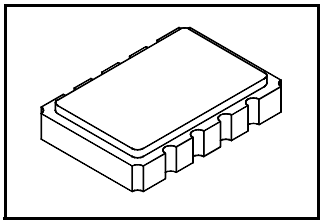
SMC-8 8-Terminal Surface Mount Case



TOP VIEW

ELECTRICAL CONNECTIONS

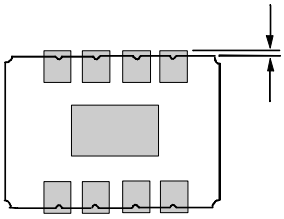
Terminal Number	Connection
1	V_{CC}
2	Ground
3	Ground
4	Q Output
5	$\overline{Q}$ Output
6	Ground
7	
8	TUNE Input
LID	Ground



Dimension	mm		Inches	
	MIN	MAX	MIN	MAX
A	13.46	13.97	0.530	0.550
B	9.14	9.66	0.360	0.380
C	1.93 Nominal		0.076 Nominal	
D	3.56 Nominal		0.141 Nominal	
E	2.24 Nominal		0.088 Nominal	
F	1.27 Nominal		0.050 Nominal	
G	2.54 Nominal		0.100 Nominal	
H	3.05 Nominal		0.120 Nominal	
J	1.93 Nominal		0.076 Nominal	
K	5.54 Nominal		0.218 Nominal	
L	4.32 Nominal		0.170 Nominal	
M	4.83 Nominal		0.190 Nominal	
N	0.50 Nominal		0.020 Nominal	

Typical Printed Circuit Board Land Pattern

A typical land pattern for a circuit board is shown below. Grounding of the metallic center pad is optional.



Typically 0.01" to 0.05" or 0.25 mm to 1.25 mm (8 Places)

(The optimum value of this dimension is dependent on the PCB assembly process employed.)