Dual, Wideband, Voltage-Feedback OPERATIONAL AMPLIFIER with Disable

FEATURES

- **FLEXIBLE SUPPLY RANGE:**
  +5V to +12V Single Supply
  ±2.5V to ±6V Dual Supply
- **WIDEBAND +5V OPERATION: 220MHz (G = 2)**
- **HIGH OUTPUT CURRENT: 190mA**
- **OUTPUT VOLTAGE SWING: ±4.0V**
- **HIGH SLEW RATE: 1800V/μs**
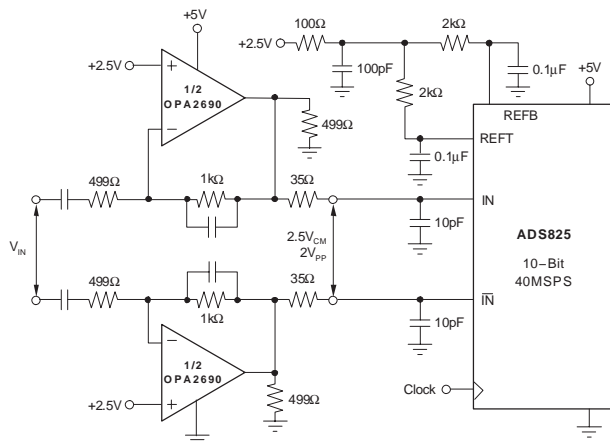- **LOW SUPPLY CURRENT: 5.5mA/ch**
- **LOW DISABLED CURRENT: 100μA/ch**

APPLICATIONS

- **VIDEO LINE DRIVING**
- **xDSL LINE DRIVER/RECEIVER**
- **HIGH-SPEED IMAGING CHANNELS**
- **ADC BUFFERS**
- **PORTABLE INSTRUMENTS**
- **TRANSIMPEDANCE AMPLIFIERS**
- **ACTIVE FILTERS**

DESCRIPTION

The OPA2690 represents a major step forward in unity-gain stable, voltage-feedback op amps. A new internal architecture provides slew rate and full-power bandwidth previously found only in wideband, current-feedback op amps. A new output stage architecture delivers high currents with a minimal headroom requirement. These give exceptional single-supply operation. Using a single +5V supply, the OPA2690 can deliver a 1V to 4V output swing with over 120mA drive current and 150MHz bandwidth. This combination of features makes the OPA2690 an ideal RGB line driver or single-supply Analog-to-Digital Converter (ADC) input driver.

The low 5.5mA/ch supply current of the OPA2690 is precisely trimmed at +25°C. This trim, along with low temperature drift, ensures lower maximum supply current than competing products. System power may be reduced further using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, will operate the OPA2690I-14D normally. If pulled LOW, the OPA2690I-14D supply current drops to less than 200μA/ch while the output goes to a high-impedance state.
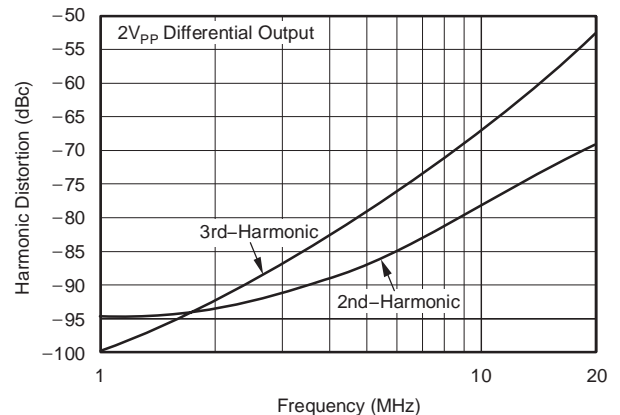
OPA2690 RELATED PRODUCTS

	SINGLES	DUALS	TRIPLES
Voltage-Feedback	OPA2690	OPA2680	OPA3690
Current-Feedback	OPA691	OPA2691	OPA3691
Fixed Gain	OPA692	—	OPA3692

Single-Supply Differential ADC Driver

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SBOS238E – JUNE 2002 – REVISED MAY 2006

ABSOLUTE MAXIMUM RATINGS[1]

```
Power Supply  . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±6.5V_DC
Internal Power Dissipation . . . . . . .  See Thermal Analysis Section
Differential Input Voltage  . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±1.2V
Input Voltage Range . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . ±V_S
Storage Temperature Range: D, 14D  . . . . . . . . . –40°C to +125°C
Lead Temperature (soldering, 10s) . . . . . . . . . . . . . . . . . . . . +300°C
Junction Temperature (T_J) . . . . . . . . . . . . . . . . . . . . . . . . . . +150°C
ESD Resistance:
   Human Body Model (HBM)  . . . . . . . . . . . . . . . . . . . . . .  2000V
   Charge Device Model (CDM)  . . . . . . . . . . . . . . . . . . . . .  1500V
   Machine Model (MM)  . . . . . . . . . . . . . . . . . . . . . . . . . . . . 200V
```

[1] Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.
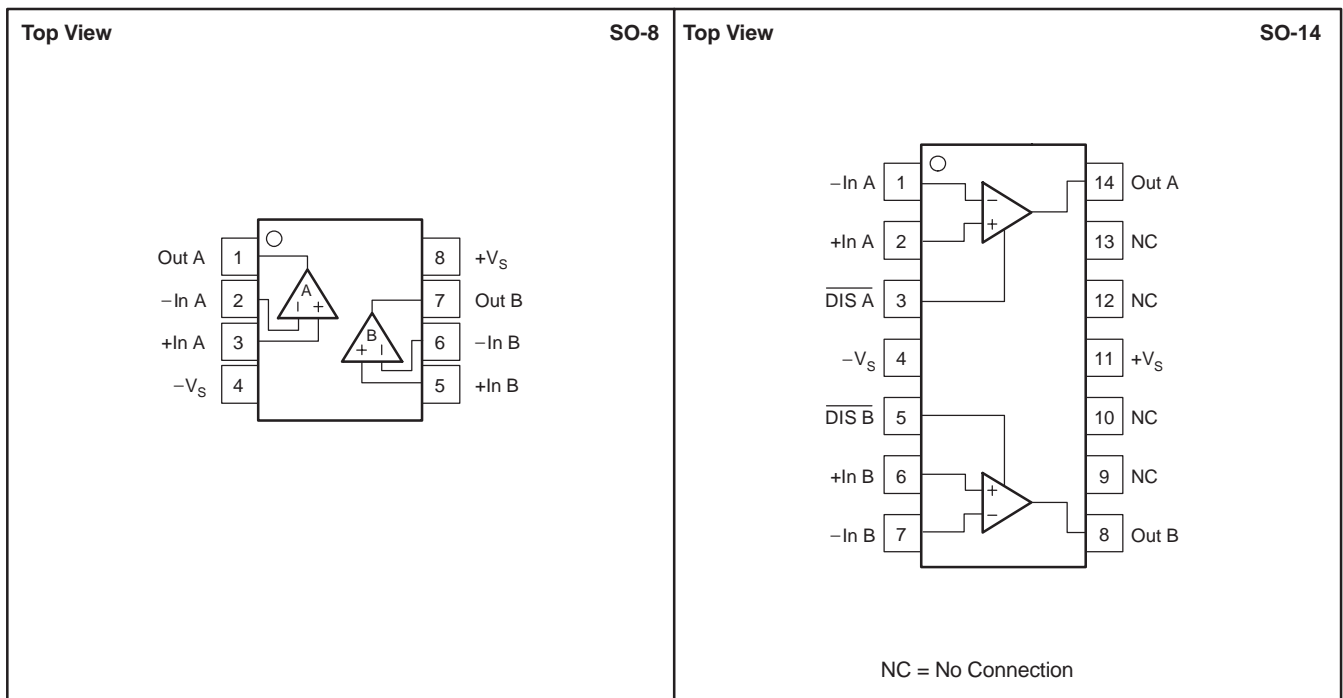
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2690	SO-8	D	–40°C to +85°C	OPA2690	OPA2690ID	Rails, 100
					OPA2690IDR	Tape and Reel, 2500
OPA2690	SO-14	D	–40°C to +85°C	OPA2690	OPA2690I-14D	Rails, 58
					OPA2690I-14DR	Tape and Reel, 2500

[1] For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN ASSIGNMENTS

Top View — SO-8

```
Out A   1        8   +V_S
−In A   2        7   Out B
+In A   3        6   −In B
−V_S    4        5   +In B
```

Top View — SO-14

```
−In A   1       14   Out A
+In A   2       13   NC
DIS A   3       12   NC
−V_S    4       11   +V_S
DIS B   5       10   NC
+In B   6        9   NC
−In B   7        8   Out B
```

NC = No Connection

ELECTRICAL CHARACTERISTICS: $V_S = \pm5V$

Boldface limits are tested at **+25°C.**

At $R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2 (see Figure 1 for AC performance only), unless otherwise noted.

		OPA2690ID, I-14D						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[1]	0°C to 70°C[2]	−40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
AC PERFORMANCE (see Figure 1)								
Small-Signal Bandwidth	G = +1, V_O = 0.5V_{PP}, R_F = 25Ω	500				MHz	typ	C
	G = +2, V_O = 0.5V_{PP}	220	165	160	150	MHz	min	B
	G = +10, V_O = 0.5V_{PP}	30	20	19	18	MHz	min	B
Gain-Bandwidth Product	G ≥ 10	300	200	190	180	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5V_{PP}	30				MHz	typ	C
Peaking at a Gain of +1	V_O < 0.5V_{PP}	4				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O = 5V_{PP}	200				MHz	typ	C
Slew Rate	G = +2, 4V Step	1800	1400	1200	900	V/µs	min	C
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.4				ns	typ	C
	G = +2, V_O = 5V Step	2.8				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 5V Step	12				ns	typ	C
Settling Time to 0.1%	G = +2, V_O = 5V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	−68	−64	−62	−60	dBc	max	
	R_L ≥ 500Ω	−77	−70	−68	−66	dBc	max	B
3rd-Harmonic	R_L = 100Ω	−70	−68	−66	−64	dBc	max	B
	R_L ≥ 500Ω	−81	−78	−76	−75	dBc	max	B
Input Voltage Noise	f > 1MHz	5.5				nV/$\sqrt{Hz}$	typ	C
Input Current Noise	f > 1MHz	3.1				pA/$\sqrt{Hz}$	typ	C
Differential Gain	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.06				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.03				deg	typ	C
Channel-to-Channel Crosstalk	f = 5MHz, Input-Referred	−85				dBc		
DC PERFORMANCE[4]								
Open-Loop Voltage Gain (A_{OL})	V_O = 0V, R_L = 100Ω	69	**58**	56	54	dB	min	A
Input Offset Voltage	V_{CM} = 0V	±1.0	**±4.5**	±5.0	±5.2	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±12	µV/°C	max	B
Input Bias Current	V_{CM} = 0V	+5	**±11**	±12	±13	µA	max	A
Average Bias Current Drift (magnitude)	V_{CM} = 0V			±20	±40	nA/°C	max	B
Input Offset Current	V_{CM} = 0V	±0.1	**±1.0**	±1.4	±1.6	µA	max	A
Average offset Current Drift	V_{CM} = 0V			±1.0	±1.5	nA/°C	max	B
INPUT								
Common-Mode Input Range (CMIR)[5]		±3.5	**±3.4**	±3.3	±3.2	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = ±1V	65	**60**	57	56	dB	min	A
Input Impedance								
Differential Mode	V_{CM} = 0V	190 || 0.6				kΩ ||pF	typ	C
Common-Mode	V_{CM} = 0V	3.2 || 0.9				MΩ ||pF	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.0	**±3.8**	±3.7	±3.6	V	min	A
	100Ω Load	±3.9	**±3.7**	±3.6	±3.3	V	min	A
Current Output, Sourcing	V_O = 0V	+190	**+160**	+140	+100	mA	min	A
Current Output, Sinking	V_O = 0V	−190	**−160**	−140	−100	mA	min	A
Short-Circuit Current	V_O = 0V	±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.04				Ω	typ	C

[1] Junction temperature = ambient for +25°C specifications.

[2] Junction temperature = ambient at low temperature limits; junction temperature = ambient +15°C at high temperature limit for over temperature specifications.

[3] Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

[4] Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

[5] Tested < 3dB below minimum specified CMRR at ± CMIR limits.

OPA2690

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ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

Boldface limits are tested at **+25°C.**

At $R_F = 402\Omega$, $R_L = 100\Omega$, and G = +2 (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	TYP +25°C	OPA2690ID, I-14D MIN/MAX OVER TEMPERATURE +25°C[1]	0°C to 70°C[2]	−40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
DISABLE (SO-14 Only)	Disabled LOW							
Power-Down Supply Current (+V$_S$)	$\overline{V_{DIS}}$ = 0, Both Channels	−200	**−400**	−480	−520	μA	max	A
Disable Time	V_{IN} = 1V$_{DC}$	200				ns	typ	C
Enable Time	V_{IN} = 1V$_{DC}$	25				ns	typ	C
Off Isolation	G = +2, R$_L$ = 150Ω, V$_{IN}$ = 0	70				dB	typ	C
Output Capacitance in Disable	G = +2, R$_L$ = 150Ω, V$_{IN}$ = 0	4				pF	typ	C
Turn-On Glitch		±50				mV	typ	C
Turn-Off Glitch		±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{V_{DIS}}$)	$\overline{V_{DIS}}$ = 0, Each Channel	75	**130**	150	160	μA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			**±6.0**	±6.0	±6.0	V	max	A
Maximum Quiescent Current (2 Channels)	V$_S$ = ±5V	11	**11.6**	12.4	13.2	mA	max	A
Minimum Quiescent Current (2 Channels)	V$_S$ = ±5V	11	**10.6**	9.2	8.6	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	75	**68**	66	64	dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Range: D, 14D		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
14D SO-14		100				°C/W	typ	C

[1] Junction temperature = ambient for +25°C specifications.

[2] Junction temperature = ambient at low temperature limits; junction temperature = ambient +15°C at high temperature limit for over temperature specifications.

[3] Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

[4] Current is considered positive out-of-node. V$_{CM}$ is the input common-mode voltage.

[5] Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

At R_F = 402Ω, R_L = 100Ω to V_S/2, and G = +2 (see Figure 2 for AC performance only), unless otherwise noted.

			OPA2690ID, I-14D					
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[1]	0°C to 70°C[2]	−40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL [3]
AC PERFORMANCE (see Figure 2)								
Small-Signal Bandwidth	G = +1, V_O < 0.5V_{PP}, R_F = ±25Ω	400				MHz	typ	C
	G = +2, V_O < 0.5V_{PP}	190	150	145	140	MHz	min	B
	G = +10, V_O < 0.5V_{PP}	25	18	17	16	MHz	min	B
Gain-Bandwidth Product	G ≥ 10	250	180	170	160	MHz	min	B
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5V_{PP}	20				MHz	typ	C
Peaking at a Gain of +1	V_O < 0.5V_{PP}	5				dB	typ	C
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	220				MHz	typ	C
Slew Rate	G = +2, 2V Step	1000	700	670	550	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	1.6				ns	typ	C
	G = +2, V_O = 2V Step	2.0				ns	typ	C
Settling Time to 0.02%	G = +2, V_O = 2V Step	12				ns	typ	C
Settling Time to 0.1%	G = +2, V_O = 2V Step	8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω to V_S/2	−65	−60	−59	−56	dBc	max	B
	R_L ≥ 500Ω to V_S/2	−75	−70	−68	−66	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	−68	−64	−62	−60	dBc	max	B
	R_L ≥ 500Ω to V_S/2	−77	−73	−71	−70	dBc	max	B
Input Voltage Noise	f > 1MHz	5.6				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	3.2				pA/√Hz	typ	C
Differential Gain	G = +2, NTSC, V_O = 1.4V_P, R_L = 150 to V_S/2	0.06				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4V_P, R_L = 150 to V_S/2	0.02				deg	typ	C
DC PERFORMANCE[4]								
Open-Loop Voltage Gain	V_O = 2.5V, R_L = 100Ω to V_S/2	63	**56**	54	52	dB	min	A
Input Offset Voltage	V_{CM} = 2.5V	±1.0	**±4.5**	±4.8	±5.2	mV	max	A
Average Offset Voltage Drift	V_{CM} = 2.5V			±10	±10	µV/°C	max	B
Input Bias Current	V_{CM} = 2.5V	+5	**±11**	±12	±13	µA	max	A
Average Bias Current Drift (magnitude)	V_{CM} = 2.5V			±20	±40	nA/°C	max	B
Input Offset Current	V_{CM} = 2.5V	±0.3	**±1.0**	±1.4	±1.6	µA	max	A
Average Offset Current Drift	V_{CM} = 2.5V			±7	±9	nA/°C	max	B
INPUT								
Least Positive Input Voltage[5]		1.5	**1.6**	1.7	1.8	V	max	A
Most Positive Input Voltage[5]		3.5	**3.4**	3.3	3.2	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 2.5V ± 0.5V	63	**58**	56	54	dB	min	A
Input Impedance								
Differential Mode	V_{CM} = 2.5V	92 ‖ 1.4				kΩ ‖pF	typ	C
Common-Mode	V_{CM} = 2.5V	2.2 ‖ 1.5				MΩ ‖pF	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4	**3.8**	3.6	3.5	V	min	A
	R_L = 100Ω to 2.5V	3.9	**3.7**	3.5	3.4	V	min	A
Least Positive Output Voltage	No Load	1	**1.2**	1.4	1.5	V	max	A
	R_L = 100Ω to 2.5V	1.1	**1.3**	1.5	1.7	V	max	A
Current Output, Sourcing		+160	**+120**	+100	+80	mA	min	A
Current Output, Sinking		−160	**−120**	−100	−80	mA	min	A
Short-Circuit Current		±250				mA	typ	C
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.04				Ω	typ	C

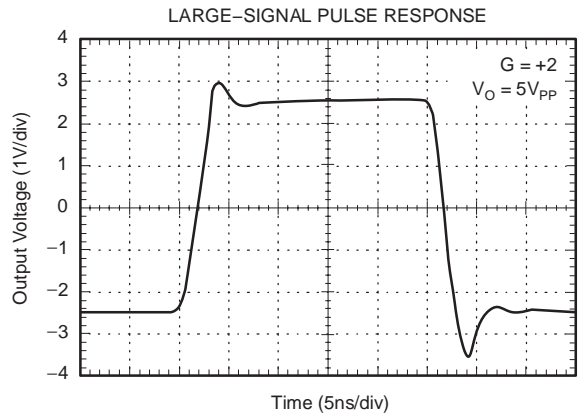[1] Junction temperature = ambient for +25°C specifications.
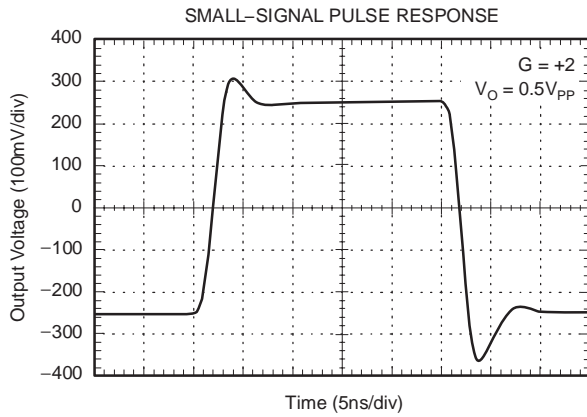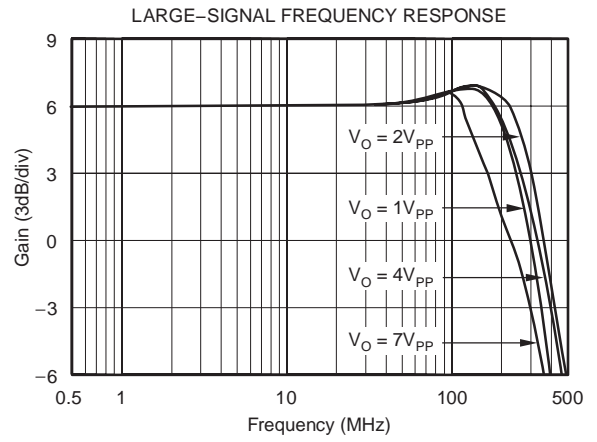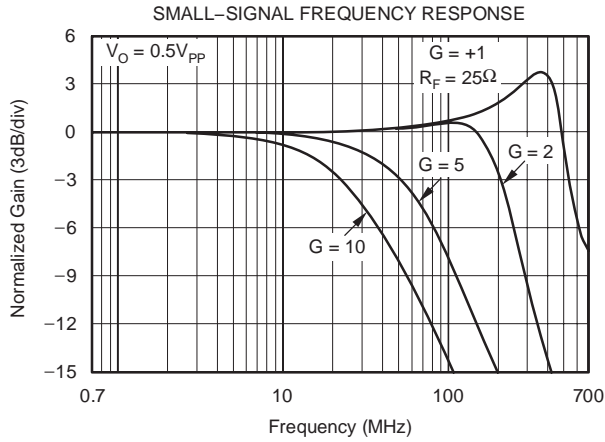[2] Junction temperature = ambient at low temperature limits; junction temperature = ambient +15°C at high temperature limit for over temperature specifications.
[3] Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
[4] Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.
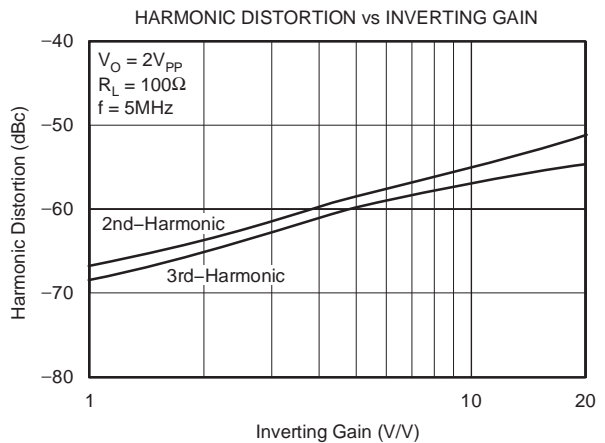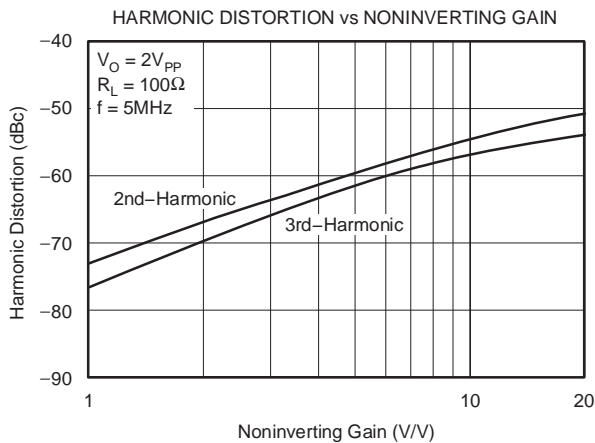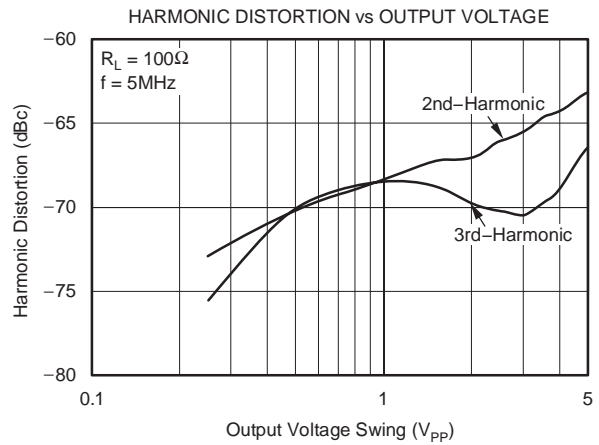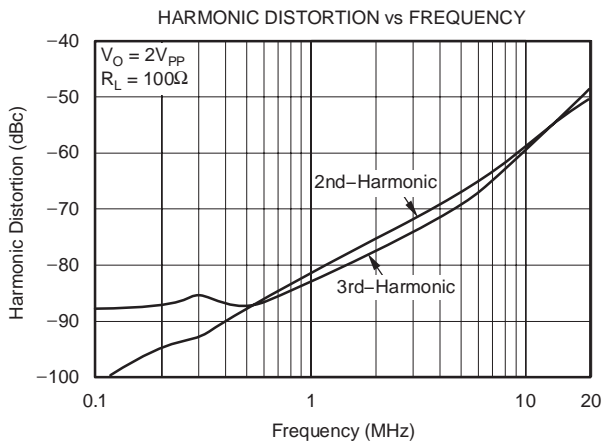[5] Tested < 3dB below minimum specified CMRR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C.**

At R_F = 402Ω, R_L = 100Ω to V_S/2, and G = +2 (see Figure 2 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	TYP +25°C	+25°C[1]	0°C to 70°C[2]	−40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL [3]
			MIN/MAX OVER TEMPERATURE					
DISABLE (SO-14 Only)	Disabled LOW							
Power-Down Supply Current (+V_S)	$\overline{V_{DIS}}$ = 0, Both Channels	−200	**−400**	−480	−520	µA	max	A
Off Isolation	G = +2, 5MHz	65				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±50				mV	typ	C
Turn-Off Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{V_{DIS}}$)	$\overline{V_{DIS}}$ = 0, Each Channel	75	130	150	160	µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Maximum Single-Supply Operating Voltage			12	12	12	V	max	B
Maximum Quiescent Current (2 Channels)	V_S = +5V	9.8	**10.88**	11.44	12.1	mA	max	A
Minimum Quiescent Current (2 Channels)	V_S = +5V	9.8	**8.96**	8.0	7.72	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	72				dB	typ	C
TEMPERATURE RANGE								
Specification: D, 14D		−40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
14D SO-14		150				°C/W	typ	C

[1] Junction temperature = ambient for +25°C specifications.

[2] Junction temperature = ambient at low temperature limits; junction temperature = ambient +15°C at high temperature limit for over temperature specifications.

[3] Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.

[4] Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

[5] Tested < 3dB below minimum specified CMRR at ± CMIR limits.

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TYPICAL CHARACTERISTICS: V$_S$ = ±5V

At T$_A$ = +25°C, G = +2, R$_F$ = 402Ω, and R$_L$ = 100Ω (see Figure 1 for AC performance only), unless otherwise noted.

SMALL–SIGNAL FREQUENCY RESPONSE

LARGE–SIGNAL FREQUENCY RESPONSE

SMALL–SIGNAL PULSE RESPONSE

LARGE–SIGNAL PULSE RESPONSE
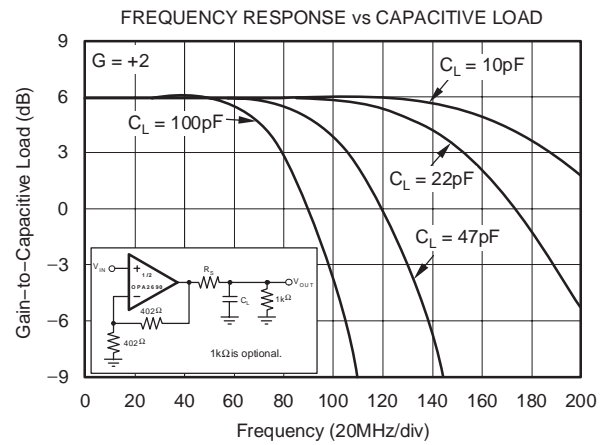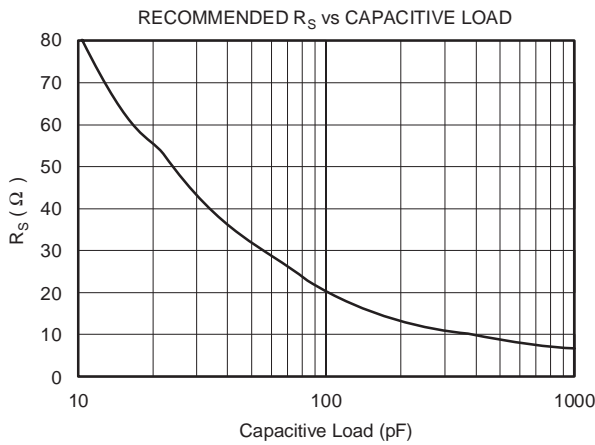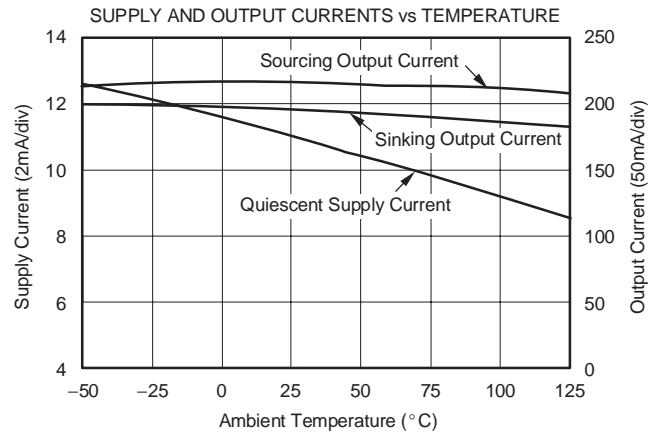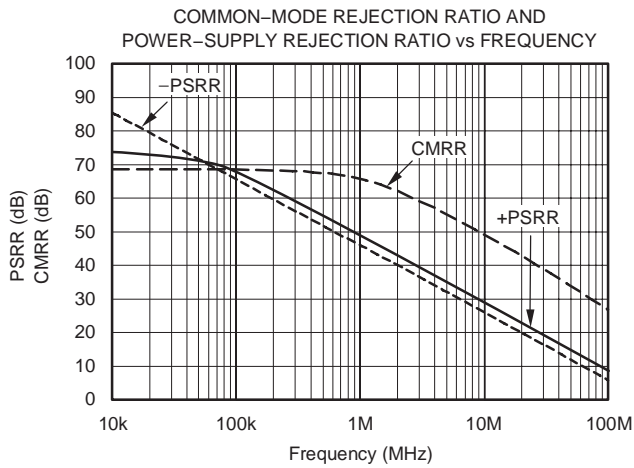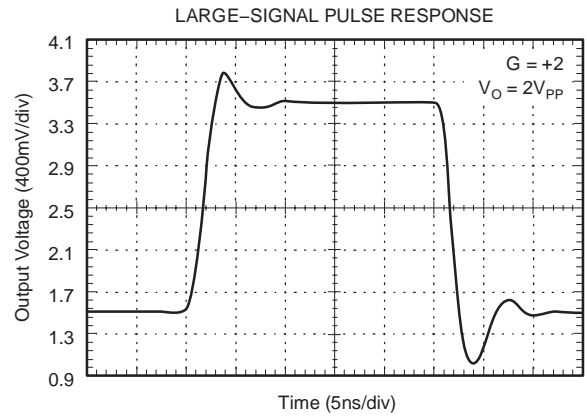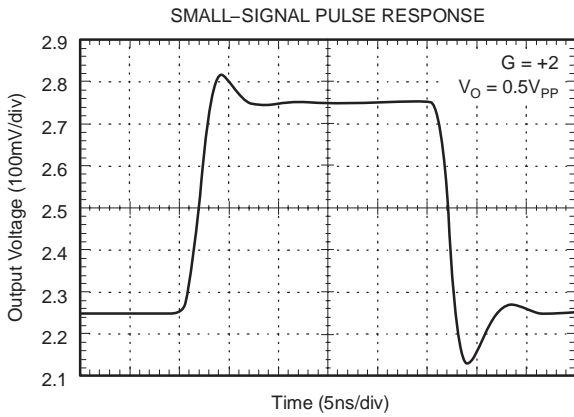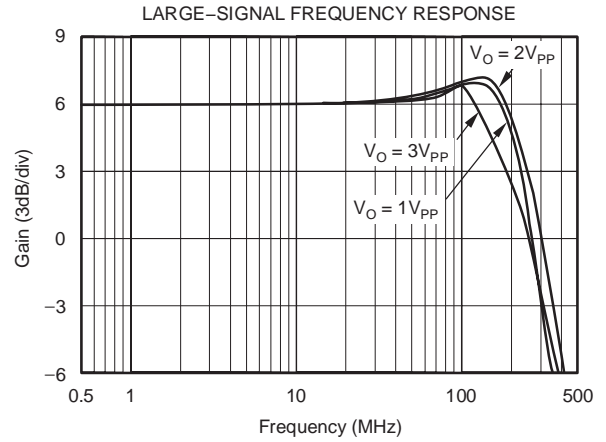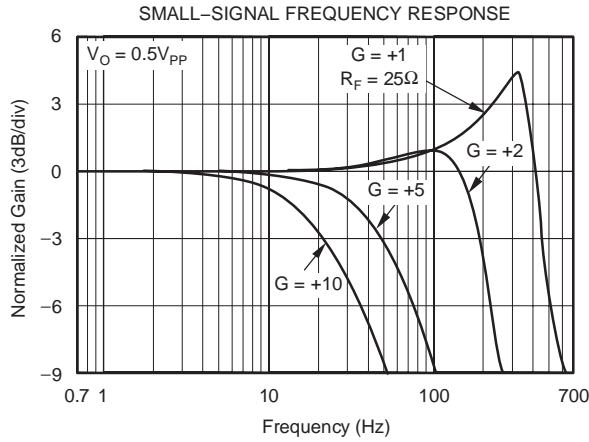

COMPOSITE VIDEO dG/dP

CHANNEL–TO–CHANNEL CROSSTALK

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 1 for AC performance only), unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

$V_O = 2V_{PP}$
f = 5MHz

2nd–Harmonic

3rd–Harmonic

5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

$V_O = 2V_{PP}$
$R_L = 100Ω$
f = 5MHz

2nd–Harmonic

3rd–Harmonic

HARMONIC DISTORTION vs FREQUENCY

$V_O = 2V_{PP}$
$R_L = 100Ω$

2nd–Harmonic

3rd–Harmonic

HARMONIC DISTORTION vs OUTPUT VOLTAGE

$R_L = 100Ω$
f = 5MHz

2nd–Harmonic

3rd–Harmonic

HARMONIC DISTORTION vs NONINVERTING GAIN

$V_O = 2V_{PP}$
$R_L = 100Ω$
f = 5MHz

2nd–Harmonic

3rd–Harmonic

HARMONIC DISTORTION vs INVERTING GAIN

$V_O = 2V_{PP}$
$R_L = 100Ω$
f = 5MHz

2nd–Harmonic

3rd–Harmonic

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

At $T_A = +25°C$, G = +2, $R_F = 402\Omega$, and $R_L = 100\Omega$ (see Figure 1 for AC performance only), unless otherwise noted.
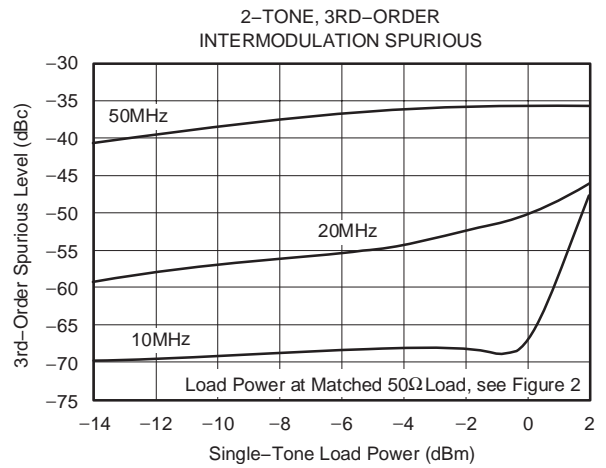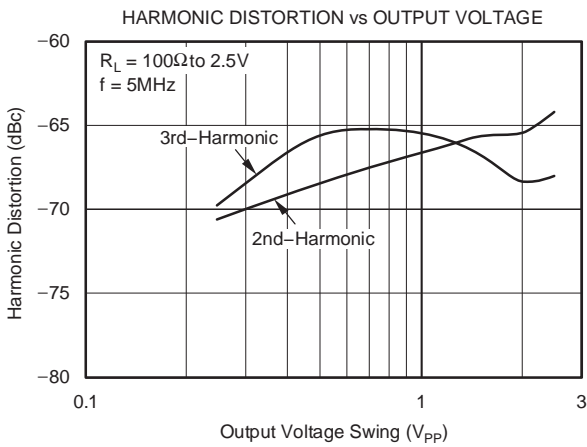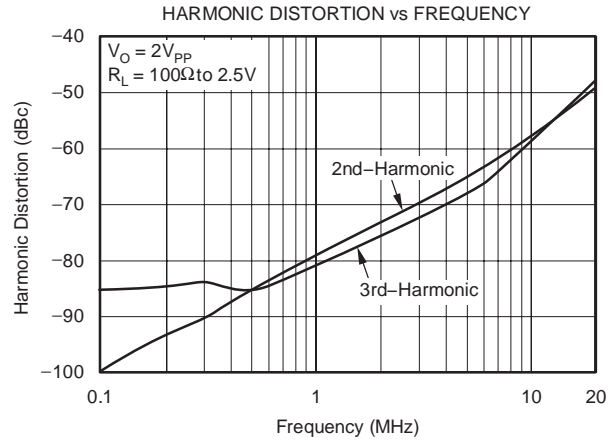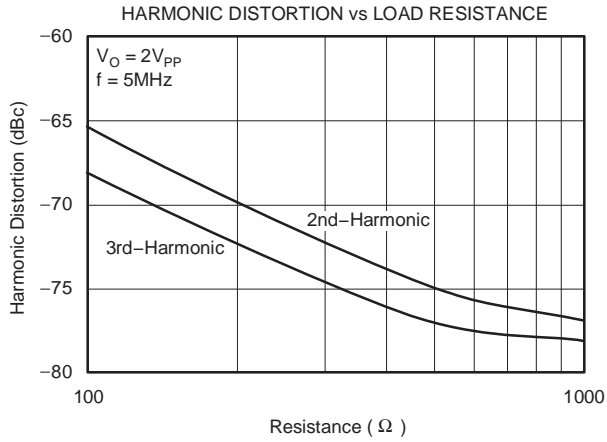
INPUT VOLTAGE AND CURRENT NOISE DENSITY

2−TONE, 3RD−ORDER INTERMODULATION SPURIOUS

RECOMMENDED R_S vs CAPACITIVE LOAD

FREQUENCY RESPONSE vs CAPACITIVE LOAD

LARGE−SIGNAL DISABLE/ENABLE RESPONSE

DISABLE FEEDTHROUGH vs FREQUENCY

TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (continued)

At $T_A = +25°C$, $G = +2$, $R_F = 402\Omega$, and $R_L = 100\Omega$ (see Figure 1 for AC performance only), unless otherwise noted.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

TYPICAL DC DRIFT OVER TEMPERATURE

COMMON−MODE REJECTION RATIO AND
POWER−SUPPLY REJECTION RATIO vs FREQUENCY

SUPPLY AND OUTPUT CURRENTS vs TEMPERATURE

CLOSED−LOOP OUTPUT IMPEDANCE vs FREQUENCY

OPEN−LOOP GAIN AND PHASE

TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 2 for AC performance only), unless otherwise noted.

SMALL–SIGNAL FREQUENCY RESPONSE

LARGE–SIGNAL FREQUENCY RESPONSE

SMALL-SIGNAL PULSE RESPONSE

LARGE–SIGNAL PULSE RESPONSE

RECOMMENDED R_S vs CAPACITIVE LOAD

FREQUENCY RESPONSE vs CAPACITIVE LOAD

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω (see Figure 2 for AC performance only), unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

HARMONIC DISTORTION vs FREQUENCY

HARMONIC DISTORTION vs OUTPUT VOLTAGE

2–TONE, 3RD–ORDER
INTERMODULATION SPURIOUS

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www.ti.com

APPLICATIONS INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA2690 provides an exceptional combination of high output power capability in a dual, wideband, unity-gain stable, voltage-feedback op amp using a new high slew rate input stage. Typical differential input stages used for voltage-feedback op amps are designed to steer a fixed-bias current to the compensation capacitor, setting a limit to the achievable slew rate. The OPA2690 uses a new input stage which places the transconductance element between two input buffers, using their output currents as the forward signal. As the error voltage increases across the two inputs, an increasing current is delivered to the compensation capacitor. This provides very high slew rate (1800V/μs) while consuming relatively low quiescent current (5.5mA/ch). This exceptional full-power performance comes at the price of a slightly higher input noise voltage than alternative architectures. The 5.5nV/$\sqrt{\text{Hz}}$ input voltage noise for the OPA2690 is exceptionally low for this type of input stage.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. This is for one channel; the other channel is connected similarly. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the electrical characteristics are taken directly at the input and output pins, while output powers (dBm) are at the matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω ∥ 804Ω. The disable control line (SO-14 package only) is typically left open for normal amplifier operation. Two optional components are included in Figure 1. An additional resistor (175Ω) is included in series with the noninverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this gives an input bias current cancelling resistance that matches the 200Ω source resistance seen at the inverting input (see the *DC Accuracy and Offset Control* section). In addition to the usual power-supply decoupling capacitors to ground, a 0.1μF capacitor is included between the two power-supply pins. In practical PC board layouts, this optional-added capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

Figure 2 shows the AC-coupled, gain of +2, single-supply circuit configuration used as the basis of the +5V Electrical and Typical Characteristics. Though not a rail-to-rail design, the OPA2690 requires minimal input and output voltage headroom compared to other very wideband voltage-feedback op amps. It will deliver a 3V$_{PP}$ output swing on a single +5V supply with > 150MHz bandwidth. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 2 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 698Ω resistors). Separate bias networks would be required at each input. The input signal is then AC-coupled into the midpoint voltage bias. The input voltage can swing to within 1.5V of either supply pin, giving a 2V$_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (59Ω) used for testing is adjusted to give a 50Ω input load when the parallel combination of the biasing divider network is included.
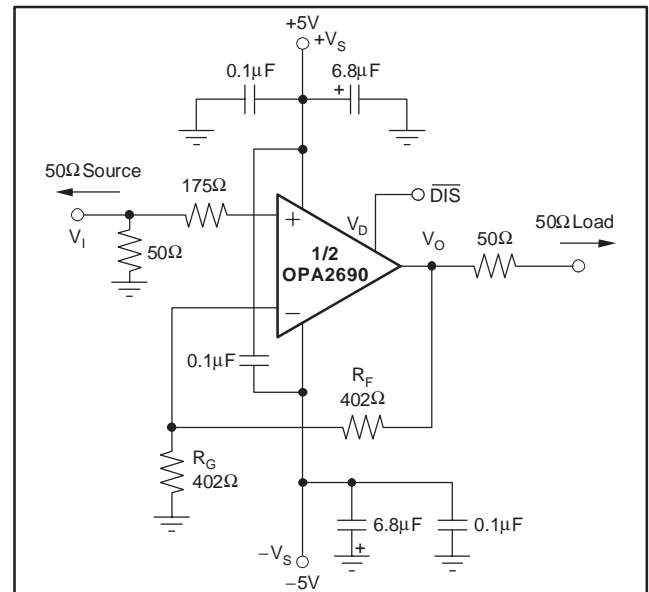

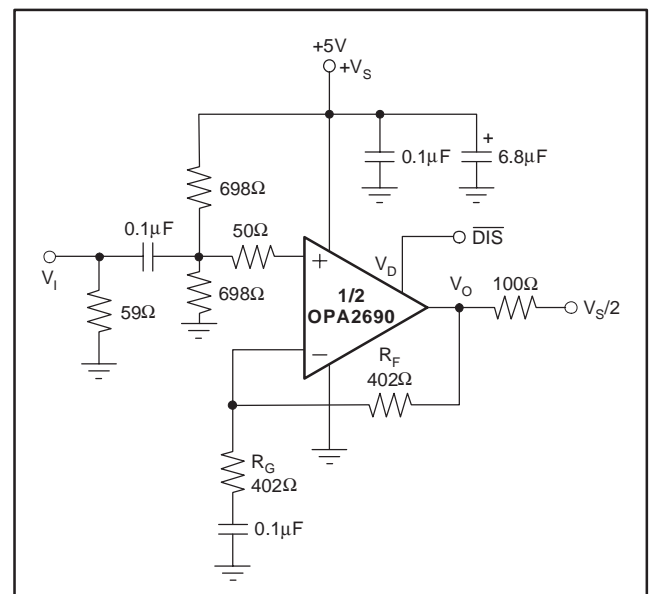**Figure 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit**

Figure 2. DC-Coupled, G = +2, Single-Supply, Specification and Test Circuit

Again, an additional resistor (50Ω in this case) is included directly in series with the noninverting input. This minimum recommended value provides part of the DC source resistance matching for the noninverting input bias current. It is also used to form a simple parasitic pole to roll off the frequency response at very high frequencies (> 500MHz) using the input parasitic capacitance. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1, which puts the input DC bias voltage (2.5V) on the output as well. The output voltage can swing to within 1V of either supply pin while delivering > 100mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage circuit used in the OPA2690 can deliver large bipolar output currents into this midpoint load with minimal crossover distortion, as shown in the +5V supply harmonic distortion plots.

SINGLE-SUPPLY ADC INTERFACE

Most modern, high-performance ADCs (such as the TI ADS8xx and ADS9xx series) operate on a single +5V (or lower) power supply. It has been a considerable challenge for single-supply op amps to deliver a low distortion input signal at the ADC input for signal frequencies exceeding 5MHz. The high slew rate, exceptional output swing, and high linearity of the OPA2690 make it an ideal single-supply ADC driver. The circuit on the front page shows one possible interface pariculary suited to differential I/O, AC-coupled requirements. Figure 4 shows the test circuit of Figure 2 modified for a capacitive (ADC) load and with an optional output pull-down resistor (R_B). This circuit would be suitable to dual-channel ADC driving with a single-ended I/O.

The OPA2690 in the circuit of Figure 4 provides > 200MHz bandwidth for a $2V_{PP}$ output swing. Minimal 3rd-harmonic distortion or 2-tone, 3rd-order intermodulation distortion will be observed due to the very low crossover distortion in the OPA2690 output stage. The limit of output Spurious-Free Dynamic Range (SFDR) will be set by the 2nd-harmonic distortion. Without R_B, the circuit of Figure 4 measured at 10MHz shows an SFDR of 57dBc. This can be improved by pulling additional DC bias current (I_B) out of the output stage through the optional R_B resistor to ground (the output midpoint is at 2.5V for Figure 4). Adjusting I_B gives the improvement in SFDR shown in Figure 3. SFDR improvement is achieved for I_B values up to 5mA, with worse performance for higher values. Using the dual OPA2690 in an I/Q receiver channel will give matched AC performance through high frequencies.
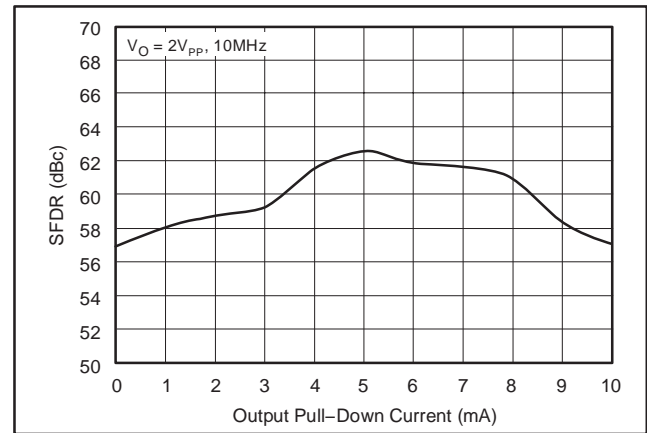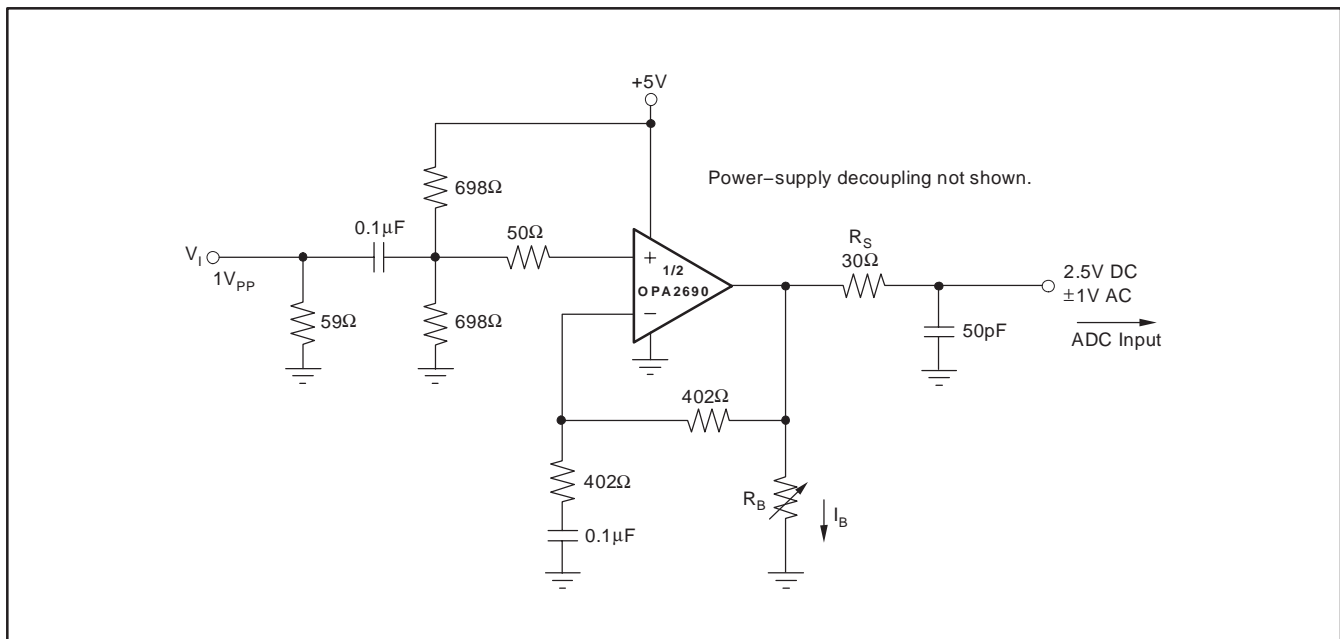

Figure 3. SFDR versus I_B

Figure 4. SFDR versus I_B

HIGH-PERFORMANCE DAC TRANSIMPEDANCE AMPLIFIER

High-frequency DDS Digital-to-Analog Converters (DACs) require a low distortion output amplifier to retain their SFDR performance into real-world loads. Figure 5 shows a single-ended output drive implementation. The diagram shows the signal output current(s) connected into the virtual ground summing junction(s) of the OPA2690, which is set up as a transimpedance stage or I-V converter. If the DAC requires that its outputs terminate to a compliance voltage other than ground for operation, the appropriate voltage level may be applied to the noninverting input of the OPA2690. The DC gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance (C_D in Figure 5) will produce a zero in the noise gain for the OPA2690 that may cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in each feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \qquad (1)$$

which will give a cutoff frequency f_{-3dB} of approximately:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \qquad (2)$$

Figure 5. DAC Transimpedance Amplifier

WIDEBAND VIDEO MULTIPLEXING

One common application for video speed amplifiers that include a disable pin is to wire multiple amplifier outputs together, then select which one of several possible video inputs to source onto a single line. This simple wired-OR video multiplexer can be easily implemented using the OP2690I-14D (SO-14 package only), as shown in Figure 6.
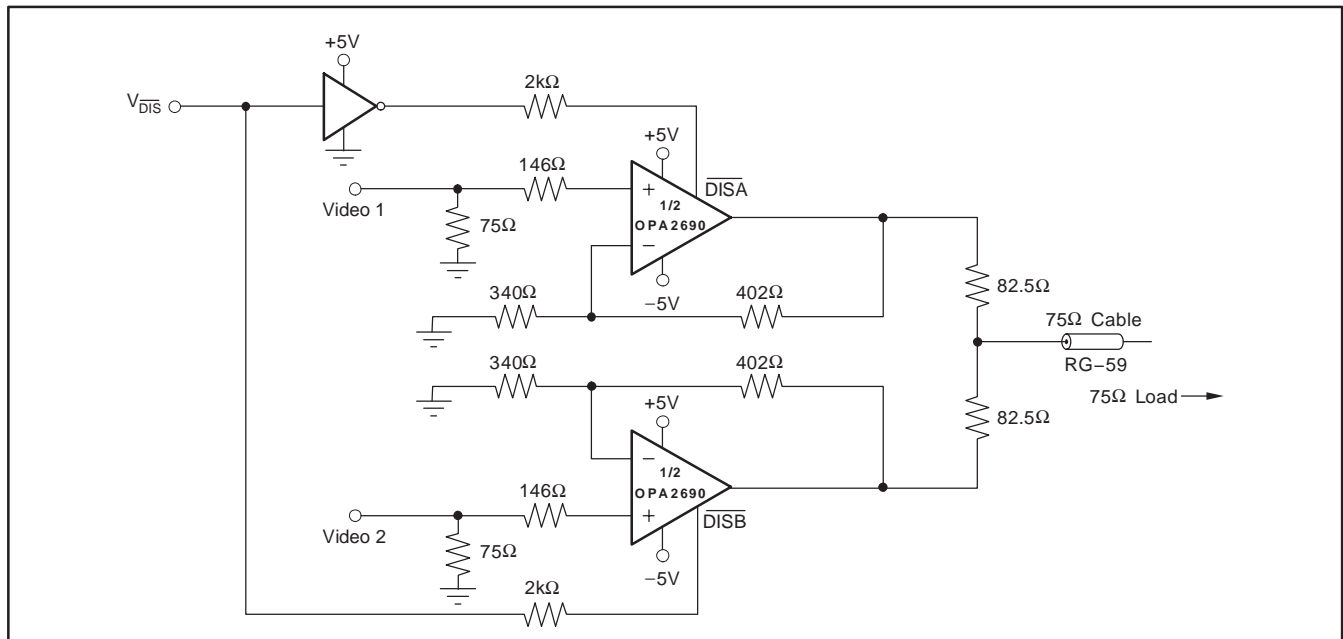
Figure 6. 2-Channel Video Multiplexer (SO-14 package only)

Typically, channel switching is performed either on sync or retrace time in the video signal. The two inputs are approximately equal at this time. The make-before-break disable characteristic of the OPA2690 ensures that there is always one amplifier controlling the line when using a wired-OR circuit like that shown in Figure 6. As both inputs may be on for a short period during the transition between channels, the outputs are combined through the output impedance matching resistors (82.5Ω in this case). When one channel is disabled, its feedback network forms part of the output impedance and slightly attenuates the signal in getting out onto the cable. The gain and output matching resistor have been slightly increased to get a signal gain of +1 at the matched load and provide a 75Ω output impedance to the cable. The video multiplexer connection (see Figure 6) also ensures that the maximum differential voltage across the inputs of the unselected channel does not exceed the rated $\pm1.2V$ maximum for standard video signal levels.

See the *Disable Operation* section for the turn-on and turn-off switching glitches using a 0V input for a single channel is typically less than $\pm50mV$. Where two outputs are switched (see Figure 6), the output line is always under the control of one amplifier or the other due to the make-before-break disable timing. In this case, the switching glitches for two 0V inputs drops to < 20mV.

HIGH-SPEED DELAY CIRCUIT

The OPA2690 makes an ideal amplifier for a variety of active filter designs. Shown in Figure 7 is a circuit that uses the two amplifiers within the dual OPA2690 to design a 2-stage analog delay circuit. For simplicity, the circuit uses a dual-supply ($\pm5V$) operation, but it can also be modified to operate on a signal supply. The input to the first filter stage is driven by the OPA692 wideband buffer amplifier to isolate the signal input from the filter network.

Each of the two filter stages is a 1st-order filter with a voltage gain of +1. The delay time through one filter is given by Equation 3.
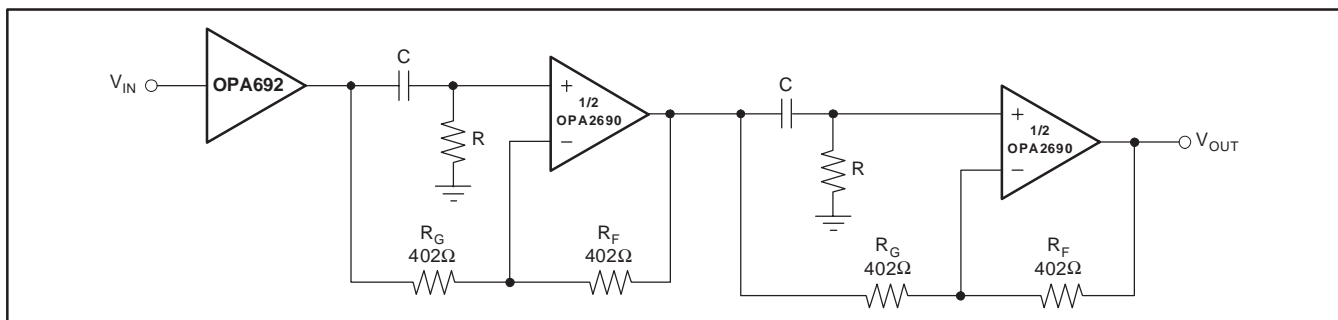
$$t_{GR0} = 2RC \tag{3}$$

For a more accurate analysis of the circuit, consider the group delay for the amplifiers. For example, in the case of the OPA2690, the group delay in the bandwidth from 1MHz to 100MHz is approximately 1.0ns. To account for this, modify the transfer function, which now comes out to be:

$$t_{GR} = 2 (2RC + T_D) \tag{4}$$

with $T_D = (1/360) \times (d\phi/df)$ = delay of the op amp itself. The values of resistors R_F and R_G should be equal and low to avoid parasitic effects. If the all-pass filter is designed for very low delay times, include parasitic board capacitances to calculate the correct delay time. Simulating this application using the PSPICE model of the OPA2690 will allow this design to be tuned to the desired performance.

DIFFERENTIAL RECEIVER/DRIVER

A very versatile application for a dual operational amplifier is the differential amplifier configuration detailed in Figure 8. With both amplifiers of the OPA2690 connected for noninverting operation, the circuit provides a high input impedance whereas the gain can easily be set by just one resistor, R_G. When operated in low gains, the output swing may be limited as a result of the common-mode input swing limits of the amplifier itself. An interesting modification of this circuit is to place a capacitor in series with the R_G. Now the DC gain for each side is reduced to +1, whereas the AC gain still follows the standard transfer function of $G = 1 + 2R_F/R_G$. This might be advantageous for applications processing only a frequency band that excludes DC or very low frequencies. An input DC voltage resulting from input bias currents is not amplified by the AC gain and can be kept low. This circuit can be used as a differential line receiver, driver, or as an interface to a differential input ADC.
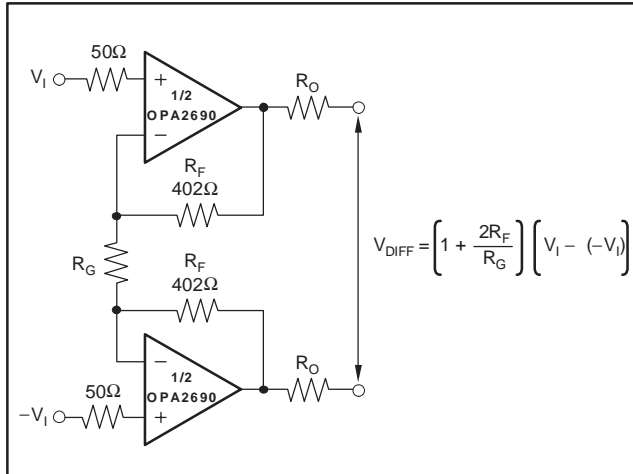

Figure 7. 2-Stage, All-Pass Network

Figure 8. High-Speed Differential Receiver

SINGLE-SUPPLY MFB DIFFERENTIAL ACTIVE FILTER: 10MHz BUTTERWORTH CONFIGURATION

The active filter circuit shown in Figure 9 can be easily implemented using the OPA2690. In this configuration, each amplifier of the OPA2690 operates as an integrator. For this reason, this type of application is also called infinite gain filter implementation. A Butterworth filter can be implemented using the following component ratios:

$$f_O = \frac{1}{2 \times \pi \times R \times C} \text{(cutoff frequency)}$$

$$R_1 = R_2 = 0.65 \times R$$

$$R_3 = 0.375 \times R$$

$$C_1 = C$$

$$C_2 = 2 \times C$$

Figure 9. Single-Supply, MFB Active Filter, 10MHz LP Butterworth

The frequency response for a 10MHz Butterworth filter is shown in Figure 10. One advantage for using this type of filter is the independent setting of ω_o and Q. Q can be easily adjusted by changing the $R_{3A, B}$ resistors without affecting ω_o.

Figure 10. Multiple Feedback Filter Frequency Response

SINGLE-SUPPLY DIFFERENTIAL ADC DRIVER

The single-supply differential ADC driver shown on the front page is ideal for driving high-frequency ADCs. As shown in the plot on the front page, *Harmonic Distortion vs Frequency for the Single-Supply Differential ADC Driver*, the 2nd-harmonic reacts as expected and drops to a –95dBc at 1MHz and –87dBc at 5MHz—a significant improvement in going to differential from single-ended.

The circuit shown on the front page has a 195MHz, –3dB bandwidth that can be easily bandlimited by using a capacitor in parallel with the feedback resistors. Refer to Figure 11 for more details. The –3dB frequency is given by Equation 5.

$$f_{-3dB} = \frac{1}{2\pi R_F C_F}$$

(5)

Figure 11. Single-Supply Differential ADC Driver

For example, $C_F = 8.6pF$ in parallel with $R_F = 402\Omega$ will control the –3dB frequency to 18MHz.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA2690 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in the table below.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA2690ID	SO-8	DEM-OPA-SO-2A	SBOU003
OPA2690I-14D	SO-14	DEM-OPA-SO-2D	SBOU002

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA2690 product folder.

MACROMODELS

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA2690 (use two OPA690 SPICE models) is available through the Texas Instruments web page (http://www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dP characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

As the OPA2690 is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a noninverting unity-gain follower application, the feedback connection should be made with a 25Ω resistor, not a direct short. This will isolate the inverting input capacitance from the output pin and improve the frequency response flatness. Usually, the feedback resistor value should be between 200Ω and 1.5kΩ. Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA2690. Above 1.5kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor can cause unintentional band-limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (see Figure 1) to be less than approximately 300Ω. The combined impedance $R_F \| R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network and thus, a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \| R_G < 300\Omega$ will keep this pole above 250MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

BANDWIDTH vs GAIN: NONINVERTING OPERATION

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the Electrical Characteristics. Ideally, dividing GBP by the noninverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (increased feedback factors), most amplifiers will exhibit a more complex response with lower phase margin. The OPA2690 is compensated to give a slightly peaked response in a noninverting gain of 2 (see Figure 1). This results in a typical gain of +2 bandwidth of 220MHz, far exceeding that predicted by dividing the 300MHz GBP by 2. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +10, the 30MHz bandwidth shown in the Electrical Characteristics agrees with that predicted using the simple formula and the typical GBP of 300MHz.

The frequency response in a gain of +2 may be modified to achieve exceptional flatness simply by increasing the noise gain to 2.5. One way to do this, without affecting the +2 signal gain, is to add an 804Ω resistor across the two inputs in the circuit of Figure 1. A similar technique may be used to reduce peaking in unity-gain (voltage follower) applications. For example, by using a 402Ω feedback resistor along with a 402Ω resistor across the two op amp inputs, the voltage follower response will be similar to the gain of +2 response of Figure 2. Reducing the value of the resistor across the op amp inputs will further limit the frequency response due to increased noise gain.

The OPA2690 exhibits minimal bandwidth reduction going to single-supply (+5V) operation as compared with ±5V. This is because the internal bias control circuitry retains nearly constant quiescent current as the total supply voltage between the supply pins is changed.

INVERTING AMPLIFIER OPERATION

Since the OPA2690 is a general-purpose, wideband voltage-feedback op amp, all of the familiar op amp application circuits are available to the designer. Inverting operation is one of the more common requirements and offers several performance benefits. See Figure 12 for a typical inverting configuration where the I/O impedances and signal gain from Figure 1 are retained in an inverting circuit configuration.

In the inverting configuration, three key design considerations must be noted. The first is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted-pair, long PCB trace, or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This is the simplest approach and results in optimum bandwidth and noise performance. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of –2, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 100Ω feedback

resistor. This has the interesting advantage that the noise gain becomes equal to 2 for a 50Ω source impedance—the same as the noninverting circuits considered in the previous section. The amplifier output, however, will now see the 100Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 200Ω to 1.5kΩ range. In this case, it is preferable to increase both the R_F and R_G values (see Figure 8), and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

Figure 12. Gain of –2 Example Circuit

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and influences the bandwidth. For the example in Figure 12, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of $50\Omega \| 67\Omega = 28.6\Omega$. This impedance is added in series with R_G for calculating the noise gain (NG). The resultant NG is 2.8 for Figure 12, as opposed to only 2 if R_M could be eliminated as discussed above. The bandwidth will therefore be slightly lower for the gain of –2 circuit of Figure 12 than for the gain of +2 circuit of Figure 1.

The third important consideration in inverting amplifier design is setting the bias current cancellation resistor on the noninverting input (R_B). If this resistor is set equal to the total DC resistance looking out of the inverting node, the output DC error, due to the input bias currents, will be reduced to (Input Offset Current) × R_F. If the 50Ω source impedance is DC-coupled in Figure 10, the total resistance to ground on the inverting input will be 228Ω.

Combining this in parallel with the feedback resistor gives the $R_B = 146\Omega$ used in this example. To reduce the additional high-frequency noise introduced by this resistor, it is sometimes bypassed with a capacitor. As long as $R_B < 350\Omega$, the capacitor is not required because the total noise contribution of all other terms will be less than that of the op amp input noise voltage. As a minimum, the OPA2690 requires an R_B value of 50Ω to damp out parasitic-induced peaking—a direct short to ground on the noninverting input runs the risk of a very high-frequency instability in the input stage.

OUTPUT CURRENT AND VOLTAGE

The OPA2690 provides exceptional output voltage and current capabilities in a low-cost monolithic op amp. Under no-load conditions at +25°C, the output voltage typically swings closer than 1V to either supply rail; the specified swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it will deliver more than ±160mA.

The specifications described previously, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or V-I product, which is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2690 output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation for each channel separately. Superimposing resistor load lines onto the plot shows that the OPA2690 can drive ±2.5V into 25Ω or ±3.5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full ±3.9V output swing capability (see the Electrical Characteristics).

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Characteristic tables. As the output transistors deliver power, their junction temperatures increase, decreasing their V_{BE}s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the over-temperature specifications because the output stage junction temperatures will be higher than the minimum specified operating ambient.

To protect the output stage from accidental shorts to ground and the power supplies, output short-circuit protection is included in the OPA2690. The circuit acts to limit the maximum source or sink current to approximately 250mA.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA2690 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the open-loop output resistance of the amplifier is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series-isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2690. Long PCB traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2690 output pin (see the *Board Layout Guidelines* section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For the OPA2690 operating in a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain will reduce the peaking as described previously. The circuit of Figure 13 demonstrates this technique, allowing lower values of R_S to be used for a given capacitive load.
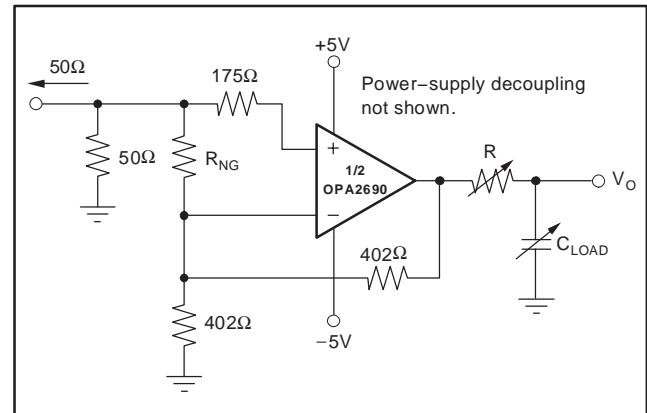

Figure 13. Capacitive Load Driving with Noise Gain Tuning

This gain of +2 circuit includes a noise gain tuning resistor across the two inputs to increase the noise gain, increasing the unloaded phase margin for the op amp. Although this technique will reduce the required R_S resistor for a given capacitive load, it does increase the noise at the output. It also will decrease the loop gain, slightly decreasing the distortion performance. If, however, the dominant distortion mechanism arises from a high R_S value, significant dynamic range improvement can be achieved using this technique. Figure 14 shows the required R_S versus C_{LOAD} parametric on noise gain using this technique. This is the circuit of Figure 13 with R_{NG} adjusted to increase the noise gain (increasing the phase margin) then sweeping C_{LOAD} and finding the required R_S to get a flat frequency response. This plot also gives the required R_S versus C_{LOAD} for the OPA2690 operated at higher signal gains without R_{NG}.
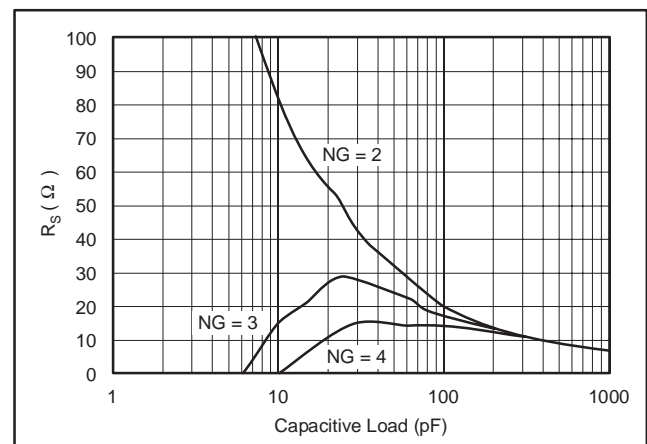

Figure 14. Required R_S vs Noise Gain

DISTORTION PERFORMANCE

The OPA2690 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +5V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 1), this is sum of $R_F + R_G$, while in the inverting configuration it is just R_F. Also, providing an additional supply-decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB). Operating differentially also lowers 2nd-harmonic distortion terms (see the plot on the front page).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The new output stage used in the OPA2690 actually holds the difference between fundamental power and the 2nd- and 3rd-harmonic powers relatively constant with increasing output power until very large output swings are required (> 4V$_{PP}$). This also shows up in the 2-tone, 3rd-order intermodulation spurious (IM3) response curves. The 3rd-order spurious levels are extremely low at low output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels. As the Typical Characteristics show, the spurious intermodulation powers do not increase as predicted by a traditional intercept model. As the fundamental power level increases, the dynamic range does not decrease significantly. For two tones centered at 20MHz, with 10dBm/tone into a matched 50Ω load (that is, 2V$_{PP}$ for each tone at the load, which requires 8V$_{PP}$ for the overall 2-tone envelope at the output pin), the Typical Characteristics show 46dBc difference between the test tone powers and the 3rd-order intermodulation spurious powers. This exceptional performance improves further when operating at lower frequencies or powers.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 5.5nV/√Hz input voltage noise for the OPA2690 is, however, much lower than comparable amplifiers. The input-referred voltage noise, and the two input-referred current noise terms, combine to give low output noise under a wide variety of operating conditions. Figure 15 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.
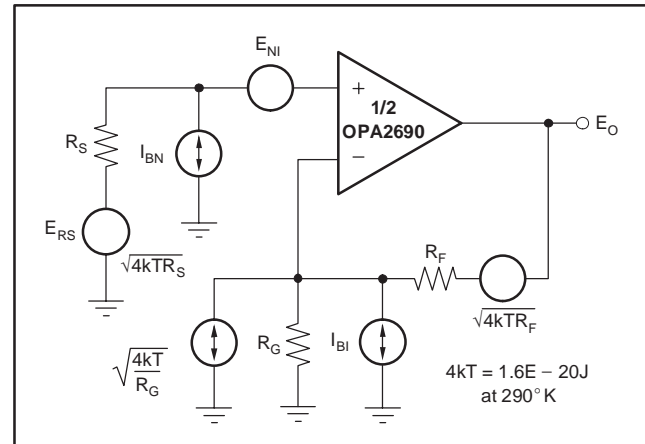

Figure 15. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 6 shows the general form for the output noise voltage using the terms shown in Figure 15.

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_F NG} \qquad (6)$$

Dividing this expression by the noise gain (NG = $(1 + R_F/R_G)$) will give the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 7.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \qquad (7)$$

Evaluating these two equations for the OPA2690 circuit and component values (see Figure 1) gives a total output spot noise voltage of 12.3nV/√Hz and a total equivalent input spot noise voltage of 6.1nV/√Hz. This is including the noise added by the bias current cancellation resistor (175Ω) on the noninverting input. This total input-referred spot noise voltage is only slightly higher than the 5.5nV/√Hz specification for the op amp voltage noise alone. This will be the case as long as the impedances appearing at each op amp input are limited to the previously recommend maximum value of 300Ω. Keeping both ($R_F \parallel R_G$) and the noninverting input source impedance less than 300Ω will satisfy both noise and frequency response flatness considerations. As the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_B) for the inverting op amp configuration of Figure 12 is not required.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output DC accuracy in a wide variety of applications. The power-supply current trim for the OPA2690 gives even tighter control than comparable amplifiers. Although the high-speed input stage does require relatively high input bias current (typically 5µA out of each input terminal), the close matching between them may be used to reduce the output DC error caused by this current. The total output offset voltage may be considerably reduced by matching the DC source resistances appearing at the two inputs. This reduces the output DC error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 1, and using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

$$\pm(NG \times V_{OS(MAX)}) \pm (R_F \times I_{OS(MAX)})$$
$$= \pm(2 \times 4.5mV) \pm (402\Omega \times 1\mu A)$$
$$= \pm 9.4mV - (NG = \text{noninverting signal gain})$$

A fine-scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp circuit. Most of these techniques eventually reduce to adding a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. However, the DC offset voltage on the summing junction will set up a DC current back into the source that must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a DC-coupled inverting amplifier, Figure 16 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the DC offsetting current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This ensures that the adjustment circuit has minimal effect on the loop gain and hence, the frequency response.

Figure 16. DC-Coupled, Inverting Gain of –2, with Offset Adjustment

DISABLE OPERATION (SO-14 Package Only)

The OPA2690I-14D provides an optional disable feature that can be used either to reduce system power or to implement a simple channel multiplexing operation. If the $\overline{DIS}$ control pin is left unconnected, the OPA2690I-14D will operate normally. To disable, the control pin must be asserted LOW. Figure 17 shows a simplified internal circuit for the disable control feature.
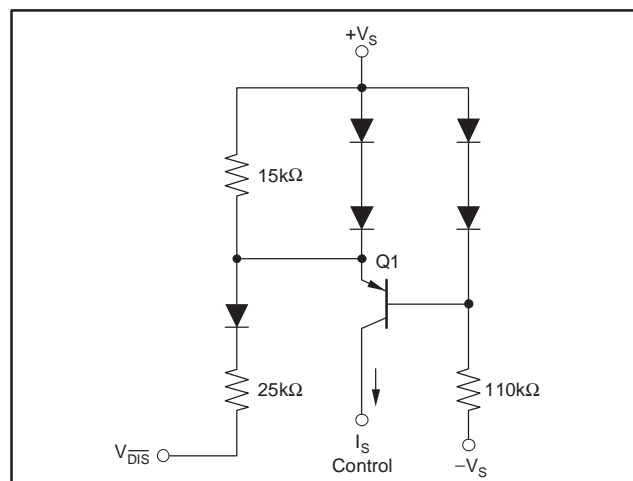

Figure 17. Simplified Disable Control Circuit

In normal operation, base current to Q1 is provided through the 110kΩ resistor, while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled LOW, additional current is pulled through the 15kΩ resistor, eventually turning on those two diodes (≈100µA). At this point, any further current pulled out of V_{DIS} goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode are only those required to operate the circuit of Figure 17. Additional circuitry ensures that turn-on time occurs faster than turn-off time (make-before-break).

When disabled, the output and input nodes go to a high-impedance state. If the OPA2690 is operating at a gain of +1, this will show a very high impedance at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance ($R_F + R_G$) and the isolation will be very poor as a result.

One key parameter in disable operation is the output glitch when switching in and out of the disabled mode. Figure 18 shows these glitches for the circuit of Figure 1 with the input signal at 0V. The glitch waveform at the output pin is plotted along with the $\overline{DIS}$ pin voltage.

The transition edge rate (dv/dt) of the $\overline{DIS}$ control line will influence this glitch. For the plot of Figure 18, the edge rate was reduced until no further reduction in glitch amplitude was observed. This approximately 1V/ns maximum slew rate may be achieved by adding a simple RC filter into the $\overline{DIS}$ pin from a higher speed logic line. If extremely fast transition logic is used, a 2kΩ series resistor between the logic gate and the $\overline{DIS}$ input pin provides adequate bandlimiting using just the parasitic input capacitance on the $\overline{DIS}$ pin while still ensuring adequate logic level swing.

Figure 18. Disable/Enable Glitch

THERMAL ANALYSIS

Due to the high output power capability of the OPA2690, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA2690ID (SO-8 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and with both outputs driving a grounded 20Ω load to +2.5V.

$P_D = 10V \times 12.6mA + 2 \, [5^2/(4 \times (20Ω \, || \, 804Ω))] = 766mW$

Maximum $T_J = +85°C + (0.766W \times 125°C/W) = 180°C$.

This absolute worst-case condition exceeds the specified maximum junction temperature. Actual P_{DL} is normally less than that considered here. Carefully consider maximum T_J in your application.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA2690 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between

the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1μF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA2690. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB traces as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 402Ω feedback used in the Electrical Characteristics is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for the unity-gain follower application. This effectively isolates the inverting input capacitance from the output pin that would otherwise cause an additional peaking in the gain of +1 frequency response.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils)

should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load*. Low parasitic capacitive loads (< 3pF) may not need an R_S because the OPA2690 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin, see Figure 14). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA2690 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2690 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *Recommended R_S vs Capacitive Load*. This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA2690 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2690 onto the board.

INPUT AND ESD PROTECTION

The OPA2690 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 19.
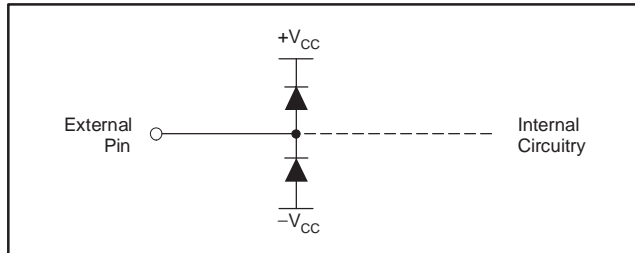

Figure 19. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA2690), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
5/06	E	18	Design-In-Tools	Demonstration fixture numbers changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
OPA2690I-14D	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2690I-14DG4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2690I-14DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2690I-14DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2690ID	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2690IDG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2690IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2690IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2690I-14DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA2690IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2690I-14DR	SOIC	D	14	2500	346.0	346.0	33.0
OPA2690IDR	SOIC	D	8	2500	346.0	346.0	29.0

D (R−PDSO−G8) PLASTIC SMALL−OUTLINE PACKAGE

0.197 (5,00)
0.189 (4,80)
C

8   5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)
D

Pin 1
Index Area

1   4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) M

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−2/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
        D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
        E. Reference JEDEC MS−012 variation AA.

D (R−PDSO−G14) PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

⚠C

14 8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) ⚠D

1 7

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ | 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.007 (0,17)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25) 0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−3/H 11/2006

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
⚠C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
not exceed .006 (0,15) per end.
⚠D Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS−012 variation AB.

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