



# OZ962

## High-Efficiency Inverter Controller

### FEATURES

- Single-stage power conversion, input voltage range of 5V to 18V
- Reduces the number of components and board size by 30% compared with conventional design
- Supports both floating and grounded secondary designs
- 90% efficiency vs. typical 75% efficiency of conventional designs
- Internal open-lamp and short-circuit protections
- Wide dimming range
- Supports synchronization among multiple inverter modules
- Reliable 2-winding transformer design, eliminates arcing problems
- Constant frequency, symmetrical, sinusoidal drive

### GENERAL DESCRIPTION

The OZ962 is a unique high-efficiency, CCFL backlight controller. It generates symmetrical, near sinusoidal output voltage and current waveforms for driving a CCFL backlight. The OZ962 operates in a single, constant frequency, pulse-width-modulation (PWM) mode. Typical operating frequency ranges between 30 KHz to 100 KHz, depending on the CCFL and the transformer's characteristics.

Operating in a PWM push-pull manner, the transformer in the OZ962 backlight inverter requires only one primary winding and one secondary winding, with the secondary winding requiring no fold-back treatment.

The OZ962 is available in both 16-pin SOIC and TSSOP packages. It is specified over the commercial temperature range: 0 °C to +70 °C.

### ORDERING INFORMATION

- OZ962R** - 16 lead TSSOP
- OZ962G** - 16-pin plastic SOP

### TYPICAL APPLICATION CIRCUIT

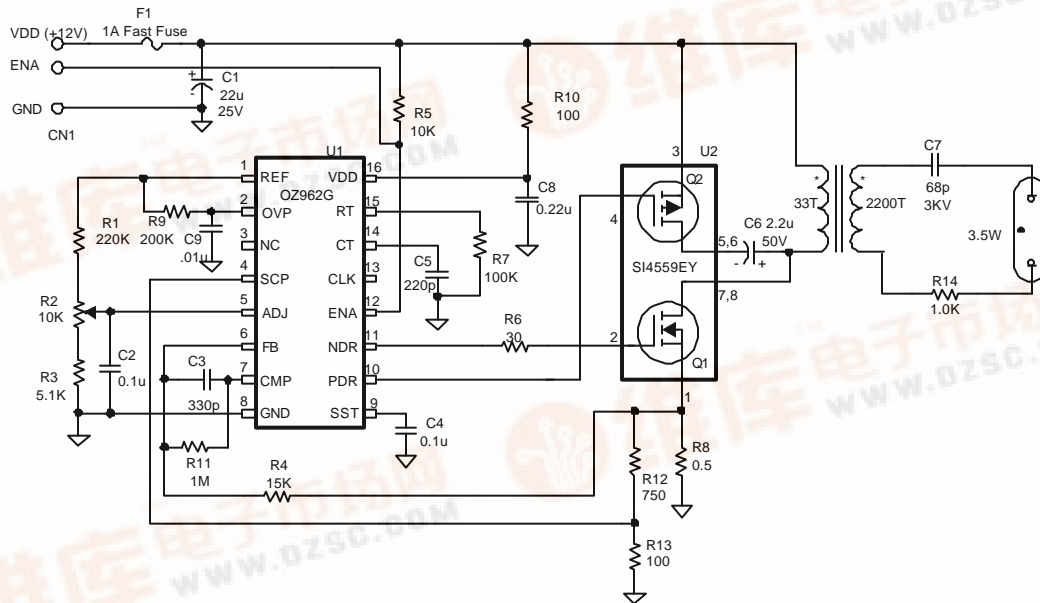
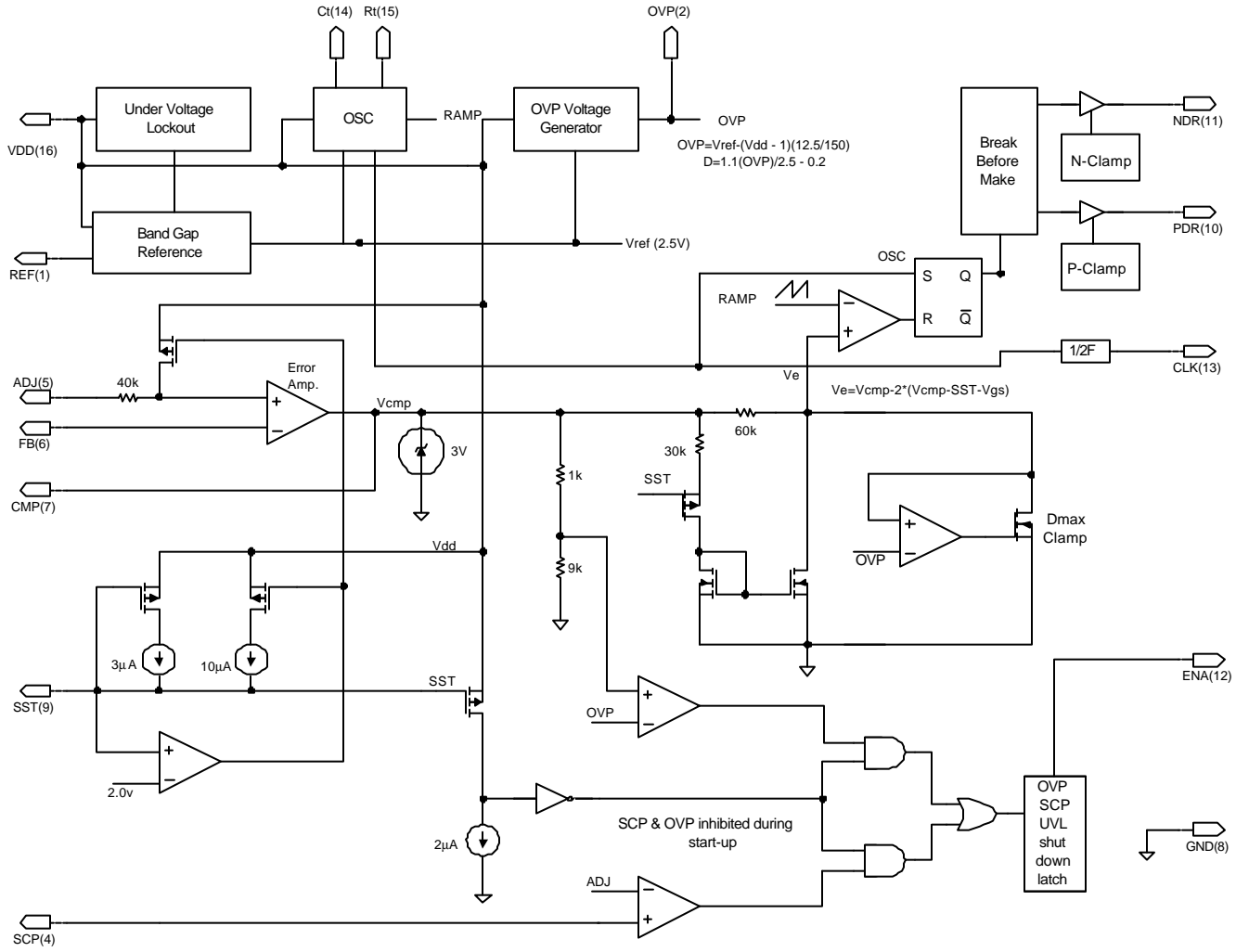


Figure 1. Typical Floating Secondary Application



## FUNCTIONAL BLOCK DIAGRAM



**Note:**  
 OVP – Over Voltage Protection  
 SCP – Short-Circuit Protection  
 UVL – Under Voltage Lockout

**Figure 2. Functional Block Diagram**

## PIN DESCRIPTION

Names	Pin No.	I/O	Description
REF	1	O	Reference voltage output. Nominal voltage is 2.5 V.
OVP	2	I	Over-voltage protection setting. Refer to formula for OVP in block diagram on page 2 of this document.
NC	3	-	No connection.
SCP	4	I	Short-circuit protection input.
ADJ	5	I	Reference voltage input for dimming control.
FB	6	I	Current sense feedback.
CMP	7	O	Compensation for the current sense feedback.
GND	8	GND	Ground.
SST	9	I	$T_{sst} \approx 0.2 C_{sst} (V_{dd} - 5)$ , where $C_{sst}$ is the soft start capacitor value in $\mu F$ and $T_{sst}$ value is in $\mu s$ .
PDR	10	O	Gate drive output for the P-MOSFET.
NDR	11	O	Gate drive output for the N-MOSFET.
ENA	12	I	Enable input, active high ( $V_{th}$ is about 1.7 V).
CLK	13	O	Open-drain clock output.
CT	14	I/O	Timing capacitor. CT and RT set the clock frequency.
RT	15	I/O	Timing resistor.
VDD	16	PWR	Supply voltage input.

## ABSOLUTE MAXIMUM RATINGS

VDD	18 V	Operating temp.	0 °C to 70 °C
GND	+/- 0.3 V	Operating junction temp.	150 °C
Logic inputs	-0.3 V to VDD+0.3 V	Storage temp.	-55 to 150 °C
Power dissipation	800 mW at 25 °C		

## RECOMMENDED OPERATING RANGE

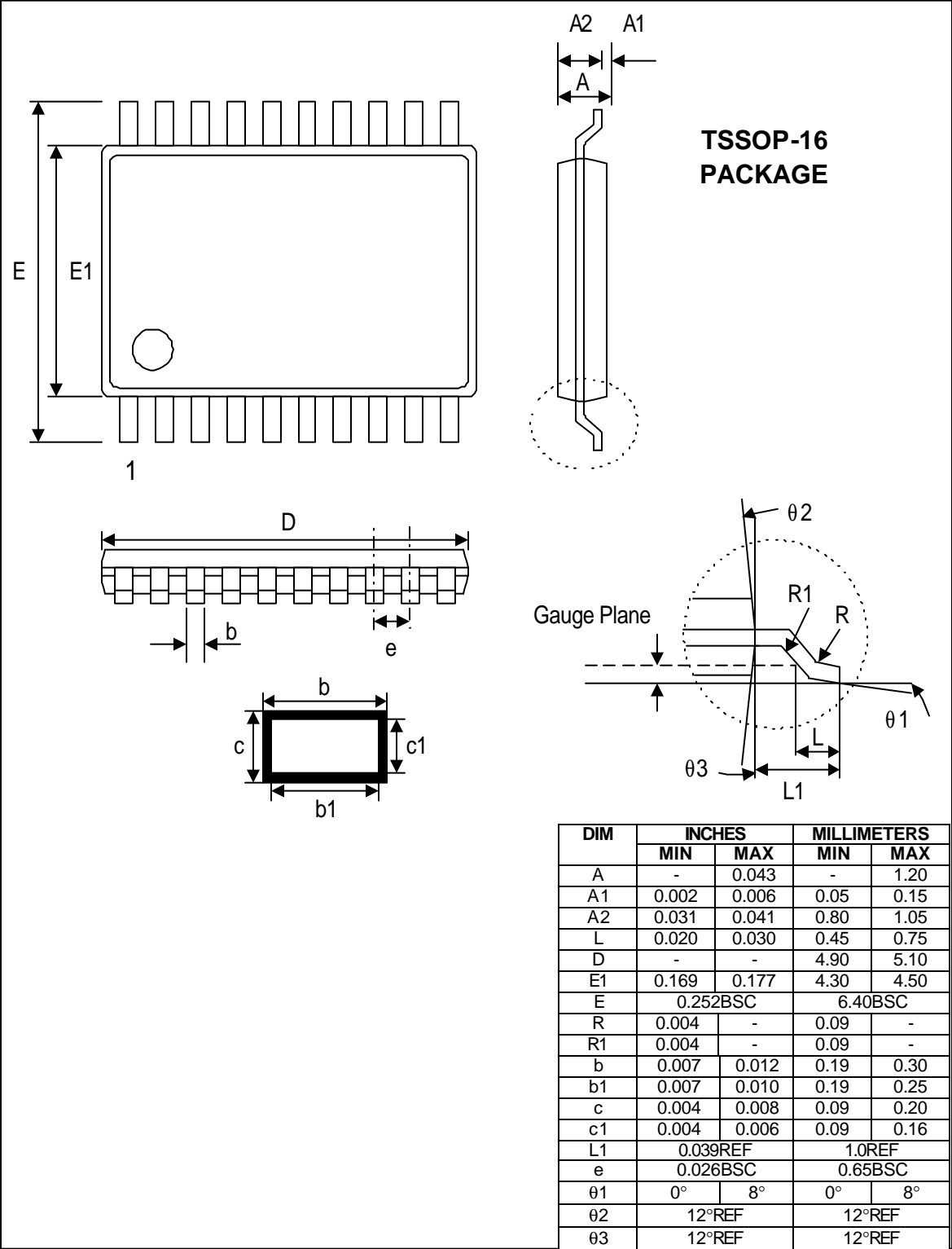
VDD	5V to 18V
Fosc	30 KHz to 100 KHz
Rosc	50 k to 150 k

## FUNCTIONAL SPECIFICATIONS

Parameter	Symbol	Test Conditions 5 V < VDD < 15 V	Limits			Unit
			Min	Typ	Max	
<b>Reference Voltage</b>						
Nominal voltage	Vref	I <sub>load</sub> = 0.25 mA, VDD = 5 V	2.37	2.50	2.63	V
Line regulation			-	8	-	mV/V
Load regulation		I <sub>load</sub> = 0.2 mA to 1.0 mA	-	1	-	mV/mA
<b>Oscillator</b>						
Initial accuracy	fosc	Ct = 220 pF, Rt = 120 k	48	53	58	KHz
Ramp peak			2.45	2.55	2.65	V
Ramp valley			0.40	0.45	0.50	V
Temp. stability		TA = 0 °C to 70 °C	-	-	200	ppm/ °C
<b>Error Amplifier</b>						
Input bias current		V <sub>ADJ</sub> =V <sub>FB</sub> =2.0 V	-	25	500	nA
Input offset voltage		V <sub>FB</sub> = 4.0 V	-	5	10	mV
Input voltage range			0	-	VDD-1.5	V
Open loop voltage gain			50	60	-	dB
Unity gain bandwidth			1	1.5	-	MHz
Power supply rejection			50	60	-	dB
<b>Under-Voltage Lockout</b>						
Positive-going threshold voltage			-	3.8	4	V
Negative-going threshold voltage			3.4	3.6	-	V
<b>Supply</b>						
Supply current - Enable Low Adj, CT = Open	I <sub>OFF</sub>	VDD = 5.0 V	-	25	120	μA
Supply current - Enable Low Adj, CT = Open	I <sub>OFF</sub>	VDD = 15 V	-	25	120	μA
Supply current - Enable High	I <sub>ON</sub>	VDD = 5.0 V	-	0.6	1.5	mA
Supply current - Enable High	I <sub>ON</sub>	VDD = 15 V	-	0.6	1.5	mA
<b>NDR output</b>						
Output high voltage	V <sub>OH</sub>	I <sub>sink</sub> = 10 mA, VDD < 7.8 V	VDD-0.3	VDD-0.5	-	V
		VDD > 7.8 V	7.0	8.0	9.0	V
Output low voltage	V <sub>OL</sub>	I <sub>source</sub> = 10 mA	-	0.3	0.8	V
Output resistance	R <sub>OUT</sub>	VDD = 5.0 V	-	50	80	Ω
<b>PDR output</b>						
Output high voltage	V <sub>OH</sub>	I <sub>sink</sub> = 10 mA	VDD-0.6	VDD-0.3	-	V
Output low voltage	V <sub>OL</sub>	I <sub>source</sub> = 10 mA, VDD < 7.8 V	0.4	0.5	0.8	V
		VDD > 7.8 V	-	VDD-6.0	VDD-4.0	V
Output resistance	R <sub>OUT</sub>	VDD = 5.0 V	-	50	80	Ω
<b>Break-Before-Make</b>						
Qn off to Qp on delay	T <sub>HL</sub>		200	240	280	ns
Qp off to Qn on delay	T <sub>LH</sub>		220	260	300	ns

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## PACKAGE INFORMATION



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