O2Micro Breathing Life into Mobility

OZ965

High-Efficiency Inverter Controller

FEATURES

- Single-stage power conversion, requiring only a +5 V voltage source
- Reduces the number of components and board size by 30% compared with conventional design
- Supports both floating and grounded secondary designs
- 90% efficiency vs. typical 75% efficiency of conventional designs
- Internal open-lamp and short-circuit protections
- Wide dimming range
- Supports multiple CCFLs
- Simple and reliable 2-winding transformer design
- Eliminates leakage current when used in a floating secondary design
- Constant-frequency design eliminates interference with LCDs

ORDERING INFORMATION

OZ965G - 16-pin plastic SOP
OZ965R - 16-pin plastic TSSOP
OZ965IG - 16-pin plastic SOP
OZ965IR - 16-pin plastic TSSOP

GENERAL DESCRIPTION

The OZ965 is a single chip, high-efficiency, Cold Cathode Fluorescent Lamp (CCFL) backlight inverter controller whose primary function is to convert +5 volt DC power to approximately 600 VAC. Additionally, the OZ965 performs the lamp dimming function with an analog voltage or low frequency Pulse Width Modulation (PWM) control.

Operating Principle:
The CCFL tube, transformer secondary, and capacitor form a resonant circuit. The OZ965 utilizes the low energy loss resonate mode principle to deliver a very high efficiency inverter.

The OZ965 drives the transformer primary with a variable pulse width voltage directly from the +5v supply. The resultant primary drive current is alternately reversing with zero-voltage-switching. Because of the transformer leakage inductance and the secondary resonant circuit, the secondary voltage and current are approximately sinusoidal. This sinusoid results in very little harmonic emi/rfi emissions.

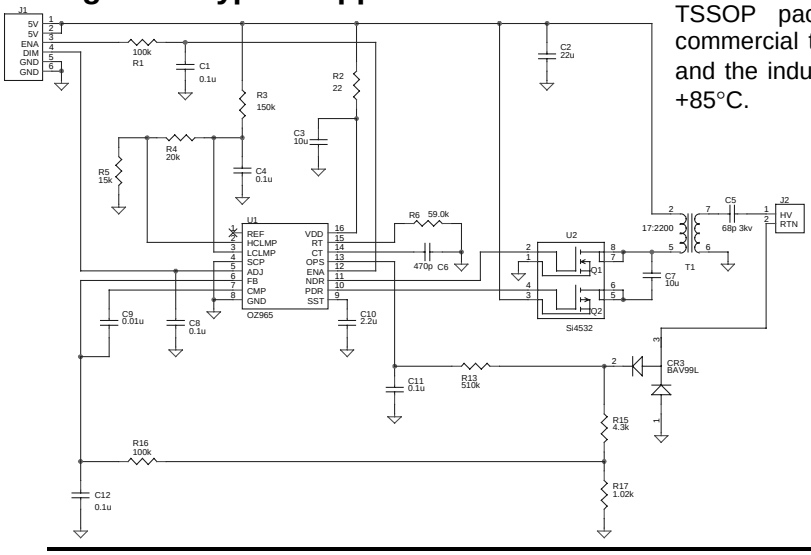
The OZ965 operates at a single, constant frequency in a PWM mode. Typical operating frequency ranges between 30 KHz to 200 KHz, dependent upon the CCFL and transformer characteristics. Intelligent open-lamp protection provides design flexibility so various transformer models/manufacturers may be used.

Its high driving capability allows the OZ965 to drive high power MOSFETs.

The single stage design results in a low cost, reliable transformer without expensive, less reliable secondary fold-back treatment. The transformer does not require a more expensive center tapped primary.

The OZ965 is available in 16-pin SOP and TSSOP packages. It is specified over the commercial temperature range of 0°C to +70°C, and the industrial temperature range of -40°C to +85°C.

Figure 1. Typical Application Circuit



FUNCTIONAL BLOCK DIAGRAM

Refer to the functional block diagram in Figure 2, below, and the Pin Description Table on page 3.

Power is transferred to the transformer primary by the N-MOSFET, driven by the MOSFET gate driver out of pin NDR. The P-MOSFET resets the primary field, driven by pin PDR. The usual design results in approximately 50% duty cycle at full lamp intensity. Terminating the NDR signal earlier than the full brightness lamp pulse width performs lamp dimming, using the analog dimming. The voltages on pins HCLMP and LCLMP set a threshold voltage for the ramp comparator setting the maximum duty cycle for NDR.

A pulse generator circuit creates the clock signal with the frequency determined by an external, constant current setting resistor (RT) and timing capacitor (CT).

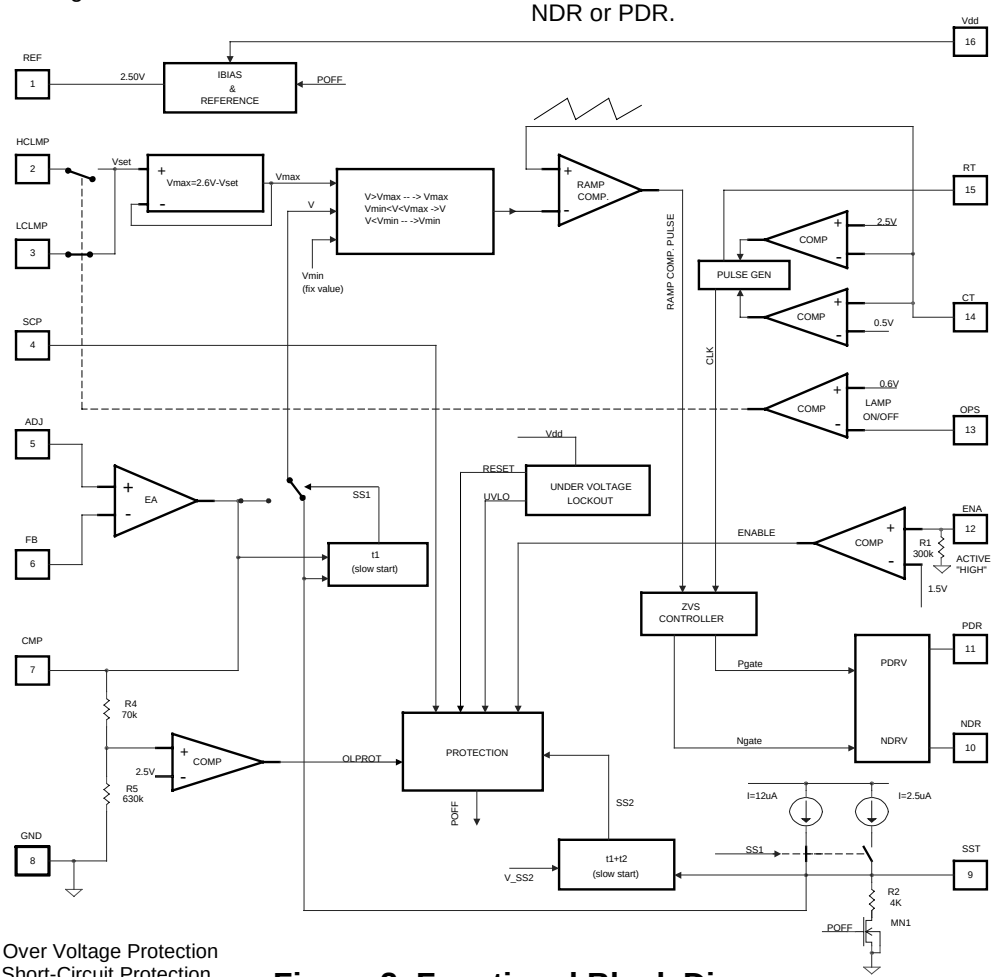
The “soft-start” circuit ensures a reliable and long lamp life starting condition.

“Soft start” gradually increases the energy delivered to the secondary.

When the OZ965 is enabled at pin ENA, the capacitor on pin SST determines the duration of the “soft-start” period, gradually increasing the NDR pulse width to the regulated brightness. The “soft-start” period provides sufficient time for the lamp to ignite.

For system reliability there are several circuit protections provided. To ensure a controlled output, the secondary current is monitored on pin FB and is compared to a reference voltage on pin ADJ. The NDR signal is shortened or lengthened dependent upon this feedback. Protection is provided by the resultant signal, CMP, monitoring for a lamp removal condition. Short circuit protection is provided at pin SCP. The OPS signal selects either HCLMP or LCLMP providing current protection against an “Open Lamp” condition at start-up. The OPS signal also allows adjustment to different transformer models.

To reduce power dissipation, the switch (MOSFET) drive signals are “break-before-make” with a short, fixed off time between activation of NDR or PDR.



Note:
OVP – Over Voltage Protection
SCP – Short-Circuit Protection
UVL – Under Voltage Lockout

Figure 2. Functional Block Diagram

PIN DESCRIPTION

Names	Pin No.	I/O	Description
REF	1	O	Reference voltage output. Nominal voltage is 2.5 V.
HCLMP	2	I	Clamping maximum duty cycle under normal operation.
LCLMP	3	I	Clamping maximum duty cycle under open-lamp condition.
SCP	4	I	Short-circuit protection input (V_{TH}=0.6V)
ADJ	5	I	Reference voltage input for dimming control.
FB	6	I	Current sense feedback.
CMP	7	O	Compensation for the current sense feedback.
GND	8	GND	Ground.
SST	9	I	Soft-start ensures lamp current pulses gradually increases to its normal value
PDR	10	O	Gate drive output for the P-MOSFET.
NDR	11	O	Gate drive output for the N-MOSFET.
ENA	12	I	Enable input, active high (V_{TH}=1.5V)
OPS	13	I	Output current sense (V_{TH}=0.6V)
CT	14	I/O	Timing capacitor. CT and RT set the clock frequency.
RT	15	I/O	Timing resistor. Fosc = 1.91 / (Rt • Ct)
VDD	16	PWR	Supply voltage input.

ABSOLUTE MAXIMUM RATINGS

VDD	5.5V
GND	+/- 0.3V
Logic inputs	-0.3 V to VDD+0.3V

	OZ965	OZ965I
Operating temp.	0°C to 70°C	-40°C to 85°C

Operating junction temp.	150°C
Storage temp.	-55°C to 150°C

	OZ965	OZ965I
Power dissipation		
- 16-pin SOP	.720W	.580W
- 16-pin TSSOP	.690W	.550W
Thermal Impedance		
- 16-pin SOP	111°C/W	111°C/W
- 16-pin TSSOP	115°C/W	115°C/W

RECOMMENDED OPERATING RANGE

VDD	5.0 V +/- 5%
Fosc	30 KHz to 200 KHz
Rosc	50 k to 150 k

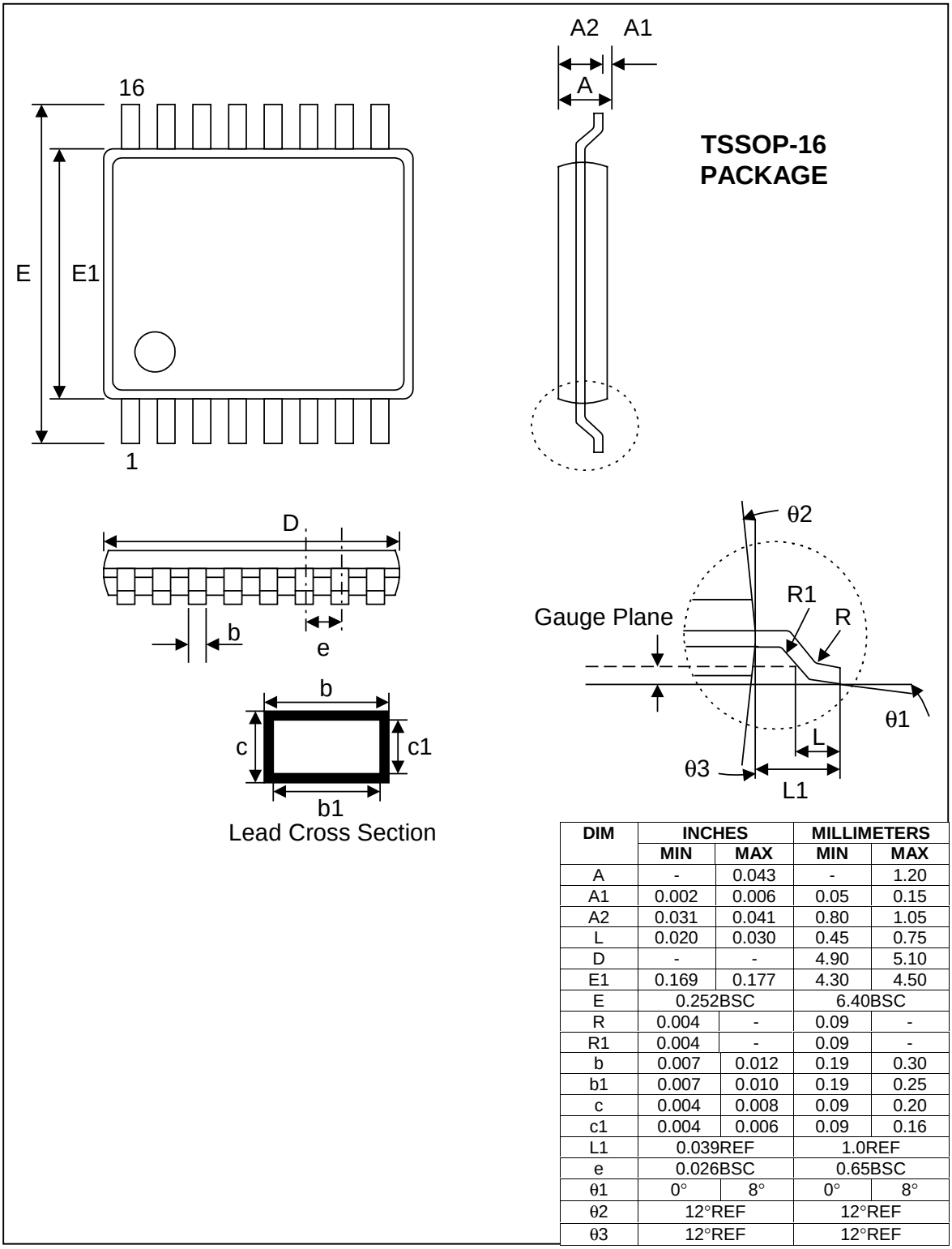
FUNCTIONAL SPECIFICATIONS

Parameter	Symbol	Test Conditions		Limits		Unit
		4.75 V < VDD < 5.25 V	Min	Typ	Max	
Reference Voltage						
Nominal voltage	Vref	I_{load} = 0.1 mA,	2.37	2.50	2.63	V
Line regulation			-	6	-	mV/V
Load regulation		I_{load} = 0.2 mA to 1.0 mA	-	1	-	mV/mA
Oscillator						
Initial accuracy	fosc	Ct = 470 pF, Rt = 49.9 k		81		KHz
Ramp peak			-	2.54	-	V
Ramp valley			-	0.48	-	V
Temp. stability		TA = -40°C to 85°C	-	-	200	ppm/°C
Error Amplifier						
Input bias current		ADJ=FB=2.0 V	-	0.25	-	uA
Input offset voltage		VFB = 4.0 V		5	10	mV
Input voltage range			0	-	VDD-1.5	V
Open loop voltage gain			-	65	-	dB
Unity gain bandwidth			-	1.5	-	MHz
Power supply rejection			-	60	-	dB
Under-Voltage Lockout						
Positive-going threshold voltage			**See Table 1, page 5**			
Negative-going threshold voltage			**See Table 1, page 5**			
Supply						
Supply current - Enable Low	I_{OFF}		-	195	-	µA
Supply current - Enable High	I_{ON}	VDD = 5.0 V	-	1.0	-	mA
NDR output						
Output high voltage	V_{OH}	Isource = 10 mA, VDD = 5V	-	4.75	-	V
Output low voltage	V_{OL}	Isink = 10 mA, VDD = 5V	-	0.25	0.5	V
Output resistance	R_{OUT}		-	10	-	Ω
PDR output						
Output high voltage	V_{OH}	Isource = 10 mA, VDD = 5V	-	4.7	-	V
Output low voltage	V_{OL}	Isink = 10 mA, VDD = 5V	-	0.5	-	V
Output resistance	R_{OUT}		-	15	-	Ω
Break-Before-Make						
Qn off to Qp on delay	T_{HL}		-	250	-	ns
Qp off to Qn on delay	T_{LH}		-	220	-	Ns
High Clamp						
Duty cycle of NDR	HCLMP	OPS=1 V V_{HCLMP}=0V	92	94	96	%
		OPS=1 V, V_{HCLMP}=1.8V	-	14	-	
Low Clamp						
Duty cycle of NDR	LCLMP	OPS=0 V, V_{LCLMP}=0V	92	94	96	%
		OPS=0 V, V_{LCLMP}=1.8V	-	14	-	
Max. / Min. Duty cycle						
Duty cycle of NDR			6	-	95	%

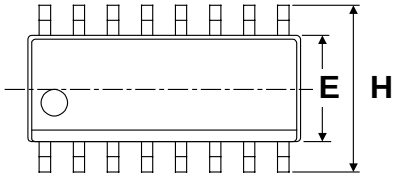
		OZ965				OZ965I			
Parameter	**Test Conditions**		**Limits**		**Unit**		**Limits**		**Unit**
	4.75V < VDD < 5.25V	Min	Typ	Max		Min	Typ	Max	
Under-Voltage Lockout									
Positive-going threshold voltage		-	3.9	4.3	V	-	3.9	4.5	V
Negative-going threshold voltage		3.2	3.4	-	V	3.0	3.4	-	V

Table 1. Under-Voltage Lockout for OZ965 and OZ965I

PACKAGE INFORMATION



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	-	0.043	-	1.20
A1	0.002	0.006	0.05	0.15
A2	0.031	0.041	0.80	1.05
L	0.020	0.030	0.45	0.75
D	-	-	4.90	5.10
E1	0.169	0.177	4.30	4.50
E	0.252BSC		6.40BSC	
R	0.004	-	0.09	-
R1	0.004	-	0.09	-
b	0.007	0.012	0.19	0.30
b1	0.007	0.010	0.19	0.25
c	0.004	0.008	0.09	0.20
c1	0.004	0.006	0.09	0.16
L1	0.039REF		1.0REF	
e	0.026BSC		0.65BSC	
θ1	0°	8°	0°	8°
θ2	12°REF		12°REF	
θ3	12°REF		12°REF	



SOP-16 PACKAGE

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.0075	0.0098	0.19	0.25
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	0.050 BCS.		1.27 BCS.	
H	0.2284	0.2440	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°