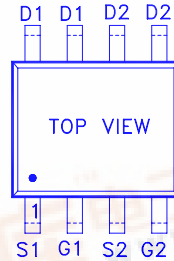
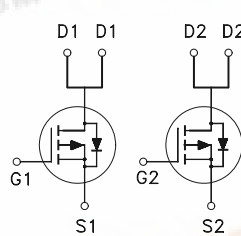


# NIKO-SEM Dual P-Channel Logic Level Enhancement P06B03LV

## Mode Field Effect Transistor SOP-8

### PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	$I_D$
-30	50mΩ	-6A



G :GATE  
D :DRAIN  
S :SOURCE

### ABSOLUTE MAXIMUM RATINGS ( $T_c = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		$V_{DS}$	-30	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$T_c = 25\text{ }^\circ\text{C}$	$I_D$	-6	A
	$T_c = 70\text{ }^\circ\text{C}$		-5	
Pulsed Drain Current <sup>1</sup>		$I_{DM}$	-30	
Power Dissipation	$T_c = 25\text{ }^\circ\text{C}$	$P_D$	2.5	W
	$T_c = 70\text{ }^\circ\text{C}$		1.3	
Operating Junction & Storage Temperature Range		$T_j, T_{stg}$	-55 to 150	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$		62.5	$^\circ\text{C} / \text{W}$

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle  $\leq 1\%$

### ELECTRICAL CHARACTERISTICS ( $T_c = 25\text{ }^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
<b>STATIC</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.9	-1.5	-3	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0V, V_{GS} = \pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -24V, V_{GS} = 0V$			1	$\mu A$
		$V_{DS} = -20V, V_{GS} = 0V, T_j = 125\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>1</sup>	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -10V$	-30			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -5A$		65	80	mΩ
		$V_{GS} = -10V, I_D = -6A$		40	50	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = -10V, I_D = -6A$		16		S

**NIKO-SEM** Dual P-Channel Logic Level Enhancement **P06B03LV**  
 Mode Field Effect Transistor **SOP-8**

DYNAMIC						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$		530		pF
Output Capacitance	$C_{oss}$			135		
Reverse Transfer Capacitance	$C_{rss}$			70		
Total Gate Charge <sup>2</sup>	$Q_g$	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = -10V,$ $I_D = -6A$		10	14	nC
Gate-Source Charge <sup>2</sup>	$Q_{gs}$			2.2		
Gate-Drain Charge <sup>2</sup>	$Q_{gd}$			2		
Turn-On Delay Time <sup>2</sup>	$t_{d(on)}$	$V_{DS} = -15V, R_L = 1\Omega$ $I_D \cong -1A, V_{GS} = -10V, R_{GS} = 6\Omega$		5.7		nS
Rise Time <sup>2</sup>	$t_r$			10		
Turn-Off Delay Time <sup>2</sup>	$t_{d(off)}$			18		
Fall Time <sup>2</sup>	$t_f$			5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ( $T_C = 25^\circ C$ )						
Continuous Current	$I_S$				-2.1	A
Pulsed Current <sup>3</sup>	$I_{SM}$				-4	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = -1A, V_{GS} = 0V$			-1.2	V
Reverse Recovery Time	$t_{rr}$	$I_F = -5A, di_F/dt = 100A / \mu S$		15.5		nS
Reverse Recovery Charge	$Q_{rr}$				7.9	

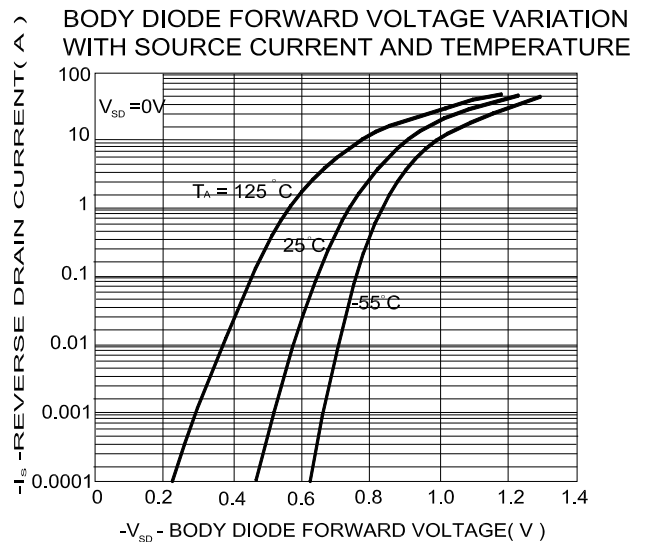
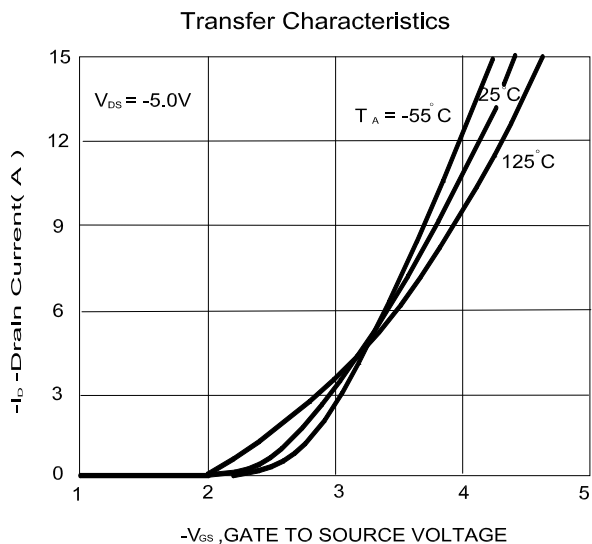
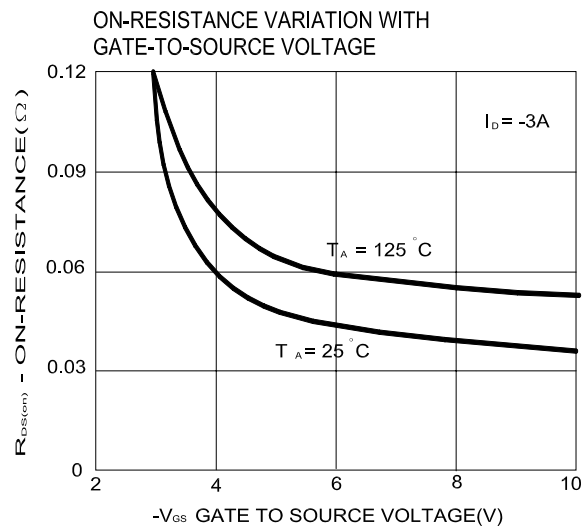
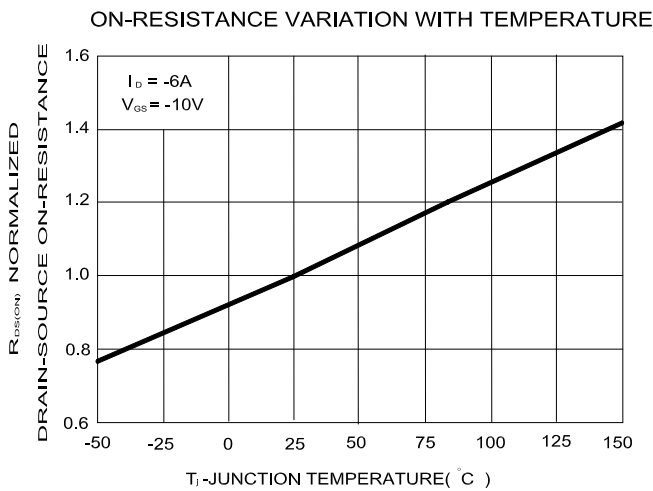
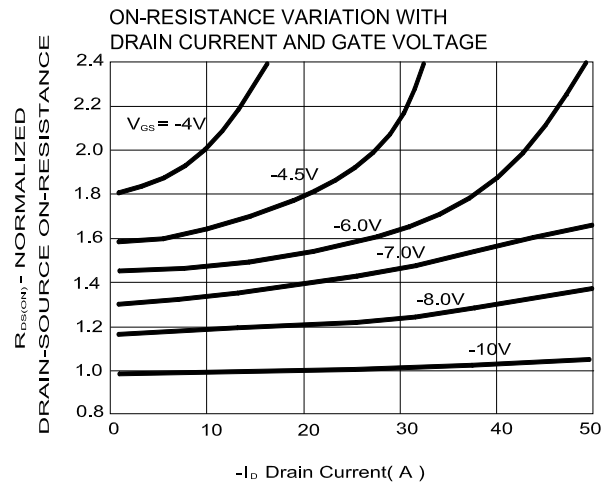
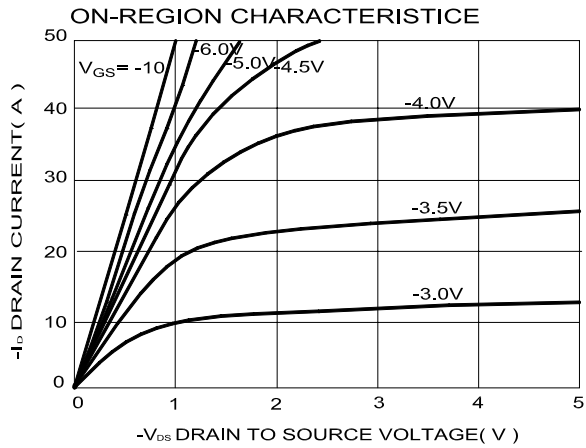
<sup>1</sup>Pulse test : Pulse Width  $\leq 300 \mu sec$ , Duty Cycle  $\leq 2\%$ .

<sup>2</sup>Independent of operating temperature.

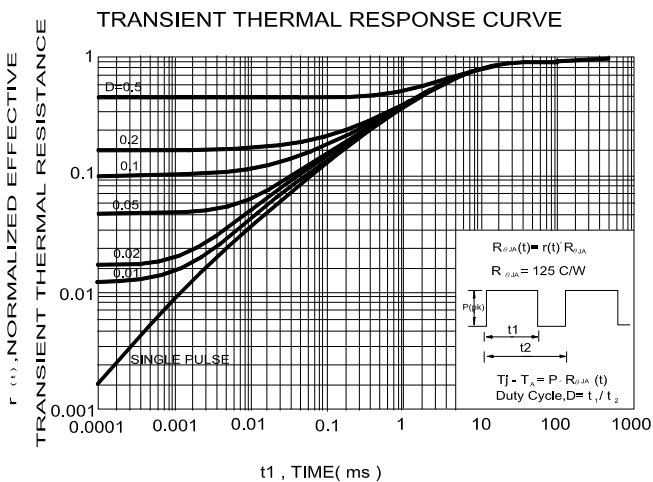
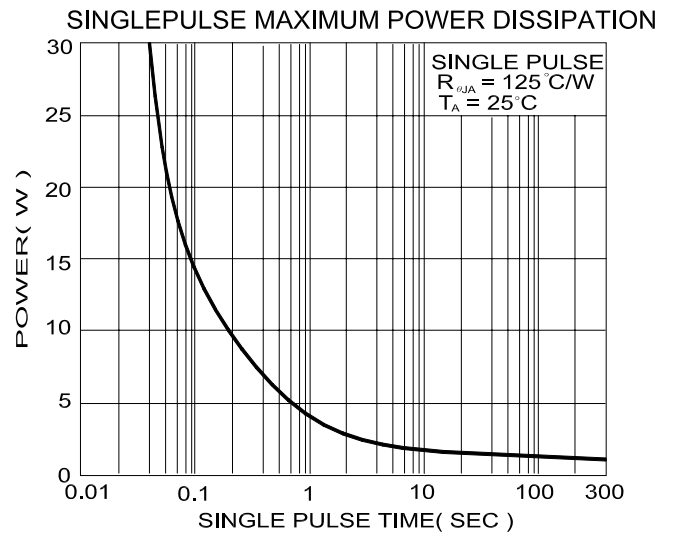
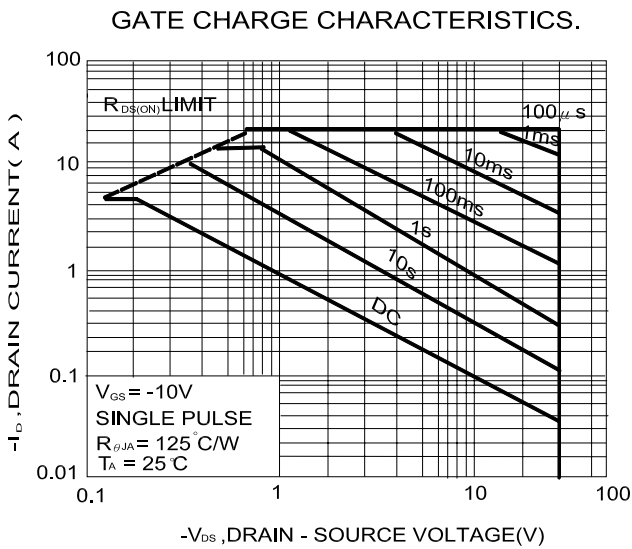
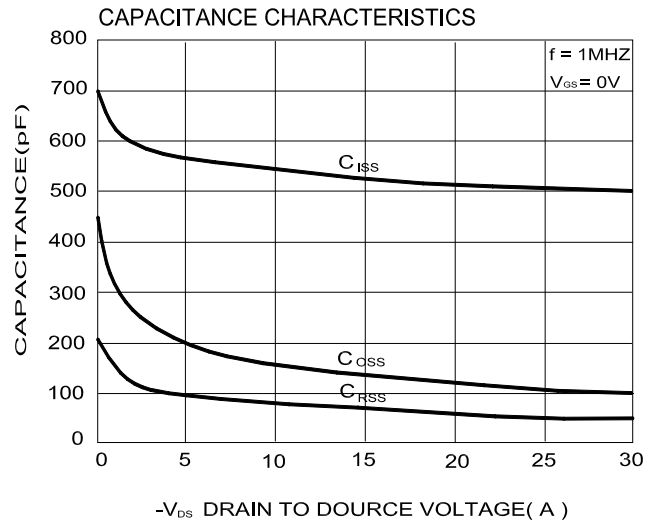
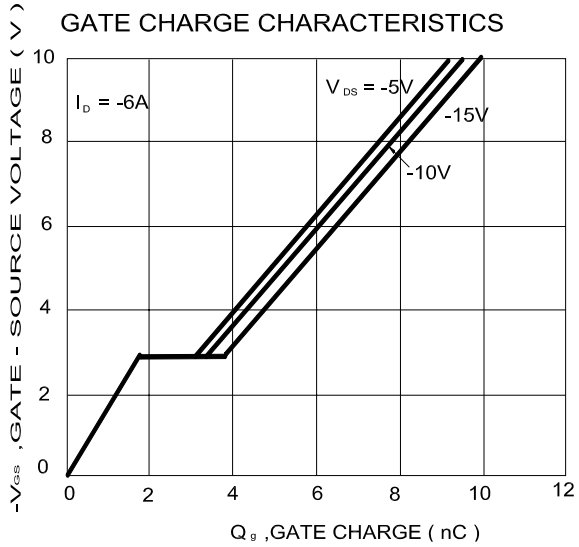
<sup>3</sup>Pulse width limited by maximum junction temperature.

**REMARK: THE PRODUCT MARKED WITH "P06B03LV", DATE CODE or LOT #**

## Typical Characteristics



# NIKO-SEM Dual P-Channel Logic Level Enhancement P06B03LV Mode Field Effect Transistor SOP-8



**SOIC-8 (D) MECHANICAL DATA**

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8	4.9	5.0	H	0.5	0.715	0.83
B	3.8	3.9	4.0	I	0.18	0.254	0.25
C	5.8	6.0	6.2	J		0.22	
D	0.38	0.445	0.51	K	0°	4°	8°
E		1.27		L			
F	1.35	1.55	1.75	M			
G	0.1	0.175	0.25	N			

