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DATA SHEET

P3Z22V10
3V zero power, TotalCMOS™, universal PLD device

Product specification
Supersedes data of 1997 May 15
IC27 Data Handbook

1997 Jul 18

Philips
Semiconductors

PHILIPS

3V zero power, TotalCMOS™, universal PLD device P3Z22V10

FEATURES

- Industry's first TotalCMOS™ 22V10 – both CMOS design and process technologies
- Fast Zero Power (FZP™) design technique provides ultra-low power and high speed
  - Static current of less than 45µA
  - Dynamic current 1/10 to 1/1000 that of competitive devices
  - Pin-to-pin delay of only 10ns
- True Zero Power device with no turbo bits or power down schemes
- Function/JEDEC map compatible with Bipolar, UVCMOS, EECMOS 22V10s
- Multiple packaging options featuring PCB-friendly flow-through pinouts (SOL and TSSOP)
  - 24-pin TSSOP—uses 93% less in-system space than a 28-pin PLCC
  - 24-pin SOL
  - 28-pin PLCC with standard JEDEC pin-out
- Available in commercial and industrial operating ranges
- Supports mixed voltage systems–5V tolerant I/Os
- Advanced 0.5µ E^2CMOS process
- 1000 erase/program cycles guaranteed
- 20 years data retention guaranteed
- Varied product term distribution with up to 16 product terms per output for complex functions
- Programmable output polarity
- Synchronous preset/asynchronous reset capability
- Security bit prevents unauthorized access
- Electronic signature for identification
- Design entry and verification using industry standard CAE tools
- Reprogrammable using industry standard device programmers

DESCRIPTION

The P3Z22V10 is the first SPLD to combine high performance with low power, without the need for "turbo bits" or other power down schemes. To achieve this, Philips Semiconductors has used their FZP™ design technique, which replaces conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates. This results in the combination of low power and high speed that has previously been unattainable in the PLD arena. For 5V operation, Philips Semiconductors offers the P5Z22V10 that offers high speed and low power in a 5V implementation.

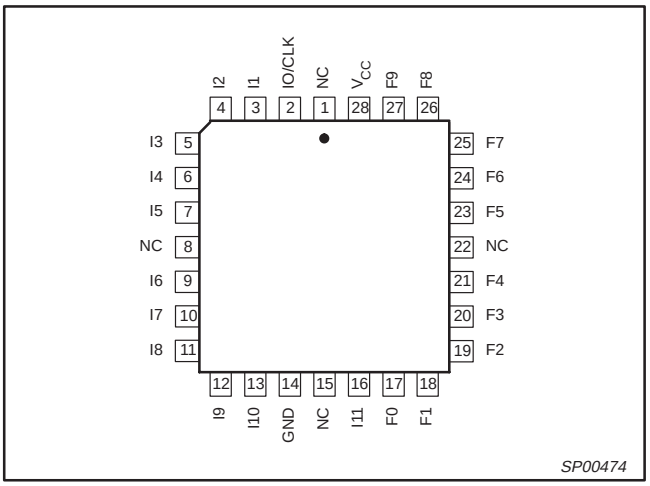
The P3Z22V10 uses the familiar AND/OR logic array structure, which allows direct implementation of sum-of-products equations. This device has a programmable AND array which drives a fixed OR array. The OR sum of products feeds an "Output Macro Cell" (OMC), which can be individually configured as a dedicated input, a combinatorial output, or a registered output with internal feedback.

ORDERING INFORMATION

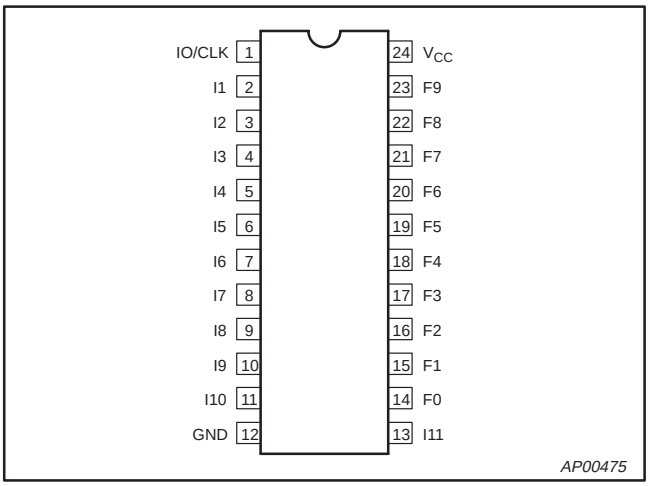
ORDER CODE	PACKAGE	PROPAGATION DELAY	TEMPERATURE RANGE	OPERATING RANGE	DRAWING NUMBER
P3Z22V10-DA	28-pin PLCC	10ns	0 to +70°C	V_{CC} = 3.3V ±10%	SOT261-3
P3Z22V10-DD	24-pin SOL	10ns	0 to +70°C	V_{CC} = 3.3V ±10%	SOT137-1
P3Z22V10-DDH	24-pin TSSOP	10ns	0 to +70°C	V_{CC} = 3.3V ±10%	SOT355-1
P3Z22V10-BA	28-pin PLCC	15ns	0 to +70°C	V_{CC} = 3.3V ±10%	SOT261-3
P3Z22V10-BD	24-pin SOL	15ns	0 to +70°C	V_{CC} = 3.3V ±10%	SOT137-1
P3Z22V10-BDH	24-pin TSSOP	15ns	0 to +70°C	V_{CC} = 3.3V ±10%	SOT355-1
P3Z22V10IBA	28-pin PLCC	15ns	–40 to +85°C	V_{CC} = 3.3V ±10%	SOT261-3
P3Z22V10IBD	24-pin SOL	15ns	–40 to +85°C	V_{CC} = 3.3V ±10%	SOT137-1
P3Z22V10IBDH	24-pin TSSOP	15ns	–40 to +85°C	V_{CC} = 3.3V ±10%	SOT355-1

PIN CONFIGURATIONS

28-Pin PLCC



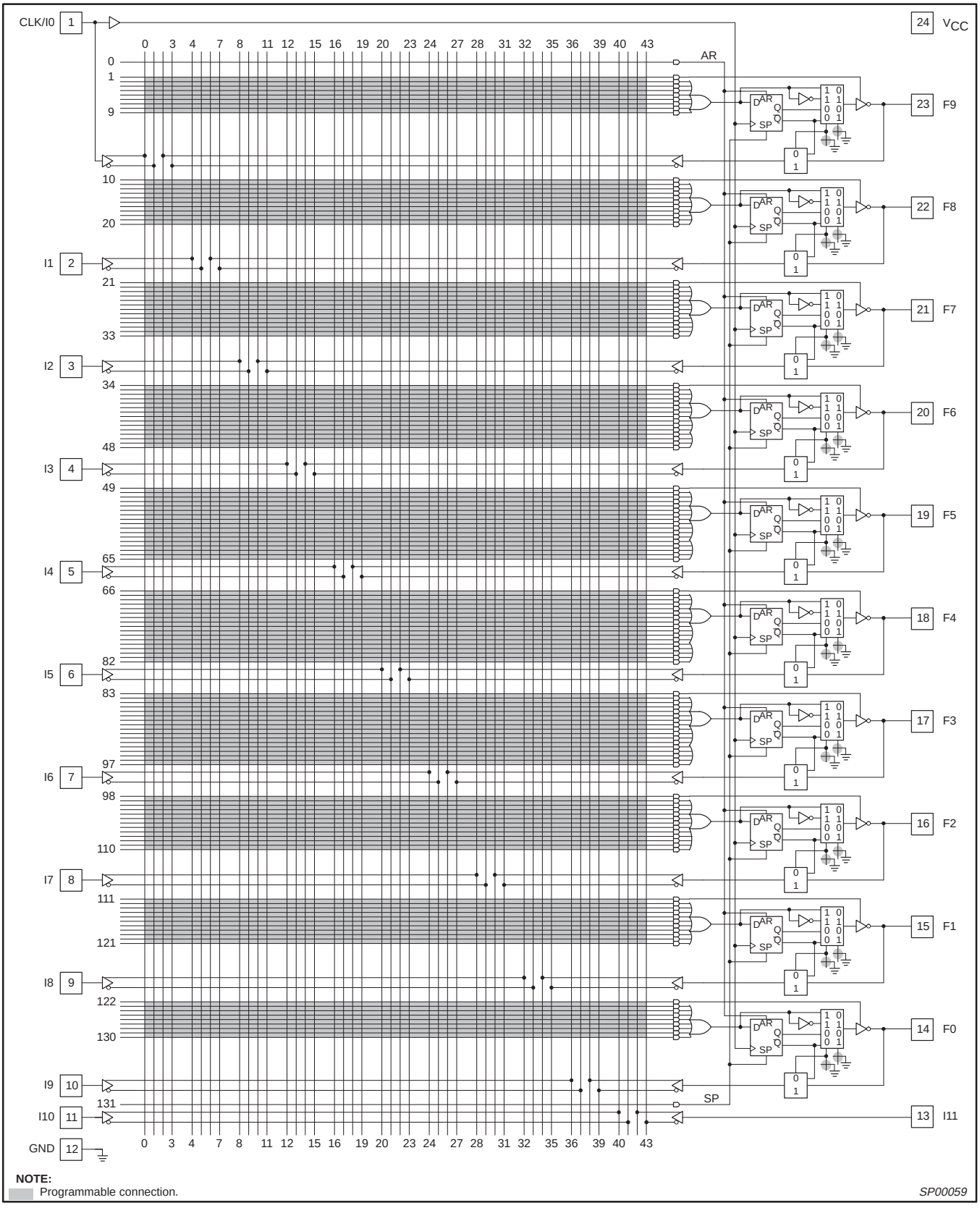
24-Pin SOL and 24-Pin TSSOP



PIN DESCRIPTIONS

PIN LABEL	DESCRIPTION
I1 – I11	Dedicated Input
NC	Not Connected
F0 – F9	Macrocell Input/Output
I0/CLK	Dedicated Input/Clock Input
V_{CC}	Supply Voltage
GND	Ground

LOGIC DIAGRAM



NOTE:
Programmable connection.

SP00059

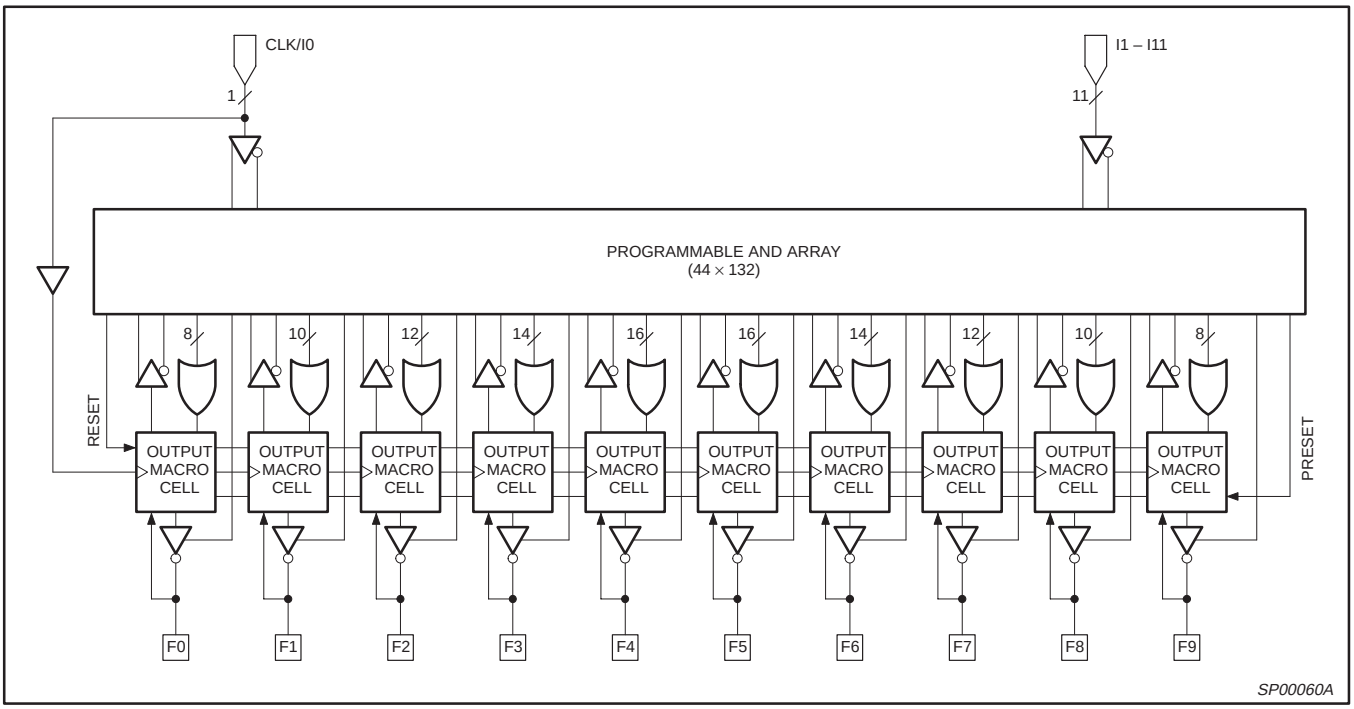


Figure 1. Functional Diagram

FUNCTIONAL DESCRIPTION

The P3Z22V10 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

ARCHITECTURE OVERVIEW

The P3Z22V10 architecture is illustrated in Figure 1. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed-OR array. With this structure, the P3Z22V10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is an I/O macrocell which can be independently programmed to one of 4 different configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions with either Active-High or Active-Low polarity.

AND/OR Logic Array

The programmable AND array of the P3Z22V10 (shown in the Logic Diagram) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

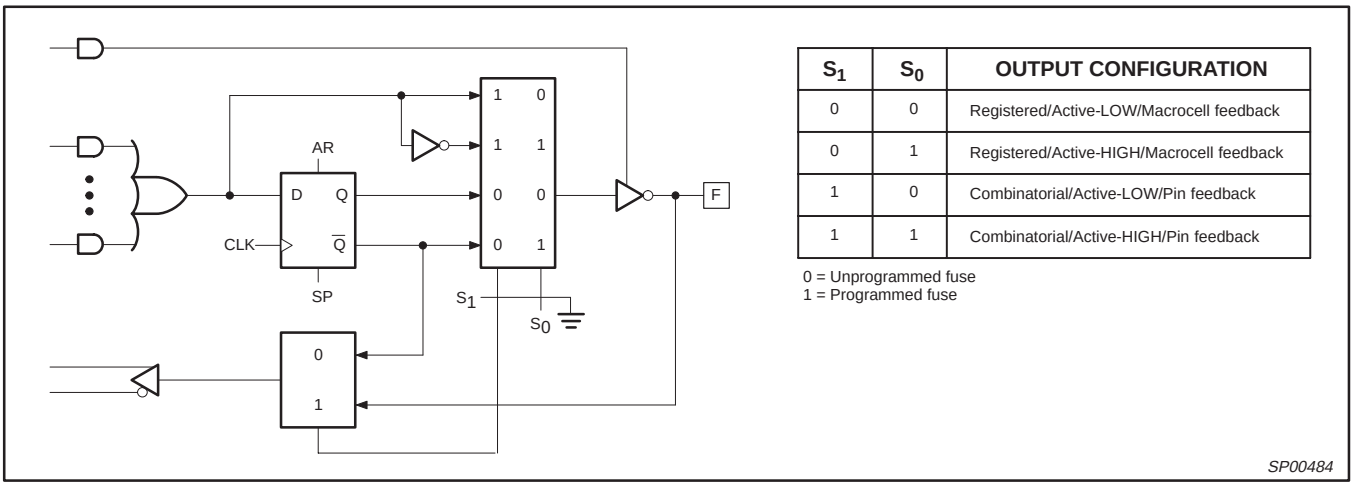
44 input lines:
- 24 input lines carry the True and Complement of the signals applied to the 12 input pins
- 20 additional lines carry the True and Complement values of feedback or input signals from the 10 I/Os

132 product terms:
- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) used to form logical sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset product term
- 1 global asynchronous clear product term

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term which is connected to both the True and Complement of an input signal will always be FALSE, and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a Don't Care state exists and that term will always be TRUE.

Variable Product Term Distribution

The P3Z22V10 provides 120 product terms to drive the 10 OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Logic Diagram). This distribution allows optimum use of device resources.



S_1	S_0	OUTPUT CONFIGURATION
0	0	Registered/Active-LOW/Macrocell feedback
0	1	Registered/Active-HIGH/Macrocell feedback
1	0	Combinatorial/Active-LOW/Pin feedback
1	1	Combinatorial/Active-HIGH/Pin feedback

0 = Unprogrammed fuse
1 = Programmed fuse

Figure 2. Output Macro Cell Logic Diagram

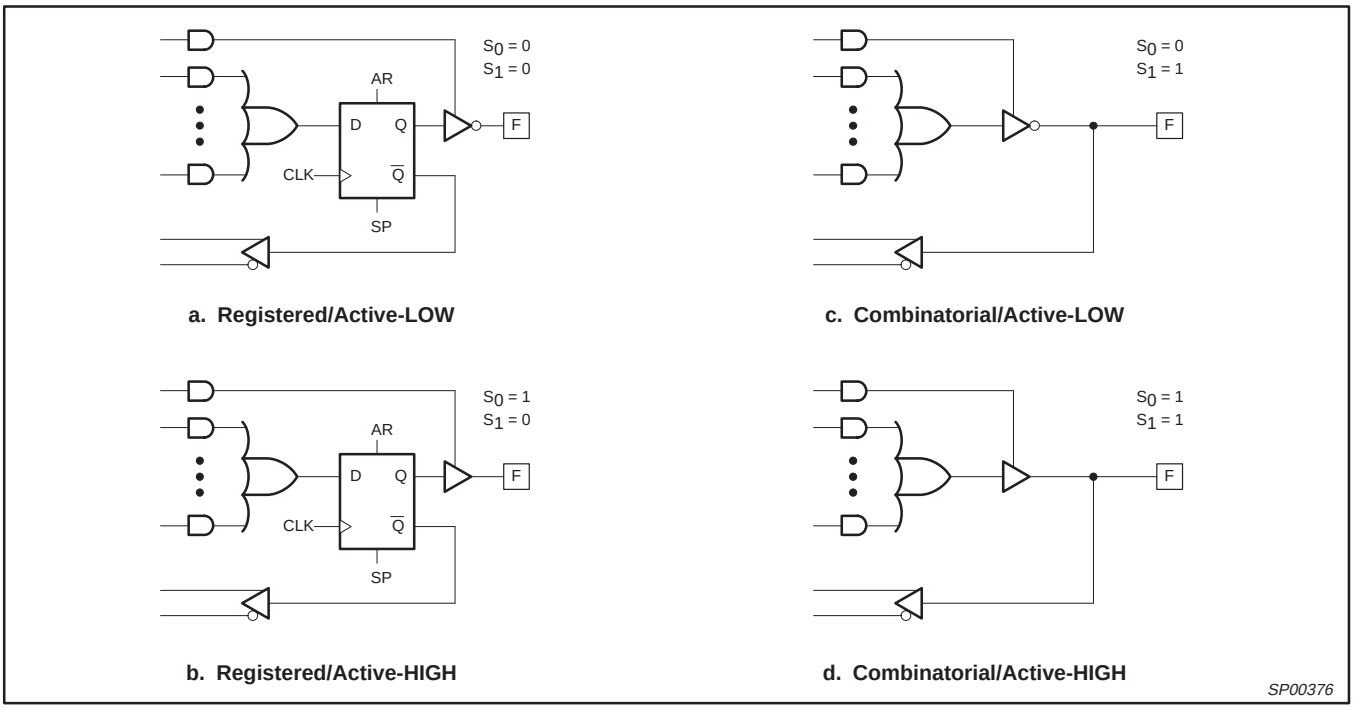


Figure 3. Output Macro Cell Configurations

Programmable I/O Macrocell

The output macrocell provides complete control over the architecture of each output. the ability to configure each output independently permits users to tailor the configuration of the P3Z22V10 to the precise requirements of their designs.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 2, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell of the P3Z22V10 is determined by the two EEPROM bits controlling these multiplexers. These bits determine output polarity, and output type (registered or non-registered). Equivalent circuits for the macrocell configurations are illustrated in Figure 3.

Output type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register will be set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear term will set Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Program/Erase Cycles

The P3Z22V10 is 100% testable, erases/programs in seconds, and guarantees 1000 program/erase cycles.

Output Polarity

Each macrocell can be configured to implement Active-High or Active-Low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is driven into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically FALSE and the I/O will function as a dedicated input.

Register Feedback Select

When the I/O macrocell is configured to implement a registered function (S1 = 0) (Figures 3a or 3b), the feedback signal to the AND array is taken from the $\overline{Q}$ output.

Bi-directional I/O Select

When configuring an I/O macrocell to implement a combinatorial function (S1 = 1) (Figures 3c or 3d), the feedback signal is taken from the I/O pin. In this case, the pin can be used as a dedicated input, a dedicated output, or a bi-directional I/O.

Power-On Reset

To ease system initialization, all flip-flops will power-up to a reset condition and the Q output will be low. The actual output of the P3Z22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic.

Design Security

The P3Z22V10 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set, it is impossible to verify (read) or program the P3Z22V10 until the entire device has first been erased with the bulk-erase function.

TotalCMOS™ Design Technique for Fast Zero Power

Philips is the first to offer a TotalCMOS™ SPLD, both in process technology and design technique. Philips employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Philips to offer SPLDs which are both high performance and low power, breaking the paradigm that to have low power, you must accept low performance. Refer to Figure 4 and Table 1 showing the I_{DD} vs. Frequency of our P3Z22V10 TotalCMOS™ SPLD.

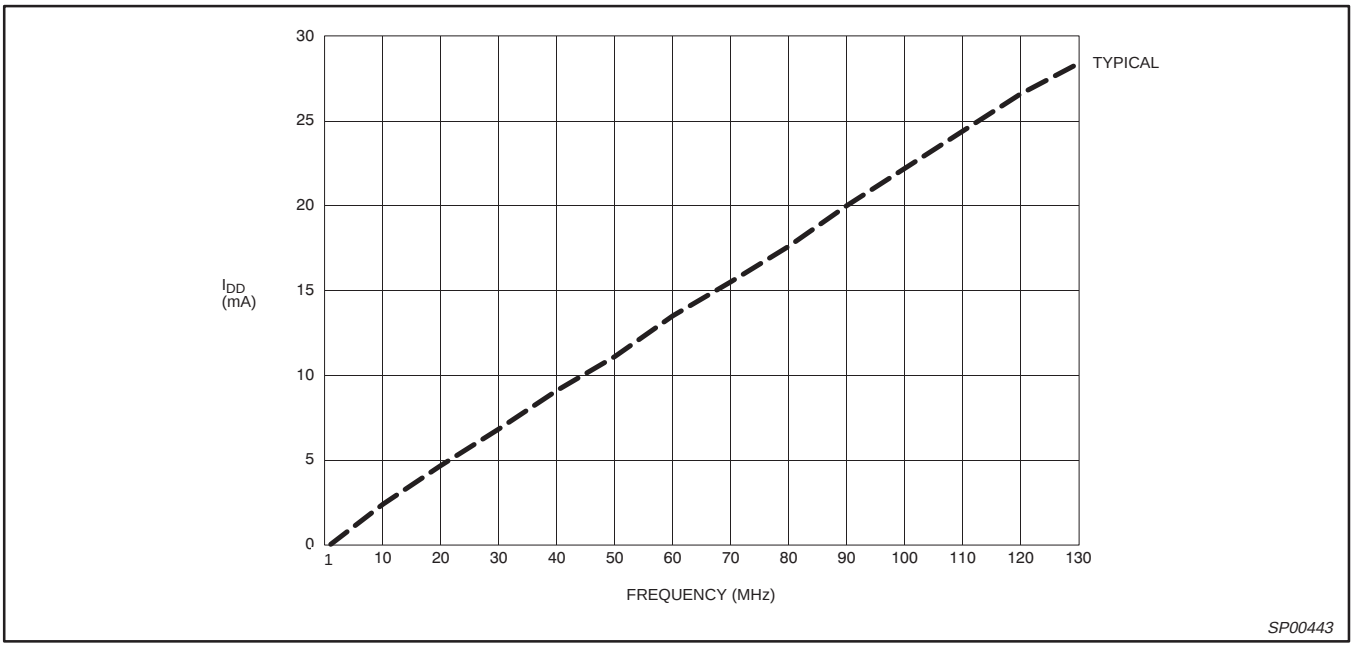


Figure 4. Typical I_{DD} vs. Frequency @ V_{DD} = 3.3V, 25°C (10-bit counter)

Table 1. Typical I_{DD} vs. Frequency

V_{DD} = 3.3V@25°C

FREQ (MHz)	1	10	20	30	40	50	60	70	80	90	100	110	120	130
Typical I_{DD} (mA)	0.2	1.5	3.0	4.5	6.0	7.4	8.9	10.4	11.8	13.2	14.5	15.8	17.0	18.2

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
V_{DD}	Supply voltage	–0.5	4.6	V
V_I	Input voltage	–0.5	5.5[2]	V
V_{OUT}	Output voltage	–0.5	5.5[2]	V
I_{IN}	Input current	–30	30	mA
I_{OUT}	Output current	–100	100	mA
T_R	Allowable thermal rise ambient to junction	0	75	°C
T_J	Junction temperature range	–40	150	°C
T_{STG}	Storage temperature range	–65	150	°C

NOTES:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. Except F7, where max = V_{DD} + 0.5V.

OPERATING RANGE

PRODUCT GRADE	TEMPERATURE	VOLTAGE
Commercial	0 to +70°C	3.3 ± 10% V
Industrial	–40 to +85°C	3.3 ± 10% V

DC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICES

Commercial: $0°C \le T_{amb} \le +70°C$; $3.0 \le V_{DD} \le 3.6V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
V_{IL}	Input voltage low	V_{DD} = 3.0V			0.8	V
V_{IH}	Input voltage high	V_{DD} = 3.6V	2			V
V_I	Input clamp voltage	V_{DD} = 3.0V; I_{IN} = –18mA			–1.2	V
V_{OL}	Output voltage low	V_{DD} = 3.0V; I_{OL} = 8mA			0.5	V
V_{OH}	Output voltage high	V_{DD} = 3.0V; I_{OH} = –4mA	2.4			V
I_I	Input leakage current	V_{IN} = 0 to V_{DD}	–10		10	µA
		V_{IN} = V_{DD} to 5.5V[2]	–10		10	
I_{OZ}	3-Stated output leakage current	V_{IN} = 0 to V_{DD}	–10		10	µA
		V_{IN} = V_{DD} to 5.5V[2]	–10		10	
I_{DDQ}	Standby current	V_{DD} = 3.6V; T_{amb} = 0°C		25	45	µA
I_{DDD} [1]	Dynamic current	V_{DD} = 3.6V; T_{amb} = 0°C @ 1MHz		.5	2	mA
		V_{DD} = 3.6V; T_{amb} = 0°C @ 50MHz		10	15	mA
I_{SC}	Short circuit output current	1 pin/time for no longer than 1 second	–15		–100	mA
C_{IN}	Input pin capacitance	T_{amb} = 25°C; f = 1MHz			8	pF
C_{CLK}	Clock input capacitance	T_{amb} = 25°C; f = 1MHz	5		12	pF
$C_{I/O}$	I/O pin capacitance	T_{amb} = 25°C; f = 1MHz			10	pF

NOTES:
1. These parameters measured with a 10-bit up counter, with all outputs enabled and unloaded. Inputs are tied to V_{DD} or ground. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where current may be affected.
2. Does not apply to F7.

AC ELECTRICAL CHARACTERISTICS FOR COMMERCIAL GRADE DEVICES

Commercial: $0°C \le T_{amb} \le +70°C$; $3.0 \le V_{DD} \le 3.6V$

SYMBOL	PARAMETER	–B		–D		UNIT
		MIN.	MAX.	MIN.	MAX.	
t_{PD}	Input or feedback to non-registered output		15		10	ns
t_{SU}	Setup time from input, feedback or SP to Clock	4.5		3.5		ns
t_{CO}	Clock to output		10		9	ns
t_{CF}	Clock to feedback[1]		6		4.5	ns
t_H	Hold time		0		0	ns
t_{AR}	Asynchronous Reset to registered output		17		17	ns
t_{ARW}	Asynchronous Reset width	5		5		ns
t_{ARR}	Asynchronous Reset recovery time		6		6	ns
t_{SPR}	Synchronous Preset recovery time		6		6	ns
t_{WL}	Width of Clock LOW	3		3		ns
t_{WH}	Width of Clock HIGH	3		3		ns
t_R	Input rise time		20		20	ns
t_F	Input fall time		20		20	ns
f_{MAX1}	Maximum internal frequency[2] $(1/t_{SU} + t_{CF})$	95		125		MHz
f_{MAX2}	Maximum external frequency[1] $(1/t_{SU} + t_{CO})$	69		80		MHz
f_{MAX3}	Maximum clock frequency[1] $(1/t_{WL} + t_{WH})$	167		167		MHz
t_{EA}	Input to Output Enable		9		9	ns
t_{ER}	Input to Output Disable		9		9	ns
Capacitance						
C_{IN}	Input pin capacitance		10		10	pF
C_{OUT}	Output capacitance		10		10	pF

NOTES:
1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
2. These parameters measured with a 10-bit up counter, with all outputs enabled and unloaded. Inputs are tied to V_{DD} or ground. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

DC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICES

Industrial: $-40°C \le T_{amb} \le +85°C$; $3.0 \le V_{DD} \le 3.6V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
V_{IL}	Input voltage low	V_{DD} = 3.0V			0.8	V
V_{IH}	Input voltage high	V_{DD} = 3.6V	2			V
V_I	Input clamp voltage	V_{DD} = 3.0V; I_{IN} = –18mA			–1.2	V
V_{OL}	Output voltage low	V_{DD} = 3.0V; I_{OL} = 8mA			0.5	V
V_{OH}	Output voltage high	V_{DD} = 3.0V; I_{OH} = –4mA	2.4			V
I_I	Input leakage current	V_{IN} = 0 to V_{DD}	–10		10	µA
		V_{IN} = V_{DD} to 5.5V[2]	–10		10	µA
I_{OZ}	3-Stated output leakage current	V_{IN} = 0 to V_{DD}	–10		10	µA
		V_{IN} = V_{DD} to 5.5V[2]	–10		10	µA
I_{DDQ}	Standby current	V_{DD} = 3.6V; T_{amb} = –40°C		30	45	µA
I_{DDD} [1]	Dynamic current	V_{DD} = 3.6V; T_{amb} = –40°C @ 1MHz		.5	3	mA
		V_{DD} = 3.6V; T_{amb} = –40°C @ 50MHz		10	20	mA
I_{SC}	Short circuit output current	1 pin/time for no longer than 1 second	–15		–100	mA
C_{IN}	Input pin capacitance	T_{amb} = 25°C; f = 1MHz			8	pF
C_{CLK}	Clock input capacitance	T_{amb} = 25°C; f = 1MHz	5		12	pF
$C_{I/O}$	I/O pin capacitance	T_{amb} = 25°C; f = 1MHz			10	pF

NOTES:
1. These parameters measured with a 10-bit up counter, with all outputs enabled and unloaded. Inputs are tied to V_{DD} or ground. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where current may be affected.
2. Does not apply to F7.

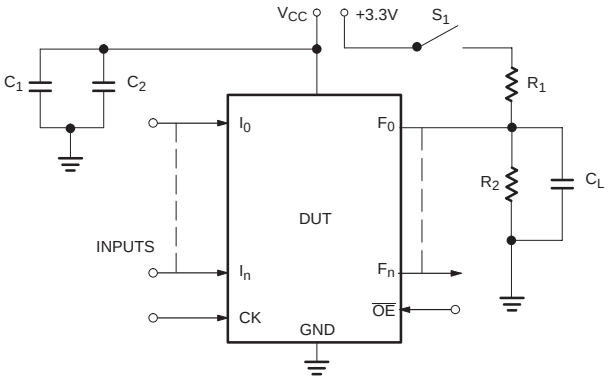
AC ELECTRICAL CHARACTERISTICS FOR INDUSTRIAL GRADE DEVICES

Industrial: $-40°C \le T_{amb} \le +85°C$; $3.0 \le V_{DD} \le 3.6V$

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN.	MAX.	
t_{PD}	Input or feedback to non-registered output		15	ns
t_{SU}	Setup time from input, feedback or SP to Clock	5		ns
t_{CO}	Clock to output		10.5	ns
t_{CF}	Clock to feedback[1]		6	ns
t_H	Hold time		0	ns
t_{AR}	Asynchronous Reset to registered output		17	ns
t_{ARW}	Asynchronous Reset width	5		ns
t_{ARR}	Asynchronous Reset recovery time		6	ns
t_{SPR}	Synchronous Preset recovery time		6	ns
t_{WL}	Width of Clock LOW	3		ns
t_{WH}	Width of Clock HIGH	3		ns
t_R	Input rise time		20	ns
t_F	Input fall time		20	ns
f_{MAX1}	Maximum internal frequency[2] $(1/t_{SU} + t_{CF})$	91		MHz
f_{MAX2}	Maximum external frequency[1] $(1/t_{SU} + t_{CO})$	65		MHz
f_{MAX3}	Maximum clock frequency[1] $(1/t_{WL} + t_{WH})$	167		MHz
t_{EA}	Input to Output Enable		11	ns
t_{ER}	Input to Output Disable		11	ns
Capacitance				
C_{IN}	Input pin capacitance		10	pF
C_{OUT}	Output capacitance		12	pF

NOTES:
1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
2. These parameters measured with a 10-bit up counter, with all outputs enabled and unloaded. Inputs are tied to V_{DD} or ground. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

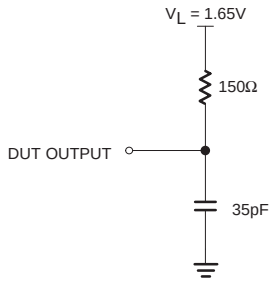
TEST LOAD CIRCUIT



NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.
R_1 = 300Ω, R_2 = 300Ω, C_L = 35pF.

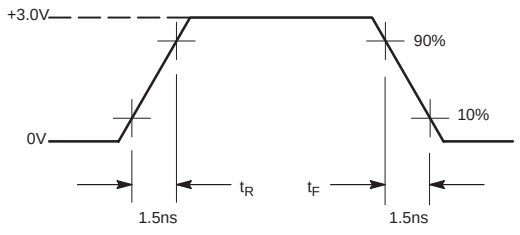
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THEVENIN EQUIVALENT



SP00479A

VOLTAGE WAVEFORM

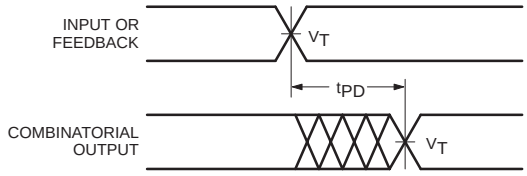


MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

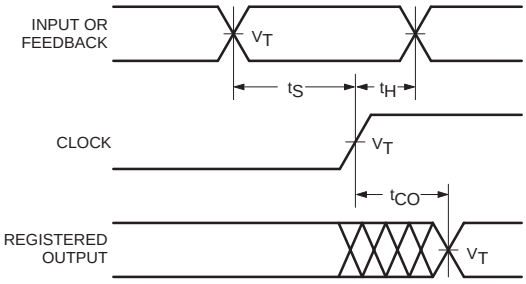
Input Pulses

SP00368

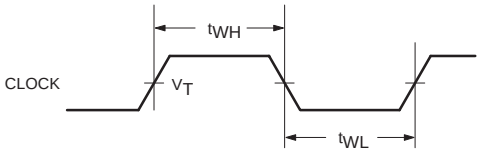
SWITCHING WAVEFORMS



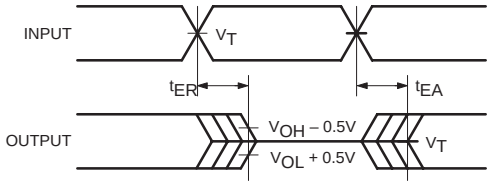
Combinatorial Output



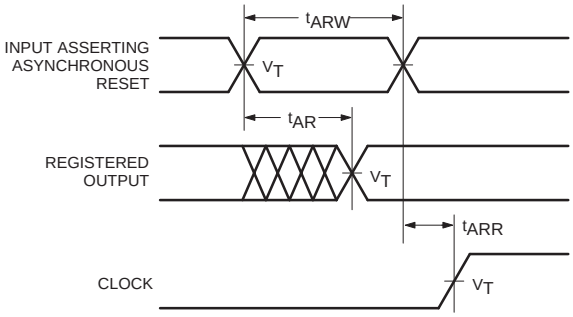
Registered Output



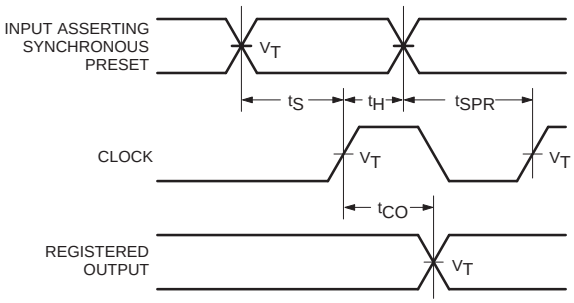
Clock Width



Input to Output Disable/Enable



Asynchronous Reset

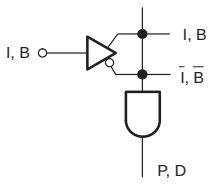


Synchronous Preset

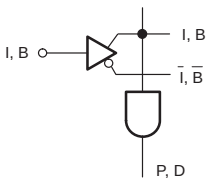
NOTES:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 2.0ns max.

SP00065

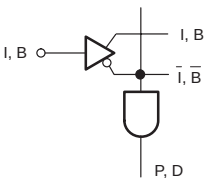
"AND" ARRAY – (I, B)



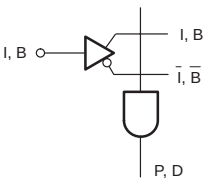
STATE	CODE
INACTIVE[1]	O



STATE	CODE
TRUE	H



STATE	CODE
COMPLEMENT	L

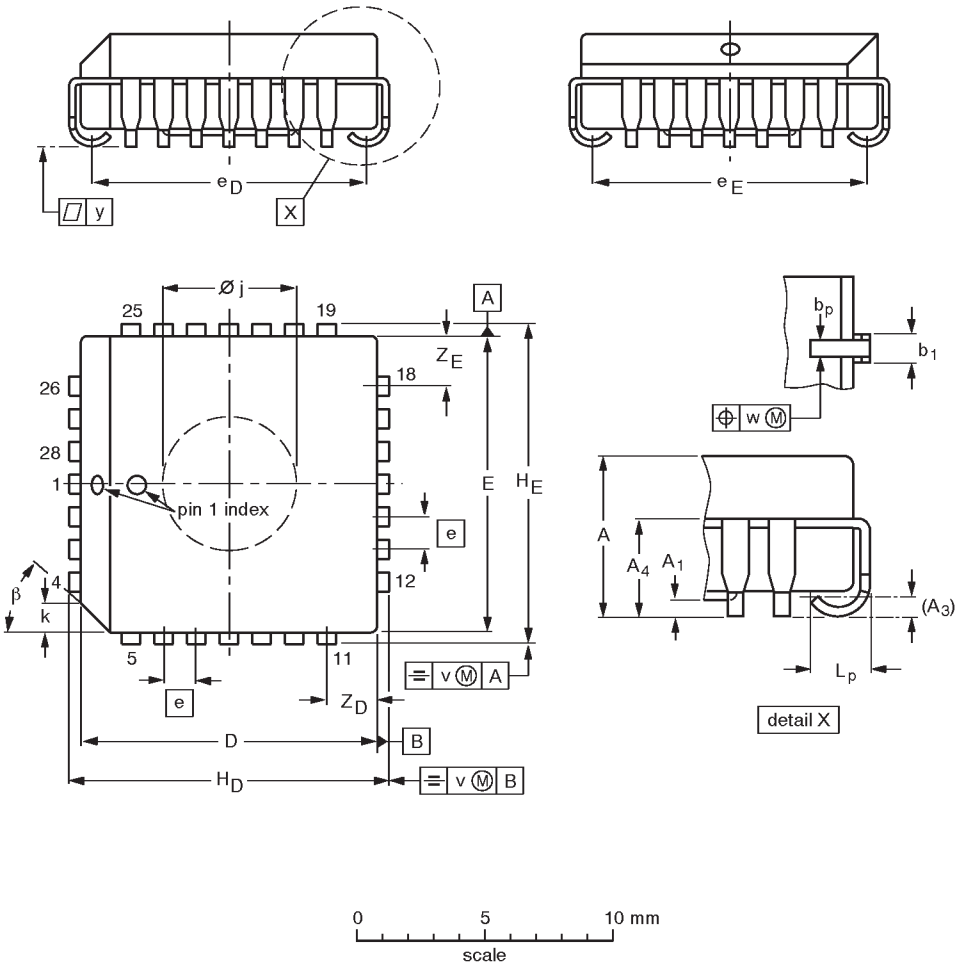


STATE	CODE
DON'T CARE	—

SP00008

NOTE:
1. This is the initial state.

PLCC28: plastic leaded chip carrer; 28 leads; pedestal SOT261-3



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

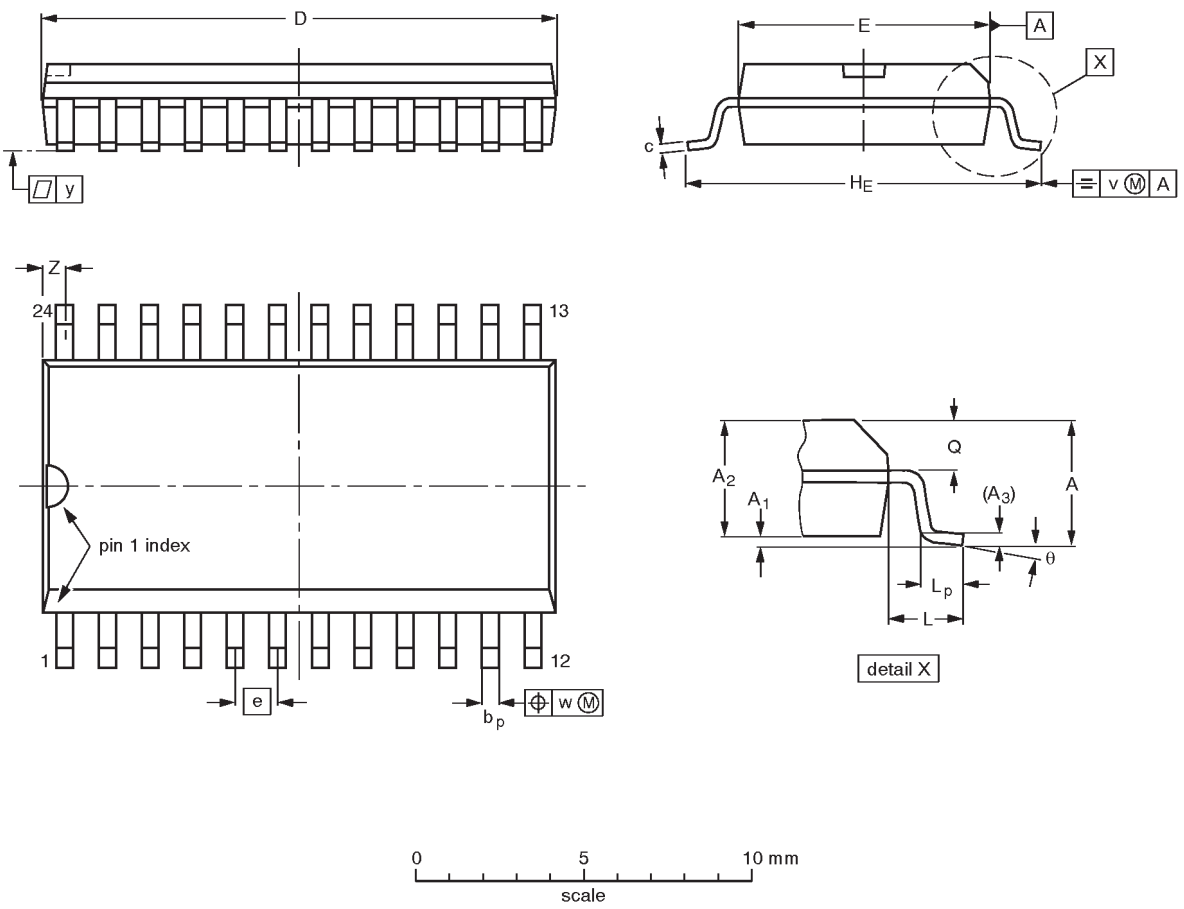
UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	$Ø_j$	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.13	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	5.69 5.54	1.44 1.02	0.18	0.18	0.10	2.06	2.06	45°
inches	0.180 0.165	0.005	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.224 0.218	0.057 0.040	0.007	0.007	0.004	0.081	0.081	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-3		MO-047AB				~~92-11-17~~ 95-02-25

SO24: plastic small outline package; 24 leads; body width 7.5 mm SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

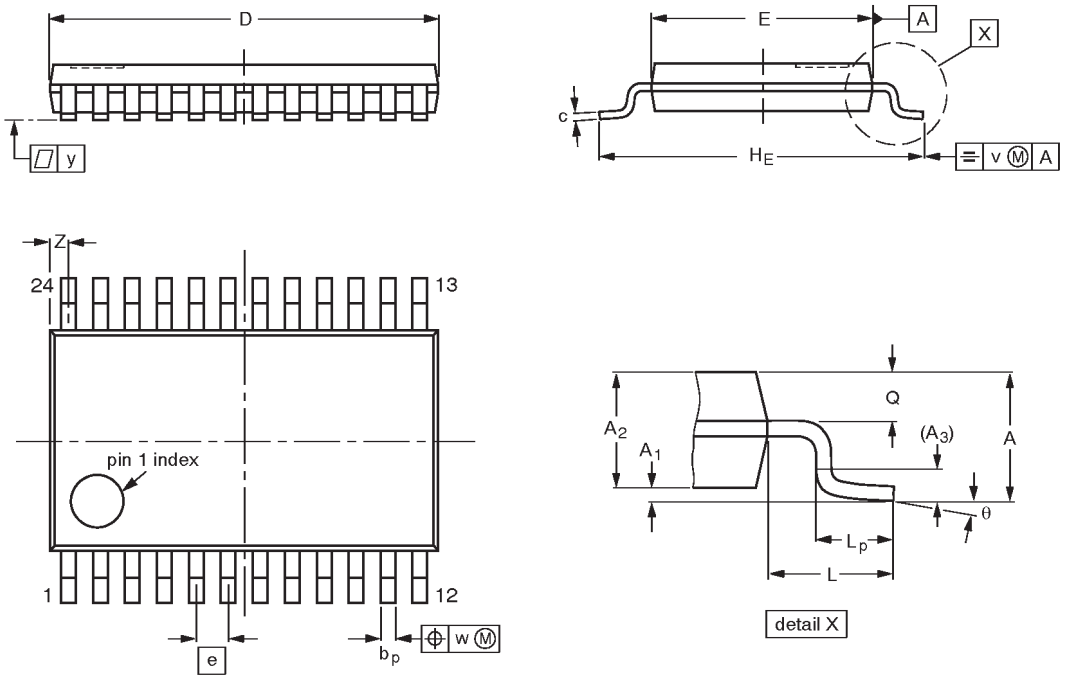
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

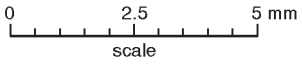
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm SOT355-1





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04

3V zero power, TotalCMOS™, universal PLD device

P3Z22V10

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Data Sheet Identification	Product Status	Definition
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