

intersil

RFP45N02L, RF1S45N02L, RF1S45N02LSM

45A, 20V, 0.022 Ohm, N-Channel
Logic Level Power MOSFETs

May 1997

Features

- 45A, 20V
- $r_{DS(ON)} = 0.022\Omega$
- *Temperature Compensating* PSpice Model
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFP45N02L	TO-220AB	FP45N02L
RF1S45N02L	TO-262AA	F45N02L
RF1S45N02LSM	TO-263AB	F45N02L

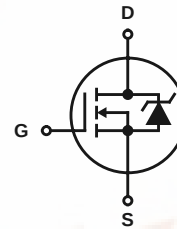
NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, e.g. RF1S45N02LSM9A.

Description

The RFP45N02L, RF1S45N02L, and RF1S45N02LSM are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

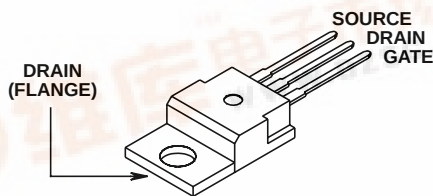
Formerly developmental type TA49243.

Symbol

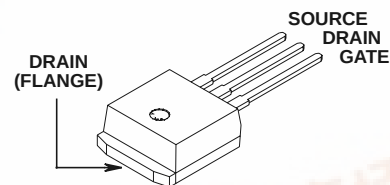


Packaging

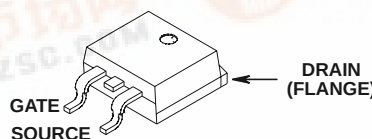
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



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Absolute Maximum Ratings $T_C = 25^{\circ}\text{C}$ Unless Otherwise Specified

	RFP45N02L, RF1S45N02L, RF1S45N02LSM	UNITS
Drain to Source Voltage	V_{DSS}	20 V
Drain to Gate Voltage	V_{DGR}	20 V
Gate to Source Voltage	V_{GS}	± 10 V
Drain Current		
Continuous	I_D	45 A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve
Power Dissipation	P_D	90 W
Derate Above 25°C		0.606 W/ $^{\circ}\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175 $^{\circ}\text{C}$
Soldering Temperature of Leads for 10s	T_L	260 $^{\circ}\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	20	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{V}, V_{GS} = 0\text{V}$	-	-	1	μA
		$T_C = 150^{\circ}\text{C}$			50	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10\text{V}$	-	-	± 100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 45\text{A}, V_{GS} = 5\text{V}$	-	-	0.022	Ω
Turn-On Time	t_{ON}	$V_{DD} = 15\text{V}, I_D \cong 45\text{A}, R_L = 0.33\Omega, V_{GS} = 5\text{V}, R_{GS} = 5\Omega$	-	-	260	ns
Turn-On Delay Time	$t_{d(ON)}$		-	15	-	ns
Rise Time	t_r		-	160	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	20	-	ns
Fall Time	t_f		-	20	-	ns
Turn-Off Time	t_{OFF}		-	-	60	ns
Total Gate Charge	$Q_g(TOT)$	$V_{GS} = 0\text{V to } 10\text{V}$	-	50	60	nC
Gate Charge at 5V	$Q_g(5)$	$V_{GS} = 0\text{V to } 5\text{V}$				
Threshold Gate Charge	$Q_g(TH)$	$V_{GS} = 0\text{V to } 1\text{V}$				
Input Capacitance	C_{ISS}	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	1300	-	pF
Output Capacitance	C_{OSS}		-	724	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	250	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	1.65	$^{\circ}\text{C/W}$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$		-	-	80	$^{\circ}\text{C/W}$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 45\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 45\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

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Typical Performance Curves

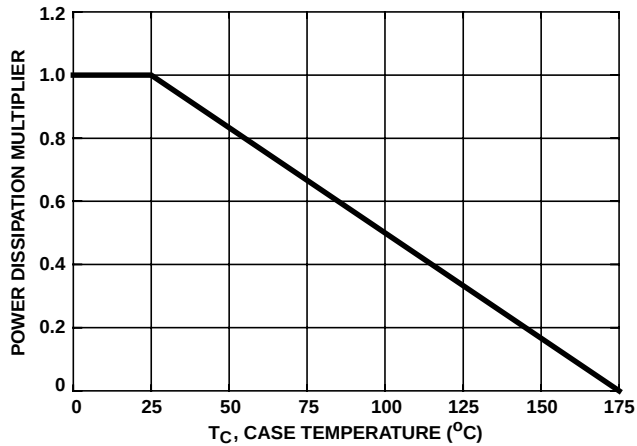


FIGURE 1. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING

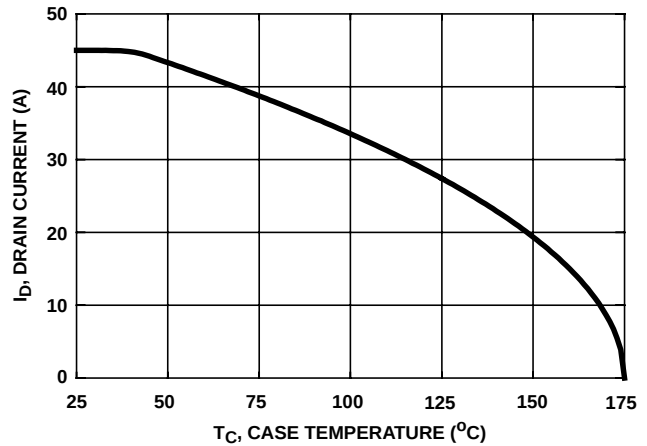


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

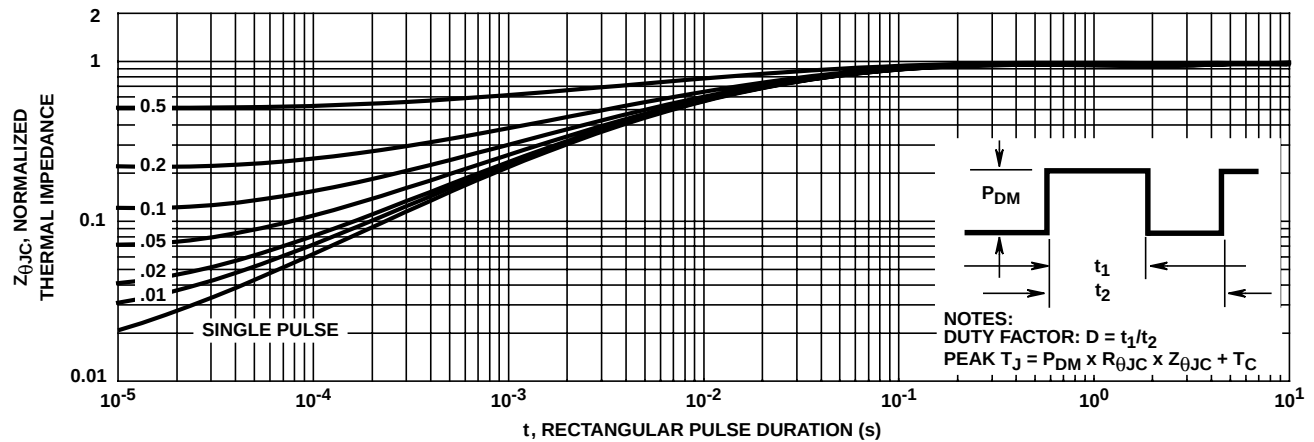


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

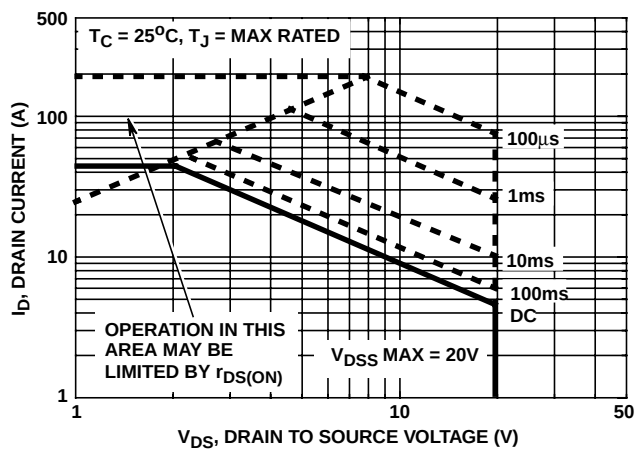


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

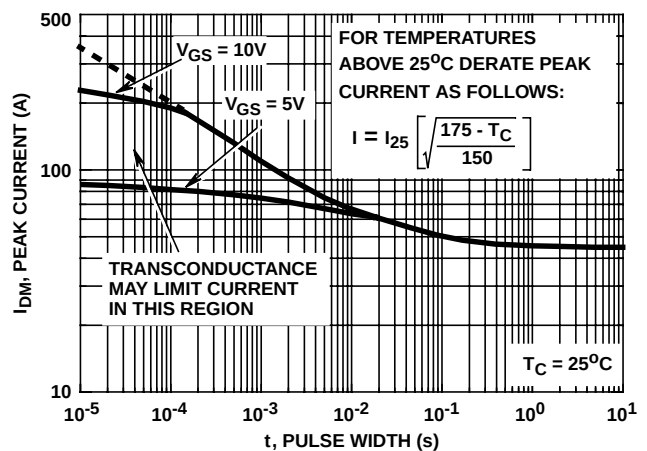
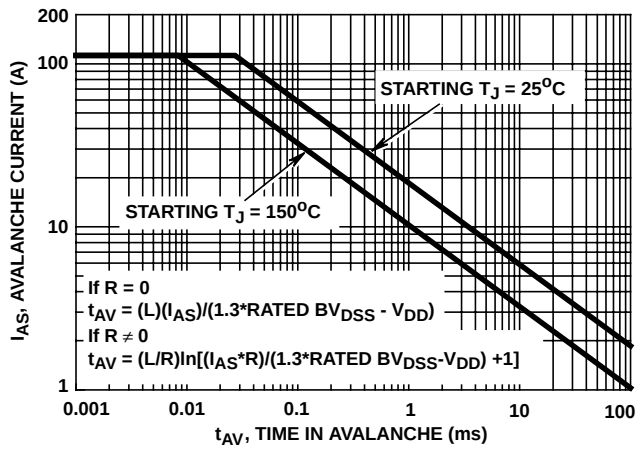


FIGURE 5. PEAK CURRENT CAPABILITY

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Typical Performance Curves (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

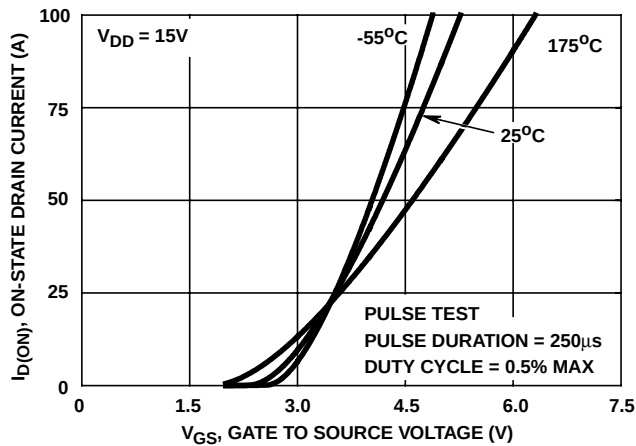


FIGURE 8. TRANSFER CHARACTERISTICS

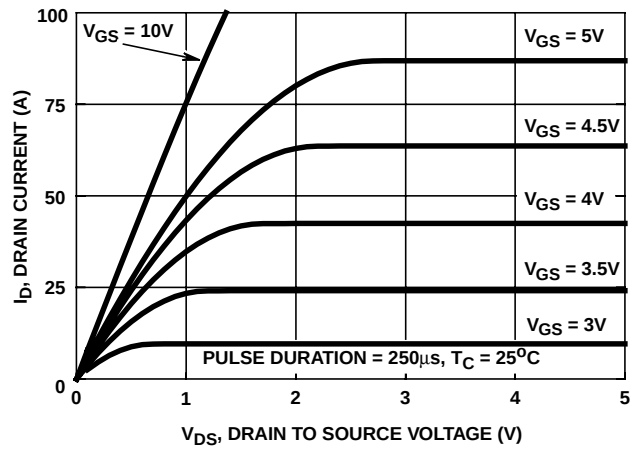


FIGURE 7. SATURATION CHARACTERISTICS

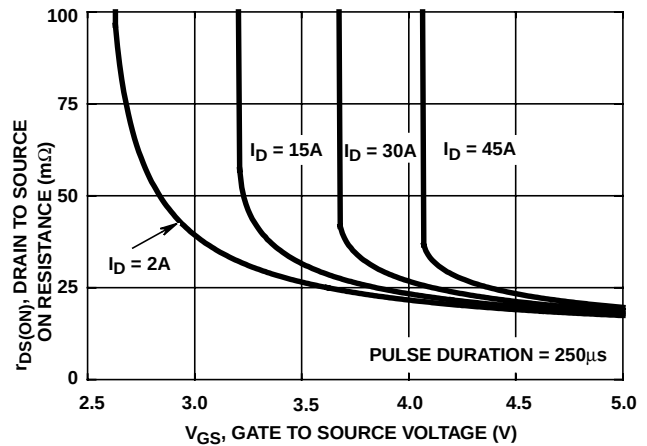


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

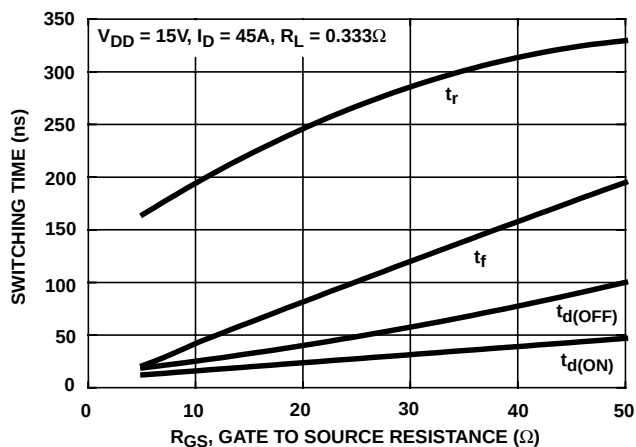


FIGURE 10. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

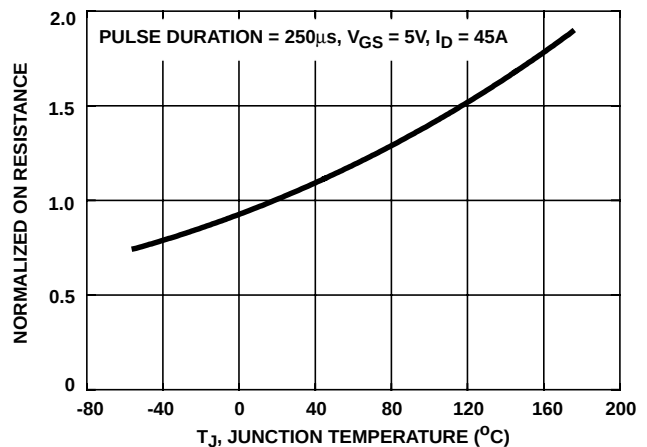


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

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Typical Performance Curves (Continued)

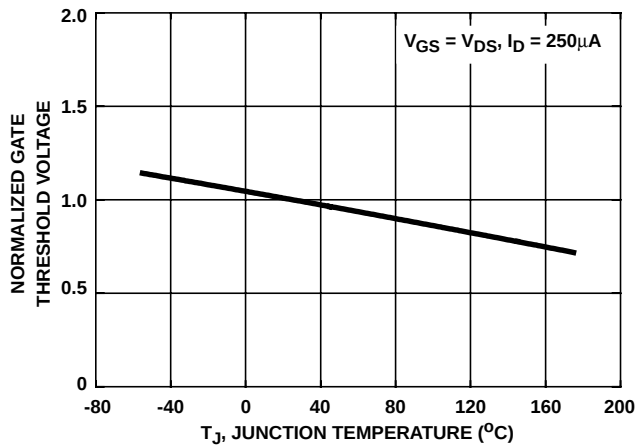


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

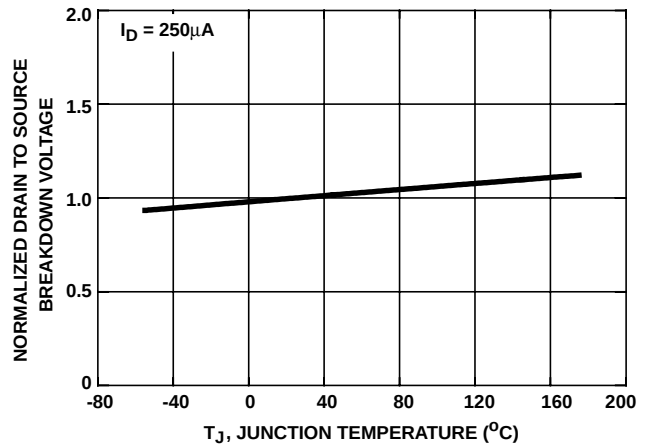


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

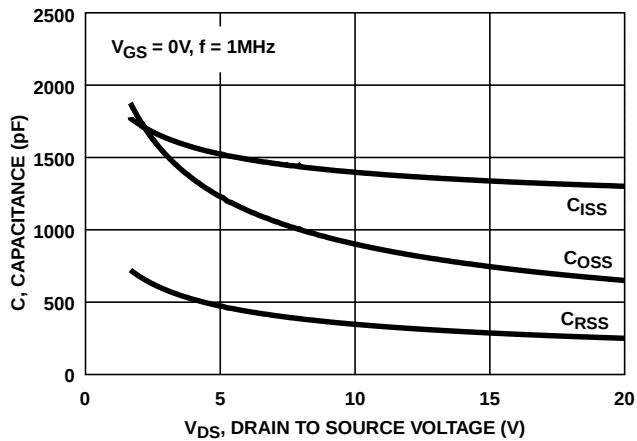
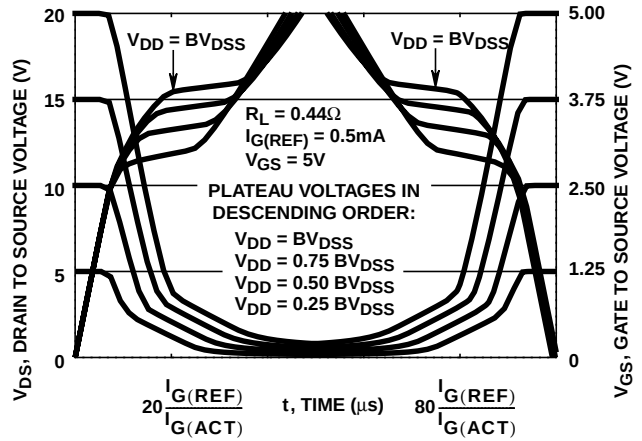


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms



RFP45N02L, RF1S45N02L, RF1S45N02LSM

Temperature Compensated PSPICE Model for the RFP45N02L, RF1S45N02L, RF1S45N02LSM

.SUBCKT RFP45N02L 2 1 3 ; rev 11/22/94

CA 12 8 2.55e-9
CB 15 14 2.64e-9
CIN 6 8 1.05e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.9e-9
LSOURCE 3 7 4.9e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 0.14e-3
RGATE 9 20 0.89
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 10.31e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

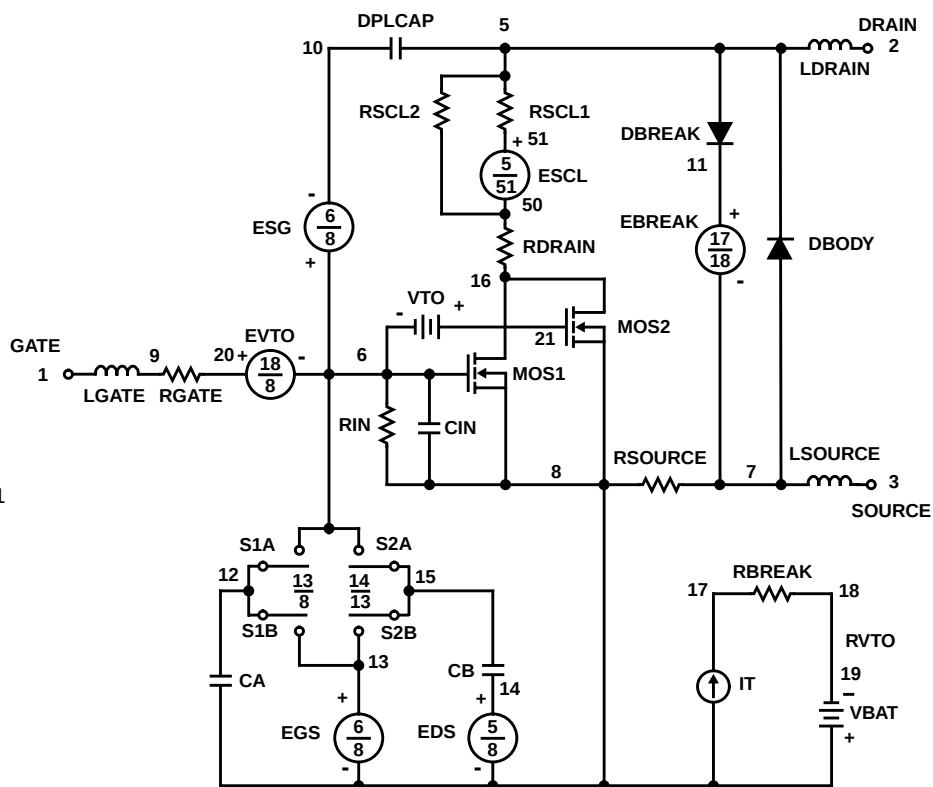
VBAT 8 19 DC 1
VTO 21 6 0.583

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/176,6))}

.MODEL DBDMOD D (IS = 3.61e-13 RS = 5.06e-3 TRS1 = 3.05e-3 TRS2 = 7.57e-6 CJO = 2.0e-9 TT = 2.18e-8)
.MODEL DBKMOD D (RS = 1.66e-1 TRS1 = -2.97e-3 TRS2 = 7.57e-6)
.MODEL DPLCAPMOD D (CJO = 1.25e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.313 KP = 53.82 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 8.95e-4 TC2 = -1e-7)
.MODEL RDSMOD RES (TC1 = 3.82e-3 TC2 = 1.17e-5)
.MODEL RSCLMOD RES (TC1 = 2.03e-3 TC2 = 0.45e-5)
.MODEL RVTOMOD RES (TC1 = -2.27e-3 TC2 = -5.75e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.82 VOFF = -2.82)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.82 VOFF = -4.82)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.67 VOFF = 2.33)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.33 VOFF = -2.67)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.



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Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
Taiwan Limited
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029