

P4C1024 HIGH SPEED 128K x 8 CMOS STATIC RAM



FEATURES

- High Speed (Equal Access and Cycle Times)
 - 15/17/20/25/35 ns (Commercial)
 - 20/25/35/45 ns (Industrial)
- Single 5 Volts $\pm 10\%$ Power Supply
- Easy Memory Expansion Using $\overline{CE}_1$, CE_2 and $\overline{OE}$ Inputs
- Common Data I/O
- Three-State Outputs
- Fully TTL Compatible Inputs and Outputs
- Advanced CMOS Technology
- Fast t_{OE}
- Automatic Power Down
- Packages
 - 32-Pin 300 mil DIP and SOJ
 - 32-Pin 400 mil SOJ



DESCRIPTION

The P4C1024 is a 1,048,576-bit high-speed CMOS static RAM organized as 128Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V $\pm 10\%$ tolerance power supply.

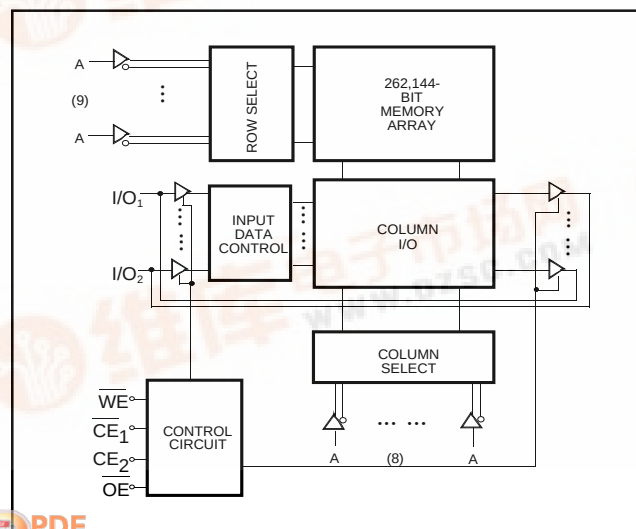
Access times of 15 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P4C1024 is a member of a family of PACE RAM™ products offering fast access times.

The P4C1024 device provides asynchronous operations with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{16} . Reading is accomplished by device selection ($\overline{CE}_1$ low and CE_2 high) and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}_1$ or $\overline{OE}$ is HIGH or $\overline{WE}$ or CE_2 is LOW.

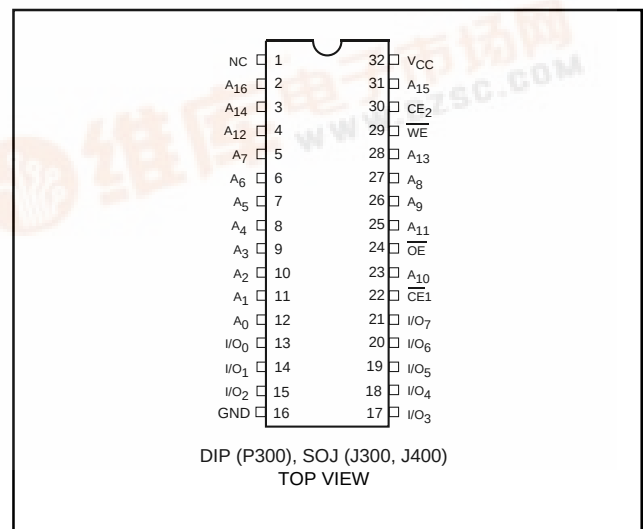
Package options for the P4C1024 include 32-pin 300 mil DIP and SOJ packages as well as 400 mil SOJ.



FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION





RECOMMENDED OPERATING TEMPERATURE & SUPPLY VOLTAGE

Temperature Range (Ambient)	Supply Voltage
Commercial (0°C to 70°C)	$4.5V \leq V_{CC} \leq 5.5V$
Industrial (-40°C to 85°C)	$4.5 \leq V_{CC} \leq 5.5V$

MAXIMUM RATINGS

Stresses greater than those listed can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Maximum Ratings for extended periods can adversely affect device reliability.

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage with Respect to GND	-0.5	7.0	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5	$V_{CC} + 0.5$	V
T_A	Operating Ambient Temperature	-55	125	°C
S_{TG}	Storage Temperature	-65	150	°C
I_{OUT}	Output Current into Low Outputs		25	mA
I_{LAT}	Latch-up Current	>200		mA

DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{OH}	Output High Voltage ($I/O_0 - I/O_7$)	$I_{OH} = -4mA$, $V_{CC} = 4.5V$	2.4		V
V_{OL}	Output Low Voltage ($I/O_0 - I/O_7$)	$I_{OL} = 8 mA$ $I_{OL} = 10 mA$		0.4 0.5	V V
V_{IH}	Input High Voltage		2.2	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{LI}	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$ Ind'l. Com'l.	-10 -5	+10 +5	μA
I_{LO}	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ Ind'l. $\overline{CE}_1 \geq V_{IH}$ or $CE_2 \leq V_{IL}$ Com'l.	-10 -5	+10 +5	μA
I_{OS}	Output Short-Circuit Current	$V_{OUT} = GND$, $V_{CC} = Max$ (Single output) not to exceed 30 second duration		-350	mA
I_{SB1}	V_{CC} Current CMOS Standby Current (CMOS Input Levels)	$V_{CC} = 5.5V$, $I_{OUT} = 0 mA$ $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$		20 (Standard)	mA

CAPACITANCES

($V_{CC} = 5.0V$, $T_A = 25^\circ C$, $f = 1.0\text{ MHz}$)

Symbol	Parameter	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	10	pF

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range	-15	-17	-20	-25	-35	-45	Unit
I_{CC}	Dynamic Operating Current	Commercial Industrial	190 N/A	180 N/A	160 175	150 165	145 160	N/A 155	mA mA

*Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate.

The device is continuously enabled for writing, i.e., $CE_2 \geq V_{IH}$ (min), $\overline{CE}_1$, and $\overline{WE} \leq V_{IL}$ (max). Switching inputs are 0V and 3V.

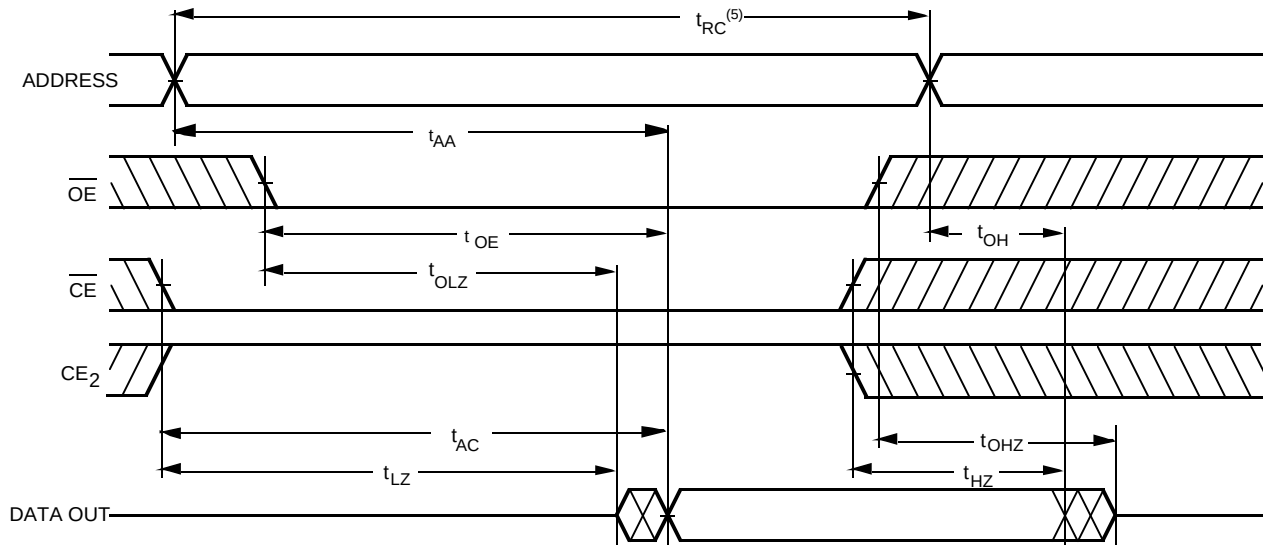
AC ELECTRICAL CHARACTERISTICS - READ CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	-15		-17		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		17		20		25		35		45		ns
t_{AA}	Address Access Time		15		17		20		25		35		45	ns
t_{AC}	Chip Enable Access Time		15		17		20		25		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	3		3		3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		8		9		9		11		15		20	ns
t_{OE}	Output Enable Low to Data Valid		6		7		9		10		15		20	ns
t_{OLZ}	Output Enable Low to Low Z	0		0		0		0		0		0		ns
t_{OHZ}	Output Enable High to High Z		6		7		9		11		15		20	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		12		15		20		20		20		25	ns



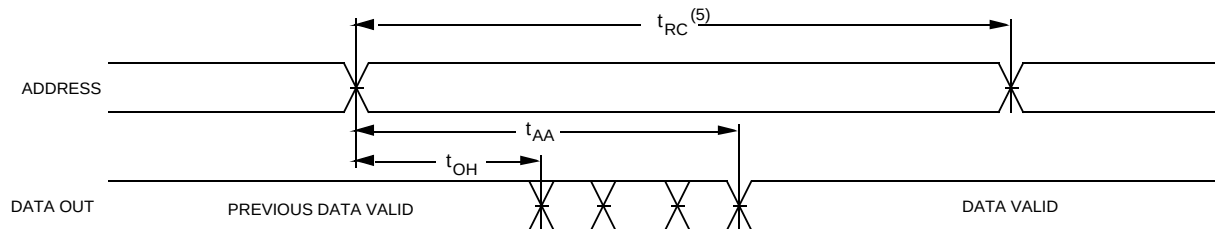
READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)⁽¹⁾



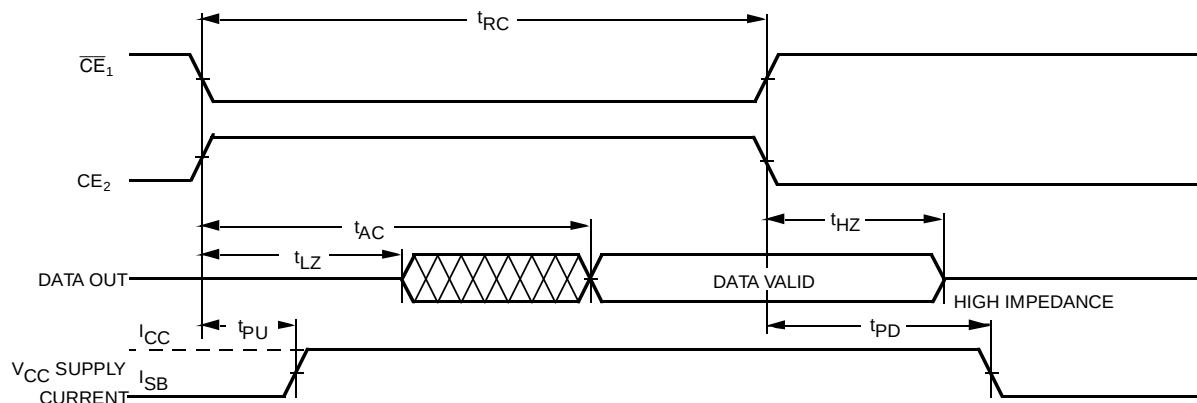
NOTES:

1. $\overline{WE}$ is HIGH for READ cycle.
2. $\overline{CE}_1$ and $\overline{OE}$ is LOW and $\overline{CE}_2$ is HIGH for read cycle.
3. ADDRESS must be valid prior to, or coincident with later of $\overline{CE}_1$ transition LOW or $\overline{CE}_2$ transition HIGH.
4. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure1. This parameter is sampled and not 100% tested.
5. READ Cycle Time is measured from the last valid address to the first transitioning address.

READ CYCLE NO. 2 (ADDRESS CONTROLLED)



READ CYCLE NO. 3 ($\overline{CE}$ CONTROLLED)

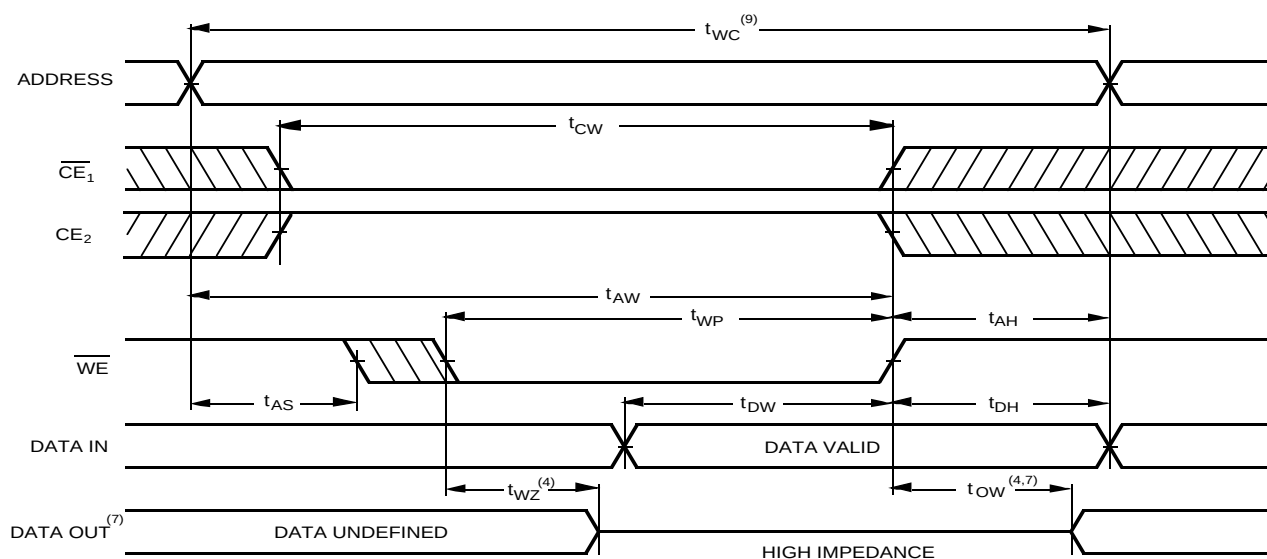


AC CHARACTERISTICS - WRITE CYCLE

(Over Recommended Operating Temperature & Supply Voltage)

Symbol	Parameter	-15		-17		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		17		20		25		35		45		ns
t_{CW}	Chip Enable Time to End of Write	12		13		15		18		22		30		ns
t_{AW}	Address Valid to End of Write	12		13		15		20		25		35		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	12		12		15		18		22		25		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	7		7		8		10		15		20		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		8		8		10		11		15		18	ns
t_{OW}	Output Active from End of Write	3		3		3		3		3		3		ns

WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)⁽⁶⁾

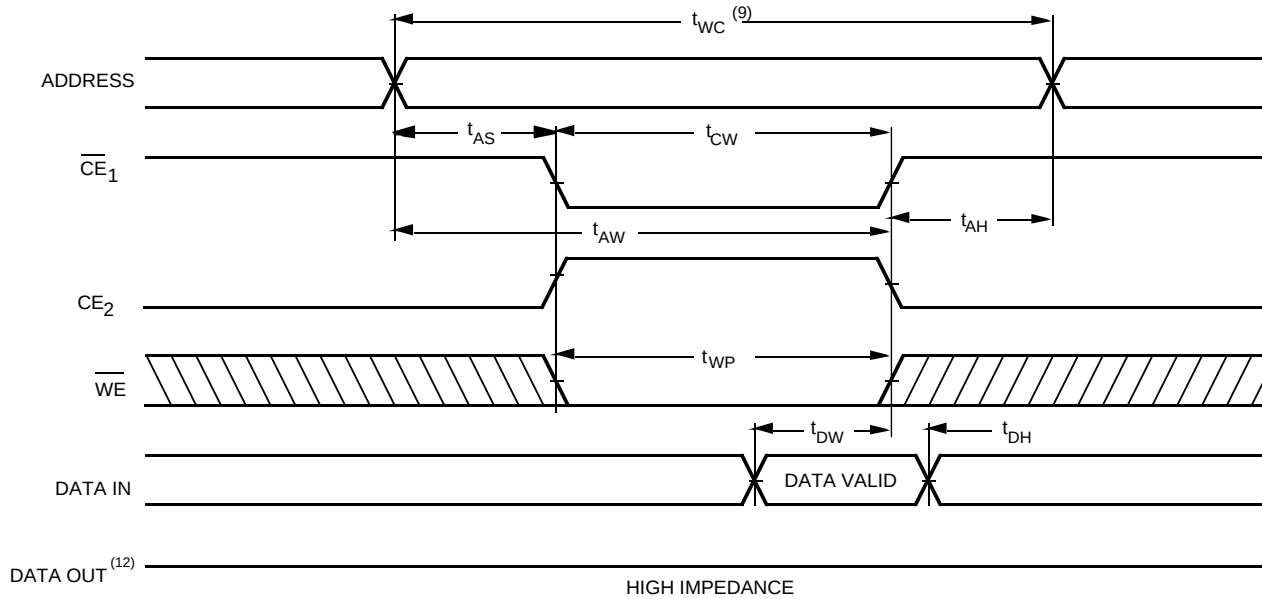


Notes:

6. $\overline{CE}_1$ and $\overline{WE}$ are LOW and CE_2 is HIGH for WRITE cycle.
7. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW} .
8. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
9. Write Cycle Time is measured from the last valid address to the first transitioning address.



TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CE}$ CONTROLLED)⁽⁶⁾



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}$	$\overline{WE}$	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	High Z	Active

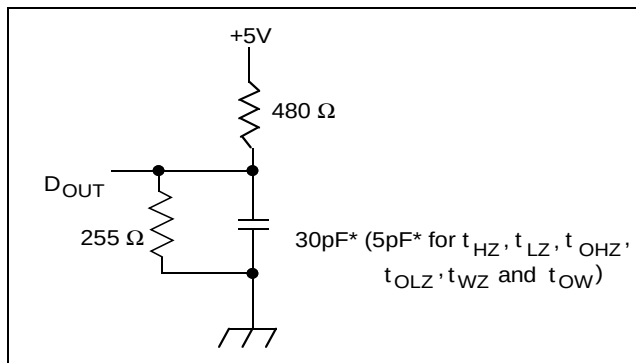


Figure 1. Output Load

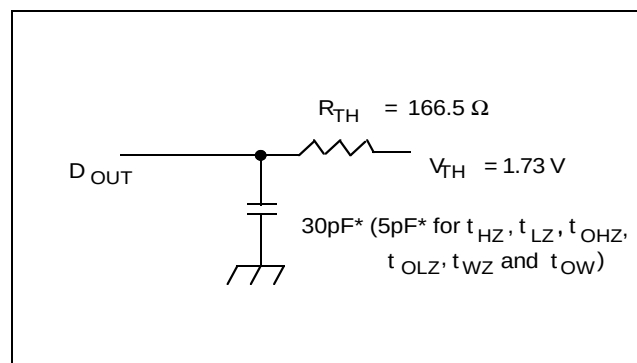


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:

Because of the ultra-high speed of the P4C1024, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 μ F high frequency capacitor is also required between V_{CC} and ground.

To avoid signal reflections, proper termination must be used; for example, a 50 Ω test environment should be terminated into a 50 Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116 Ω resistor must be used in series with D_{OUT} to match 166 Ω (Thevenin Resistance).

PACKAGE SUFFIX

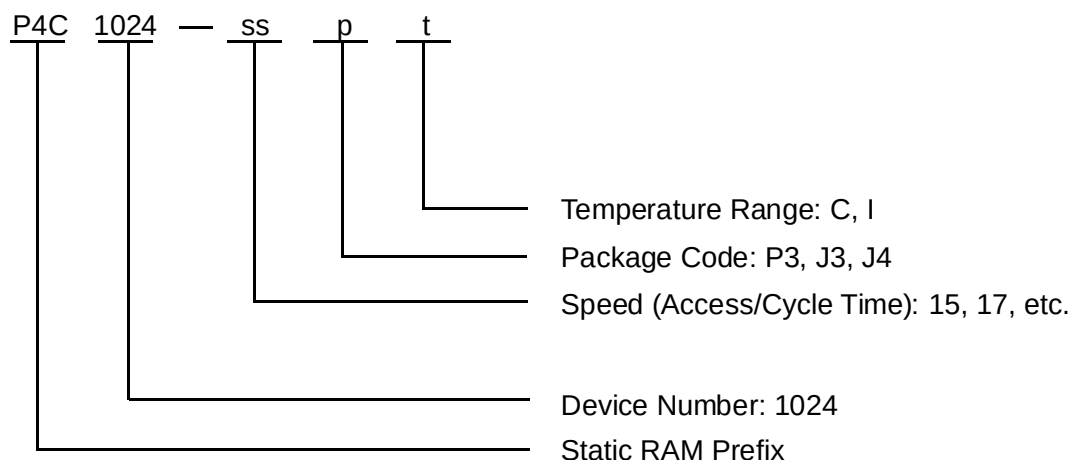
Package Suffix	Description
P3	Plastic DIP, 300 mil wide standard
J3	Plastic SOJ, 300 mil wide standard
J4	Plastic SOJ, 400 mil wide standard

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C
I	Industrial Temperature Range, -40°C to +85°C

ORDERING INFORMATION

Performance Semiconductor's part numbering scheme is as follows:

**SELECTION GUIDE**

The P4C1024 is available in the following temperature, speed and package options.

Temperature Range	Package	Speed (ns)				
		-15	-17	-20	-25	-35
Commercial Temperature	Plastic DIP 300	-15P3C	-17P3C	-20P3C	-25P3C	-35P3C
	Plastic SOJ 300	-15J3C	-17J3C	-20J3C	-25J3C	-35J3C
	Plastic SOJ 400	-15J4C	-17J4C	-20J4C	-25J4C	-35J4C
Industrial Temperature	Plastic DIP 300	N/A	N/A	-20P3I	-25P3I	-35P3I
	Plastic SOJ 300	N/A	N/A	-20J3I	-25J3I	-35J3I
	Plastic SOJ 400	N/A	N/A	-20J4I	-25J4I	-35J4I

N/A = Not Available

