**CMOS IC** 





# 8-Bit Single Chip Microcontroller with the One-Time Programmable PROM

#### **Preliminary**

#### Overview

The LC86P5420 is a CMOS 8-bit single chip microcontroller with one-time PROM for the LC865500 / LC865400 series.

This microcontroller has the function and the pin description of the LC865500 / LC865400 series mask ROM version, and the 20K-byte PROM.

#### **Features**

(1) Option switching by PROM data

The option function of the LC865400 series can be specified by the PROM data.

The LC86P5420 can be checked the functions of the trial pieces using the mass production board.

(2) Internal one-time PROM capacity
 (3) Internal RAM capacity
 512 bytes

Mask ROM version	PROM capacity	RAM capacity
LC865520	20480 bytes	512 bytes
LC865516	16384 bytes	512 bytes
LC865512	12288 bytes	512 bytes
LC865508	8192 bytes	512 bytes
LC865504	4096 bytes	512 bytes
LC865412	12288 bytes	224 bytes
LC865408	8192 bytes	224 bytes
LC865404	4096 bytes	224 bytes

(4) Operating supply voltage
 (5) Instruction cycle time
 (6) Operating temperature
 (7) 4.5V to 6.0V
 (8) 1.0μs to 366μs
 (9) 2.70°C to +70°C

(7) The pin and the package compatible with the LC865400 series mask ROM devices

(8) Applicable mask ROM version : LC865520 / LC865516 / LC865512 / LC865508 / LC865504

LC865412 / LC865408 / LC865404

(9) Factory shipment : DIP42S, QFP48E

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#### Notice for use

The LC86P5420 is provided for the first release and small shipping of the LC865500 / LC865400 series. At using, take notice of the followings.

(1) A point of difference the LC86P5420 and the LC865500 / LC865400 series

Item	LC86P5420	LC865520 / 16 / 12 / 08 / 04 LC865412 / 08 / 04
Operation after reset	The option is specified by degrees	The program is executed from 00H of the
releasing	until 3ms after going to a 'H' level	program counter immediately after going
	to the reset terminal. The program	to a 'H' level to the reset terminal.
	is executed from 00H of the	
	program counter.	
Operating supply	4.5V to 6.0V	2.5V to 6.0V
voltage range (VDD)		
Power dissipation	Refer to 'electrical characteristics' or	n the semiconductor news.

The LC86P5420 functions same as the followings while resetting; LC865520 / 16 / 12 / 08 / 04, LC865412 / 08 / 04.

The LC86P5420 uses 256 bytes that is addressed on 7F00H to 7FFFH in the program memory as the option configulation data area.

•A kind of the option corresopnding of the LC86P5420

A kind of option	Pins, Circuits		Contents of the option				
Input / output form of	Port 0		1. N-channel open drain output				
input / output ports			2. CMOS output				
			1. Pull-up MOS Tr. provided				
			2. Pull-up MOS Tr. not provided				
	Port 1		1. Input	: Programmable pull-up MOS Tr.			
			Output	: N-channel open drain			
			2. Input	: Programmable pull-up MOS Tr.			
		*1	Output	: CMOS			
	Port 3		1. Input	: No Programmable pull-up			
				MOS Tr.			
			Output	: N-channel open drain			
			2. Input	: Programmable pull-up MOS Tr.			
		*1	Output	: CMOS			

<sup>\*1)</sup> Specified in bit

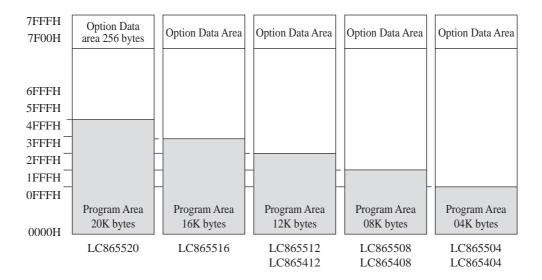
#### (2) Option

The option data is created by the option specified program "SU86K.EXE". The created option data is linked to the program area by the linkage loader "L86K.EXE".

<sup>\*2)</sup> Specified in nibble unit. Pull-up MOS Tr. is not provided in N-channel open drain output port.

#### (3) ROM space

The LC86P5420 and LC865500 / LC865400 series use 256 bytes that is addressed on 7F00H to 7FFFH in the program memory as the option specified data area. These program memory capacity are 20480 bytes that is addressed on 0000H to 4FFFH.



#### (4) Ordering information

- When ordering the identical mask ROM and PROM devices simultaneously.
   Provide an EPROM containing the target memory contents together with the separate order forms for each of the mask ROM and PROM versions.
- 2. When ordering a PROM device.

  Provide an EPROM containing the target memory contents together with an order form.

#### How to use

(1) Create a programming data for LC86P5420

Programming data for EPROM of the LC86P5420 is required.

Debugged evaluation file (EVA file) must be converted to an INTEL-HEX formatted file (HEX file) with file converter program, EVA2HEX.EXE. The HEX file is used as the programming data for the LC86P5420.

#### (2) How to program for the EPROM

The LC86P5420 can be programmed by the EPROM programmer with attachment; W86EP5420D, W86EP5420Q.

• Recommended EPROM programmer

Productor	EPROM programmer
Advantest	R4945, R4944, R4943
Andou	AF-9704
AVAL	PKW-1100, PKW-3000
Minato electronics	MODEL1890A

• "27512 (Vpp=12.5V) Intel high speed programming" mode available. The address must be set to "0000H to 7FFFH" and a jumper (DASEC) must be set to 'OFF' at programming.

- (3) How to use the data security function
  - "Data security" is the disabled function to read the data of the EPROM.

The following is the process in order to execute the data security.

- 1. Set 'ON' the jumper of attachment.
- 2. Program again. Then the EPROM programmer displays the error. The error means normally activity of the data security. It is not a trouble of the EPROM programmer or the LSI.

#### **Notes**

- Data security is not executed when the data of all address have 'FFH' at the sequence 2 above.
- The programming by a sequential operation "BLANK=>PROGRAM=>VERIFY" cannot be executed data security at the sequence 2 above.
- Set 'OFF' to the jumper after executing the data security.

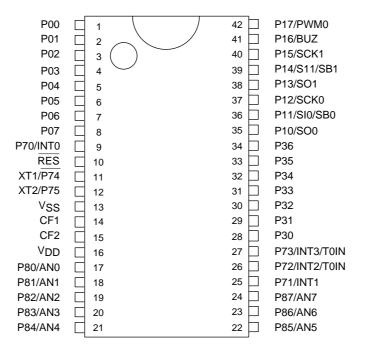
W86EP5420D

# Data security Not data security Not data security Not data security

W86EP5420Q

# **Pin Assignment**

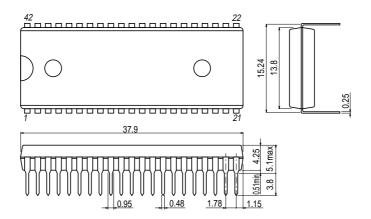
•DIP42S



ILC00019

#### **Package Dimension**

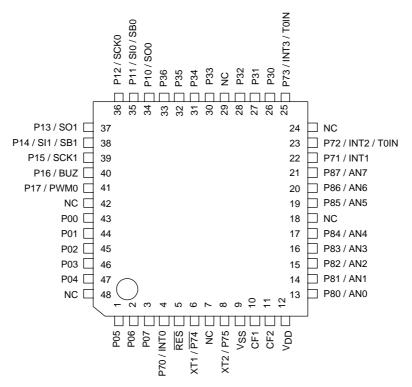
(unit : mm) 3025B



SANYO: DIP-42S(600mil)

#### **Pin Assignment**

•QFP48E

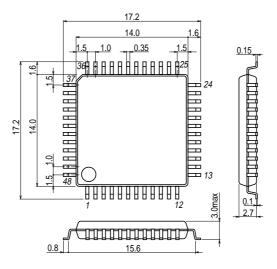


\*NC pin must not connect to anything.

ILC00020

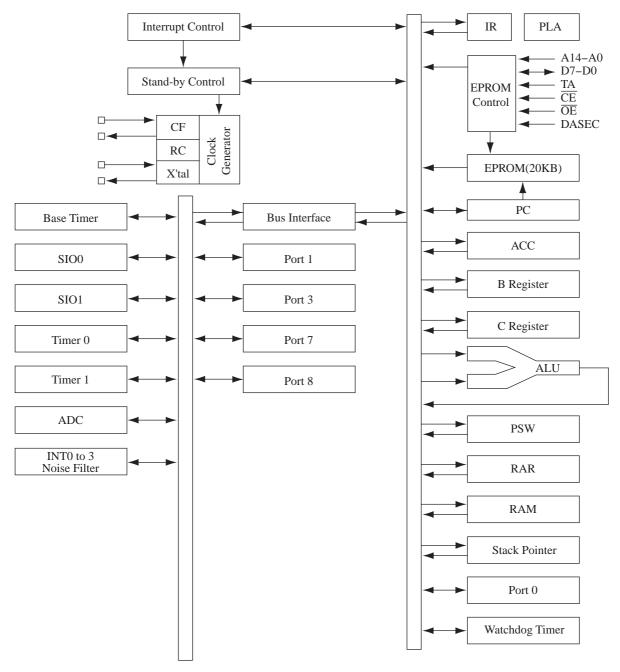
#### **Package Dimension**

(unit : mm) 3156



SANYO: QIP-48E

# **System Block Diagram**



# Pin Description

Pin name I / O Function description Option PROM m  VSS Power pin (-)  VDD Power pin (+)  PORTO I / O •8-bit input / output port Input / output in nibble units •Input for port 0 interrupt (specify every 4-bit)	ouc
VDD Power pin (+) PORTO I / O •8-bit input / output port P00 - P07 Input / output in nibble units Provided / Not provided	
PORTO I / O •8-bit input / output port P00 - P07 Input / output in nibble units Provided / Not provided	
P00 - P07   Input / output in nibble units   Provided / Not provided	
• Input for port o interrupt (specify every 4-bit)	
•Input for HOLD release •Output form :	
•15V withstand at N-channel open CMOS / N-channel open drain	
drain output (specify in bit)	
PORT1 I/O •8-bit input / output port Output form : Data line P10 - P17 Input / output can be specified CMOS / N-channel open drain D0 to D7	
P10 - P17   Input / output can be specified   CMOS / N-channel open drain   D0 to D7   (specify in bit)	
•Other pin functions	
P10 SIO0 data output	
P11 SIO0 data input /	
bus input / output	
P12 SIO0 clock input / output	
P13 SIO1 data output	
P14 SIO1 data input /	
bus input / output	
P15 SIO1 clock input / output	
P16 Buzzer output	
P17 Timer1 (PWM0) output	
PORT3 I/O •7-bit input / output port •Pull-up resistor:	
P30 - P36 Input / output in bit unit Provided / Not provided	
•15V withstand at N-channel open •Output form :	
drain output   CMOS / N-channel open drain	
Input / output in bit unit	
•2-bit input port	
•Other pin functions	
P70 - P73 I / O P70 : INTO input / HOLD release PROM control	o1
170-173   170   170. IN 10 input/ HOLD release   FROM Control	Л
input / N. channel Tr. output for	1
input / N-channel Tr. output for signals	1
watchdog timer •DASEC (*1)	
watchdog timer  P74, P75  I P71 : INT1 input / HOLD release input P72 : INT2 input / timer 0 event input P73 : INT3 input with noise filter / timer 0 event input  P84 P75  •DASEC (*1) • $\overline{OE}$ (*2) • $\overline{CE}$ (*3)	
watchdog timer  P74, P75  I P71 : INT1 input / HOLD release input P72 : INT2 input / timer 0 event input P73 : INT3 input with noise filter / timer 0 event input P74 : Input pin XT1 for 32.768kHz	
watchdog timer  P74, P75  I P71: INT1 input / HOLD release input P72: INT2 input / timer 0 event input P73: INT3 input with noise filter / timer 0 event input P74: Input pin XT1 for 32.768kHz crystal oscillation	
watchdog timer  P74, P75  I P71: INT1 input / HOLD release input P72: INT2 input / timer 0 event input P73: INT3 input with noise filter / timer 0 event input P74: Input pin XT1 for 32.768kHz crystal oscillation P75: Output pin XT2 for 32.768kHz	
watchdog timer  P74, P75  I P71: INT1 input / HOLD release input P72: INT2 input / timer 0 event input P73: INT3 input with noise filter / timer 0 event input P74: Input pin XT1 for 32.768kHz crystal oscillation  P75: Output pin XT2 for 32.768kHz crystal oscillation	
watchdog timer  P74, P75  I P71: INT1 input / HOLD release input P72: INT2 input / timer 0 event input P73: INT3 input with noise filter / timer 0 event input P74: Input pin XT1 for 32.768kHz crystal oscillation P75: Output pin XT2 for 32.768kHz crystal oscillation •Interrupt received form,	
watchdog timer  P74, P75  I P71: INT1 input / HOLD release input P72: INT2 input / timer 0 event input P73: INT3 input with noise filter / timer 0 event input P74: Input pin XT1 for 32.768kHz crystal oscillation  P75: Output pin XT2 for 32.768kHz crystal oscillation  Interrupt received form, vector address	
watchdog timer  P74, P75  I P71: INT1 input / HOLD release input P72: INT2 input / timer 0 event input P73: INT3 input with noise filter / timer 0 event input P74: Input pin XT1 for 32.768kHz crystal oscillation P75: Output pin XT2 for 32.768kHz crystal oscillation •Interrupt received form, vector address rising falling rising high low vector	
watchdog timer  P74, P75  P75  P76  P77 : INT1 input / HOLD release input P77 : INT2 input / timer 0 event input P78 : INT3 input with noise filter / timer 0 event input P79  EVEN TO SET (*1)  **OE (*2)  **OE (*2)  **OE (*3)  **OE (*3)  **OE (*3)  **OE (*3)  **OE (*3)  **OE (*4)  **OE (*4)  **OE (*2)  **OE (*3)  **OE (*2)  **OE (*3)  **OE (*4)  **OE	
watchdog timer  P74, P75  P75  P76   P77 : INT1 input / HOLD release input P77 : INT2 input / timer 0 event input P78 : INT3 input with noise filter / timer 0 event input P74 : Input pin XT1 for 32.768kHz crystal oscillation  P75 : Output pin XT2 for 32.768kHz crystal oscillation  Interrupt received form, vector address    rising   falling   rising   high   low   vector   level   level	
watchdog timer  P74, P75  I P71: INT1 input / HOLD release input P72: INT2 input / timer 0 event input P73: INT3 input with noise filter / timer 0 event input P74: Input pin XT1 for 32.768kHz crystal oscillation P75: Output pin XT2 for 32.768kHz crystal oscillation •Interrupt received form, vector address  rising falling rising high low vector level falling INT0 enable enable disable enable enable 03H	
watchdog timer  P74, P75  P75  P76   P77 : INT1 input / HOLD release input P77 : INT2 input / timer 0 event input P77 : INT3 input with noise filter / timer 0 event input P77 : Input pin XT1 for 32.768kHz crystal oscillation  P75 : Output pin XT2 for 32.768kHz crystal oscillation  P16 : Input pin XT2 for 32.768kHz crystal oscillation  P17 : Input pin XT2 for 32.768kHz crystal oscillation  P17 : Input pin XT2 for 32.768kHz crystal oscillation  P18 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation  P19 : Input pin XT2 for 32.768kHz crystal oscillation	

Pin name	I/O	Function description	Option	PROM mode
PORT8				
P80 - P83	I	•4-bit input port		TA (*4)
P84 - P87	I/O	•4-bit input / output port		
		Input / output can be specified in		
		bit unit		
		•Other function		
		AD input port (AN7 to AN0)		
RES	I	Reset pin		
XT1 / P74	I	•Input pin for the 32.768kHz cyrstal		
		oscillation		
		•Other function		
		XT1 : Input port P74		
		In case of non use, connect to V <sub>DD</sub>		
XT2 / P75	О	•Output pin for the 32.768kHz		
		crystal oscillation		
		•Other function		
		XT2 : Input port P75		
		In case of non use, connect to V <sub>DD</sub>		
		at using as port or unconnect at using		
		as oscillation.		
CF1	I	Input pin for the ceramic resonator		
		oscillation		
CF2	О	Output pin for the ceramic resonator		
		oscillation		

<sup>■</sup> All of port options except the pull-up resistor option of Port 0 can be specified in a bit unit.

- \*1 Memory select input for data security
- \*2 Output enable input
- \*3 Chip enable input
- \*4 TA-> PROM control signal input

# 1. Absolute Maximum Ratings at $V_{SS}$ = 0V and Ta=25°C

Dama		Carrala a I	Din a	C = 1:4: = = =			Ratings		:4
Para	meter	Symbol	Pins	Conditions	VDD [V]	min.	typ.	max.	unit
Supply	voltage	V <sub>DD</sub> MAX	$V_{ m DD}$	$V_{ m DD}$		-0.3		+7.0	V
Input v	oltage	VI(1)	•Ports 74, 75 •Ports 80, 81, 82, 83 •RES			-0.3		V <sub>DD</sub> +0.3	
Input / o	-	VIO(1)	•Port 1 •Ports 70, 71, 72, 73 •Ports 84, 85, 86, 87 •Ports 0,3 at CMOS output option			-0.3		VDD+0.3	
		VIO(2)	Ports 0, 3 at N-ch open drain output option			-0.3		15	
1 -	Peak output current	ІОРН	•Ports 0, 1, 3 •Ports 71, 72, 73 •Ports 84, 85, 86, 87	CMOS output At each pins		-10			mA
current	Total output	ΣIOAH(1)	Ports 0, 1	The total all pins		-30			
	current	∑IOAH(2)	Port 3	The total all pins		-15			
		∑IOAH(3)	•Ports 71, 72, 73 •Ports 84, 85, 86, 87	The total all pins		-10			
Low	Peak	IOPL(1)	Ports 0, 1, 3	At each pins				20	
Level output	output current	IOPL(2)	•Ports 70, 71, 72, 73 •Ports 84, 85, 86, 87	At each pins				15	
	Total output	$\Sigma$ IOAL(1)	Ports 0, 1, 70	The total all pins				60	
	current	ΣIOAL(2)	Port 3	The total all pins				40	
		ΣIOAL(3)	•Ports 71, 72, 73 •Ports 84, 85, 86, 87	The total all pins				20	
Power		Pd max (1)	DIP42S	$Ta = -30 \text{ to } +70^{\circ}\text{C}$				630	mW
dissipat (max.)	ion	Pd max (2)	QFP48E	Ta=-30 to +70°C	l I			410	
Operation temperature range	ature	Topg				-30		70	°C
Storage tempera range		Tstg				-65		150	

# 2. Recommended Operating Range at Ta = -30°C to +70°C, $V_{SS} = 0V$

Parameter	Symbol	Pins	Conditions			Ratings		unit
	•			VDD [V]	min.	typ.	max.	
Operating supply voltage range	VDD	VDD	0.98μs≤ tCYC tCYC≤400μs		4.5		6.0	V
HOLD voltage	VHD	VDD	RAMs and Registers hold voltage at HOLD mode.		2.0		6.0	
Input high voltage	VIH(1)	Port 0 at CMOS output	Output disable	4.5 to 6.0	0.33V <sub>DD</sub> +1.0		V <sub>DD</sub>	
J	VIH(2)	Port 0 at N-ch open drain output option.	Output disable	4.5 to 6.0	0.75V <sub>DD</sub>		13.5	
	VIH(3)	•Port 1 •Ports 72, 73 •Port 3 at CMOS output	Output disable	4.5 to 6.0	0.75VDD		VDD	
	VIH(4)	Port 3 at N-ch open drain output option.	Output disable	4.5 to 6.0	0.75V <sub>DD</sub>		13.5	
	VIH(5)	•Port 70 Port input / interrupt •Port 71 •RES	Output disable	4.5 to 6.0	0.75V <sub>DD</sub>		VDD	
	VIH(6)	Port 70 Watchdog timer	Output disable	4.5 to 6.0	0.9V <sub>DD</sub>		V <sub>DD</sub>	
	VIH(7)	•Port 8 •Ports 74, 75	Output disable Using as port	4.5 to 6.0	0.75VDD		VDD	
Input low voltage	VIL(1)	Port 0 at CMOS output option	Output disable	4.5 to 6.0	VSS		0.2V <sub>DD</sub>	
	VIL(2)	Port 0 at N-ch open drain output option.	Output disable	4.5 to 6.0	VSS		0.25V <sub>DD</sub>	
	VIL(3)	•Ports 1, 3 •Ports 72, 73	Output disable	4.5 to 6.0	VSS		0.25V <sub>DD</sub>	
	VIL(4)	•Port 70 Port input / interrupt •Port 71 •RES	Output disable	4.5 to 6.0	VSS		0.25VDD	
	VIL(5)	Port 70 Watchdog timer	Output disable	4.5 to 6.0	VSS		0.8V <sub>DD</sub> -1.0	
	VIL(6)	•Port 8 •Ports 74, 75	Output disable Using as port	4.5 to 6.0	VSS		0.25V <sub>DD</sub>	
Operation cycle time	tCYC			4.5 to 6.0	0.98		400	μs

Parameter	Symbol	Pins	Conditions			Ratings		unit
Parameter	Symbol	Pills	Conditions	V <sub>DD</sub> [V]	min.	typ.	max.	uiiit
Oscillation fre-	FmCF(1)	CF1, CF2	•6MHz (ceramic	4.5 to 6.0	5.88	6	6.12	MHz
quency range			resonator oscil-					
(Note 1)			lation)					
			•Refer to figure 1					
	FmCF(2)	CF1, CF2	•3MHz (ceramic	4.5 to 6.0	2.94	3	3.06	
			resonator oscil-					
			lation)					
			•Refer to figure 1					
	FmRC		RC oscillation	4.5 to 6.0	0.3	0.8	3.0	
	FsXtal	XT1, XT2	•32.768kHz	4.5 to 6.0		32.768		kHz
			(crystal oscillation)					
			•Refer to figure 2					
Oscillation	tmsCF(1)	CF1, CF2	•6MHz (ceramic	4.5 to 6.0		0.05	0.50	ms
stable time			resonator oscil-					
period			lation)					
(Note 1)			•Refer to figure 3					
	tmsCF(2)	CF1, CF2	•3MHz (ceramic	4.5 to 6.0		0.10	1.00	
			resonator oscil-					
			lation)					
			•Refer to figure 3					
	tssXtal	XT1, XT2	•32.768kHz	4.5 to 6.0		1.00	1.50	S
			(crystal oscillation)					
			•Refer to figure 3					

(Note 1) The oscillation constant is shown on table 1 and table 2.

# 3. Electrical Characteristics at Ta = -30°C to +70°C, $V_SS = 0V$

Parameter	Symbol	Pins	Conditions			Ratings		unit
				VDD [V]	min.	typ.	max.	
Input high current	IIH(1)	Ports 0, 3 of Open drein output	•Output disable •VIN=13.5V (including off-leak current of the				5	μΑ
			output Tr.)					
	IIH(2)	•Port 0 without pull-up MOS Tr.	•Output disable •Pull-up MOS Tr.	4.5 to 6.0			1	_
		•Ports 1, 3 •Ports 70, 71, 72, 73	OFF. •VIN=VDD					
		•Port 8	(including off-leak current of the output Tr.)					
	IIH(3)	RES	VIN=VDD	4.5 to 6.0			1	
	IIH(4)	Ports 74, 75	VIN=VDD at using as port	4.5 to 6.0			1	
Input low current	IIL(1)	•Ports 1, 3, •Port 0 without pull-up MOS Tr. •Ports 70, 71, 72, 73 •Port 8	•Output disable •Pull-up MOS Tr. OFF. •VIN=VSS (including off-leak current of the output Tr.)		-1			
	IIL(2)	RES	V <sub>IN</sub> =V <sub>SS</sub>	4.5 to 6.0	-1			1
	IIL(3)	Ports 74, 75	VIN=VSS at using as port	4.5 to 6.0	-1			
Output high voltage	VOH(1)	Ports 0, 1, 3 of CMOS output	IOH=-1.0mA	4.5 to 6.0	V <sub>DD</sub> -1			V
	VOH(2)	•Ports 71, 72, 73 •Ports 84, 85, 86, 87	IOH=-0.1mA	4.5 to 6.0	V <sub>DD</sub> -0.5			
Output low	VOL(1)	Ports 0, 1, 3	IOL=10mA	4.5 to 6.0			1.5	
voltage	VOL(2)		IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(3)	•Ports 71, 72, 73 •Ports 84, 85, 86, 87	IOL=1.6mA	4.5 to 6.0			0.4	
	VOL(4)	Port 70		4.5 to 6.0			0.4	
Pull-up MOS Tr. resistor	Rpu	•Ports 0, 1, 3 •Ports 70, 71, 72, 73 •Ports 84, 85, 86, 87		4.5 to 6.0	15	40	70	kΩ
Hysteresis voltage	VHIS	•Port 1 •Ports 70, 71, 72, 73 •RES	Output disable	4.5 to 6.0		0.1V <sub>DD</sub>		V
Pin capacitance	СР	All pins	•f=1MHz Unmeasurement terminals for input are set to VSS level. •Ta=25°C	4.5 to 6.0		10		pF

# 4. Serial Input / Output Characteristics at Ta=-30°C to +70°C, $V_{SS}$ = 0V

		meter	Symbol	Pins	Conditions		Ratings		unit	
	Гага	illetei	Symbol		Conditions	VDD [V]	min.	typ.	max.	uiiit
		Cycle	tCKCY(1)	SCK0, SCK1	Refer to figure 5		2			tCYC
		Low	tCKL(1)			4.5 to 6.0	1			
	ck	level								
	clo	width								
	Input clock	High	tCKH(1)			4.5 to 6.0	1			
	In]	level								
		pulse								
4		width								
Serial clock		Cycle	tCKCY(2)	SCK0, SCK1	•Use pull-up	4.5 to 6.0	2			
al c					resistor (1k $\Omega$ )					
eri					when open drain					
	쏭	Low	tCKL(2)		output.	4.5 to 6.0		1 / 2 tCKCY		
	Output clock	level			•Refer to figure 5					
	m	pulse								
	lutp	width								
		High	tCKH(2)			4.5 to 6.0		1 / 2 tCKCY		
		level								
		pulse								
		width								
nt		ta set-up	tICK	•SI0, SI1	•Data set-up to	4.5 to 6.0	0.1			μs
Serial input	tim			•SB0, SB1	SCK0, 1					
la]		ta hold	tCKI		•Data hold from	4.5 to 6.0	0.1			
Seri	tim	ie			SCK0, 1					
<b>J</b>					•Refer to figure 5					
	l		tCKO(1)	•SO0, SO1	•Use pull-up	4.5 to 6.0			7 / 12 tCYC	
	tim			•SB0, SB1	resistor (1k $\Omega$ )				+0.2	
	`	rial clock			when open drain					
hdı		extrnal			output.					
ont	l	ock)								
Serial output			tCKO(2)		•Data hold from	4.5 to 6.0			1/3 tCYC	
Ser	tim				SCK0, 1				+0.2	
	,	rial clock			•Refer to figure 5					
		internal								
	clo	ock)								

#### **5. Pulse Input Conditions** at Ta=-30°C to +70°C, $V_{SS} = 0V$

Donomatan	Cramb of	Pins	Conditions			Ratings		
Parameter	Symbol	Pilis	Conditions	VDD [V]	min.	typ.	max.	unit
High / low	tPIH(1)	•INT0, INT1	•Interrupt accept-	4.5 to 6.0	1			tCYC
level pulse	tPIL(1)	•INT2 / T0IN	able					
width			•Timer0-countable					
	tPIH(2)	INT3 / TOIN	•Interrupt accept-	4.5 to 6.0	2			1
	tPIL(2)	(The noise	able					
		rejection clock	•Timer0-countable					
		select to 1 / 1.)						
	tPIH(3)	INT3 / TOIN	•Interrupt accept-	4.5 to 6.0	32			
	tPIL(3)	(The noise	able					
		rejection clock	•Timer0-countable					
		select to 1 / 16.)						
	tPIH(4)	INT3 / TOIN	•Interrupt accept-	4.5 to 6.0	128			]
	tPIL(4)	(The noise	able					
		rejection clock	•Timer0-countable					
		select to 1 / 64.)						
	tPIL(5)	RES	Reset acceptable	4.5 to 6.0	200			μs

#### **6. A / D** Converter Characteristics at Ta=-30°C to +70°C, VSS=0V

Parameter	Symbol	Pins	Conditions		Ratings			unit
				V <sub>DD</sub> [V]	min.	typ.	max.	unit
Resolution	N			4.5 to 6.0		8		bit
Absolute	ET			4.5 to 6.0			±1.5	LSB
precision								
(Note 2)								
Conversion	tCAD		AD conversion	4.5 to 6.0	15.68		65.28	μs
time			time=16 X tCYC		(tCYC =		(tCYC =	
			(ADCR2=0)		0.98µs)		4.08µs)	
			(Note 3)					
			AD conversion		31.36		130.56	
			time=32 X tCYC		(tCYC =		(tCYC =	
			(ADCR2=1)		0.98µs)		4.08µs)	
			(Note 3)					
Analog input	VAIN	AN0 to AN7		4.5 to 6.0	Vss		$V_{\mathrm{DD}}$	V
voltage range								
Analog port	IAINH		VAIN=V <sub>DD</sub>	4.5 to 6.0			1	μΑ
input current	IAINL		VAIN=VSS	4.5 to 6.0	-1			

<sup>(</sup>Note 2) Absolute precision excepts quantizing error (±1/2 LSB).

<sup>(</sup>Note 3) The conversion time means the time from executing the AD conversion instruction to setting the complete digital conversion value to the register.

7. Current Dissipation Characteristics at Ta=-30°C to +70°C,  $V_{SS}=0V$ 

Parameter	Symbol	Pins	Conditions	Ratings			unit	
	•			VDD [V]	min.	typ.	max.	uiiit
Current	IDDOP(1)	VDD	•FmCF=6MHz	4.5 to 6.0		14	26	mA
dissipation			Ceramic resona-					
during basic			tor oscillation					
operation			•FsXtal=32.768kHz					
(Note 4)			crystal oscillation					
			•System clock:					
			CF oscillation					
			•Internal RC					
			oscillation stops.					
			•1 / 1 divider					
	IDDOP(2)		•FmCF=3MHz	4.5 to 6.0		6.5	14	
			Ceramic resona-	-				
			tor oscillation					
			•FsXtal=32.768kHz					
			crystal oscillation					
			•System clock:					
			CF oscillation					
			•Internal RC					
			oscillation stops.					
			•1 / 2 divider					
	IDDOP(3)		•FmCF=0Hz	4.5 to 6.0		4	12	
	, ,		(when oscillation					
			stops).					
			•FsXtal=32.768kHz					
			crystal oscillation					
			•System clock:					
			RC oscillation					
			•1 / 2 divider					
	IDDOP(4)		•FmCF=0Hz	4.5 to 6.0		3.5	9	-
			(when oscillation				-	
			stops).					
			•FsXtal=32.768kHz					
			crystal oscillation					
			•System clock:					
			crystal oscillation					
			•Internal RC					
			oscillation stops.					
			•1 / 2 divider					

Parameter	Symbol	Pins	Conditions	Ratings			umit	
Parameter	-			V <sub>DD</sub> [V]	min.	typ.	max.	unit
Current	IDDHALT(1)	V <sub>DD</sub>	•HALT mode	4.5 to 6.0		4	9	mA
dissipation			•FmCF=6MHz					
HALT mode			Ceramic resona-					
(Note 4)			tor oscillation					
			•FsXtal=32.768kHz	I I				
			crystal oscillation					
			•System clock:					
			CF oscillation					
			•Internal RC					
			oscillation stops.					
	IDDIIAI T(2)		•1 / 1 devider	154560		2.2	5	-
	IDDHALT(2)		•HALT mode FmCF=3MHz	4.5 to 6.0		2.2	) 3	
			Ceramic resona-					
			tor oscillation					
			•FsXtal=32.768kHz	I I				
			crystal oscillation	1				
			•System clock:					
			CF oscillation					
			•Internal RC					
			oscillation stops.					
	IDDIIA I T(2)		•1 / 2 devider	1.7. 60		400	1.000	
	IDDHALT(3)		•HALT mode	4.5 to 6.0		400	1600	μΑ
			FmCF=0Hz					
			(when oscillation					
			stops).					
			•FsXtal=32.768kHz					
			crystal oscillation					
			•System clock : RC oscillation					
	IDDHALT(4)		•1 / 2 devider	15. 60		25	100	-
			•HALT mode	4.5 to 6.0		25	100	
			FmCF=0Hz					
			(when oscillation					
			stops).					
			•FsXtal=32.768kHz					
			crystal oscillation					
			•System clock: 32.768kHz					
			•Internal RC					
			oscillation stops.					
Current	IDDIIOLD	Vpp	•1 / 2 devider HOLD mode	15 to 60		0.05	30	-
Current	IDDHOLD	$V_{DD}$	HOLD mode	4.5 to 6.0		0.05	30	
dissipation HOLD mode								
(Note 4)		<u> </u>	nd null-un MOS tra	l		L		

(Note 4) The currents of output transistors and pull-up MOS transistors are ignored.

Table 1. Ceramic resonator oscillation guaranteed constant (main-clock)

A kind of oscillation	Producer	Oscillator	C1	C2
6MHz ceramic resonator	Murata	CSA 6.00MG	33pF	33pF
oscillation		CST 6.00MGW	on c	hip
	Kyocera	KBR-6.0MSA	33pF	33pF
		PBRC 6.00A (chip type)	33pF	33pF
		KBR-6.0MKS	on chip	
		PBRC 6.00B (chip type)		
3MHz ceramic resonator	Murata	CSA 3.00MG	33pF	33pF
oscillation		CST 3.00MGW	on c	hip
	Kyocera	KBR-3.0MS	47pF	47pF

<sup>\*</sup> Both C1 and C2 must use K rank (±10%) and SL characteristics.

Table 2. Crystal oscillation guaranteed constant (sub-clock)

A kind of oscillation	Producer	Oscillator	C3	C4
32.768kHz crystal	Kyocera	KF-38G-13P0200	18pF	18pF
oscillation				

<sup>\*</sup> Both C3 and C4 must use J rank (±5%) and CH characteristics.

(It is about the application which is not in need of high precision. Use K rank ( $\pm 10\%$ ) and SL characteristics.)

Notes

- •Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest possible pattern length.
- •If you use other oscillators herein, we provide no guarantee for the characteristics.

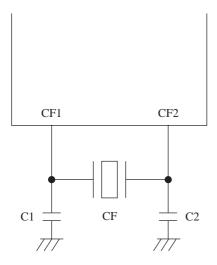


Figure 1. Main-clock circuit Ceramic resonator oscillation

XT1 XT2

C3 X'tal C4

Figure 2. Sub-clock circuit Cryatal oscillation

ILC00065

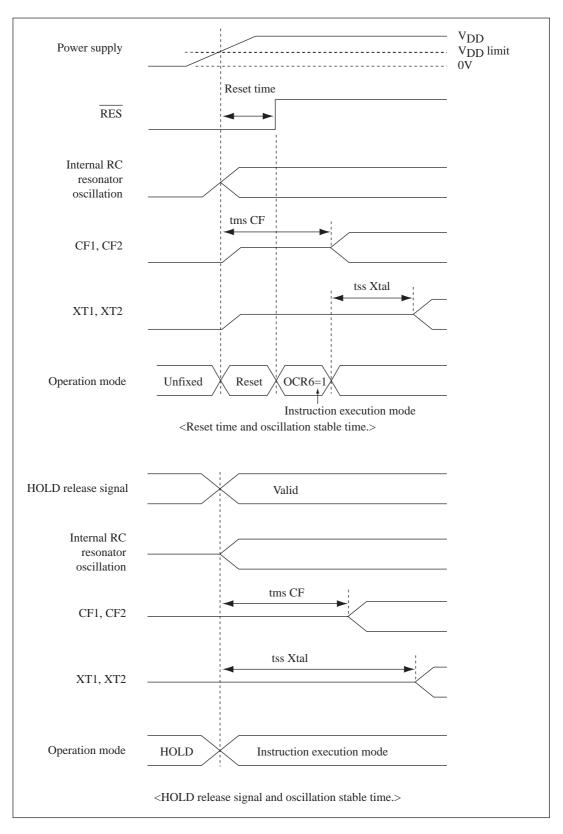
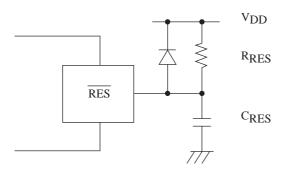


Figure 3. Oscillation stable time

ILC00044



(Note) Fix the value of  $R_{RES}$ , CRES that is sure to reset untill 200 $\mu$ s, after Power supply has been over inferior limit of supply voltage.

Figure 4. Reset circuit

ILC00052

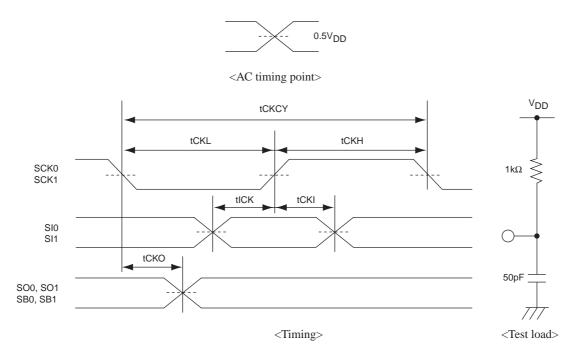


Figure 5. Serial input / output test condition

ILC00073

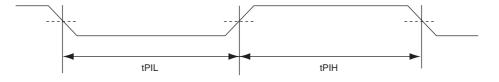


Figure 6. Pulse input timing condition

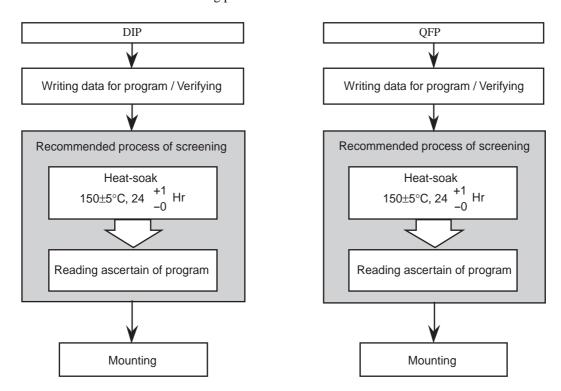
ILC00074

#### Notice for use

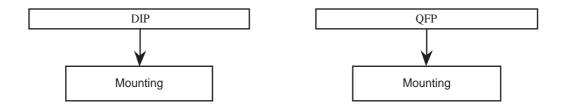
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  The environment must be held at a temparature of 30°C or less and a humidity level of 70% or less.
- After opening the packing
  After opening the packing, a controlled environment must be maintained until soldering.
  The environment must be held at a temperature of 30°C or less and a humidity level of 70% or less.
  Please solder within 96 hours.
- a. Shipping with a blank PROM (Programming the data by yourself)

  This microcomputer is provided DIP / QFP packages, but the condition before mounting is different. Refer to the mounting procedure as follows.



b. Shipping with a programmed PROM (Programming the data by Sanyo)



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