

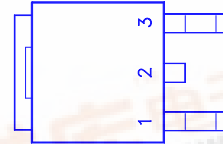
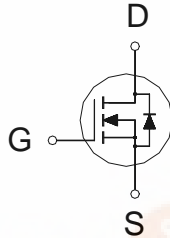
NIKO-SEM

**N-Channel Logic Level Enhancement
Mode Field Effect Transistor**

**P55N02LD
TO-252 (DPAK)**

PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
25	10mΩ	55A



- 1. GATE
- 2. DRAIN
- 3. SOURCE

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ °C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	$T_C = 25\text{ °C}$	I_D	55	A
	$T_C = 100\text{ °C}$		36	
Pulsed Drain Current ¹		I_{DM}	140	
Avalanche Current		I_{AR}	20	
Avalanche Energy	$L = 0.1\text{mH}$	E_{AS}	140	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	5.6	
Power Dissipation	$T_C = 25\text{ °C}$	P_D	60	W
	$T_C = 100\text{ °C}$		38	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C
Lead Temperature (¹ / ₁₆ " from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		65	
Case-to-Heatsink	$R_{\theta CS}$	0.7		

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS ($T_C = 25\text{ °C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	25			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			±250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V$			25	μA
		$V_{DS} = 20V, V_{GS} = 0V, T_J = 125\text{ °C}$			250	



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On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 10V, V_{GS} = 10V$	55			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 7V, I_D = 24A$		11	14	mΩ
		$V_{GS} = 10V, I_D = 30A$		10	13	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 15V, I_D = 30A$		16		S

DYNAMIC

Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$		2700		pF
Output Capacitance	C_{oss}			500		
Reverse Transfer Capacitance	C_{rss}			200		
Total Gate Charge ²	Q_g	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = 10V,$ $I_D = 30A$		25		nC
Gate-Source Charge ²	Q_{gs}			7		
Gate-Drain Charge ²	Q_{gd}			11		
Turn-On Delay Time ²	$t_{d(on)}$	$V_{DS} = 15V, R_L = 1\Omega$ $I_D \cong 30A, V_{GS} = 10V, R_{GS} = 2.5\Omega$		7		nS
Rise Time ²	t_r			7		
Turn-Off Delay Time ²	$t_{d(off)}$			24		
Fall Time ²	t_f			6		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)

Continuous Current	I_S			55		A
Pulsed Current ³	I_{SM}			150		
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$		1.3		V
Reverse Recovery Time	t_{rr}	$I_F = I_S, di_F/dt = 100A / \mu S$		37		nS
Peak Reverse Recovery Current	$I_{RM(REC)}$			200		A
Reverse Recovery Charge	Q_{rr}			0.043		μC

¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.²Independent of operating temperature.³Pulse width limited by maximum junction temperature.**REMARK: THE PRODUCT MARKED WITH "P55N02LD", DATE CODE or LOT #**

TO-252 (DPAK) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	9.35		10.1	H		0.8	
B	2.2		2.4	I	6.4		6.6
C	0.48		0.6	J	5.2		5.4
D	0.89		1.5	K	0.6		1
E	0.45		0.6	L	0.64		0.9
F	0.03		0.23	M	4.4		4.6
G	6		6.2	N			

