NCP565

1.5 A Low Dropout Linear Regulator

The NCP565 low dropout linear regulator will provide 1.5 A at a fixed output voltage or an adjustable voltage down to 0.9 V. The fast loop response and low dropout voltage make this regulator ideal for applications where low voltage and good load transient response are important. Device protection includes current limit, short circuit protection, and thermal shutdown. The NCP565 is packaged in a 5 pin D^2PAK for adjustable voltage version and a 3 pin D^2PAK for fixed voltage version.

Features

- Pb−Free Packages are Available
- Ultra Fast Transient Response (< 1.0 μs)
- Low Ground Current (1.1 mA @ Iload = 1.5 A)
- Low Dropout Voltage (0.9 V @ Iload = 1.5 A)
- Low Noise (28 μVrms)
- 0.9 V Reference Voltage
- Adjustable Output Voltage from 7.7 V down to 0.9 V
- 1.2 V Fixed Output Version. Other Fixed Voltages Available on Request
- Current Limit Protection (3.5 A)
- Thermal Shutdown Protection (155°C)

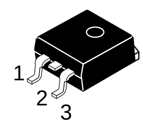
Typical Applications

- Servers
- ASIC Power Supplies
- Post Regulation for Power Supplies
- Constant Current Source

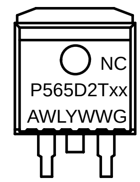
ON Semiconductor®

http://onsemi.com

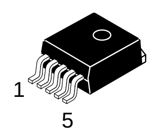
MARKING DIAGRAMS



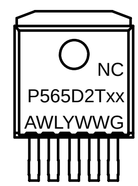
D^2PAK
CASE 936
FIXED



Tab = Ground
Pin 1. V_{in}
2. Ground
3. V_{out}



D^2PAK
CASE 936A
ADJUSTABLE



Tab = Ground
Pin 1. N.C.
2. V_{in}
3. Ground
4. V_{out}
5. Adj

xx = R4 or 12
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

PIN DESCRIPTION

Pin No. Adjustable Version	Pin No. Fixed Version	Symbol	Description
1	–	N.C.	–
2	1	V_{in}	Positive Power Supply Input Voltage
3, Tab	2, Tab	Ground	Power Supply Ground
4	3	V_{out}	Regulated Output Voltage
5	–	Adj	This pin is to be connected to the R_{sense} resistors on the output. The linear regulator will attempt to maintain 0.9 V between this pin and ground. Refer to Figure 1 for the equation.

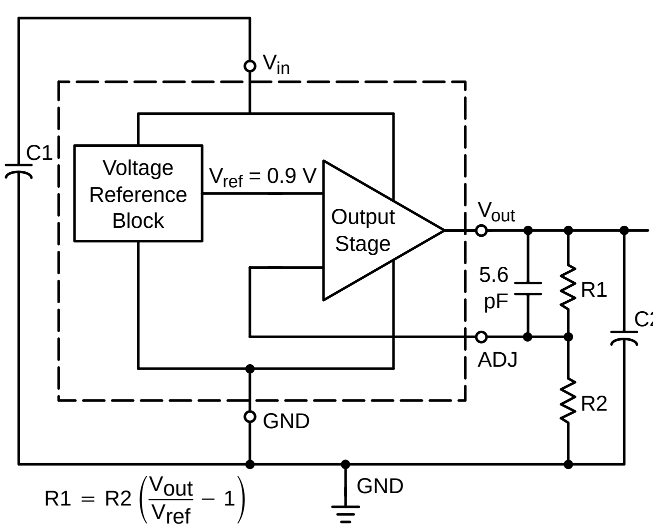
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{in}	9.0	V
Output Pin Voltage	V_{out}	−0.3 to V_{in} + 0.3	V
Adjust Pin Voltage	V_{adj}	−0.3 to V_{in} + 0.3	V
Thermal Characteristics (Note 2) Case 936A Thermal Resistance, Junction−to−Air Thermal Resistance, Junction−to−Case	 $R_{\theta JA}$ $R_{\theta JC}$	 45 5.0	°C/W
Operating Junction Temperature Range	T_J	−40 to 150	°C
Storage Temperature Range	T_{stg}	−55 to 150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model JESD 22−A114−B
   Machine Model JESD 22−A115−A
2. The maximum package power dissipation is:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$



$$R1 = R2\left(\frac{V_{out}}{V_{ref}} - 1\right)$$

Figure 1. Typical Schematic, Adjustable Output

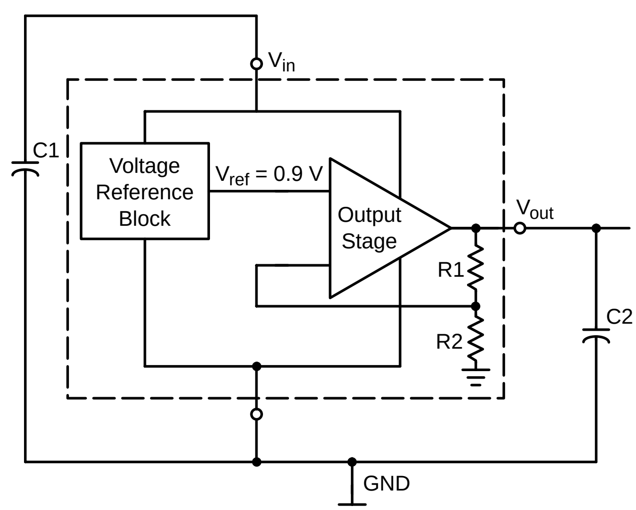


Figure 2. Typical Schematic, Fixed Output

ELECTRICAL CHARACTERISTICS ($V_{in} - V_{out}$ = 1.6 V, V_{out} = 0.9 V, T_J = 25°C, $C_{in} = C_{out}$ = 150 μF, values unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ADJUSTABLE OUTPUT VERSION					
Reference Voltage (10 mA < I_{out} < 1.5 A; 2.5 V < V_{in} < 9.0 V; T_J = −10 to 105°C)	V_{ref}	0.882 (−2%)	0.9	0.918 (+2%)	V
Reference Voltage (10 mA < I_{out} < 1.5 A; 2.5 V < V_{in} < 9.0 V; T_J = −40 to 125°C)	V_{out}	0.873 (−3%)	0.9	0.927 (+3%)	V
ADJ Pin Current	I_{Adj}	−	30	−	nA
Line Regulation (I_{out} = 10 mA)	Reg_{line}	−	0.03	−	%
Load Regulation (10 mA < I_{out} < 1.5 A)	Reg_{load}	−	0.03	−	%
Dropout Voltage (I_{out} = 1.5 A) (Note 3)	Vdo	−	0.9	1.3	V
Current Limit	I_{lim}	1.6	3.5	−	A
Ripple Rejection (120 Hz; I_{out} = 1.5 A)	RR	−	85	−	dB
Ripple Rejection (1 kHz; I_{out} = 1.5 A)	RR	−	75	−	dB
Thermal Shutdown		−	150	−	°C
Ground Current (I_{out} = 1.5 A)	Iq	−	1.1	3.0	mA
Output Noise Voltage (f = 100 Hz to 100 kHz, I_{out} = 1.5 A)	V_n	−	28	−	μVrms
FIXED OUTPUT VOLTAGE					
Output Voltage (10 mA < I_{out} < 1.5 A; 2.5 V < V_{in} < 9.0 V; T_J = −10 to 105°C)	V_{out}	1.176 (−2%)	1.2	1.224 (+2%)	%
Output Voltage (10 mA < I_{out} < 1.5 A; 2.5 V < V_{in} < 9.0 V; T_J = −40 to 125°C)	V_{out}	1.164 (−3%)	1.2	1.236 (+3%)	%
Line Regulation (I_{out} = 10 mA)	Reg_{line}	−	0.03	−	%
Load Regulation (10 mA < I_{out} < 1.5 A)	Reg_{load}	−	0.03	−	%
Dropout Voltage (I_{out} = 1.5 A) (Note 3)	Vdo	−	0.9	1.3	V
Current Limit	I_{lim}	1.6	3.5	−	A
Ripple Rejection (120 Hz; I_{out} = 1.5 A)	RR	−	85	−	dB
Ripple Rejection (1 kHz; I_{out} = 1.5 A)	RR	−	75	−	dB
Thermal Shutdown		−	150	−	°C
Ground Current (I_{out} = 1.5 A)	Iq	−	1.1	3.0	mA
Output Noise Voltage (f = 100 Hz to 100 kHz, I_{out} = 1.5 A)	V_n	−	28	−	μVrms

3. Dropout voltage is a measurement of the minimum input/output differential at full load.

ORDERING INFORMATION

Device	Nominal Output Voltage*	Package	Shipping†
NCP565D2T	Adj	D^2PAK	50 Tube
NCP565D2TR4	Adj	D^2PAK	800 Tape & Reel
NCP565D2TR4G	Adj	D^2PAK (Pb−Free)	800 Tape & Reel
NCP565D2T12	Fixed	D^2PAK	50 Tube
NCP565D2T12R4	Fixed	D^2PAK	800 Tape & Reel
NCP565D2T12R4G	Fixed	D^2PAK (Pb−Free)	800 Tape & Reel

*For other fixed output versions, please contact the factory.
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

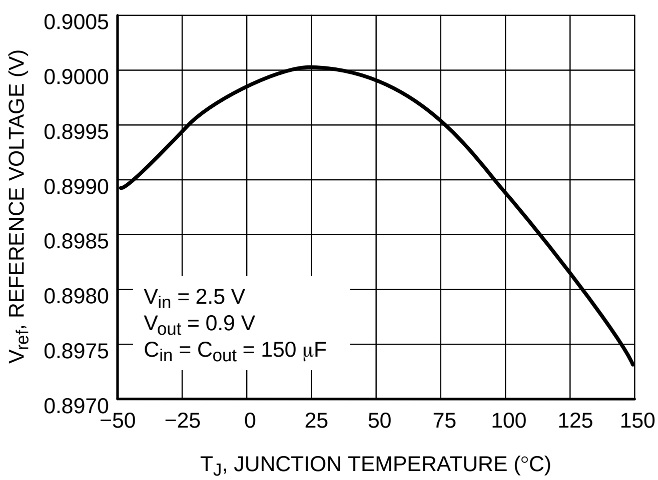


Figure 3. Output Voltage vs. Temperature

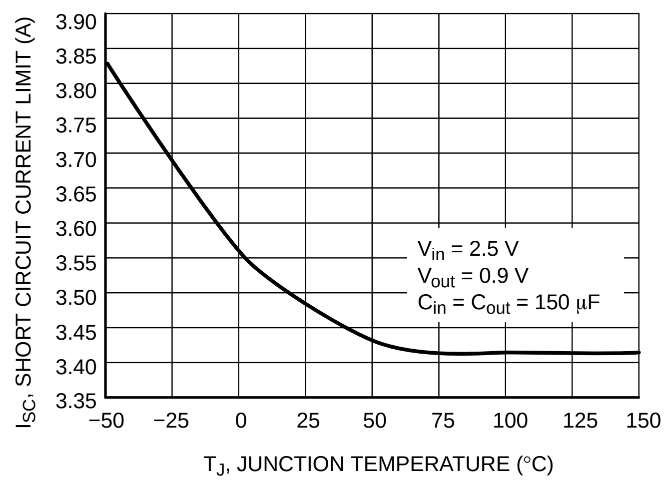


Figure 4. Short Circuit Current Limit vs. Temperature

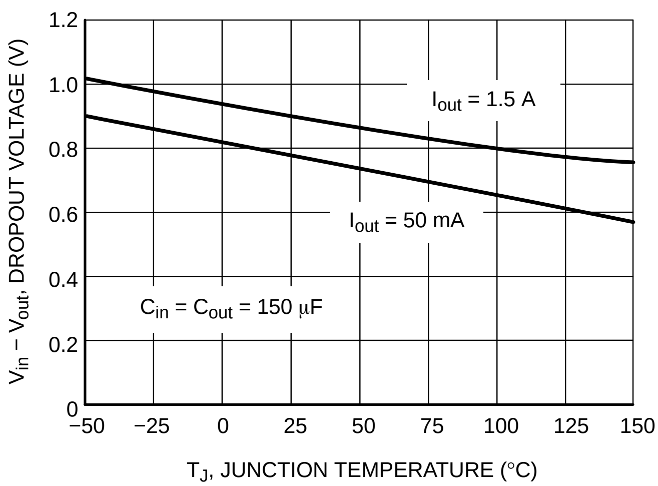


Figure 5. Dropout Voltage vs. Temperature

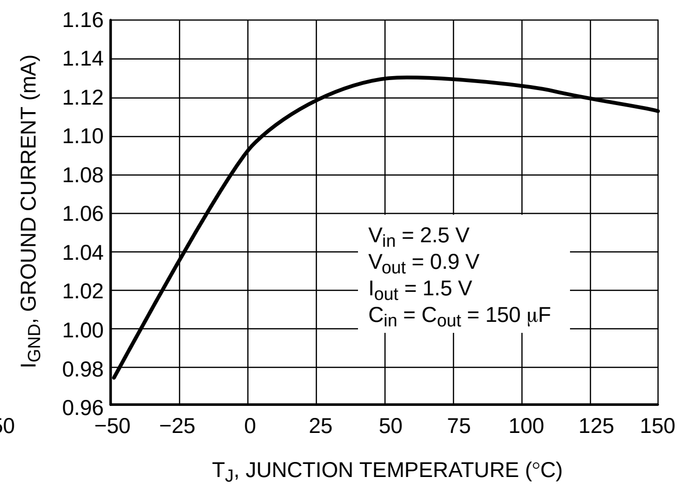


Figure 6. Ground Current vs. Temperature

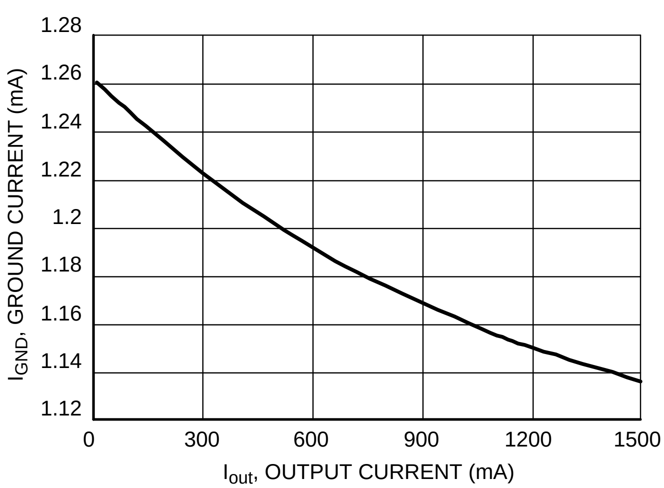


Figure 7. Ground Current vs. Output Current

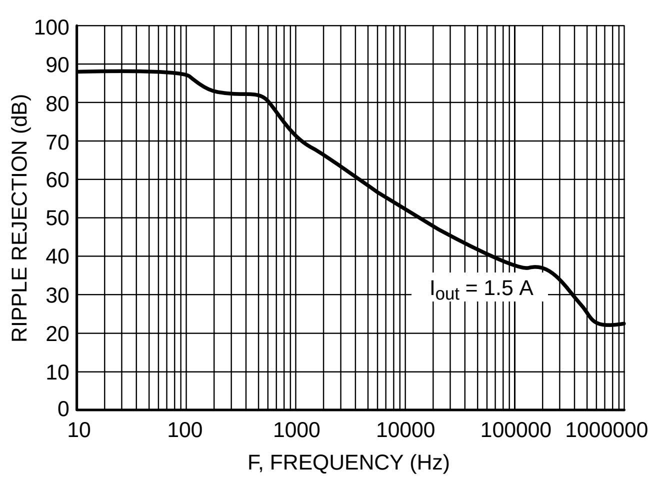


Figure 8. Ripple Rejection vs. Frequency

TYPICAL CHARACTERISTICS

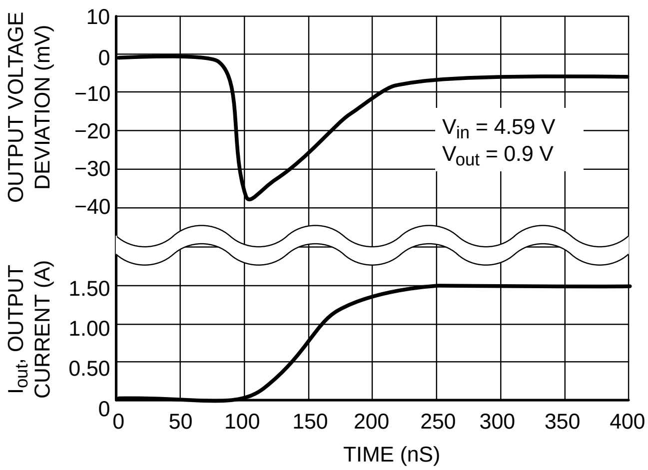


Figure 9. Load Transient from 10 mA to 1.5 A

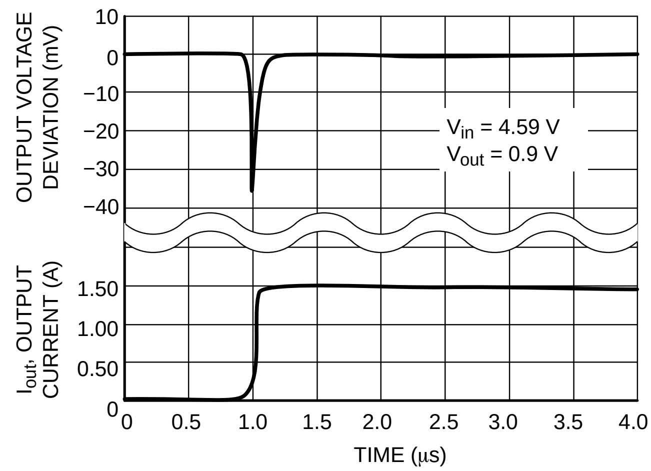


Figure 10. Load Transient from 10 mA to 1.5 A

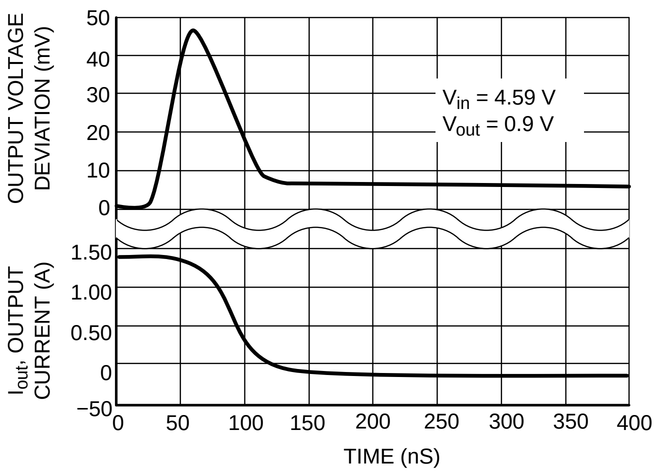


Figure 11. Load Transient from 1.5 A to 10 mA

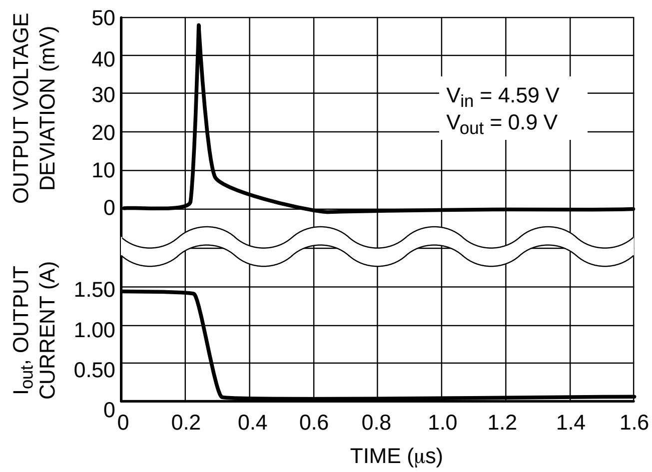


Figure 12. Load Transient from 1.5 A to 10 mA

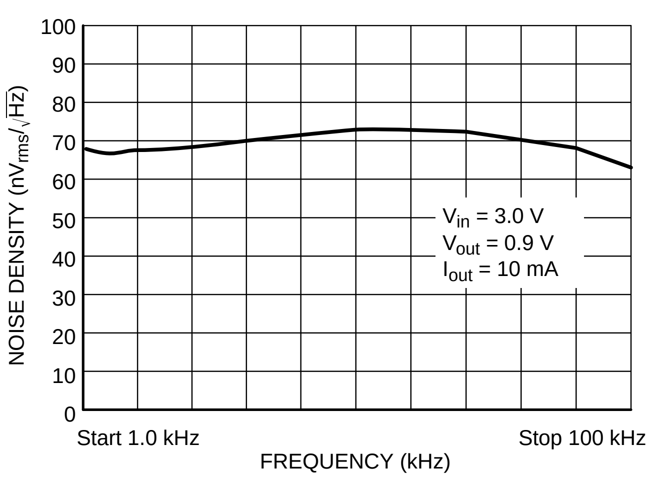


Figure 13. Noise Density vs. Frequency

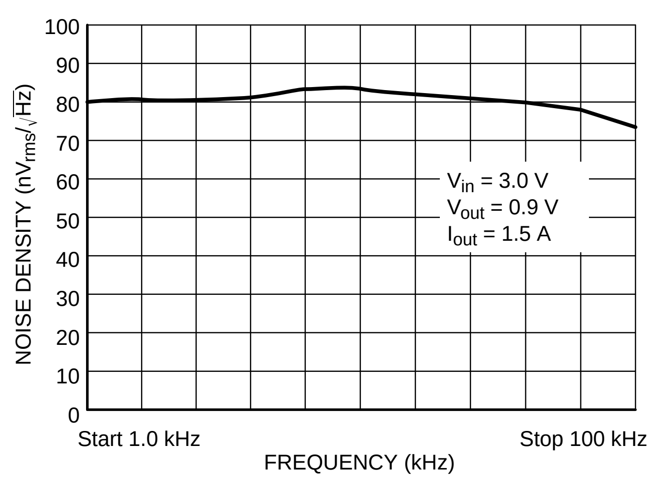


Figure 14. Noise Density vs. Frequency

APPLICATION INFORMATION

The NCP565 low dropout linear regulator provides adjustable voltages at currents up to 1.5 A. It features ultra fast transient response and low dropout voltage. These devices contain output current limiting, short circuit protection and thermal shutdown protection.

Input, Output Capacitor and Stability

An input bypass capacitor is recommended to improve transient response or if the regulator is located more than a few inches from the power source. This will reduce the circuit's sensitivity to the input line impedance at high frequencies and significantly enhance the output transient response. Different types and different sizes of input capacitors can be chosen dependent on the quality of power supply. A 150 μF OSCON 16SA150M type from Sanyo should be adequate for most applications. The bypass capacitor should be mounted with shortest possible lead or track length directly across the regulator's input terminals.

The output capacitor is required for stability. The NCP565 remains stable with ceramic, tantalum, and aluminum−electrolytic capacitors with a minimum value of 1.0 μF as long as the ESR remains between 50 mΩ and 2.5 Ω. The NCP565 is optimized for use with a 150 μF OSCON 16SA150M type in parallel with a 10 μF OSCON 10SL10M type from Sanyo. The 10 μF capacitor is used for best AC stability while 150 μF capacitor is used for achieving excellent output transient response. The output capacitors should be placed as close as possible to the output pin of the device. If not, the excellent load transient response of NCP565 will be degraded.

Adjustable Operation

The typical application circuit for the adjustable output regulators is shown in Figure 1. The adjustable device develops and maintains the nominal 0.9 V reference voltage between Adj and ground pins. A resistor divider network R1 and R2 causes a fixed current to flow to ground. This current creates a voltage across R1 that adds to the 0.9 V across R2 and sets the overall output voltage.

The output voltage is set according to the formula:

$$V_{out} = V_{ref} \times \left(\frac{R1 + R2}{R2}\right) - I_{Adj} \times R2$$

The adjust pin current, Iadj, is typically 30 nA and normally much lower than the current flowing through R1 and R2, thus it generates a small output voltage error that can usually be ignored.

Load Transient Measurement

Large load current changes are always presented in microprocessor applications. Therefore good load transient performance is required for the power stage. NCP565 has the feature of ultra fast transient response. Its load transient responses in Figures 9 through 12 are tested on evaluation board shown in Figure 15. On the evaluation board, it consists of NCP565 regulator circuit with decoupling and filter capacitors and the pulse controlled current sink to obtain load current transitions. The load current transitions are measured by current probe. Because the signal from current probe has some time delay, it causes un−synchronization between the load current transition and output voltage response, which is shown in Figures 9 through 12.

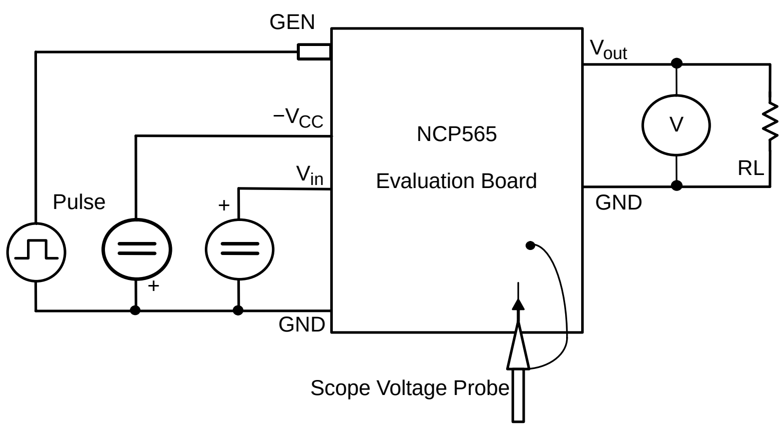


Figure 15. Schematic for Transient Response Measurement

PCB Layout Considerations

Good PCB layout plays an important role in achieving good load transient performance. Because it is very sensitive to its PCB layout, particular care has to be taken when tackling Printed Circuit Board (PCB) layout. The figures below give an example of a layout where parasitic elements are minimized. For microprocessor applications it is customary to use an output capacitor network consisting of several capacitors in parallel. This reduces the overall ESR and reduces the instantaneous output voltage drop under transient load conditions. The output capacitor network should be as close as possible to the load for the best results. The schematic of NCP565 typical application circuit, which this PCB layout is base on, is shown in Figure 16. The output voltage is set to 3.3 V for this demonstration board according to the feedback resistors in the Table 1.

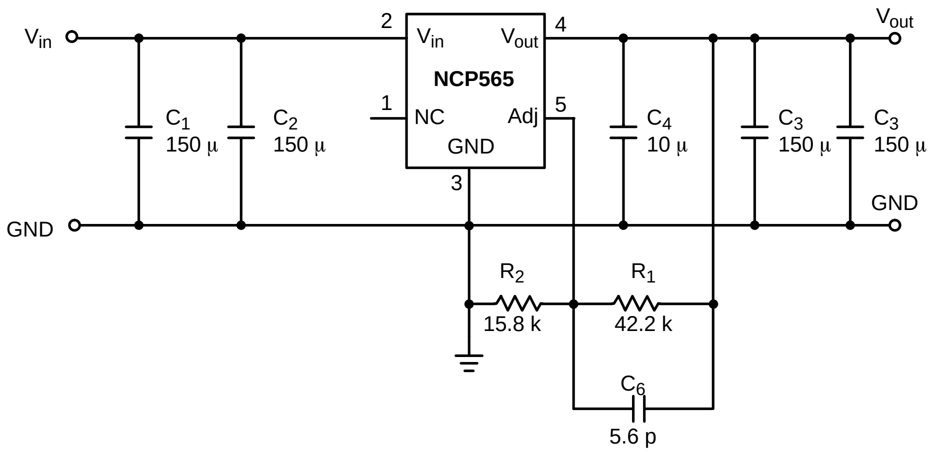


Figure 16. Schematic of NCP565 Typical Application Circuit

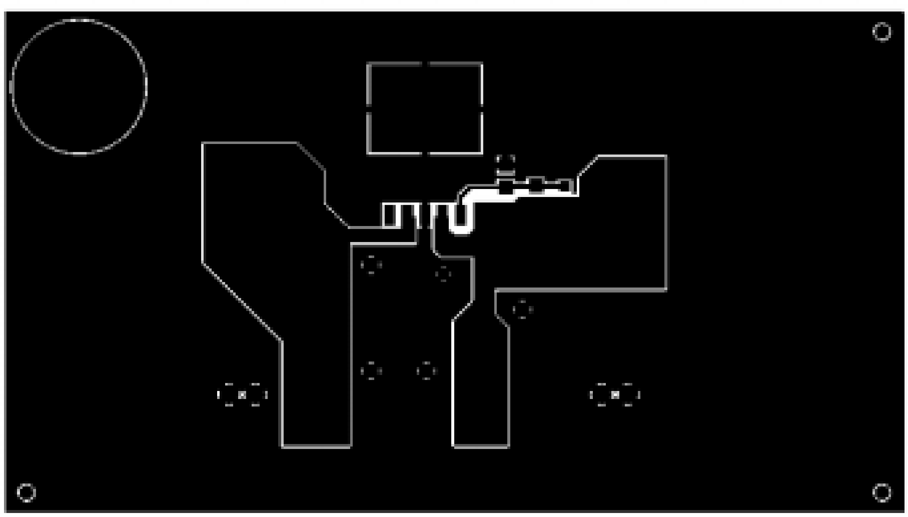


Figure 17. Top Layer

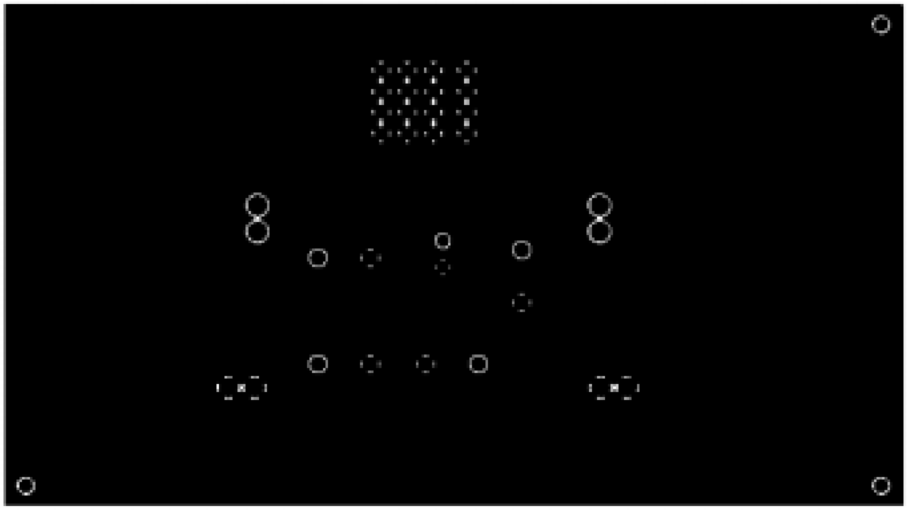


Figure 18. Bottom Layer

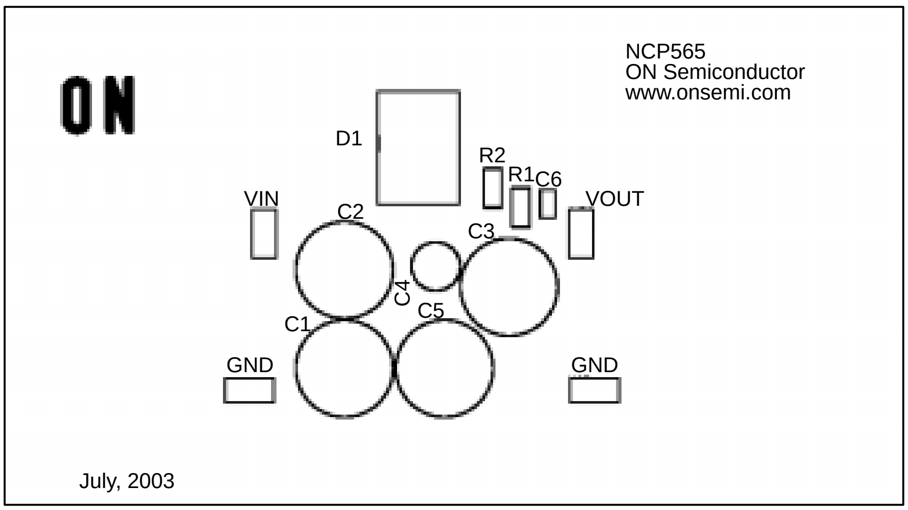


Figure 19. Silkscreen Layer

Table 1. Bill of Materials for NCP565 Adj Demonstration Board

Item	Used #	Component	Designators	Suppliers	Part Number
1	4	Radial Lead Aluminum Capacitor 150 μF/16 V	C1, C2, C3, C5	Sanyo Oscon	16SA150M
2	1	Radial Lead Aluminum Capacitor 10 μF/10 V	C4	Sanyo Oscon	10SL10M
3	1	SMT Chip Resistor (0805) 15.8 K 1%	R2	Vishay	CRCW08051582F
4	1	SMT Chip Resistor (0805) 42.2 K 1%	R1	Vishay	CRCW08054222F
5	1	SMT Ceramic Capacitor (0603) 5.6 pF 10%	C6	Vishay	VJ0603A5R6KXAA
6	1	NCP565 Low Dropout Linear Regulator	U1	ON Semiconductor	NCP565D2TR4

Protection Diodes

When large external capacitors are used with a linear regulator it is sometimes necessary to add protection diodes. If the input voltage of the regulator gets shorted, the output capacitor will discharge into the output of the regulator. The discharge current depends on the value of the capacitor, the output voltage and the rate at which V_{in} drops. In the NCP565 linear regulator, the discharge path is through a large junction and protection diodes are not usually needed. If the regulator is used with large values of output capacitance and the input voltage is instantaneously shorted to ground, damage can occur. In this case, a diode connected as shown in Figure 20 is recommended.

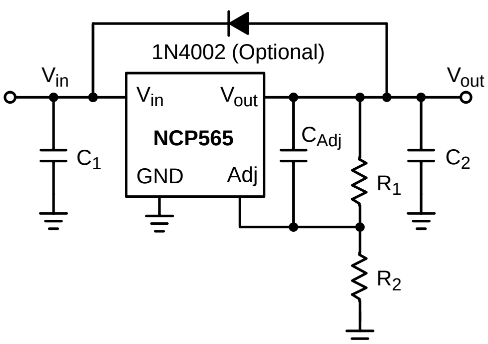


Figure 20. Protection Diode for Large Output Capacitors

Thermal Considerations

This series contains an internal thermal limiting circuit that is designed to protect the regulator in the event that the maximum junction temperature is exceeded. This feature provides protection from a catastrophic device failure due to accidental overheating. It is not intended to be used as a substitute for proper heat sinking. The maximum device power dissipation can be calculated by:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The devices are available in surface mount D^2PAK package. The package has an exposed metal tab that is specifically designed to reduce the junction to air thermal resistance, $R_{\theta JA}$, by utilizing the printed circuit board copper as a heat dissipater. Figure 21 shows typical $R_{\theta JA}$ values that can be obtained from a square pattern using economical single sided 2.0 ounce copper board material. The final product thermal limits should be tested and quantified in order to insure acceptable performance and reliability. The actual $R_{\theta JA}$ can vary considerably from the graph shown. This will be due to any changes made in the copper aspect ratio of the final layout, adjacent heat sources, and air flow.

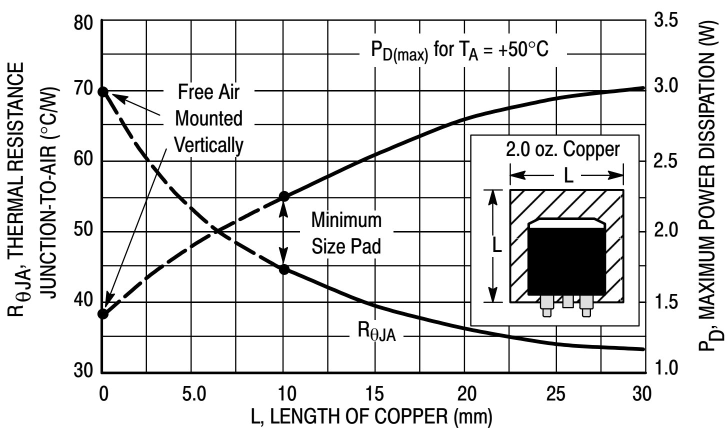
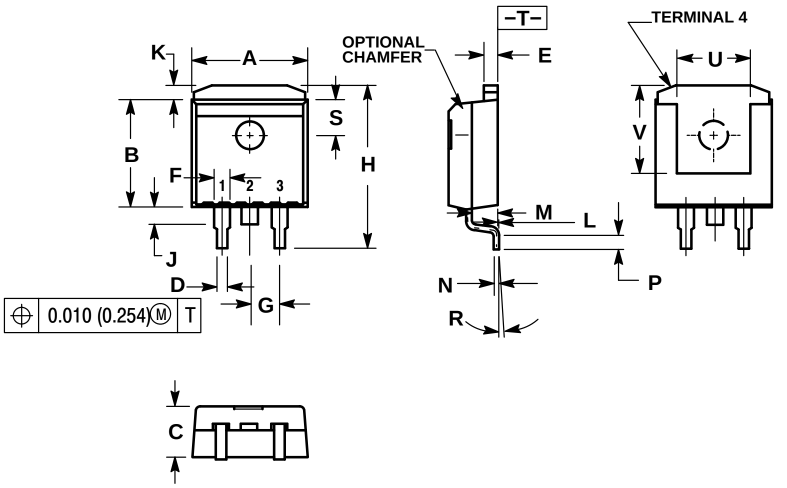


Figure 21. 3−Pin and 5−Pin D^2PAK Thermal Resistance and Maximum Power Dissipation vs. P.C.B Length

PACKAGE DIMENSIONS

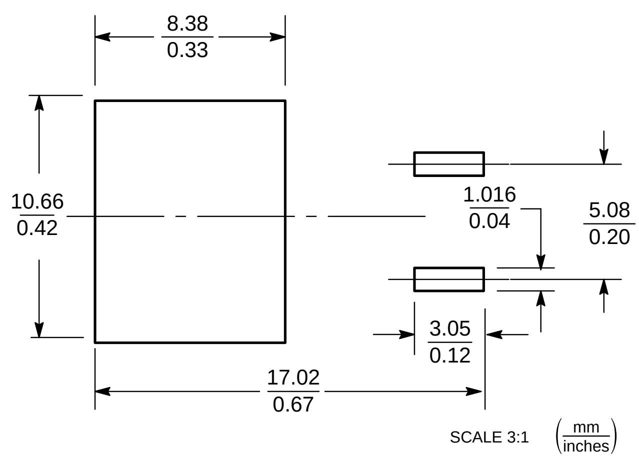
D^2PAK−3
D2T SUFFIX
CASE 936−03
ISSUE B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
F	0.051 REF		1.295 REF	
G	0.100 BSC		2.540 BSC	
H	0.539	0.579	13.691	14.707
J	0.125 MAX		3.175 MAX	
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

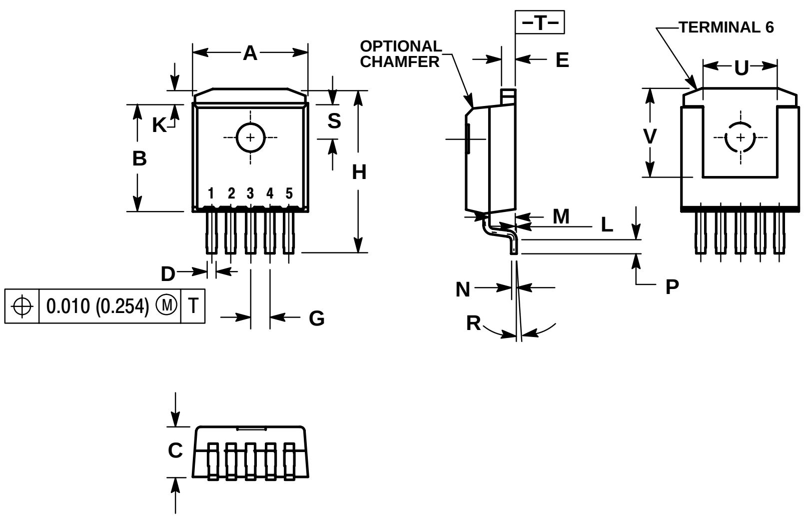
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

D2PAK−5
D2T SUFFIX
CASE 936A−02
ISSUE B



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3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
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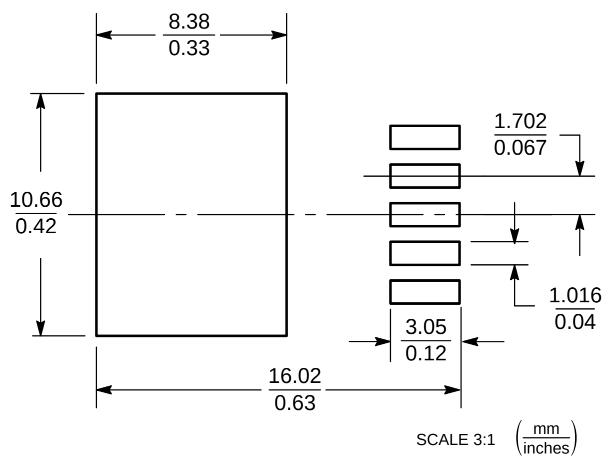
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.386	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
E	0.045	0.055	1.143	1.397
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	5° REF		5° REF	
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

The product described herein (NCP565), may be covered by one or more of the following U.S. patents: 5,920,184; 5,834,926. There may be other patents pending.

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