

## SP8J3

### Transistors

# Switching (−30V, −3.5A)

## SP8J3

#### ●Features

- 1) Low On-resistance. (100mΩ at 4.5V)
- 2) High Power Package.
- 3) High speed switching.
- 4) Low voltage drive. (4.5V)

#### ●Applications

Power switching, DC-DC converter

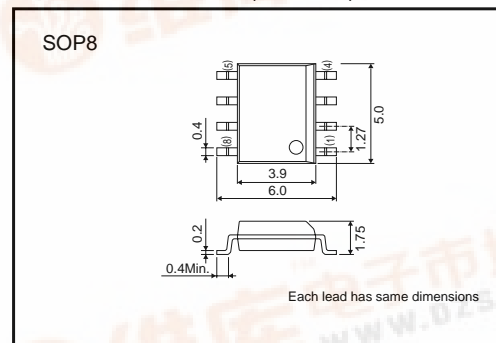
#### ●Structure

Silicon P-channel  
MOS FET

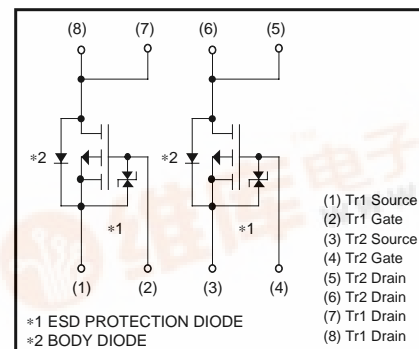
#### ●Packaging specifications

| Type  | Package                      | Taping |
|-------|------------------------------|--------|
|       | Code                         | TB     |
|       | Basic ordering unit (pieces) | 2500   |
| SP8J3 |                              | ○      |

#### ●External dimensions (Unit : mm)



#### ●Equivalent circuit



## Transistors

## ●Absolute maximum ratings (Ta=25°C)

| Parameter                      | Symbol           | Limits          | Unit |
|--------------------------------|------------------|-----------------|------|
| Drain-source voltage           | V <sub>DSS</sub> | −30             | V    |
| Gate-source voltage            | V <sub>GSS</sub> | ±20             | V    |
| Drain current                  | Continuous       | I <sub>D</sub>  | ±3.5 |
|                                | Pulsed           | I <sub>DP</sub> | ±14  |
| Source current<br>(Body diode) | Continuous       | I <sub>S</sub>  | −1.6 |
|                                | Pulsed           | I <sub>SP</sub> | −14  |
| Total power dissipation        | P <sub>D</sub>   | 2.0             | W    |
| Channel temperature            | T <sub>ch</sub>  | 150             | °C   |
| Range of Storage temperature   | T <sub>stg</sub> | −55 to +150     | °C   |

\*1 Pw≤10μs, Duty cycle≤1%

\*2 Mounted on a ceramic board

## ●Electrical characteristics (Ta=25°C)

| Parameter                               | Symbol                | Min. | Typ. | Max. | Unit | Conditions                                       |
|---|-----------------------|------|------|------|------|--|
| Gate-source leakage                     | I <sub>GSS</sub>      | −    | −    | ±10  | μA   | V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V       |
| Drain-source breakdown voltage          | V <sub>(BR) DSS</sub> | −30  | −    | −    | V    | I <sub>D</sub> = −1mA, V <sub>GS</sub> =0V       |
| Zero gate voltage drain current         | I <sub>DSS</sub>      | −    | −    | −1   | μA   | V <sub>DS</sub> = −30V, V <sub>GS</sub> =0V      |
| Gate threshold voltage                  | V <sub>GS(th)</sub>   | −1.0 | −    | −2.5 | V    | V <sub>DS</sub> = −10V, I <sub>D</sub> = −1mA    |
| Static drain-source on-state resistance | R <sub>DS(on)</sub>   | −    | 65   | 90   | mΩ   | I <sub>D</sub> = −3.5A, V <sub>GS</sub> = −10V   |
|   |                       | −    | 100  | 140  | mΩ   | I <sub>D</sub> = −1.75A, V <sub>GS</sub> = −4.5V |
|   |                       | −    | 120  | 165  | mΩ   | I <sub>D</sub> = −1.75A, V <sub>GS</sub> = −4.0V |
| Forward transfer admittance             | Y <sub>fs</sub>       | 1.8  | −    | −    | S    | V <sub>DS</sub> = −10V, I <sub>D</sub> = −1.75A  |
| Input capacitance                       | C <sub>iss</sub>      | −    | 490  | −    | pF   | V <sub>DS</sub> = −10V                           |
| Output capacitance                      | C <sub>oss</sub>      | −    | 110  | −    | pF   | V <sub>GS</sub> =0V                              |
| Reverse transfer capacitance            | C <sub>rss</sub>      | −    | 75   | −    | pF   | f=1MHz   |
| Turn-on delay time                      | t <sub>d(on)</sub>    | −    | 10   | −    | ns   | I <sub>D</sub> = −1.75A                          |
| Rise time                               | t <sub>r</sub>        | −    | 15   | −    | ns   | V <sub>DD</sub> ≒ −15V                           |
| Turn-off delay time                     | t <sub>d(off)</sub>   | −    | 35   | −    | ns   | V <sub>GS</sub> = −10V                           |
| Fall time                               | t <sub>f</sub>        | −    | 10   | −    | ns   | R <sub>L</sub> =8.6Ω                             |
| Total gate charge                       | Q <sub>g</sub>        | −    | 5.5  | −    | nC   | V <sub>DD</sub> ≒ −15V                           |
| Gate-source charge                      | Q <sub>gs</sub>       | −    | 1.5  | −    | nC   | V <sub>GS</sub> = −5V                            |
| Gate-drain charge                       | Q <sub>gd</sub>       | −    | 2.0  | −    | nC   | I <sub>D</sub> = −3.5A                           |

\*Pulsed

## Body diode characteristics (source-drain characteristics)

|                 |                 |   |   |      |   |   |
|-----------------|-----------------|---|---|------|---|---|
| Forward voltage | V <sub>SD</sub> | − | − | −1.2 | V | I <sub>S</sub> = −1.6A, V <sub>GS</sub> =0V |
|-----------------|-----------------|---|---|------|---|---|

## Transistors

## ●Electrical characteristic curves

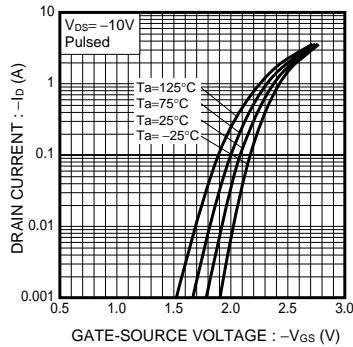


Fig.1 Typical Transfer Characteristics

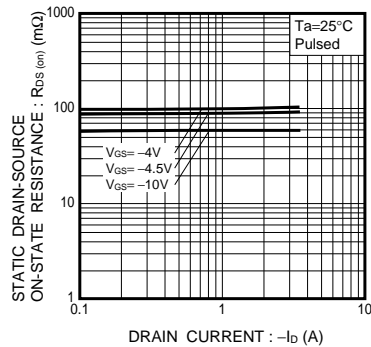


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

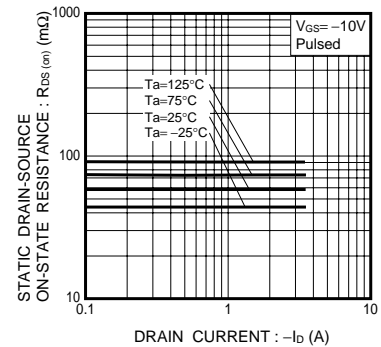


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

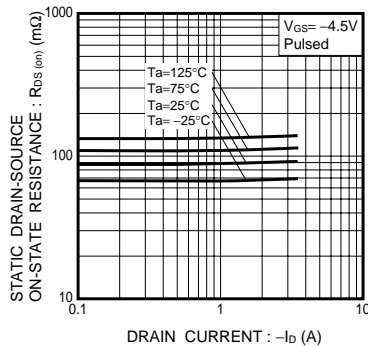


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

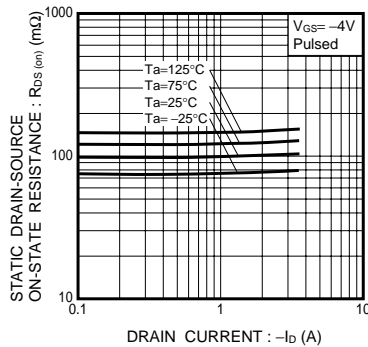


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

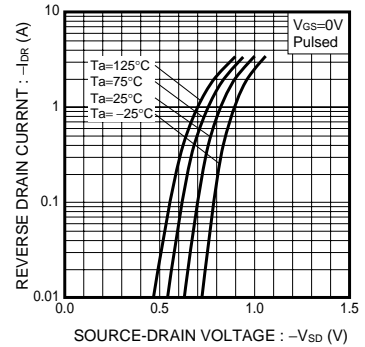


Fig.6 Reverse Drain Current Source-Drain Current

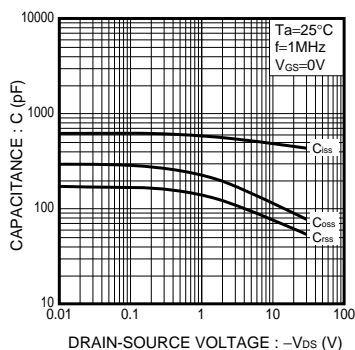


Fig.7 Typical Capacitance vs. Drain-Source Voltage

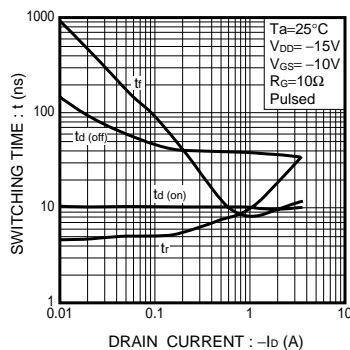


Fig.8 Switching Characteristics

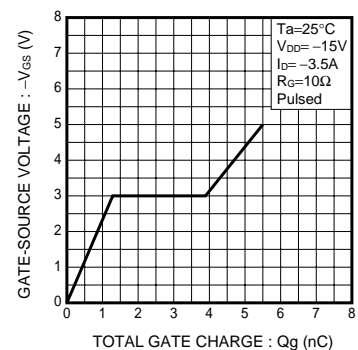


Fig.9 Dynamic Input Characteristics

## Transistors

### ●Measurement circuits

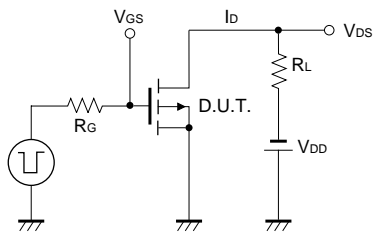


Fig.10 Switching Time Test Circuit

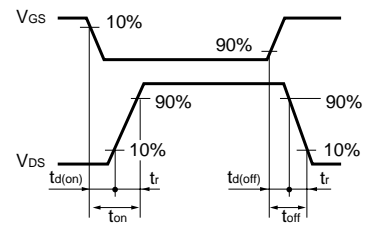


Fig.11 Switching Time Waveforms

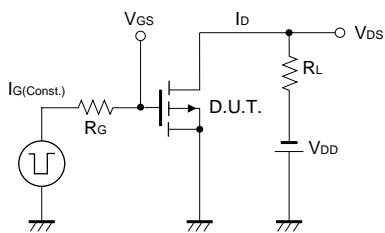


Fig.12 Gate Charge Test Circuit

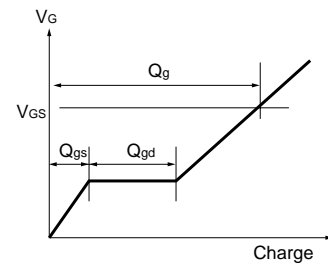


Fig.13 Gate Charge Waveform

## Appendix

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