



# PA83 • PA83A

## FEATURES

- LOW BIAS CURRENT, LOW NOISE — FET Input
- FULLY PROTECTED INPUT — Up to ±150V
- WIDE SUPPLY RANGE — ±15V to ±150V

## APPLICATIONS

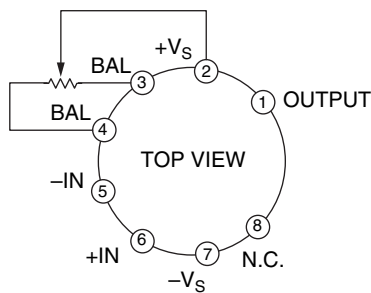
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS & DEFLECTION
- PROGRAMMABLE POWER SUPPLIES UP TO 290V
- ANALOG SIMULATORS

## DESCRIPTION

The PA83 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual (±) supply or 290V with a single supply. Its input stage is protected against transient and steady state overvoltages up to and including the supply rails. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA83 features an unprecedented supply range and excellent supply rejection. The output stage is biased in the class A/B mode for linear operation. Internal phase compensation assures stability at all gain settings without need for external components. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 120V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid circuit utilizes beryllia (BeO) substrates, thick (cermet) film resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible thermal isolation washers and/or improper mounting torque voids product warranty. Please see Application Note 1 "General Operating Considerations".

## EXTERNAL CONNECTIONS

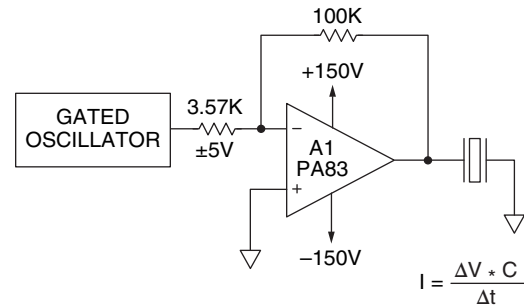


**NOTE:**

1. Pin 8 not internally connected.
2. Input offset trimpot optional. Recommended value of 100KΩ.



8-PIN TO-3 PACKAGE STYLE CE

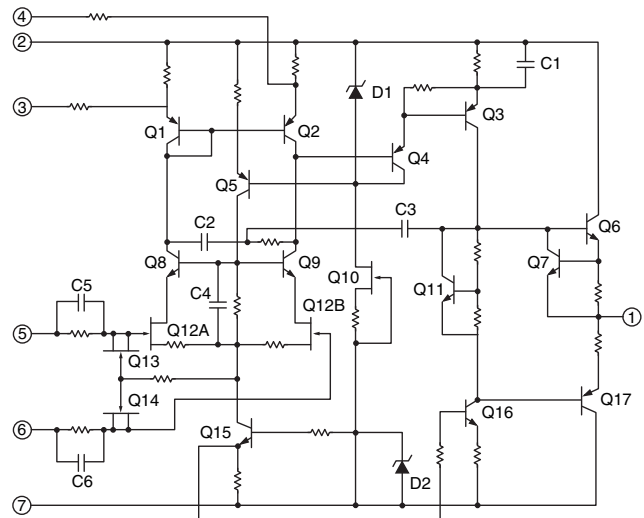


SIMPLE PIEZO ELECTRIC TRANSDUCER DRIVE

## TYPICAL APPLICATION

While piezo electric transducers present a complex impedance, they are often primarily capacitive at useful frequencies. Due to this capacitance, the speed limitation for a given transducer/amplifier combination may well stem from limited current drive rather than power bandwidth restrictions. With its drive capability of 75mA, the PA83 can drive transducers having up to 2nF of capacitance at 40kHz at maximum output voltage. In the event the transducer may be subject to shock or vibration, flyback diodes, voltage clamps or other protection networks must be added to protect the amplifier from high voltages which may be generated.

## EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, +V <sub>S</sub> to -V <sub>S</sub>	300V
OUTPUT CURRENT, within SOA	Internally Limited
POWER DISSIPATION, internal at T <sub>C</sub> = 25°C <sup>1</sup>	17.5W
INPUT VOLTAGE, differential	±300V
INPUT VOLTAGE, common mode	±300V
TEMPERATURE, pin solder - 10s max (solder)	300°C
TEMPERATURE, junction	175°C
TEMPERATURE RANGE, storage	-65 to +150°C
OPERATING TEMPERATURE RANGE, case	-55 to +125°C

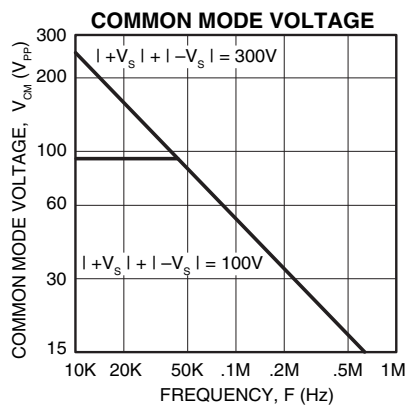
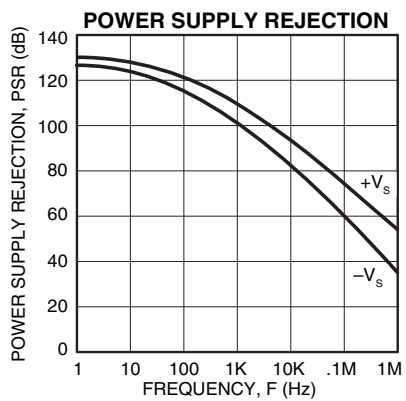
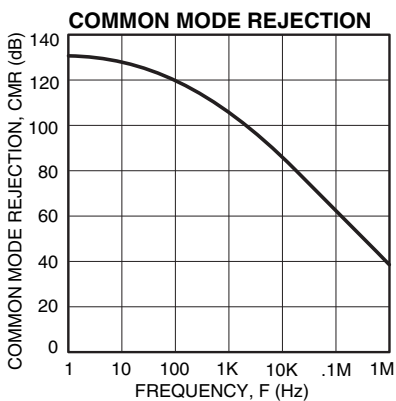
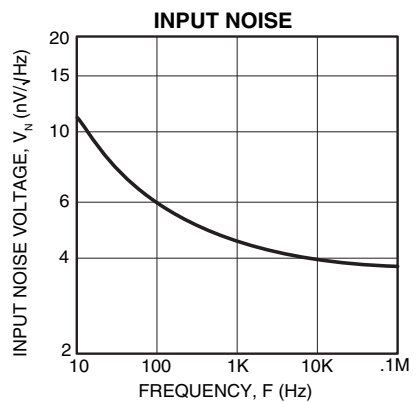
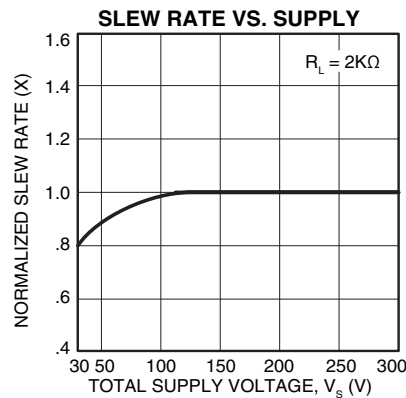
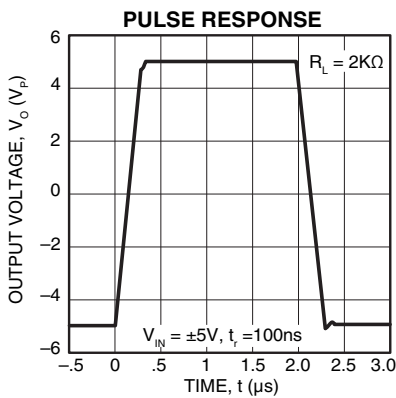
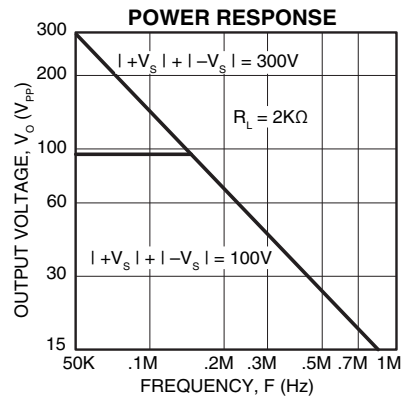
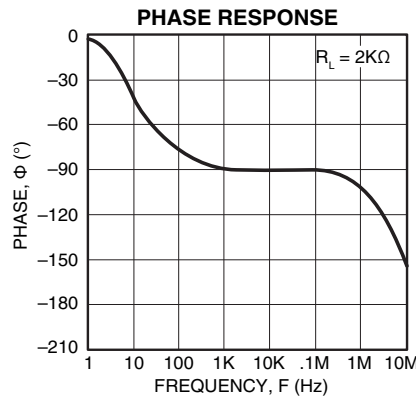
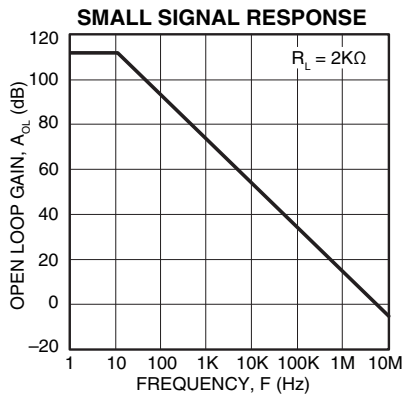
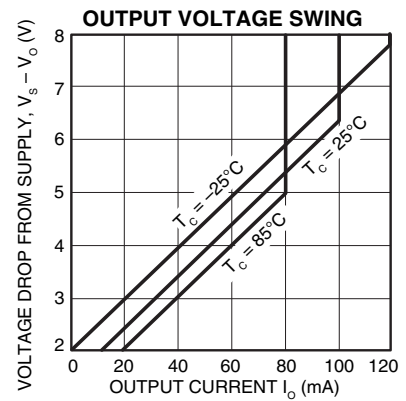
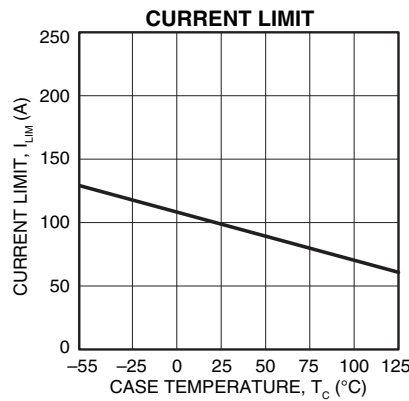
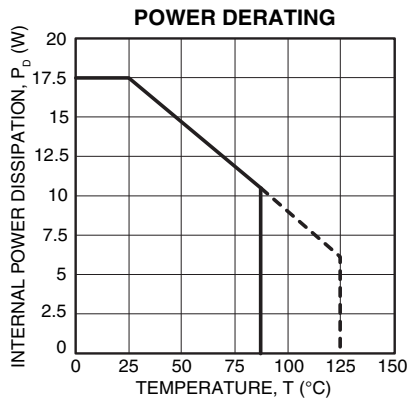
SPECIFICATIONS

PARAMETER	TEST CONDITIONS <sup>2</sup>	PA83			PA83A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT</b>								
OFFSET VOLTAGE, initial	T <sub>C</sub> = 25°C		±1.5	±3		±.5	±1	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±25		±5	±10	μV/°C
OFFSET VOLTAGE, vs. supply	T <sub>C</sub> = 25°C		±.5			±.2		μV/V
OFFSET VOLTAGE, vs. time	T <sub>C</sub> = 25°C		±75			*		μV/jkh
BIAS CURRENT, initial <sup>3</sup>	T <sub>C</sub> = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T <sub>C</sub> = 25°C		.01			*		pA/V
OFFSET CURRENT, initial <sup>3</sup>	T <sub>C</sub> = 25°C		±2.5	±50		±1.5	±10	pA
OFFSET CURRENT, vs. supply	T <sub>C</sub> = 25°C		±.01			*		pA/V
INPUT IMPEDANCE, DC	T <sub>C</sub> = 25°C		10 <sup>11</sup>			*		Ω
INPUT CAPACITANCE	Full temperature range		6			*		pF
COMMON MODE VOLTAGE RANGE <sup>4</sup>	Full temperature range	±V <sub>S</sub> -10			*			V
COMMON MODE REJECTION, DC	Full temperature range		130			*		dB
<b>GAIN</b>								
OPEN LOOP GAIN at 10Hz	T <sub>C</sub> = 25°C, R <sub>L</sub> = 2KΩ	96	116		*	*		dB
UNITY GAIN Crossover FREQ.	T <sub>C</sub> = 25°C, R <sub>L</sub> = 2KΩ		5		3	*		MHz
POWER BANDWIDTH	T <sub>C</sub> = 25°C, R <sub>L</sub> = 10KΩ		60		40	*		kHz
PHASE MARGIN	Full temperature range		60			*		°
<b>OUTPUT</b>								
VOLTAGE SWING <sup>4</sup> , full load	Full temp. range, I <sub>O</sub> = 75mA	±V <sub>S</sub> -10	±V <sub>S</sub> -5		*	*		V
VOLTAGE SWING <sup>4</sup>	Full temp. range, I <sub>O</sub> = 15mA	±V <sub>S</sub> -5	±V <sub>S</sub> -3		*	*		V
CURRENT, peak	T <sub>C</sub> = 25°C	75			*			mA
CURRENT, short circuit	T <sub>C</sub> = 25°C		100			*		mA
SLEW RATE <sup>6</sup>	T <sub>C</sub> = 25°C, R <sub>L</sub> = 2KΩ	20	30		*	*		V/μs
CAPACITIVE LOAD, unity gain	Full temperature range			10			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	μF
SETTLING TIME to .1%	T <sub>C</sub> = 25°C, R <sub>L</sub> = 2KΩ, 10V step		12			*		μs
<b>POWER SUPPLY</b>								
VOLTAGE	T <sub>C</sub> = -55°C to +125°C	±15	±150	±150	*	*	*	V
CURRENT, quiescent	T <sub>C</sub> = 25°C		6	8.5		*	*	mA
<b>THERMAL</b>								
RESISTANCE, AC, junction to case <sup>5</sup>	F > 60Hz		4.26			*		°C/W
RESISTANCE, DC, junction to case	F < 60Hz		6.22	8.57		*	*	°C/W
RESISTANCE, case to air			30			*		°C/W
TEMP. RANGE, case (PA83/PA83A)	Meets full range specification	-25		+85	*		*	°C

- NOTES: \* The specification of PA83A is identical to the specification for PA83 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
  2. The power supply voltage for all tests is the TYP rating, unless otherwise noted as a test condition.
  3. Doubles for every 10°C of temperature increase.
  4. +V<sub>S</sub> and -V<sub>S</sub> denote the positive and negative supply rail respectively. Total V<sub>S</sub> is measured from +V<sub>S</sub> to -V<sub>S</sub>.
  5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
  6. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

**CAUTION**

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



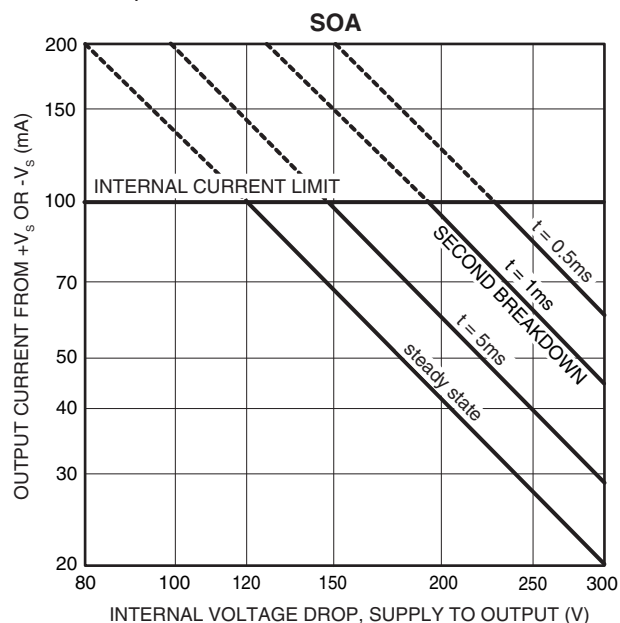
**GENERAL**

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit [www.apexmicrotech.com](http://www.apexmicrotech.com) for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit and heat sink selection. The "Application Notes" and "Technical Seminar" sections contain a wealth of information on specific types of applications. Package outlines, heat sinks, mounting hardware and other accessories are located in the "Packages and Accessories" section. Evaluation Kits are available for most Apex product models, consult the "Evaluation Kit" section for details. For the most current version of all Apex product data sheets, visit [www.apexmicrotech.com](http://www.apexmicrotech.com).

**SAFE OPERATING AREA (SOA)**

The bipolar output stage of this high voltage amplifier has two distinct limitations.

1. The internal current limit, which limits maximum available output current.
2. The second breakdown effect, which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specified limits.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

$\pm V_s$	C(MAX)	L(MAX)
150V	.7 F	1.5H
125V	2.0 $\mu$ F	2.5H
100V	5. $\mu$ F	6.0H
75V	60 $\mu$ F	30H
50V	ALL	ALL

2. Short circuits to ground are safe with dual supplies up to 120V or single supplies up to 120V.
3. Short circuits to the supply rails are safe with total supply voltages up to 120V, e.g.  $\pm 60V$ .
4. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

**INDUCTIVE LOADS**

Two external diodes as shown in Figure 1, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. Be sure the diode voltage rating is greater than the total of both supplies. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

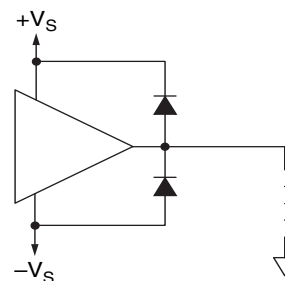


FIGURE 1. PROTECTION, INDUCTIVE LOAD

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