查询PALC22V10B供应商

This is an abbreviated data sheet. Contact a Cypress representative for complete specifications.

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PALC22V10B

Reprogrammable CMOS PAL® Device

Features

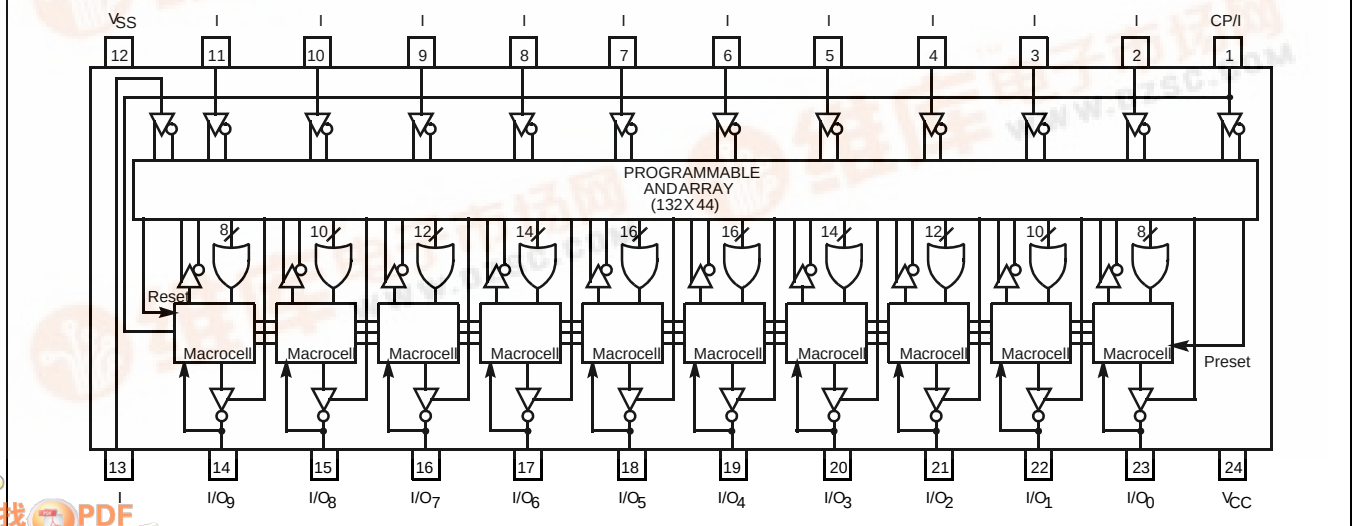
- Advanced second generation PAL architecture
- Low power
  - 90 mA max. standard
  - 100 mA max. military
- CMOS EPROM technology for reprogrammability
- Variable product terms
  - 2 x (8 through 16) product terms
- User-programmable macrocell
  - Output polarity control
  - Individually selectable for registered or combinatorial operation
  - 15 ns commercial and industrial
    - 10 ns t_{CO}
    - 10 ns t_S
    - 15 ns t_{PD}
    - 50 MHz
  - 15 ns and “20 ns” military
    - 10/15 ns t_{CO}
    - 10/17 ns t_S
    - 15/20 ns t_{PD}
    - 50/31 MHz
- Up to 22 input terms and 10 outputs
- Enhanced test features
  - Phantom array
  - Top test
  - Bottom test
  - Preload
- High reliability
  - Proven EPROM technology
  - 100% programming and functional testing
- Windowed DIP, windowed LCC, DIP, LCC, PLCC available

Functional Description

The Cypress PALC22V10B is a CMOS second-generation programmable logic array device. It is implemented with the familiar sum-of-products (AND-OR) logic structure and a new concept, the “Programmable Macrocell.”

The PALC22V10B is executed in a 24-pin 300-mil molded DIP, a 300-mil windowed cerDIP, a 28-lead square ceramic leadless chip carrier, a 28-lead square plastic leaded chip carrier, and provides up to 22 inputs and 10 outputs. When the windowed cerDIP is exposed to UV light, the 22V10B is erased and can then be reprogrammed. The programmable macrocell provides the capability of defining the architecture of each output individually. Each of the 10 potential outputs may be specified as “registered” or “combinatorial.” Polarity of each output may also be individually

Logic Block Diagram (PDIP/CDIP)



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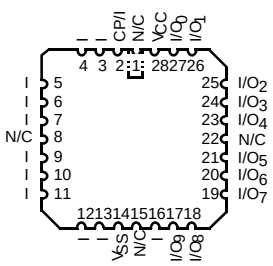
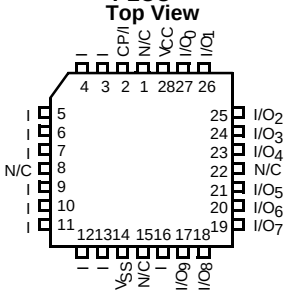
Pin Configurations

LCC
Top View



PLCC
Top View



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