ERICSSON

September 1989

PBL 3762 Subscriber Line Interface Circuit

Description

The PBL 3762 Subscriber Line Interface Circuit (SLIC) is a bipolar integrated circuit in 75 V technology which replaces the conventional transformer based analog line interface circuit in PABX and other telecommunications equipment with a modern, compact solid state design. Not only is required PCB area reduced, but lesser component weight and height result as well. The PBL 3762 has been optimized for low cost and to require only a minimum of external components.

The PBL 3762 programmable, resistive battery feed system can operate with battery supply voltages down to 24 V to reduce line card power dissipation.

The SLIC incorporates loop current, ground key and ring trip detection functions as well as a ring relay driver.

Two- to four-wire and four- to two-wire voice frequency (vf) signal conversion is accomplished by the SLIC in conjunction with either a conventional CODEC/filter or with a programmable CODEC/filter (e.g. SLAC, SiCoFi, Combo II). The programmable CODEC/filter option provides for flexible line card designs with features such as transmit and receive gains, hybrid balance and two-wire impedance adjustable by the system controller. In the conventional CODEC/filter implementation the two-wire impedance is set by a simple external network.

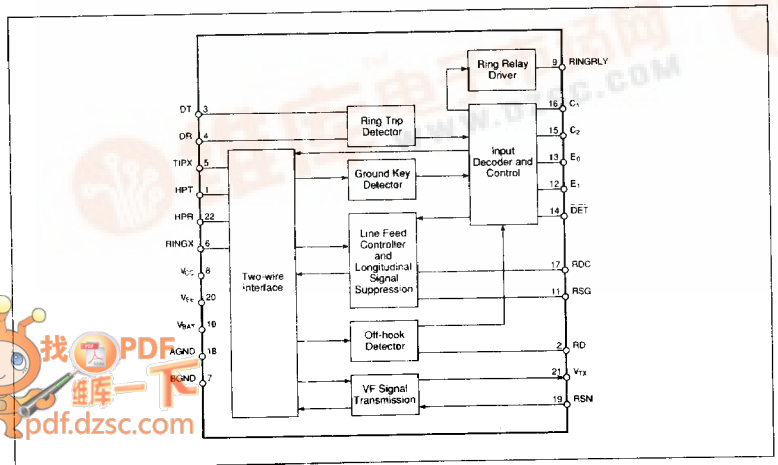
Longitudinal line voltages are suppressed by a feedback loop in the SLIC. Longitudinal balance specifications exceed FCC and EIA requirements.

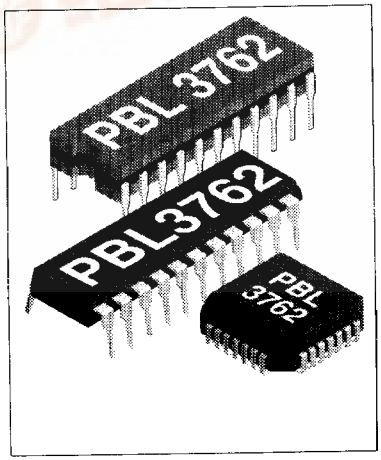
The PBL 3762 package is 22-pin, dual-in-line; 28-pin, j-leaded chip carrier; or 32-pin, ceramic leadless chip carrier.

Refer to Ericsson Components AB family of central office SLICs for applications requiring additional functions.

Key Features

- Battery feed characteristics programmable via external resistors; feed characteristics independent of SLIC battery supply variations
- Battery supply voltage as low as 24 V for power efficient line card designs
- Ring relay driver
- Loop current, ground key and ring trip detection functions
- Programmable loop current detector threshold
- Hybrid function with all types of CODEC/filter devices
- Programmable line terminating impedance, complex or real
- On-hook transmission
- Longitudinal balance specifications in excess of FCC and EIA requirements
- Low 21 mW on-hook power dissipation
- Tip-ring open circuit state
- -40°C to +85°C ambient temperature range





Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Temperature, Humidity				
Storage temperature range	T_{Stg}	-60	+150	°C
Operating temperature range	T_{Case}	-40	+110	°C
Operating junction temperature range	T_J	-40	+140	°C
Storage humidity, Note 1	RH	5	95	% RH
Power supply, $-40°C \le T_{Amb} \le 85°C$				
V_{CC} with respect to AGND	V_{CC}	-0.5	7	V
V_{EE} with respect to AGND	V_{EE}	-7	0.5	V
V_{Bat} with respect to BGND	V_{Bat}	-70	0.5	V
Power dissipation				
Continuous power dissipation at $T_{Amb} \le 70$ °C	P_D		1.5	W
Peak power dissipation at $T_{Amb} \le 70$ °C, t < 100 ms, $t_{Rep} > 1$ sec.	P_{DP}		4	W
Ground				
Voltage between AGND and BGND	V_G	-0.3	0.3	V
Relay driver				
Ring relay supply voltage	V_{Ring}	0	V_{Bat}+75	V
Ring relay current	I_{Ring}		50	mA
Ring trip comparator				
Input voltage	V_{DT}, V_{DR}	V_{Bat}	0	V
Input current	I_{DT}, I_{DR}	-5	5	mA
Digital inputs, outputs (C1, C2, E0, E1, $\overline{DET}$)				
Input voltage	V_{ID}	0	V_{CC}	V
Output voltage ($\overline{DET}$ not active)	V_{OD}	0	V_{CC}	V
Output current ($\overline{DET}$)	I_{OD}		5	mA
TIPX and RINGX terminals, $-40°C < T_{Amb} < 85°C$				
TIPX or RINGX voltage, continuous (referenced to AGND), Note 2	V_{TA}, V_{RA}	V_{Bat}	2	V
TIPX or RINGX, pulse < 10 ms, $t_{Rep} > 10$ s, Note 2	V_{TA}, V_{RA}	V_{Bat} -20V	5	V
TIPX or RINGX, pulse < 1 µs, $t_{Rep} > 10$ s, Note 2	V_{TA}, V_{RA}	V_{Bat} -40V	10	V
TIP or RING, pulse < 250 ns, $t_{Rep} > 10$ s, Note 3	V_{TA}, V_{RA}	V_{Bat} -70V	15	V
TIPX or RINGX current	I_{DCMET}		70	mA

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Case temperature	T_{Case}	-40	100	°C
V_{CC} with respect to AGND	V_{CC}	4.75	5.25	V
V_{EE} with respect to AGND	V_{EE}	-5.25	-4.75	V
V_{Bat} with respect to BGND	V_{Bat}	-58	-24	V

Notes

1. Applicable for ceramic package.
2. A diode in series with the V_{Bat} input increases the permitted continuous voltage and pulse < 10ms to -70V and pulse < 1µs to the greater of |-70V| or $|V_{Bat} - 40V|$.
3. R_{F1}, $R_{F2} \ge 20\ \Omega$ is also required. Pulse is supplied to TIP and RING outside R_{F1}, R_{F2}.

Electrical Characteristics

-40 °C ≤ T_{Amb} ≤ 85 °C, V_{CC} = +5V ±5 %, V_{EE} = -5V ±5%, V_{Bat} = -28V, AGND = BGND, R_{SG} = ∞, R_{DC1} = R_{DC2} = 20 kΩ, Z_L = 600 Ω C_{HP} = 10 nF, C_{DC} = 3.3 µF unless otherwise specified. All pin number references in the text and figures refer to the 22-pin DIP unless otherwise specified.

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Two-wire port						
Overload level, V_{TRO}	1	Z_L = 600 Ω, 1% THD, Note 1	3.1			V_{Peak}
Input impedance, Z_{TR}		Note 2				
Longitudinal impedance, Z_{LT}, Z_{LR}		0 < f < 100 Hz		20	35	Ω/wire
Longitudinal current limit, I_{LT}, I_{LR}		active state			20	mA_{Peak}/wire
		stand-by state			5	mA_{Peak}/wire
Longitudinal to metallic balance, B_{LM}		IEEE standard 455-1985				
		0.2 kHz < f < 4.0 kHz				
		0°C ≤ T_{Amb} ≤ 70°C	63	70		dB
		-40°C ≤ T_{Amb} ≤ 85°C	55	70		dB
Metallic to longitudinal balance, B_{ML}		FCC part 68, paragraph 68.310				
		0.2 kHz < f < 1.0 kHz	60	65		dB
		1.0 kHz < f < 4.0 kHz	50	55		dB
Longitudinal to metallic balance, B_{LME}	2	0.2 kHz < f < 4.0 kHz				
		$B_{LME} = 20 \cdot \text{Log} \left\lvert \frac{E_L}{V_{TR}} \right\rvert$				
		0°C ≤ T_{Amb} ≤ 70°C	63	70		dB
		-40°C ≤ T_{Amb} ≤ 85°C	55	70		dB
Longitudinal to four-wire balance, B_{LFE}	2	0.2 kHz < f < 4.0kHz				
		$B_{LFE} = 20 \cdot \text{Log} \left\lvert \frac{E_L}{V_{TX}} \right\rvert$				
		0°C ≤ T_{Amb} ≤ 70°C	63	70		dB
		-40°C ≤ T_{Amb} ≤ 85°C	55	70		dB
Metallic to longitudinal balance, B_{MLE}	3	0.2 kHz < f < 4.0kHz				
		$B_{MLE} = 20 \cdot \text{Log} \left\lvert \frac{E_{TR}}{V_L} \right\rvert, E_{RX} = 0$				
		0°C ≤ T_{Amb} ≤ 70°C	63	70		dB
		-40°C ≤ T_{Amb} ≤ 85°C	55	55		dB

Figure 1. Overload level, V_{TRO}, two-wire port.

$\frac{1}{\omega C} << R_L$, R_L = 600 ohms

R_T = 600 kohms, R_{RX} = 300 kohms

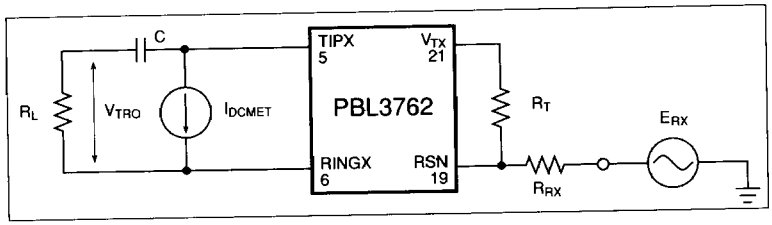
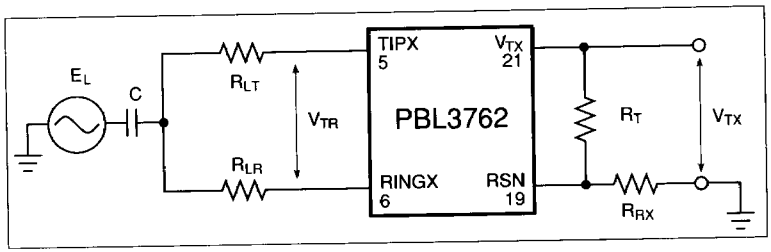


Figure 2. Longitudinal to metallic (B_{LME}) and Longitudinal to four-wire (B_{LFE}) balance.

$\frac{1}{\omega C} << 150$ ohms, $R_{LR} = R_{LT}$ = 300 ohms

R_T = 600 kohms, R_{RX} = 300 kohms



Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to longitudinal balance, B_{FLE}	3	0.2 kHz < f < 4.0 kHz	50	55		dB
		$B_{FLE} = 20 \cdot \text{Log} \left\lvert \frac{E_{RX}}{V_L} \right\rvert$				
		E_{TR} source removed				
Two-wire return loss, r		$r = 20 \cdot \text{Log} \frac{\lvert Z_{TR} + Z_L \rvert}{\lvert Z_{TR} - Z_L \rvert}$				
		$Z_{TR} \approx Z_L$ = nom. 600 Ω				
		0.2 kHz < f < 0.5 kHz	25			dB
		0.5 kHz < f < 1.0 kHz	27			dB
		1.0 kHz < f < 3.4 kHz, Note 3	23			dB
TIPX idle voltage, V_{TI}		active, $I_L = 0$		- 4		V
		stand-by, $I_L = 0$		0		V
RINGX idle voltage, V_{RI}		active, $I_L = 0$		- 24		V
		stand-by, $I_L = 0$		- 28		V
Four-wire transmit port (VTX)						
Overload level, V_{TXO}	4	Load impedance > 20 kΩ, 1% THD, Note 4	3.1			V_{Peak}
Output offset voltage, ΔV_{TX}		0°C ≤ T_{Amb} ≤ 70°C	-25	±5	25	mV
		-40°C ≤ T_{Amb} ≤ 85°C	-40		30	mV
Output impedance, z_{TX}		0.2 kHz < f < 3.4 kHz		<5	20	Ω
TIPX-RINGX metallic voltage to V_{TX} voltage gain, G_{TX}		0.3 kHz < f < 3.4 kHz				
		0°C ≤ T_{Amb} ≤ 70°C	0.988	1.000	1.012	ratio
		-40°C ≤ T_{Amb} ≤ 85°C	0.980	1.000	1.020	ratio
Four-wire receive port (RSN)						
Receive summing node (RSN) dc voltage		I_{RSN} = 0 mA		0		V
Receive summing node (RSN) impedance		0.2 kHz < f < 3.4 kHz			20	Ω
Receive summing node (RSN) current (I_{RSN}) to metallic loop current (I_M) gain, G_{RX}		0.3 kHz < f < 3.4 kHz				
		0°C ≤ T_{Amb} ≤ 70°C	988	1000	1012	ratio
		-40°C ≤ T_{Amb} ≤ 85°C	980	1000	1020	ratio
Frequency response						
Two-wire to four-wire, g_{2-4}	5	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz. E_{RX} = 0 V				
		0°C ≤ T_{Amb} ≤ 70°C	-0.1	±0.03	0.1	dB
		-40°C ≤ T_{Amb} ≤ 85°C	-0.2	±0.03	0.2	dB

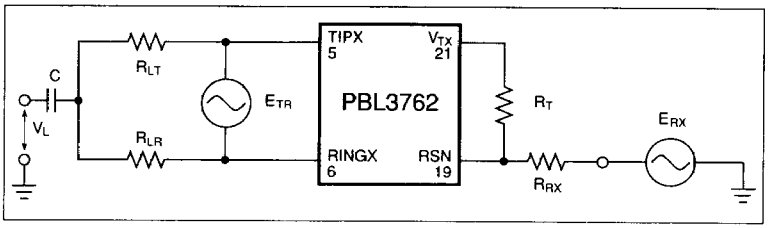


Figure 3. Metallic to longitudinal and four-wire to longitudinal balance.

$\frac{1}{\omega C} << 150$ ohms, $R_{LT} = R_{LR} = 300$ ohms

$R_T = 600$ kohms, $R_{RX} = 300$ kohms

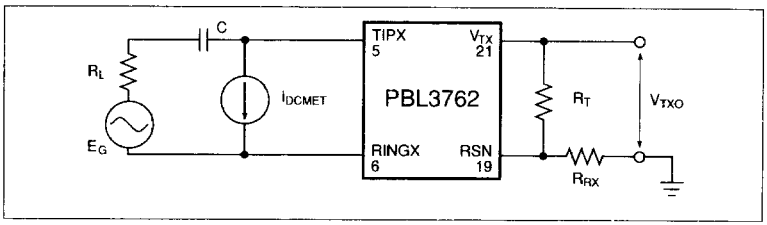


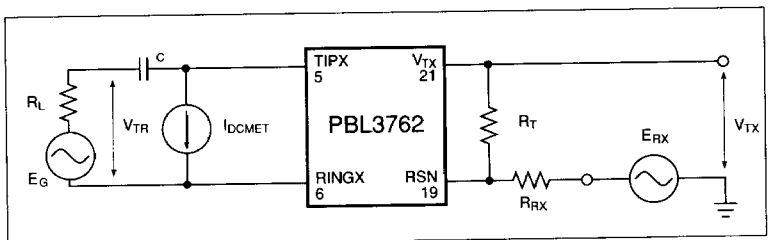
Figure 4. Overload level, V_{TXO}, four-wire transmit port.

$\frac{1}{\omega C} << R_L$, $R_L = 600$ ohms

$R_T = 600$ kohms, $R_{RX} = 300$ kohms

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Four-wire to two-wire, g_{4-2}	5	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz. E_G = 0 V				
		$0°C \le T_{Amb} \le 70°C$	-0.1	±0.03	0.1	dB
		$-40°C \le T_{Amb} \le 85°C$	-0.2	±0.03	0.2	dB
Four-wire to four-wire, g_{4-4}	5	0.3 kHz < f < 3.4 kHz relative to 0 dBm, 1.0 kHz. E_G = 0 V				
		$0°C \le T_{Amb} \le 70°C$	-0.1	±0.03	0.1	dB
		$-40°C \le T_{Amb} \le 85°C$	-0.2	±0.03	0.2	dB
Insertion loss						
Two-wire to four-wire, G_{2-4}	5	0 dBm, 1.0 kHz, Note 5 $G_{2-4} = 20 \cdot \text{Log} \left\lvert \frac{V_{TX}}{V_{TR}} \right\rvert, E_{RX} = 0$				
		$0°C \le T_{Amb} \le 70°C$	-0.1	±0.03	0.1	dB
		$-40°C \le T_{Amb} \le 85°C$	-0.2	±0.03	0.2	dB
Four-wire to two-wire, G_{4-2}	5	0 dBm, 1.0 kHz, Notes 5, 6 $G_{4-2} = 20 \cdot \text{Log} \left\lvert \frac{V_{TR}}{E_{RX}} \right\rvert, E_G = 0$				
		$0°C \le T_{Amb} \le 70°C$	-0.1	±0.03	0.1	dB
		$-40°C \le T_{Amb} \le 85°C$	-0.2	±0.03	0.2	dB
Gain tracking						
Two-wire to four-wire	5	Ref. -10 dBm, 1.0 kHz, Note 7				
		-40 dBm to +3 dBm	-0.1	±0.03	0.1	dB
		-55 dBm to -40 dBm	-0.2	±0.03	0.2	dB
Four-wire to two-wire	5	Ref. -10 dBm, 1.0 kHz, Note 8				
		-40 dBm to +7 dBm	-0.1	±0.03	0.1	dB
		-55 dBm to -40 dBm	-0.2	±0.03	0.2	dB
Noise						
Idle channel noise at two-wire (TIPX-RINGX) or four-wire (V_{TX}) output		C-message weighting		7.5	8.9	dBrnC
		Psophometrical weighting Note 9		-83	-81.6	dBmp
Harmonic distortion						
Two-wire to four-wire		0 dBm, 1.0 kHz test signal		-65	-54	dB
Four-wire to two-wire		0.3 kHz < f < 3.4 kHz		-65	-54	dB
Battery feed characteristics						
Apparent battery voltage			48	50	52	V
Feed resistance to programming resistance conversion factor, K_1 $R_{FEED} = \frac{R_{DC1} + R_{DC2}}{K_1}$			48	50	52	ratio
Stand-by state loop current, I_L, tolerance range		$I_L = \frac{\lvert V_{Bat} \rvert - 3}{R_L + 1800}$ $T_{Amb} = 25°C$	$0.80 \cdot I_L$	I_L	$1.20 \cdot I_L$	mA

Figure 5.
Frequency response, insertion loss, gain tracking.



$\frac{1}{\omega C} << R_L$, R_L = 600 ohms

R_T = 600 kohms, R_{RX} = 300 kohms

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
Loop current detector						
Loop current detector conversion factor, K_2		$R_D = K_2/I_{LTH}$, Note 10				
		$0°C \leq T_{Amb} \leq 70°C$	325	375	420	V
		$-40°C \leq T_{Amb} \leq 85°C$	300	375	450	V
Ground key detector						
I_{TIPX} and I_{RINGX} current difference, ΔI_{LON}, to trigger the ground key detector		$0°C \leq T_{Amb} \leq 70°C$	9	12	16	mA
		$-40°C \leq T_{Amb} \leq 85°C$	8	12	17	mA
I_{TIPX} and I_{RINGX} current difference, ΔI_{LOFF}, to return the triggered ground key detector to idle state		$0°C \leq T_{Amb} \leq 70°C$	4	7	11	mA
		$-40°C \leq T_{Amb} \leq 85°C$	3	7	12	mA
Hysteresis, ΔI_{LTH}		$\lvert\Delta I_{LOn} - \Delta I_{LOff}\rvert$				
		$0°C \leq T_{Amb} \leq 70°C$	3	5	8	mA
		$-40°C \leq T_{Amb} \leq 85°C$	0	5	9	mA
Ring trip detector						
Offset voltage, V_{DTR}		Source resistance, $R_S = 0\ \Omega$	-20	0	20	mV
Input bias current, I_B		$I_B = (I_{DT} + I_{DR})/2$	-500	-100		nA
Input resistance						
unbalanced			1			MΩ
balanced			3			MΩ
Input common mode range, V_{DT}, V_{DR}			V_{Bat}		-2	V
Ring relay driver						
Saturation voltage, V_{OL}		$I_{OL} = 25$ mA		1.0	1.5	V
Off state leakage current, I_{LK}		$V_{OH} = 12$ V			10	µA
Digital inputs (C1, C2, E0, E1)						
Input low voltage, V_{IL}			0		0.8	V
Input high voltage, V_{IH}			2.0		V_{CC}	V
Input low current, I_{IL}		$V_{IL} = 0.4$ V				
C1, C2			-200			µA
E0, E1			-100			µA
Input high current, I_{IH}		$V_{IH} = 2.4$ V			40	µA
Detector output ($\overline{DET}$)						
Output low voltage, V_{OL}		$I_{OL} = 2$ mA			0.45	V
Output high voltage, V_{OH}		$I_{OH} = 100$ µA	2.7			V
Internal pull-up resistor			10	15	20	kΩ
Power dissipation ($V_{Bat} = -28$V)						
P_1		Open circuit state, C_1, $C_2 = 0, 0$		14	23	mW
P_2		Stand-by state, C_1, $C_2 = 1, 1$; on-hook		21	30	mW
		Active state, C_1, $C_2 = 0, 1$				
P_3		On-hook, $R_L = \infty$ ohms		100	150	mW
P_4		Off-hook, $R_L = 0$ ohm		1.9	2.1	W
P_5		Off-hook, $R_L = 300$ ohms		0.7	0.9	W
P_6		Off-hook, $R_L = 600$ ohms		0.4	0.6	W
Temperature Guard						
Junction threshold temperature, T_{JG}				150		°C
Power supply currents ($V_{Bat} = -48$V)						
V_{CC} current, I_{CC}		Open circuit state		1.2	1.5	mA
V_{EE} current, I_{EE}		C_2, $C_1 = 0, 0$		0.5	0.8	mA
V_{Bat} current, I_{Bat}		On-hook		0.2	0.4	mA

Parameter	Ref fig	Conditions	Min	Typ	Max	Unit
V_{CC} current, I_{CC}		Stand-by state		1.4	1.7	mA
V_{EE} current, I_{EE}		C_2, C_1 = 1, 1		0.5	0.8	mA
V_{Bat} current, I_{Bat}		On-hook		0.4	0.6	mA
V_{CC} current, I_{CC}		Active state		4.0	5.5	mA
V_{EE} current, I_{EE}		C_2, C_1 = 1, 0		1.5	2.2	mA
V_{Bat} current, I_{Bat}		On-hook		2.6	3.9	mA
Power supply rejection ratios						
V_{CC} to 2- or 4-wire port		Active State	48	50		dB
V_{EE} to 2- or 4-wire port		C2, C1 = 1, 0	48	50		dB
V_{Bat} to 2- or 4-wire port		50 Hz < f< 3400 Hz, V_n = 100mV	48	50		dB

Notes

1. The overload level is specified at the two-wire port with the signal source at the four-wire receive port.
2. The two-wire impedance is programmable by selection of external component values according to:

   $Z_{TRX} = Z_T / |G_{TX} G_{RX}|$ where:

   Z_{TRX} = impedance between the TIPX and RINGX terminals

   Z_T = programming network between the V_{TX} and RSN terminals

   G_{TX} = transmit gain, nominally = 1

   G_{RX} = receive current gain, nominally = -1000 (current defined as positive flowing into the receive summing node, RSN, and when flowing from tip to ring).
3. Higher return loss values can be achieved by adding a reactive component to R_T, the two-wire terminating impedance programming resistance, e.g. by dividing R_T into two equal halves and connecting a capacitor from the common point to ground. For R_T = 560 kohms this capacitor would be approximately 30 pF. Increasing C_{HP} to 0.033 µF improves low frequency return loss.
4. The overload level is specified at the four-wire transmit port, V_{TX}, with the signal source at the two-wire port. Note that the gain from the two-wire port to the four-wire transmit port is G_{TX} = 1.
5. Fuse resistors R_F impact the insertion loss as explained in the text, section Transmission. The specified insertion loss is for R_F = 0.
6. The specified insertion loss tolerance does not include errors caused by external components.
7. The level is specified at the two-wire port.
8. The level is specified at the four-wire receive port and referenced to a 600 ohm impedance level.
9. The two-wire idle noise is specified with the port terminated in 600 ohms (R_L) and with the four-wire receive port grounded (E_{RX} = 0; see figure 5).

   The four-wire idle noise at V_{TX} is specified with the two-wire port terminated in 600 ohms (R_L). The noise specification is referenced to a 600 ohm impedance level at V_{TX}. The four-wire receive port is grounded (E_{RX} = 0).
10. The loop current value, at which the loop current detector changes state, is programmable by selecting the value of resistor R_D. R_D connects between pins RD (pin 2) and V_{EE} (pin 20). The programming resistor can be calculated as $R_D = K_2 / I_{LTH}$, where K_2 is the conversion factor and I_{LTH} is the loop current threshold. Numerical values for K_2 are given in the table. For further information, refer to the section "Loop monitoring functions, Loop current detector."

Pin Descriptions

Refer to figure 6. Note: All pin number references in the text and figures refer to the 22-pin DIP unless otherwise specified.

DIP	PLCC	Symbol	Description
1	21	HPT	Tip side of ac/dc separation capacitor C_{HP}. Other end of C_{HP} connects to pin 22, HPR.
2	22	RD	Off-hook detector programming resistor R_D in parallel with filter capacitor C_D connect from RD to V_{EE}.
3	23	DT	Inputs to the ring trip comparator. With DR more positive than DT the detector output, $\overline{DET}$ (pin 14), is at
4	25	DR	logic level low, indicating off-hook condition. The ring trip network connects to these two inputs.
5	27	TIPX	The TIPX and RINGX pins connect to the tip and ring leads of the two-wire.
6	28	RINGX	interface via overvoltage protection components and ring relay (and optional test relay).
7	2	BGND	Battery ground.
8	4	V_{CC}	+5V power supply.
9	5	RINGRLY	Ring relay driver output. Open collector. Sinks 50 mA to BGND. Must be protected by external inductive kick-back diode.

10	6	V_{Bat}	Battery supply voltage, -24V to -58V. Negative with respect to BGND (pin 7).
11	7	RSG	Saturation guard programming resistor, R_{SG}, connects from this terminal to V_{EE} (pin 20). Refer to section Battery feed for detailed information.
12	8	E1	TTL compatible enable input. Enables desired detector to be gated to the $\overline{DET}$ (pin 14) output. Refer to section Enable inputs for detailed information.
13	9	E0	TTL compatible enable input. Enables the $\overline{DET}$ (pin 14) output when set to logic level low and disables the $\overline{DET}$ output when set to logic level high. Refer to section Enable inputs for detailed information.
14	11	$\overline{DET}$	Detector output. Inputs C1 (pin 16) and C2 (pin 15) together with enable inputs E0 (pin 13) and E1 (pin 12) select one of the three detectors to be connected to the $\overline{DET}$ output. A logic low at the enabled $\overline{DET}$ output indicates a triggered detector condition. The $\overline{DET}$ output is open collector with internal pull-up resistor (approximately 15 kohms to V_{CC} (pin 8)).
15	12	C2	C1 and C2 are TTL compatible inputs controlling the SLIC operating states.
16	13	C1	Refer to section Control inputs for details.
17	14	RDC	Constant current feed is programmed by two resistors connected in series from this pin to the receive summing node (RSN, pin 19). The resistor junction point is decoupled to AGND to isolate the ac signal components.
18	15	AGND	Analog and digital ground. Analog ground is a quiet ground for vf signal processing circuits.
19	16	RSN	Receive summing node. 1 000 times the current (dc and ac) flowing into this pin equals the metallic (transversal) current flowing from RINGX (pin 6) to TIPX (pin 5). Programming networks for constant current feed, two- wire impedance and receive gain connect to the receive summing node.
20	18	V_{EE}	-5V power supply.
21	19	V_{TX}	Transmit vf output. The ac voltage difference between TIPX (pin 5) and RINGX (pin 6), the ac metallic voltage, is reproduced as an unbalanced AGND referenced signal at V_{TX} with a gain of one. The two-wire impedance programming network connects between V_{TX} and RSN (pin 19).
22	20	HPR	Ring side of ac/dc separation capacitor C_{HP}. Other end of C_{HP} capacitor connects to pin 1, HPT.
	3	N/C	Some of the pins marked N/C will be used for heat sinking and may be internally connected to V_{Bat}. Contact the factory for further information before making external connections to these pins.
	10	N/C	
	17	N/C	
	24	N/C	
	26	$TIPX_{Sense}$	$TIPX_{Sense}$ and $RINGX_{Sense}$ are internally connected to TIPX and RINGX respectively. $TIPX_{Sense}$ and $RINGX_{Sense}$
	1	$RINGX_{Sense}$	are used during manufacturing, but require no connections in SLIC applications, i.e. leave open.

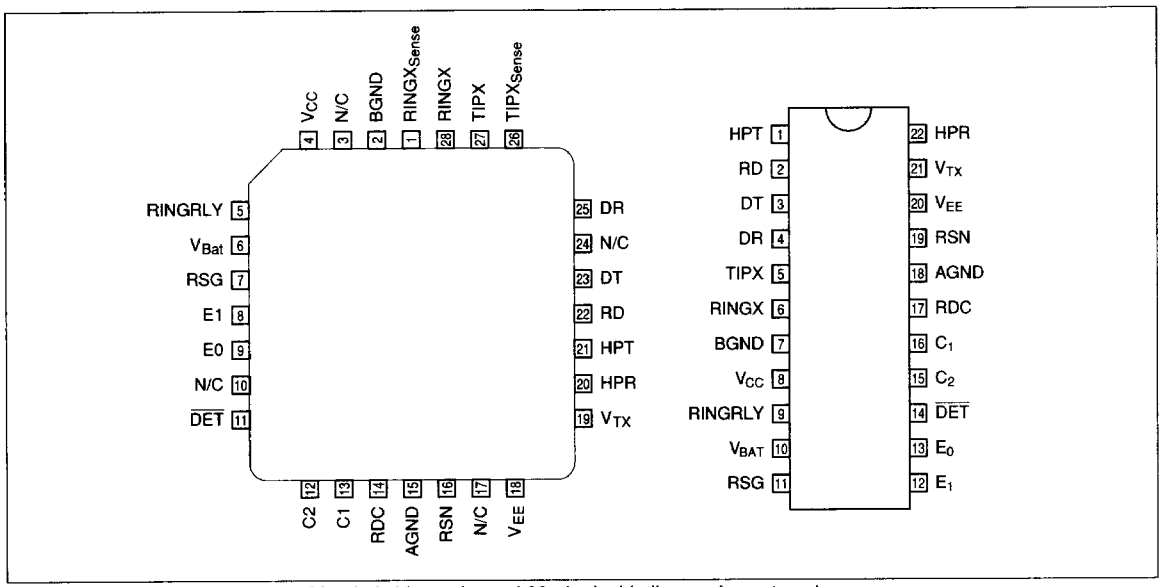


Figure 6. Pin configuration, 28-pin j-leaded chip carrier and 22-pin dual-in line package, top view.

Functional Description and Applications Information

Transmission

General

A simplified ac model of the transmission circuits is shown in figure 7. Circuit analysis yields:

$$V_{TR} = V_{TX} + I_M \cdot 2R_F \quad (1)$$

$$\frac{V_{TX}}{Z_T} + \frac{V_{RX}}{Z_{RX}} = \frac{I_M}{1000} \quad (2)$$

$$V_{TR} = E_G - I_M \cdot Z_L \quad (3)$$

where:

- V_{TX} is a ground referenced unity gain version of the ac metallic voltage between the TIPX and RINGX terminals.
- V_{TR} is the ac metallic voltage between tip and ring.
- E_G is the line open circuit ac metallic voltage.
- I_M is the ac metallic current.
- R_F is a fuse resistor.
- Z_L is the line impedance.
- Z_T determines the SLIC TIPX to RINGX impedance.
- Z_{RX} controls four- to two-wire gain.
- V_{RX} is the analog ground referenced receive signal.

Two-wire impedance

To calculate Z_{TR}, the impedance presented to the two-wire line by the SLIC including the fuse resistors R_F, let:

$V_{RX} = 0$. Then from (1) and (2):

$$Z_{TR} = Z_T/1000 + 2R_F$$

Thus with Z_{TR} and R_F known:

$$Z_T = 1000 \cdot (Z_{TR} - 2R_F)$$

Example:

Calculate Z_T to make $Z_{TR} = 900\ \Omega$ in series with 2.16 µF. $R_F = 20\ \Omega$

$$Z_T = 1000 \cdot \left(900 + \frac{1}{j\omega \cdot 2.16 \cdot 10^{-6}} - 2 \cdot 20\right)$$

which yields:

$Z_T = 860\ k\Omega$ in series with 2.16 nF.

Two-wire to four-wire gain

From (1) and (2) with $V_{RX} = 0$:

$$G_{2\text{-}4} = \frac{V_{TX}}{V_{TR}} = \frac{Z_T/1000}{Z_T/1000 + 2R_F}$$

Four-wire to two-wire gain

From (1), (2) and (3) with $E_G = 0$:

$$G_{4\text{-}2} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L}{Z_T/1000 + 2R_F + Z_L}$$

For applications where $Z_T/1000 + 2R_F$ is chosen to be equal to Z_L the expression for $G_{4\text{-}2}$ simplifies to:

$$G_{4\text{-}2} = -\frac{Z_T}{Z_{RX}} \cdot \frac{1}{2}$$

Four-wire to four-wire gain

From (1), (2) and (3) with $E_G = 0$:

$$G_{4\text{-}4} = \frac{V_{TR}}{V_{RX}} = -\frac{Z_T}{Z_{RX}} \cdot \frac{Z_L + 2R_F}{Z_T/1000 + 2R_F + Z_L}$$

Hybrid function

The PBL 3762 SLIC forms a particularly flexible and compact line interface when used with a SLAC (Subscriber Line Audio Processing Circuit) or other programmable CODEC/filters. The SLAC allows for system controller adjustment of hybrid balance to accommodate different line impedances without change of hardware. In addition, the SLAC permits transmit and receive gain adjustments in 0.1 dB steps. Please, refer to SLAC or other programmable CODEC/filters data sheets for design information.

The hybrid function can also be implemented utilizing the uncommitted amplifier in conventional CODEC/filter combinations. Please, refer to figure 8. Via impedance Z_B a current proportional to V_{RX} is injected into the summing node of the combination CODEC/filter amplifier. As can be seen from the expression for the four-wire to four-wire gain a voltage proportional to V_{RX} is returned to V_{TX}. This voltage is converted by R_{TX} to a current flowing into the same summing node. These currents can be made to cancel by letting:

$$\frac{V_{TX}}{R_{TX}} + \frac{V_{RX}}{Z_B} = 0 \qquad (E_G = 0)$$

The four-wire to four-wire gain, $G_{4\text{-}4}$, includes the required phase shift and thus the balance network Z_B can be calculated from:

$$Z_B = -R_{TX} \cdot \frac{V_{RX}}{V_{TX}}$$

$$= R_{TX} \cdot \frac{Z_{RX}}{Z_T} \cdot \frac{Z_T/1000 + 2R_F + Z_L}{Z_L + 2R_F}$$

Example: calculate R_B for the line interface shown in figure 10.

$$R_B = 20 \cdot 10^3 \cdot \frac{634 \cdot 10^3}{562 \cdot 10^3} \cdot \frac{562 \cdot 10^3/1000 + 2 \cdot 20 + 600}{600 + 2 \cdot 20}$$

= 42.37 kohms, i.e. standard value 42.2 kohms, 1%

Longitudinal impedance

A feed back loop counteracts longitudinal voltages at the two-wire port by injecting longitudinal currents in opposing phase. Thus longitudinal disturbances will appear as longitudinal currents and the TIPX and RINGX

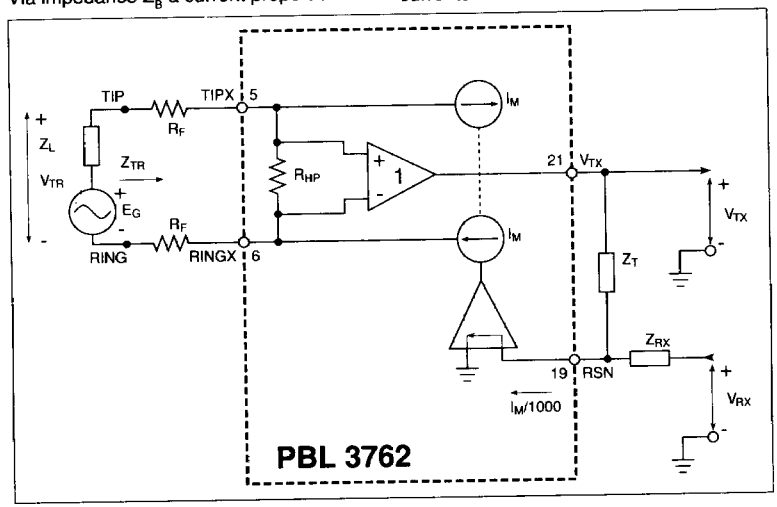


Figure 7. Simplified ac transmission circuit.

terminals will experience very small longitudinal voltage excursions, leaving metallic voltages well within the SLIC common mode range. This is accomplished by comparing the instantaneous two-wire longitudinal voltage to an internal longitudinal reference voltage, V_{LBias}. As shown below, the SLIC appears as 20 ohms per wire to longitudinal disturbances. It should be noted that longitudinal currents may exceed the DC loop current without disturbing the vf transmission. Refer to figure 9.

Circuit analysis yields:

$(V_L/2 + V_L/2)/R_{LI} = I_L/1000$

which reduces to $R_{LT} = R_{LR} = V_L/I_L = 20$ ohms where:

R_{LI} = 20 kohms
$R_{LT} = R_{LR}$ = longitudinal resistance/wire
V_L = longitudinal voltage at TIPX, RINGX
I_L = longitudinal current

Ac transmission circuit stability

To ensure stability of the feedback loop shown in block diagram form in figure 7 two compensation capacitors C_{TC} and C_{RC} are required. Figure 10 includes these capacitors. Recommended value is 2200 pF.

Ac - dc separation capacitor, C_{HP}

The high pass filter capacitor connected between terminals 1 and 22 provides the separation between circuits sensing tip-ring dc conditions and circuits processing ac signals. A C_{HP} value of 10 nF will position the low end frequency response 3dB break point at 48 Hz (f_{3dB}) according to $f_{3dB} = 1/(2 \cdot \pi \cdot R_{HP} \cdot C_{HP})$ where $R_{HP} \approx 330$ kohms.

Battery Feed

The block diagram in figure 11 shows the PBL 3762 battery feed system.

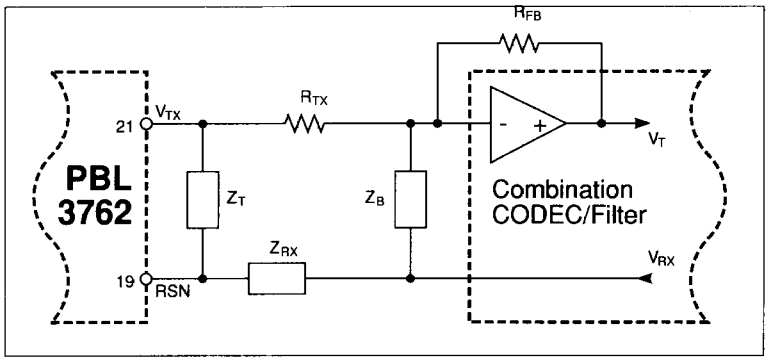


Figure 8. Hybrid function.

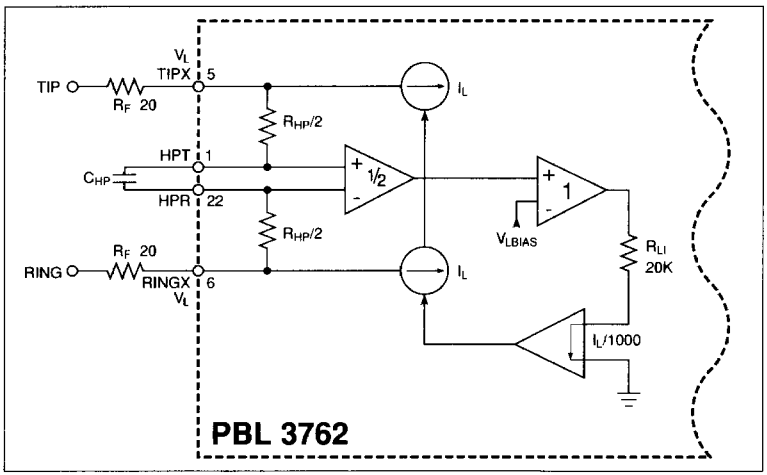


Figure 9. Longitudinal impedance.

For a tip to ring dc voltage V_{TR} less than the saturation guard reference voltage V_{SGRef}, the SLIC emulates a resistive feed characteristic with an apparent battery voltage of 50 V. The apparent battery voltage is independent of the actual battery voltage, V_{Bat}, connected to the SLIC.

With the tip to ring dc voltage V_{TR} exceeding V_{SGRef}, the feed characteristic changes to a nearly-constant voltage feed. This is to prevent the tip and ring drive amplifiers from distorting the ac signal as might have otherwise occurred due to insufficient voltage margin between V_{TR} and V_{Bat} (pin 10). Thus the SLIC automatically adjusts the tip to ring dc voltage V_{TR} to the maximum safe value.

With the SLIC in the stand-by state (C_1, C_2 = 1,1) a high resistance feed characteristic is enabled.

The following text explains the three battery feed cases in more detail.

Case 1: SLIC in the active state; $V_{TR} < V_{SGRef}$.

In the active state $C_1 = 0$ and $C_2 = 1$. In this operating state tip to ring voltages V_{TR} less than V_{SGRef} cause the block titled saturation guard (figure 11) to be disabled, i.e. its output is equal to zero. For this case circuit analysis yields:

$$V_{TR} = 50 \cdot \frac{R_L}{R_L + R_{DC}/50} \quad \text{or,}$$

$$I_L = \frac{50}{R_L + R_{Feed}}$$

where:

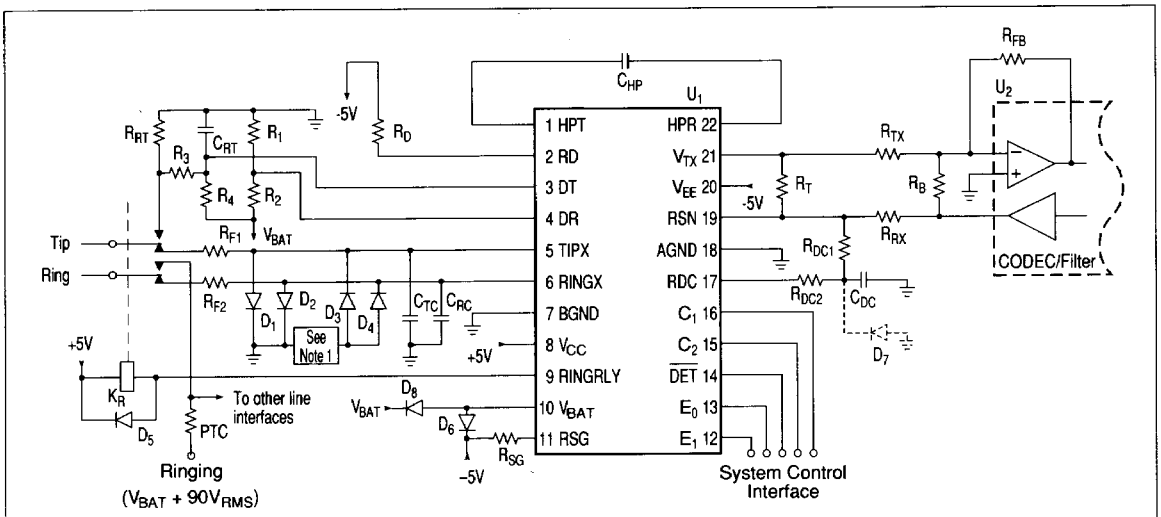
I_L = the loop current
R_L = the line resistance
R_{DC} = $(= R_{DC1} + R_{DC2})$ the programming resistance which sets the equivalent feed resistance, $R_{Feed} = R_{DC}/50$
V_{TR} = the tip to ring dc metallic voltage

Note that for simplicity the fuse resistors R_F have not been included.

For tip to ring voltages V_{TR} less than V_{SGRef} the PBL 3762 thus emulates a resistive battery feed with 50 V apparent battery and a feed resistance, R_{Feed}, equal to $R_{DC}/50$.

Capacitor C_{DC} at the R_{DC1} - R_{DC2} common point removes vf signals from the battery feed control loop. C_{DC} is calculated according to:

$$C_{DC} = T \cdot \left(\frac{1}{R_{DC1}} + \frac{1}{R_{DC2}}\right), \text{ where } T = 30\text{ms}$$



U1	SLIC (Subscriber Line Interface Circuit) PBL 3762	R_2	910 kohms, 5%, 1/4 W	C_{HP}	0.033 µF, 20%, 100V
U2	Combination CODEC/Filter, e.g. TP3054 or programmable CODEC/ filter, e.g. SLAC	R_4	1.2 Mohms, 5%, 1/4 W	C_{RT}	0.39 µF, 20%, 100V
		R_B	42.2 kohms, 1%, 1/4 W	C_{TC}, C_{RC}	2200 pF, 20%, 100V
K_R	Relay, 2C contacts, 12V coil	R_D	39 kohms, 5%, 1/4 W		
D_1 - D_4	Diode, 100V, 3A	R_{DC1}, R_{DC2}	20 kohms, 5%, 1/4 W	Note 1:	The D_3 and D_4 anodes may be connected directly to the V_{Bat} supply rail in applications exposed only to low energy transients. In other applications, it is advisable to clamp negative transients to ground, which then requires the anodes of D_3 and D_4 to be connected to ground via a device (e.g. General Semiconductor Transzorb, RCA Surgector) which conducts only when exposed to the overvoltages.
D_5, D_6	Diode, 1N4454	R_{FB}	24.3 kohms, 1%, 1/4 W		
D_8	Diode, e.g. 1N4148	R_{RX}	634 kohms, 1%, 1/4 W		
R_{F1}, R_{F2}	Line resistor, 20 ohms, 1% match, Ericsson Components PBR 5067	R_{SG}	Open Circuit		
		R_T	562 kohms, 1%, 1/4 W		
R_1, R_3	200 kohms, 5%, 1/4 W	R_{TX}	20 kohms, 1%, 1/4 W		
		R_{RT}	150 ohms, 5%, 2 W		
		C_{DC}	3.3 µF, 20%, 10V		

Figure 10. Single-channel subscriber line interface with PBL 3762 and combination CODEC/filter.

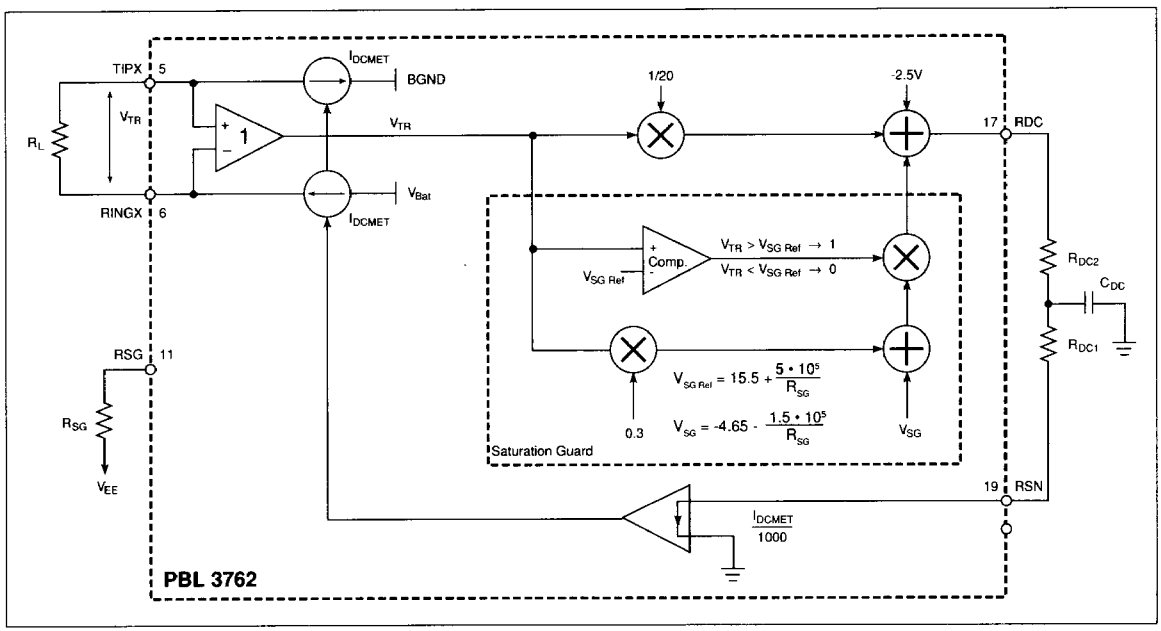


Figure 11. Battery feed (C_{TC}, C_{RC} = 1.0; active state).

Note that $R_{DC1} = R_{DC2}$ yields minimum C_{DC} value. For this case the feed resistance programming resistors can be calculated from $R_{DC1} = R_{DC2} = R_{Feed} \cdot 50$, where R_{Feed} is the desired feed resistance.

Case 2: SLIC in the active state; $V_{TR} > V_{SGRef}$

In the active state $C_1 = 0$ and $C_2 = 1$. The saturation guard reference voltage is user programmable according to:

$$V_{SGRef} = 15.5 + \frac{5 \cdot 10^5}{R_{SG}}$$

where:

R_{SG} = saturation guard reference programming resistor in ohms.

V_{SGRef} = saturation guard reference voltage in volts.

Once the dc metallic voltage, V_{TR}, exceeds the saturation guard reference voltage, V_{SGRef}, the saturation guard becomes active and the following expression describes the battery feed characteristic:

$$V_{TR} = \frac{(20.4 + 4.29 \cdot 10^5/R_{SG}) \cdot R_L}{R_L + R_{DC}/350}$$

where R_{SG}, R_L and V_{TR} have the same meaning as described above. The reduced apparent battery voltage limits the open circuit dc voltage to:

$$V_{TR} = 20.4 + \frac{4.29 \cdot 10^5}{R_{SG}}$$

The saturation guard ensures the line drive amplifiers of sufficient bias voltage at high R_L values or even at open loop by limiting the tip-to-ring dc voltage. Without this function, distortion of the vf signal would result. Of interest for some applications is, that the saturation guard permits on-hook (open loop) transmission. The function of the saturation guard is user-programmable through R_{SG}, which can be calculated from:

$$R_{SG} = \frac{4.29 \cdot 10^5}{\frac{(|V_{Bat}| - V_{Margin}) \cdot [R_{LMax} + (R_{DC1} + R_{DC2})/350]}{R_{LMax}} - 20.4}$$

which for $R_{LMax} \rightarrow \infty$ simplifies to:

$$R_{SG} = \frac{4.29 \cdot 10^5}{|V_{Bat}| - V_{Margin} - 20.4}$$

where

R_{LMax} = maximum loop resistance in ohms

V_{TRMax} = tip-to-ring dc voltage at maximum loop resistance in volts

V_{Margin} = $|V_{Bat}| - V_{TRMax} = 8V$ to allow distortion-free transmission of a $3.1V_{Peak}$ vf signal

Note that at $V_{Bat} = -28.4V$ and $V_{Margin} = 8V$, $R_{SG} \rightarrow \infty$, i.e. the R_{SG} terminal can be left open. For higher battery voltages, e.g. -48V, a finite value R_{SG} must be calculated and installed or the tip-to-ring dc voltage would be limited to 20.4V, thus not yielding the expected loop resistance range.

In many applications a less than $3.1V_{Peak}$ maximum vf signal is satisfactory. In such applications, V_{Margin} may be set to less than 8V in accordance with the diagram shown in figure 12. The maximum tip-to-ring dc voltage will consequently be somewhat greater and a correspondingly longer loop can be accommodated.

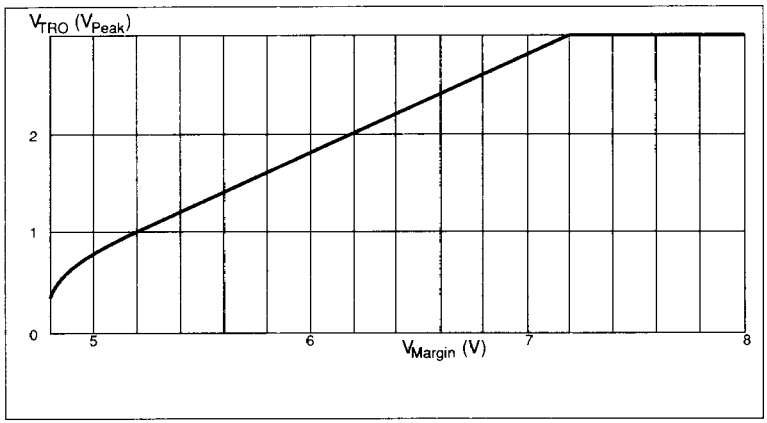


Figure 12. Overload level, V_{TRO}, as a function of V_{Margin}

Case 3: SLIC in the stand-by state.

In the stand-by state, $C_1 = 1$ and $C_2 = 1$. With the SLIC operating in the stand-by, power saving state the tip and ring drive amplifiers are disconnected and a high resistance battery feed is engaged. The loop current can be calculated from:

$$I_L \approx \frac{|V_{Bat}| - 3\ V}{R_L + 1800\ \Omega}$$

where:

I_L = loop current

R_L = loop resistance

V_{Bat} = battery supply voltage

Figure 14 illustrates three PBL 3762 battery feed curves. Note the knee where the saturation guard becomes active. The R_{SG} terminal is left open for these three curves, i.e. $V_{SGRef} = 15.5$ V. $R_{SG} = \infty$ is selected for operation with $-28\ V < V_{Bat} < -24$ V. For other V_{Bat} values the knee can be transported along the R_L axis by calculation of R_{SG} as described in the text.

Figure 16 illustrates the power dissipation advantage of PBL 3762 line feed with $V_{Bat} = -28$ V over a conventional –48 V resistive feed.

PBL 3762 battery feed in long loop applications

To feed a long loop, e.g. 2000 ohms, from a 50 V battery with a minimum of 16 mA to 18 mA demands a low feed resistance value. While the PBL 3762 is capable of meeting such requirements, two other parameters must be considered simultaneously: short loop SLIC power dissipation and vf signal amplitude at long loops.

The short circuit SLIC power dissipation, P_{STot}, caused by the loop current is

$$P_{STot} = I_{LS} \cdot (V_{BAT} - I_{LS} \cdot 2R_F) + 0.1W$$

where V_{Bat} is the battery voltage connected to the SLIC at pin 10 and R_F is the fuse resistance, 20 Ω.

$$I_{LS} = \frac{50}{(R_{DC1} + R_{DC2})/50 + 2R_F}$$

is the short circuit loop current and $(R_{DC1} + R_{DC2})/50$ is the feed resistance.

Consult the power derating diagram, figure 13, to determine allowable safe dissipation. For extreme reliabilty requirements select 110°C maximum junction temperature and for normal requirements 140°C. Note that a short circuited loop is not a normal operating condition. The terminating equipment will

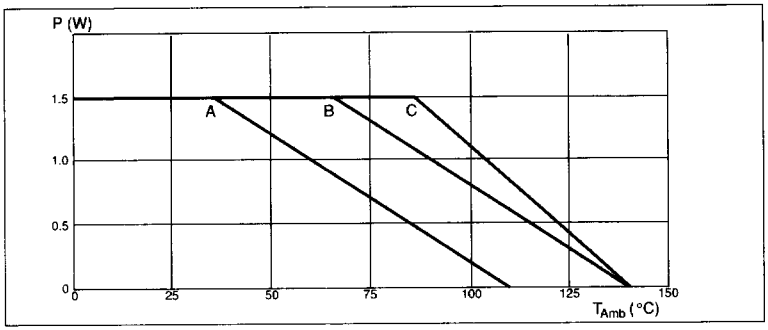


Figure 13. Power derating.

$$P = \frac{T_J - T_{Amb}}{\Theta_{JA}}$$

P = Power

T_{Amb} = Ambient Temperature

Curve A: T_J = 110°C, Junction Temperature
Θ_{JA} = 50°C/W, Junction-to-ambient Thermal Resistance

Curve B: T_J = 140°C, Junction Temperature
Θ_{JA} = 50°C/W, Junction-to-ambient Thermal Resistance

Curve C: T_J = 140°C, Junction Temperature
Θ_{JA} = 36.5°C/W, Junction-to-ambient Thermal Resistance (heatsink added to PBL 3762)

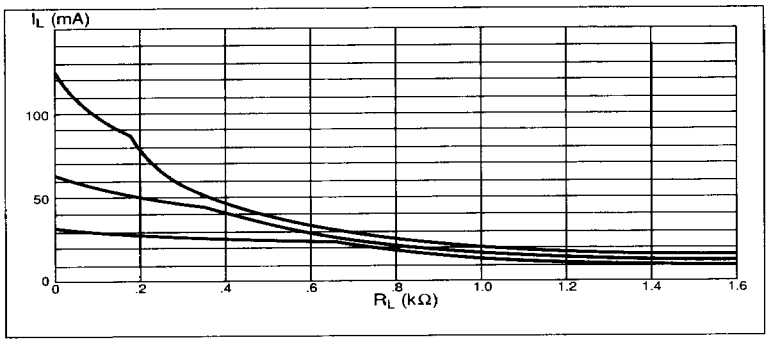


Figure 14. Examples of PBL 3762 loop feed. $R_{SG} \rightarrow \infty$, V_{Bat} = -28V.

$$R_L < \text{Knee} : I_L = \frac{50}{R_L + R_{DC}/50}$$

$$R_L > \text{Knee} : I_L = \frac{20.4}{R_L + R_{DC}/350} \quad (R_{SG} \rightarrow \infty)$$

Curve A: 2 • 200 Ω Feed
Curve B: 2 • 400 Ω Feed
Curve C: 2 • 800 Ω Feed

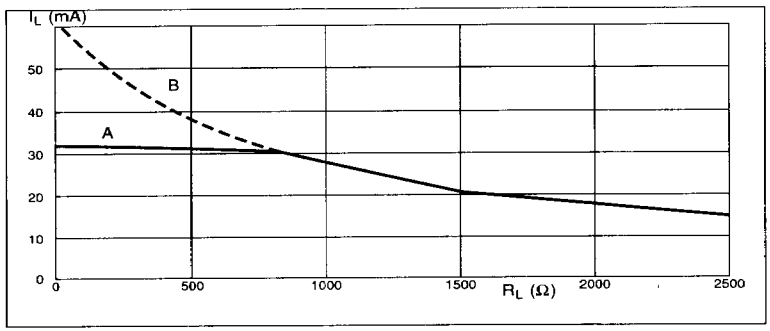


Figure 15. Example of PBL 3762 loop feed with current limiting.

Curve A: 50V apparent battery voltage
782 Ω + 40 Ω feed resistance
Current limited to 32 mA
$V_{SGRef} \approx 37V$

Curve B: 50V apparent battery voltage
782 Ω + 40 Ω feed resistance
Current not limited
$V_{SGRef} \approx 37V$

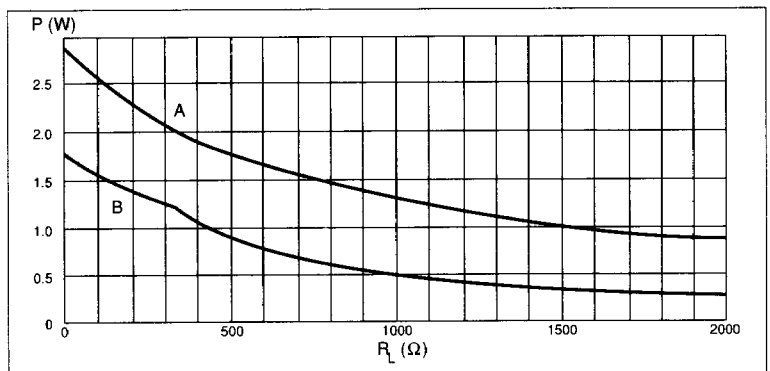


Figure 16. Power dissipation as a function of loop resistance, R_L.

Curve A: Conventional resistive feed:
-48V, 2 • 400Ω

Curve B: PBL3762 resistive feed:
-28V, 2 • 400Ω

add some dc resistance (200 Ω to 300 Ω) even if the wire resistance is near 0 Ω.

If the total short circuit SLIC power dissipation, P_{STot}, exceeds the maximum allowable dissipation, P_{Max}, according to the derating curves in figure 13, the short circuit loop current, I_{LS}, must be limited. The maximum, safe short circuit current, I_{LSMax}, can be calculated from:

$$I_{LSMax} = \frac{V_{Bat}}{4R_F} - \left[\left(\frac{V_{Bat}}{4R_F}\right)^2 - \frac{P_{Max} - 0.1}{2R_F}\right]^{0.5}$$

To comply with this requirement, the short circuit loop current can be limited by installing a diode (D_7 in figure 10) with its anode connected to ground and its cathode to the R_{DC1}, R_{DC2} common point. By clamping the voltage at R_{DC1}, the current flowing out of RSN (virtual ground) is limited and consequently the loop current is limited to $1000 \cdot (V_D/R_{DC1})$. V_D is the voltage drop across the conducting diode; approximately 0.5V at the applicable current range. R_{DC1} and R_{DC2} can then be calculated from:

$$R_{DC1} = (1000 \cdot V_D)/I_{LSMax}$$

$$R_{DC2} = R_{Feed} \cdot 50 - R_{DC1}$$

Figure 15 illustrates a PBL 3762 battery feed curve with loop current limiting as described above. The battery feed is resistive for long loops and constant current for short loops.

To ensure that the maximum vf signal intended to be received/transmitted by the SLIC will not experience limiting in the TIPX (pin 5)/RINGX (pin 6) drive amplifiers at long loops, the saturation guard must be correctly progammed. Section Battery Feed, Case 2 describes how to calculate a value for the saturation guard programming resistor R_{SG}.

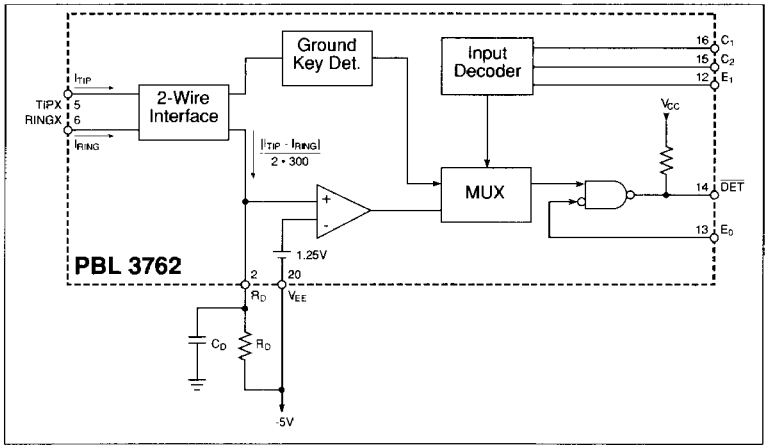


Figure 17. Loop current and ground key detectors.

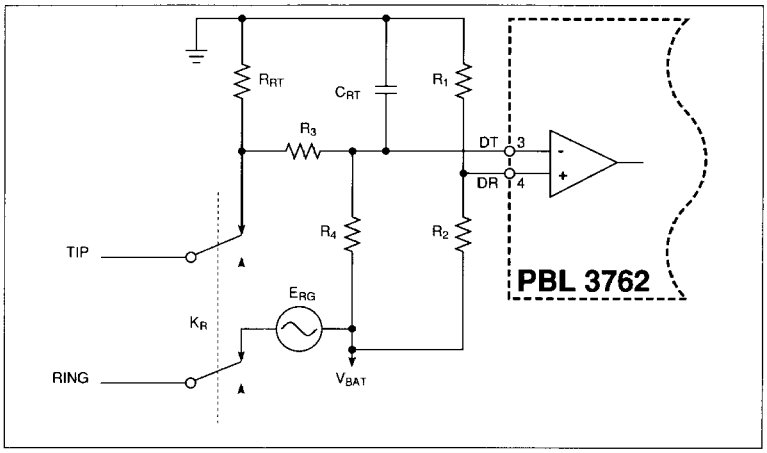


Figure 18. Ring trip network

Temperature guard

A ring to ground short circuit fault condition as well as other improper operating conditions may cause excessive SLIC power dissipation. If junction temperature increases beyond 150°C, the temperature guard will trigger, causing the SLIC to be set to a high-impedance state. In this high-impedance state, power dissipation is reduced and the junction temperature will return to a safe value. Once below 150°C, the SLIC is returned back to its normal operating mode and will remain in that state, assuming the fault condition has been removed..

Loop monitoring functions

The loop current, ground key and ring trip detectors report their status through a common output, $\overline{DET}$ (pin 14). The detector to be connected to $\overline{DET}$ is selected via the four bit wide control interface C_1, C_2, E_0, E_1. Please refer to section Control Inputs for a description of the control interface.

Loop current detector

The loop current value, at which the loop current detector changes state, is programmable by selecting the value of resistor R_D. R_D connects between pins RD (2) and V_{EE} (20). Figure 17 shows a block diagram of the loop current detector. The two-wire interface produces a current flowing out of pin RD (2):

$I_{RD} = |I_{Tip} - I_{Ring}|/600 = I_L/300$

where I_{Tip} and I_{Ring} are currents flowing into the TIPX and RINGX terminals and I_L is the loop current. The voltage generated by I_{RD} across the programming resistor R_D is compared to an internal 1.25 V reference. A logic low results at $\overline{DET}$ (pin 14), when I_{RD} exceeds the corresponding threshold current, $I_{RD} = I_{RDTH} = I_{LTH}/300$ and a logic high when $I_{RD} < I_{RDTH}$. The programming resistor can then be calculated as $R_D = 375/I_{LTH}$, when the desired threshold loop current I_{LTH} is known. R_D is in kohms for I_{LTH} in mA. The filter capacitor is calculated according to $C_D = T_D/R_D$ with time constant $T_D = 0.5$ ms. Note that C_D may not be required if the $\overline{DET}$ output is software filtered.

Ground key detector

The ground key detector circuit examines the difference in TIPX and RINGX currents. Should the current difference exceed the threshold value, ΔI_{LOn}, the detector is triggered. As the current difference decreases the detector is reset at current threshold, ΔI_{LOff}. $\Delta I_{LOn} > \Delta I_{LOff}$, i.e. the detector has hysteresis. The triggered detector results in a logic low at the $\overline{DET}$ (pin 14) output, assuming the ground key detector has been selected via the four-bit control input (C_1, C_2, E_0, E_1). For ΔI_{LON} and ΔI_{LOFF} numerical values please refer to table Electrical characteristics.

Ring trip detector

Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT (pin 3) and DR (pin 4). The ringing source can be balanced or unbalanced superimposed on V_{Bat}. The unbalanced ringing source may be applied to either the ring lead or the tip lead with return via the other wire. A ring relay driven by the SLIC ring relay driver connects the ringing source to tip and ring.

The ring trip function is based on a polarity change at the comparator input when the line goes off-hook. In the on-hook state no dc current flows through the loop and the voltage at comparator input DT is more positive than the voltage at input DR. When the line goes off-hook, while the ring relay is energized, dc current flows and the comparator input voltage reverses polarity.

Figure 18 is an example of a ring-trip detection network. This network is applicable, when the ring voltage superimposed on V_{Bat} is injected on the ring lead of the two-wire port. The dc voltage across sense resistor R_{RT} is monitored by the ring trip comparator input DT via the network R_3, R_4 and C_{RT}. Input DR is set to a reference voltage by resistors R_1 and R_2. With the line on-hook (no dc current) DT is more positive than DR and the $\overline{DET}$ output will report logic level high, i.e. the detector is not tripped. When the line goes off-hook, while ringing, a dc current will flow through the loop, including the sense resistor, R_T, and will cause input DT to become more negative than input DR. This changes output $\overline{DET}$ to logic level low, i.e. tripped detector condition. The system controller (or line card processor) responds by de-energizing the ring relay, i.e. ring trip.

Complete filtering of the 20 Hz ac component at terminal DT is not necessary. A toggling $\overline{DET}$ output can be examined by a software routine to determine the duty cycle. When the $\overline{DET}$ output is at logic level low for more than half the time, off-hook condition is indicated.

Relay Driver

The PBL 3762 SLIC incorporates a ring relay driver designed as open collector (npn) with a current sinking capability of 50 mA. The drive transistor emitter is connected to BGND. An external inductive kick-back clamp diode must be employed to protect the drive transistor.

Control Inputs

The PBL 3762 SLIC has two TTL compatible control inputs, C_1 and C_2. A decoder in the SLIC interprets the control input conditions and sets up the commanded operating state.

Open circuit state (C_2, C_1 = 0, 0)

In the Open Circuit State the TIPX and RINGX line drive amplifiers as well as other circuit blocks are powered down. This causes the SLIC to present a high impedance to the line. Power dissipation is at a minimum. No detectors are active.

Ringing State (C_2, C_1 = 0, 1)

The ring relay driver and the ring trip detector are activated. TIPX and RINGX are in the high impedance state and signal transmission is inhibited.

Active State (C_2, C_1 = 1, 0)

TIPX is the terminal closest to ground and sources loop current while RINGX is the more negative terminal and sinks loop current. Vf signal transmission is normal. Both the loop current and the ground key detectors are activated. Inputs E_0 and E_1 control the selection of one of these detectors to be gated to the $\overline{DET}$ output. Please, refer to section Enable Inputs.

Stand-By State (C_2, C_1 = 1, 1)

In the stand-by state the line drive amplifiers are disconnected. The loop feed is converted to resistive form

State	E0	E1	C1	C2	SLIC operating state	Active detector	$\overline{DET}$ Output
1	0	0	0	0	Open circuit	No active detector	Logic level high
2	0	0	0	1	Active	Ground key detector	Ground key status
3	0	0	1	0	Ringing	No active detector	Logic level high
4	0	0	1	1	Stand-by	Ground key detector	Ground key status
5	0	1	0	0	Open circuit	No active detector	Logic level high
6	0	1	0	1	Active	Loop current detector	Loop current status
7	0	1	1	0	Ringing	Ring trip detector	Ring trip status
8	0	1	1	1	Stand-by	Loop current detector	Loop current status
9	1	0	0	0	Open circuit	Note 1	Logic level high Note 1
10	1	0	0	1	Active		
11	1	0	1	0	Ringing		
12	1	0	1	1	Stand-by		
13	1	1	0	0	Open circuit		
14	1	1	0	1	Active		
15	1	1	1	0	Ringing		
16	1	1	1	1	Stand-by		

Table 1. SLIC operating states

Note 1 For operating states 9-16 active detectors are as for operating states 1-8. The $\overline{DET}$ output is, however, disabled and remains at logic level high regardless of detector status.

Note 2 For operating states 1-8 the $\overline{DET}$ output is enabled and will report the status

according to:

$$I_L \approx \frac{V_{Bat} - 3\,V}{R_L + 1800\,\Omega}$$

where:

I_L = loop current (A)

V_{Bat} = battery supply voltage (V)

R_L = loop resistance (ohm)

The stand-by short circuit loop current (I_{LS}) for V_{BAT} = -28 V is then limited to $I_{LS} \approx 14.7$ mA.

The SLIC on-hook power dissipation is 13 mW at V_{Bat} = -28 V.

Both the loop current and ground key detectors are activated in this operating state. Inputs E_0 and E_1 control the selection of one of these detectors to be gated to the $\overline{DET}$ output. Please, refer to section "Enable Inputs".

Table 1 summarizes the above description of the control inputs.

Enable Inputs (E_0, E_1)

Two TTL-compatible enable inputs E_0 (pin 13) and E_1 (pin 12) control the function of the $\overline{DET}$ (pin 14) output.

E_0, when set to logic level low, enables the $\overline{DET}$ output, which is a collector output with internal pull-up resistor (approx. 15 kohms). A $\overline{DET}$ output at logic level low indicates triggered detector condition (loop current above threshold current, ground key depressed or telephone off-hook during the ringing cycle). A $\overline{DET}$ output at logic level high indicates a non triggered detector condition.

E_0, when set to logic level high, disables the $\overline{DET}$ output; i.e. it appears as a resistor connected to V_{CC}.

E_1, when set to logic level low, gates the ground key detector to the $\overline{DET}$ output.

E_1, when set to logic level high, gates the loop or ring trip detector to the $\overline{DET}$ output.

Table 1 summarizes the above description of the enable inputs.

Overvoltage Protection

The PBL 3762 SLIC must be protected against overvoltages and power crosses. Refer to "Maximum Ratings," TIPX and RINGX terminals for maximum allowable transient voltages that may be applied to the SLIC. The circuit shown in figure 10 utilizes diodes together with a clamping device to protect against high voltage transients.

Diodes D_1 and D_2 clamp positive transients directly to ground. These two diodes are reverse biased by the normal negative tip, ring operating voltages.

Diodes D_3 and D_4 clamp negative transients to ground via a device, which is not conducting when exposed to the normal, negative tip, ring operating voltages, but will conduct when exposed to negative transient voltages. This device is necessary since D_3 and D_4 would otherwise be forward biased in the normal operating mode. A zener diode type device (e.g. General Semiconductor Tranzorb) is suitable for lower energy transients and an SCR type device (e.g. RCA Surgector) is suitable for higher energy transients due to its enegy foldback characteristic. In applications requiring protection only against low energy transients, it is acceptable to connect the anodes of D_3 and D_4 directly to the V_{Bat} supply rail, thus eliminating the need for a device to block normal operating voltages.

The line resistors, R_F, serve the dual purpose of being non-destructing energy dissipaters, when transients are clamped and of being fuses when the line is exposed to a power cross. Ericsson Components AB line resistor PBR 5067 is designed for this application.

Power-up Sequence

The voltage at pin V_{Bat} sets the substrate voltage, which must at all times be kept more negative than the voltage at any other pin to prevent possible latch-up. The correct power-up sequence is ground and V_{Bat}, then other supplies and signal leads.

A diode with a 2A current rating connected with its cathode to V_{EE} and anode to V_{Bat} ensures the presence of the most-negative supply voltage at the V_{Bat} pin if the V_{Bat} supply voltage be absent. The V_{Bat} pin should not be applied at a faster rate than corresponds to the time constant formed by a 5.1 Ω resistor in series with the V_{Bat} pin and a 0.47 µF capacitor from the V_{Bat} pin to ground. This RC network may be shared by several SLICs.

Printed Circuit Board Lay-out

Care in PCB lay-out is essential for proper PBL 3762 function. The components connecting to the RSN pin (19) should be in close proximity of that pin such that no interference is injected into the RSN terminal. Ground plane surrounding the RSN pin is advisable.

The two ground pins AGND and BGND should be connected together on the PCB at the device location.

Ordering Information

Package	Temp. Range	Part No.
Plastic DIP	0 to 70°C	PBL 3762N*
Ceramic DIP	0 to 70°C	PBL 3762J
Ceramic DIP	-40 to 85°C	PBL 3762/2J
PLCC	0 to 70°C	PBL 3762QN*
CLCC	0 to 70°C	PBL 3762QC
CLCC	-40 to 85°C	PBL 3762/2QC
LLCC	0 to 70°C	PBL 3762CC

*: Contact factory for availability.

ERICSSON

Ericsson Components AB
S-164 81 Kista-Stockholm, Sweden
Telephone: (08) 757 50 00