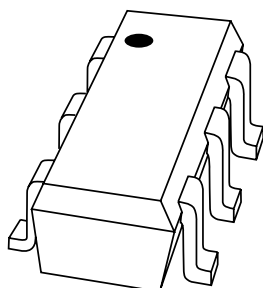


# DATA SHEET



## **PBSS5240Y** 40 V low $V_{CEsat}$ PNP transistor

Product specification  
Supersedes data of 2001 Oct 24

2002 Feb 28

40 V low  $V_{CEsat}$  PNP transistor

PBSS5240Y

FEATURES

- Low collector-emitter saturation voltage
- High current capability
- Improved device reliability due to reduced heat generation
- Replacement for SOT89/SOT223 standard packaged transistors due to enhanced performance.

APPLICATIONS

- Supply line switching circuits
- Battery management applications
- DC/DC converter applications
- Strobe flash units
- Heavy duty battery powered equipment (motor and lamp drivers).

DESCRIPTION

PNP low  $V_{CEsat}$  transistor in a SOT363 (SC-88) plastic package.  
NPN complement: PBSS4240Y.

MARKING

TYPE NUMBER	MARKING CODE <sup>(1)</sup>
PBSS5240Y	52*

Note

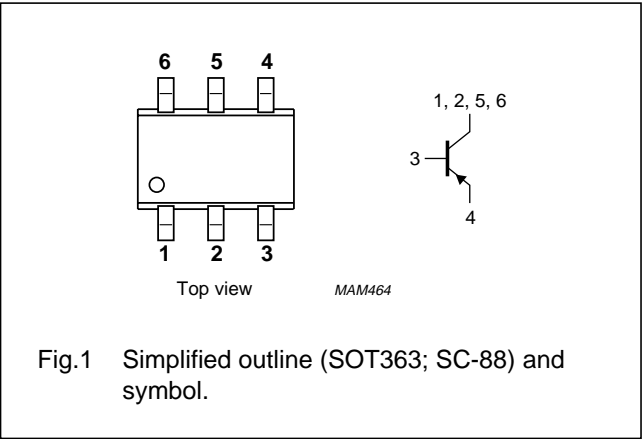
1. \* = p: made in Hongkong.  
\* = t: made in Malaysia.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{CEO}$	collector-emitter voltage	−40	V
$I_{CM}$	peak collector current	−3	A
$I_C$	collector current (DC)	−2	A
$R_{CEsat}$	equivalent on-resistance	<200	mΩ

PINNING

PIN	DESCRIPTION
1	collector
2	collector
3	base
4	emitter
5	collector
6	collector



40 V low  $V_{CEsat}$  PNP transistor

## PBSS5240Y

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–40	V
$V_{CEO}$	collector-emitter voltage	open base	–	–40	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)		–	–2	A
$I_{CM}$	peak collector current		–	–3	A
$I_{BM}$	peak base current		–	–300	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	270	mW
		$T_{amb} \leq 25\text{ °C}$ ; note 2	–	430	mW
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

**Notes**

1. Device mounted on a printed-circuit board, single side copper, tinplated and standard footprint.
2. Device mounted on a printed-circuit board, single side copper, tinplated and mounting pad for collector 1 cm<sup>2</sup>.

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	463	K/W
		note 2	291	K/W

**Notes**

1. Device mounted on a printed-circuit board, single side copper, tinplated and standard footprint.
2. Device mounted on a printed-circuit board, single side copper, tinplated and mounting pad for collector 1 cm<sup>2</sup>.

40 V low  $V_{CEsat}$  PNP transistor

PBSS5240Y

**CHARACTERISTICS** $T_{amb} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$I_{CBO}$	collector-base cut-off current	$V_{CB} = -30\text{ V}; I_E = 0$	–	–100	nA
		$V_{CB} = -30\text{ V}; I_E = 0; T_j = 150\text{ }^{\circ}\text{C}$	–	–50	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = -4\text{ V}; I_C = 0$	–	–100	nA
$h_{FE}$	DC current gain	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}$	300	–	
		$V_{CE} = -2\text{ V}; I_C = -500\text{ mA}$	260	–	
		$V_{CE} = -2\text{ V}; I_C = -1000\text{ mA}$	210	–	
		$V_{CE} = -2\text{ V}; I_C = -2000\text{ mA}$	100	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -100\text{ mA}; I_B = -1\text{ mA}$	–	–100	mV
		$I_C = -500\text{ mA}; I_B = -50\text{ mA}$	–	–110	mV
		$I_C = -750\text{ mA}; I_B = -15\text{ mA}$	–	–225	mV
		$I_C = -1000\text{ mA}; I_B = -50\text{ mA}$	–	–225	mV
		$I_C = -2000\text{ mA}; I_B = -200\text{ mA}$	–	–350	mV
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -2000\text{ mA}; I_B = -200\text{ mA}$	–	–1.1	V
$V_{BEon}$	base-emitter turn-on voltage	$V_{CE} = -2\text{ V}; I_C = -100\text{ mA}$	–	–0.75	V
$C_c$	collector capacitance	$V_{CB} = -10\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	40	pF
$F_T$	transition frequency	$I_C = -100\text{ mA}; V_{CE} = -10\text{ V}; f = 100\text{ MHz}$	100	–	MHz

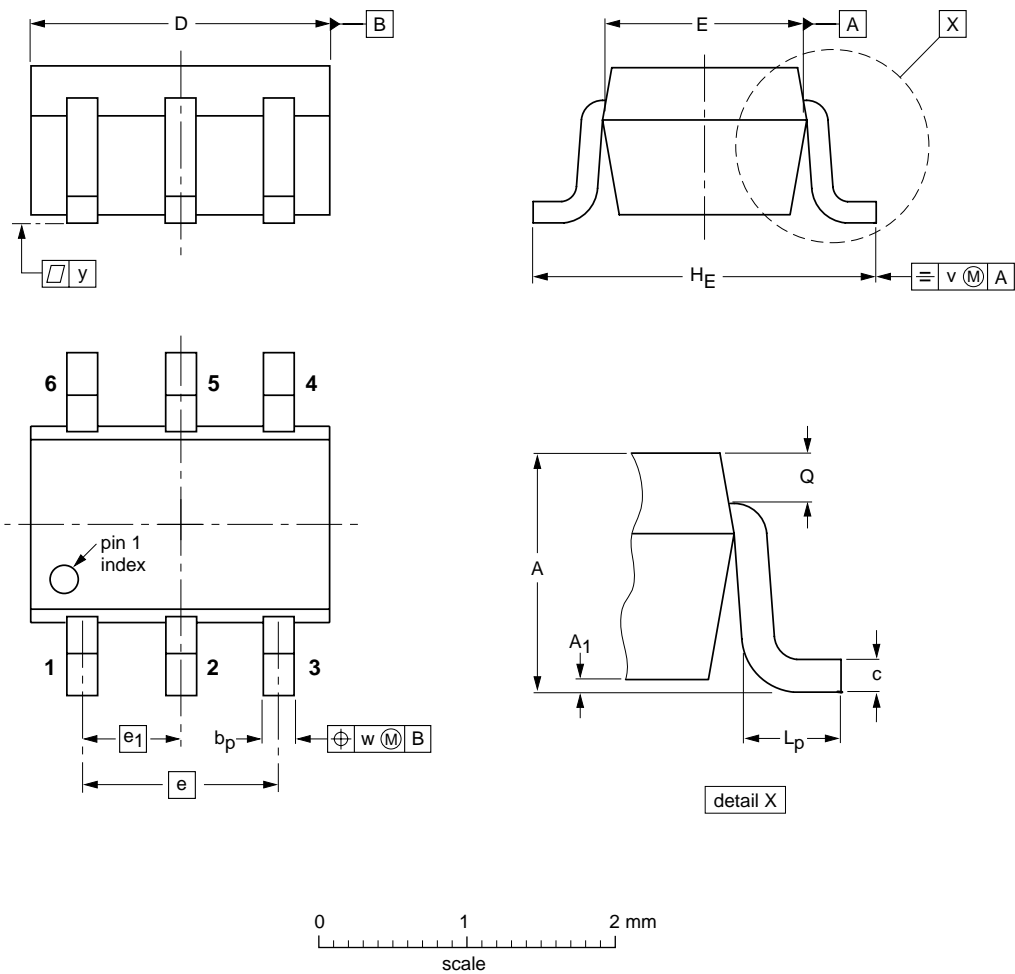
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PACKAGE OUTLINE


Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

40 V low  $V_{CEsat}$  PNP transistor

PBSS5240Y

## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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40 V low  $V_{CEsat}$  PNP transistor

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PBSS5240Y

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**NOTES**

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Printed in The Netherlands

613514/02/pp8

Date of release: 2002 Feb 28

Document order number: 9397 750 09503

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