National Semiconductor

PRELIMINARY
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PC16553
Dual Universal Asynchronous Receiver/Transmitter with FIFOs plus High Performance Parallel Interface†

PC16553 Dual Universal Asynchronous Receiver/Transmitter with FIFOs plus High Performance Parallel Interface

General Description

The PC16553 integrates two CMOS NS16550AF UARTs with a bidirectional parallel interface into a single IC. The serial ports are compatible with all existing software written for the INS8250A, NS16450, NS16C450 and NS16550AF. The parallel port is compatible with all existing software written for the IBM® PC®, XT®, AT®, PS/2® and Centronics parallel ports.

The serial ports can operate with on-chip transmitter and receiver FIFOs (FIFO mode) to relieve the CPU of excessive software overhead. In FIFO mode each channel is capable of buffering 16 bytes (plus 3 bits of error data per byte in the RCVR FIFO) of data in both the transmitter and receiver. All the FIFO control logic is on-chip to minimize system overhead and maximize system efficiency.

Signalling for DMA transfers to and from the FIFOs is done through two pins per channel ($\overline{TXRDY}$ and $\overline{RXRDY}$). The $\overline{RXRDY}$ function is multiplexed on one pin with the $\overline{OUT2}$ and BAUDOUT functions. The CPU can select these functions through a new UART register (Alternate Function Register).

Each UART channel includes one programmable baud rate generator capable of dividing the clock input by divisors of 1 to $(2^{16} - 1)$, and producing a 16 × clock for driving the internal logic of both the receiver and transmitter sections. Both channels have complete MODEM control capability and a processor interrupt system.

The parallel port can operate in the AT parallel port compatible mode, extended (bidirectional) mode or high performance FIFO mode. In the compatible and extended mode, there are three accessable registers, two of which provide status and control for the data register. The CPU can transfer data through this register in both directions by control of the $\overline{POS}$ Mode Pin, a bit in the Control register and the $\overline{RD}$ and $\overline{WR}$ signals. All of the signals required by PC and Centronics printers to transfer data and monitor printer status are provided.

FIFO enable software commands activate the parallel port FIFO mode. In this mode, an on-chip, 16-byte bidirectional FIFO together with automatic handshaking allows multiple byte transfers without the CPU needing to effect each transfer. A write to the compatible mode Status Register bit 0 enables an additional register (High Performance register) which contains control and status bits for the FIFO mode.

Features

- Dual UART capable of interfacing with existing INS8250A, NS16450 and NS16550AF software
- Capable of interfacing with all PC, PS/2 and Centronics parallel port software
- High current drivers that meet or exceed all MicroChannel and PS/2 parallel port drive current requirements
- Provides all control and status pins for a complete PC, PS/2 and Centronics parallel port interface
- 84 ns read and write cycle time
- After reset, all UART registers are identical to the 16450 register set
- In the UART FIFO mode both channels' transmitter and receiver are buffered with 16-byte FIFOs to reduce the number of interrupts presented to the CPU
- In the parallel port FIFO mode, the data register is replaced by a 16-byte, bidirectional FIFO and automatic handshaking
- Adds or deletes asynchronous communication bits (start, stop, and parity) to or from the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable divide-by-13 clock input
- Programmable baud generators divide any input clock by 1 to $(2^{16} - 1)$ and generate the 16 × clock
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
- Programmable transmission enable/disable by $\overline{CTS}$
- Fully programmable serial-interface characteristics:
  - 5-, 6-, 7-, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1-, 1½-, or 2-stop bit generation
  - Baud generation (DC to 1.5M baud) with 16 × clock
- False start bit detection
- Line break generation and detection
- Loopback controls for communications link fault isolation
- Break, parity, overrun, framing error simulation
- Full prioritized interrupt system controls
- Capable of DMA service of high performance parallel port and serial port FIFOs
- Parallel port interrupt generated by DMA TC signal
- Individual UART and parallel port resets available
- Fabricated using National Semiconductor's advanced M²CMOS

†**Note:** This part is patented.

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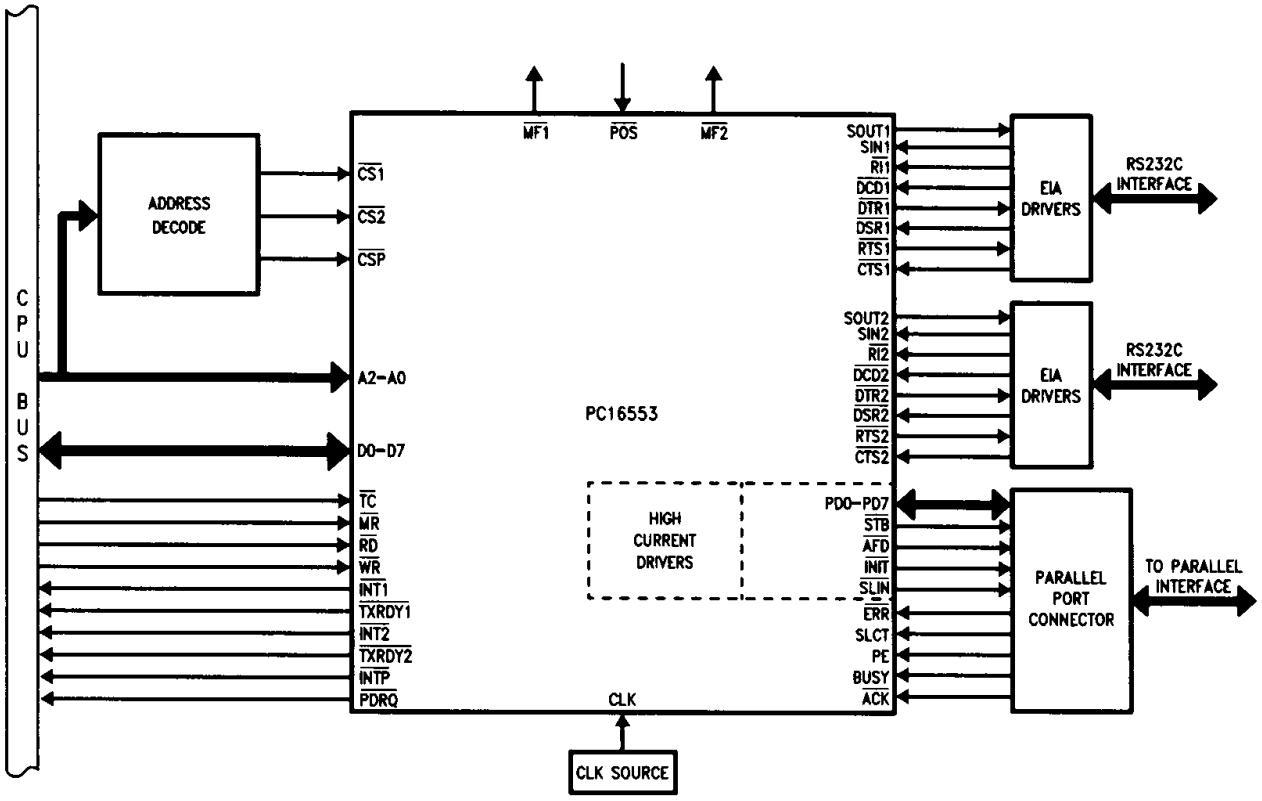
Basic Configuration



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1.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Temperature under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1W

Note: *Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.*

2.0 DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +5V ±10%, V_{SS} = 0V, unless otherwise specified

Symbol	Parameter	Conditions		Min	Max	Units
V_{IL}	Input Low Voltage			−0.5	0.8	V
V_{IH}	Input High Voltage			2	V_{CC}	V
V_{OL}	Output Low Voltage	1.6 mA	All Outputs except Notes 1, 2, 3		0.4	V
V_{OH}	Output High Voltage	−1.0 mA		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 1)			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −15 mA (Note 1)		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA (Note 2)			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA (Note 2)		2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 24 mA (Note 3)			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4 mA (Note 3)		2.4		V
I_{CC}(AV)	Average Power Supply Current	V_{DD} = 5.5V No Loads on Output CS, RD, WR, SIN, DSR, DCD, CTS, RI = 2V All Other Inputs = 0.8V CLK = 24 MHz DIVISOR = EFFF			40	mA
I_{IL}	Input Leakage	V_{DD} = 5.5V, V_{SS} = 0V			±10	µA
I_{OZ}	TRI-STATE Leakage	V_{DD} = 5.5V, V_{SS} = 0V V_{OUT} = 0V, 5.5V 1) Chip Deselected or 2) WRITE Mode, Chip Selected			±20	µA
V_{ILMR}	MR Schmitt V_{IL}				0.8	V
V_{IHMR}	MR Schmitt V_{IH}			2		V

Note 1: This is the maximum current for the data (PD0–PD7) and interrupt ($\overline{INT1}$, $\overline{INT2}$, $\overline{INTP}$) pins.

Note 2: This is the maximum current for the control ($\overline{STB}$, $\overline{AFD}$, $\overline{INIT}$, $\overline{SLIN}$) pins. These are open collector drivers and require 4.7 kΩ external pull-up resistors.

Note 3: This is the maximum current for the CPU data bus pins (D0–D7)

Note 4: T_A = 25°C

Capacitance T_A = 25°C, V_{DD} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	f_C = 1 MHz Unmeasured Pins Returned to V_{SS}		5	7	pF
C_{OUT}	Output Capacitance			6	8	pF
$C_{I/O}$	Input/Output Capacitance			10	12	pF

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Symbol	Parameter	Conditions	Min	Max	Units
3.1 CPU INTERFACE					
t_{AR}	$\overline{RD}$ Delay from Address		15		ns
t_{AW}	$\overline{WR}$ Delay from Address		15		ns
t_{CSH}	$\overline{CS}$ Hold from $\overline{MR}$ (Inactive)		0		ns
t_{DH}	Data Hold Time		5		ns
t_{DR}	SOUT to $\overline{MR}$ inactive (Divide-by-13 initialization)		15		ns
t_{DS}	Data Setup Time		15		ns
t_{HZ}	$\overline{RD}$ to Floating Data Delay	(Note 1)	10	20	ns
t_{MR}	Master Reset Pulse Width		500		ns
t_{RA}	Address Hold Time from $\overline{RD}$		0		ns
t_{RC}	Read Cycle Update		29		ns
t_{RD}	$\overline{RD}$ Strobe Width		40		ns
t_{RES}	$\overline{CS}$ Setup to Active $\overline{MR}$		15		ns
t_{RVD}	Delay from $\overline{RD}$ to Data			25	ns
t_{SIF}	Serial Interrupt Float			33	ns
t_{WA}	Address Hold Time from $\overline{WR}$		0		ns
t_{WC}	Write Cycle Update		29		ns
t_{WR}	$\overline{WR}$ Strobe Width		40		ns
t_{CH}	Duration of Clock High Pulse	External Clock (24 MHz Max)	17		ns
t_{CL}	Duration of Clock Low Pulse	External Clock (24 MHz Max)	17		ns
RC	Read Cycle = $t_{AR} + t_{RD} + t_{RC}$		84		ns
WC	Write Cycle = $t_{AW} + t_{WR} + t_{WC}$		84		ns
3.2 SERIAL INTERFACE BAUD GENERATOR					
N	Baud Divisor		1	$2^{16} - 1$	
t_{BHD}	Baud Output Positive Edge Delay	CLK = 24 MHz, ÷2		45	ns
t_{BLD}	Baud Output Negative Edge Delay	CLK = 24 MHz, ÷2		45	ns

Note 1: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

Note 2: All AC timings can be met with current loads that don't exceed 3.2 mA or −80 μA at 100 pF capacitive loading.

Note 3: For capacitive loads that exceed 100 pF the following typical derating factors should be used:

100 PF < $C_L \leq$ 150 pF t = (0.1 ns/pF) (C_L − 100 pF)

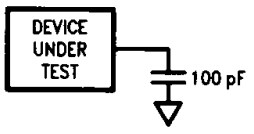
150 PF < $C_L \leq$ 200 pF t = (0.08 ns/pF) (C_L − 100 pF) and

t = (0.5 ns/mA) (I_{SINK} mA) or

t = −(0.5 ns/mA) (I_{SOURCE} mA)

I_{SOURCE} is always negative, $I_{SINK} \leq 4.8$ mA, $I_{SOURCE} \leq -120$ μA, $C_L \leq 250$ pF

AC Testing Load Circuit



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3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$ (Continued)

Symbol	Parameter	Conditions	Min	Max	Units
RECEIVER					
t_{RAI}	Delay from Active Edge of $\overline{RD}$ to Reset Interrupt			78	ns
t_{RINT}	Delay from Inactive Edge of $\overline{RD}$ (RD LSR) to Reset Interrupt			40	ns
t_{RXI}	Delay from READ to RXRDY Inactive			55	ns
t_{SINT}	Delay from Stop to Set Interrupt	(Note 1)		2	BAUDOUT Cycles
TRANSMITTER					
t_{ETS}	Enable Transmitter to Start Bit		16	24	BAUDOUT Cycles
t_{HR}	Delay from $\overline{WR}$ (WR THR) to Reset Interrupt			40	ns
t_{IR}	Delay from $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)			40	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to Interrupt	(Note 2)	16	24	BAUDOUT Cycles
t_{STI}	Delay from Start to Interrupt (THRE)	(Note 2)		8	BAUDOUT Cycles
t_{SXA}	Delay from Start to TXRDY Active			8	BAUDOUT Cycles
t_{WXI}	Delay from Write to TXRDY Inactive			25	ns
MODEM CONTROL					
t_{MDO}	Delay from $\overline{WR}$ (WR MCR) to Output			40	ns
t_{RIM}	Delay to Reset Interrupt from $\overline{RD}$ (RD MSR)			78	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input			40	ns

Note 1: In the FIFO mode (FCR0 = 1) the trigger level interrupts, the receiver data available indication, the active RXRDY indication and the overrun error indication will be delayed 3 RCLKs. Status indicators (PE, FE, BI) will be delayed 3 RCLKs after the first byte has been received. For subsequently received bytes these indicators will be updated immediately after RDRBR goes inactive. Timeout interrupt is delayed 8 RCLKs.

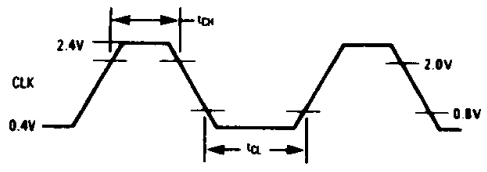
Note 2: This delay will be lengthened by 1 character time, minus the last stop bit time if the transmitter interrupt delay circuit is active. (See FIFO Interrupt Mode Operation.)

3.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$ (Continued)

Symbol	Parameter	Conditions	Min	Max	Units
3.3 PARALLEL INTERFACE					
t_{AA}	Inactive $\overline{ACK}$ to Active $\overline{ACK}$		10		ns
t_{AD}	$\overline{ACK}$ Valid to Data			25	ns
t_{AID}	$\overline{ACK}$ Inactive to Data		15		ns
t_{AK}	$\overline{ACK}$ Strobe Width (Input)		40		ns
t_{DZ}	Inactive $\overline{ACK}$ to Inactive Port Data (Data Hold)		0		ns
t_{INTP}	$\overline{ACK}$ to Interrupt Active			33	ns
t_{PDH}	Port Data Hold		500		ns
t_{PDRQ}	$\overline{ACK}$ of Last Byte in FIFO to $\overline{PDRQ}$ Assertion			50	ns
t_{PDS}	Port Data Setup		500		ns
t_{PHR}	Write of First FIFO Byte to $\overline{INTP}$ Deassertion			40	ns
t_{PI}	Port Interrupt		33		ns
t_{PIF}	Port Interrupt Float			33	ns
t_{PRAI}	Leading Edge of $\overline{RD}$ of Byte Dropping FIFO Level Below Trigger to $\overline{INTP}$ Deassertion			78	ns
t_{PRXI}	Leading Edge of Final FIFO Read to $\overline{PDRQ}$ Deassertion			55	ns
t_{PS}	Port Setup		10		ns
t_{PWXI}	Write Strobe of 16th FIFO Byte to $\overline{PDRQ}$ Deassertion			25	ns
t_{RDRQ}	$\overline{ACK}$ Strobe of Trigger Level Byte (14th) to $\overline{PDRQ}$ Assertion			50	ns
t_{SA}	$\overline{SLIN}$ Active to $\overline{ACK}$ Active		0		ns
t_{SLD}	$\overline{ACK}$ Strobe of Byte which Fills Input FIFO to $\overline{SLIN}$ Deassertion			33	ns
t_{SLN}	Leading Edge of $\overline{RD}$ of Last Byte in FIFO to $\overline{SLIN}$ Assertion			33	ns
t_{STINT}	Status Input Active Edge to $\overline{INTP}$ Assertion			33	ns
t_{SW}	Strobe Width		500		ns
t_{TCH}	TC Hold from $\overline{CSP}$ Deassertion		0		ns
t_{TCINT}	Acknowledge of Last Byte in FIFO (after TC) to $\overline{INTP}$			33	ns
t_{TCS}	TC Setup to $\overline{CSP}$ Deassertion		15		ns
t_{SIC}	Read of Performance Register to $\overline{INTP}$ Deassertion			33	ns
t_{WD}	TC to $\overline{PDRQ}$ Deassertion			33	ns
t_{WDI}	TC to $\overline{PDRQ}$ and $\overline{SLIN}$ Deassertion and $\overline{INTP}$ Assertion			33	ns
t_{WO}	Write to Control Pin Update		33		ns

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1

External Clock Input (24 MHz Max)



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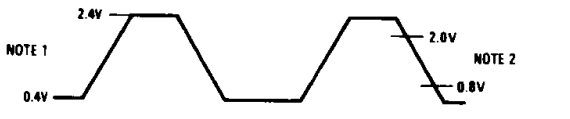
AC Test Points



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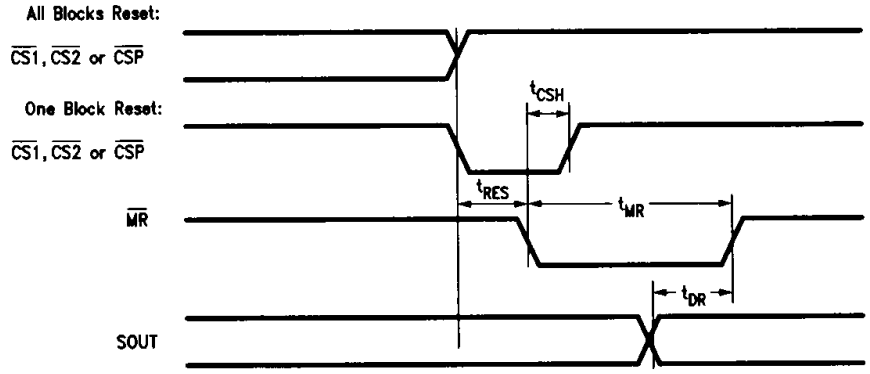
Note 1: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.

Note 2: The 2.0V and 0.8V levels are the voltages at which the timing tests are made.

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

4.1 CPU INTERFACE

Reset Timing



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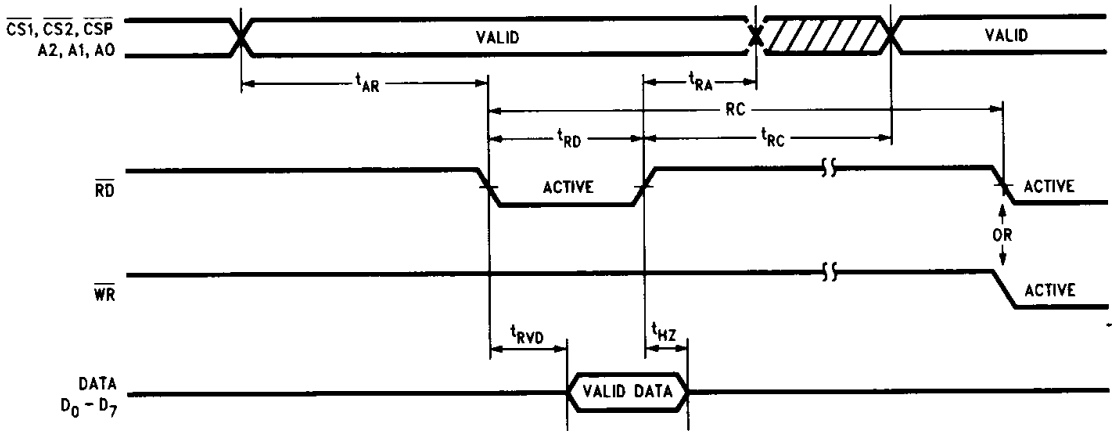
Read Cycle (Serial and Parallel Port Registers)



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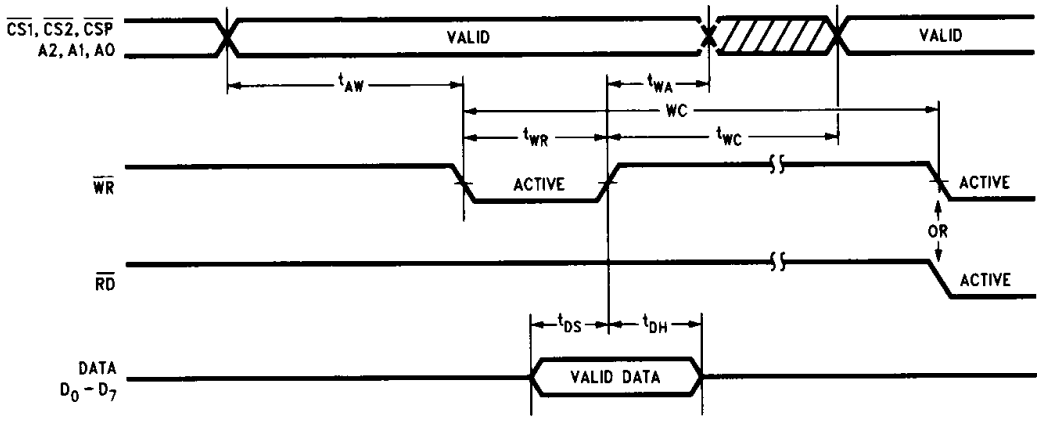
Write Cycle (Serial and Parallel Port Registers)



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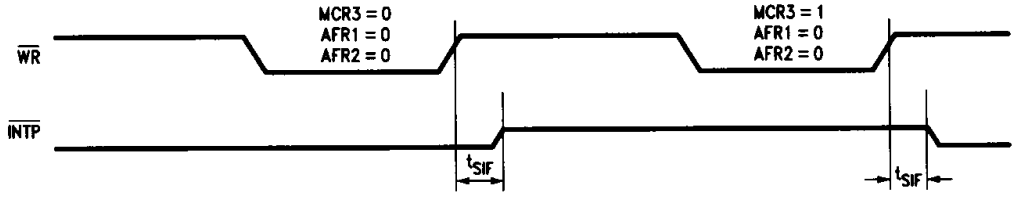
4.2 SERIAL INTERFACE

Serial Interrupt Enable



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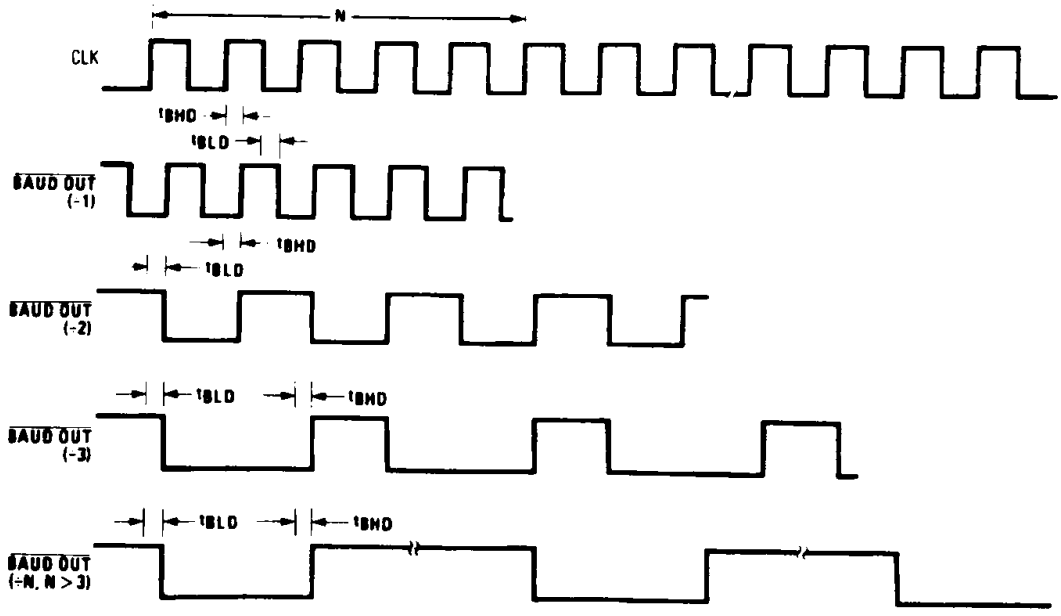
4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

$\overline{\text{BAUDOUT}}$ Timing



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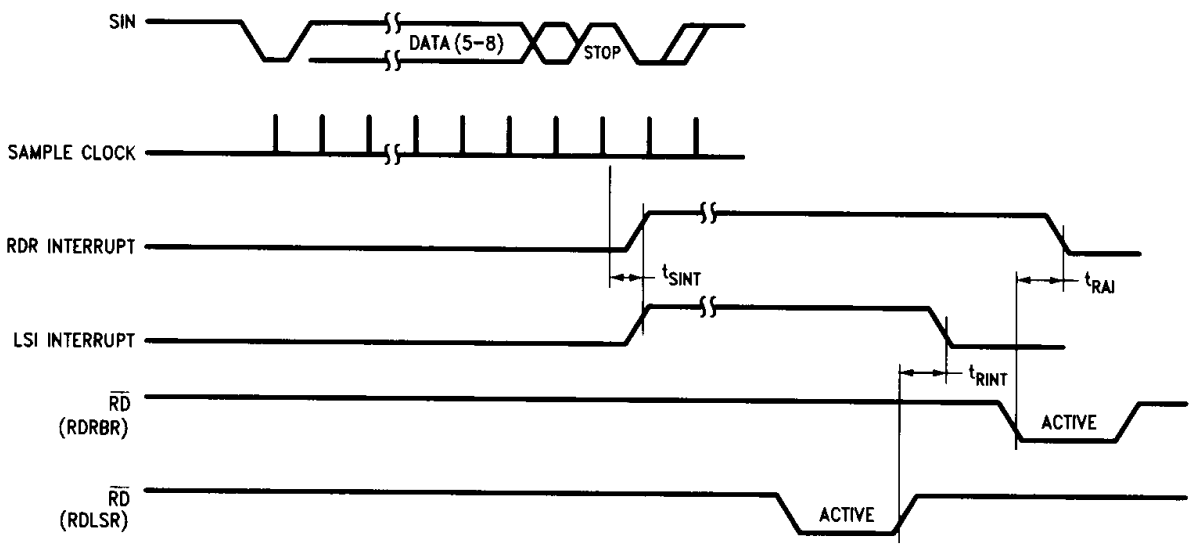
Receiver Timing

NS16450 MODE:



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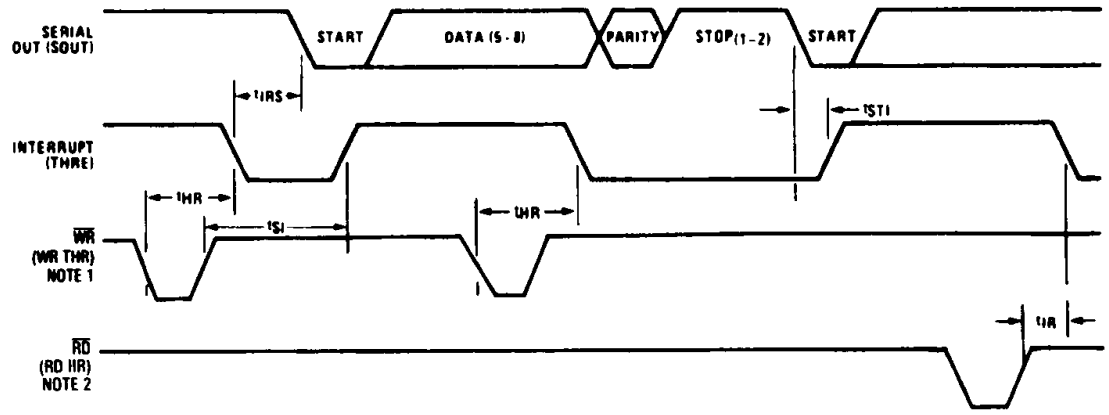
4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

Transmitter Timing



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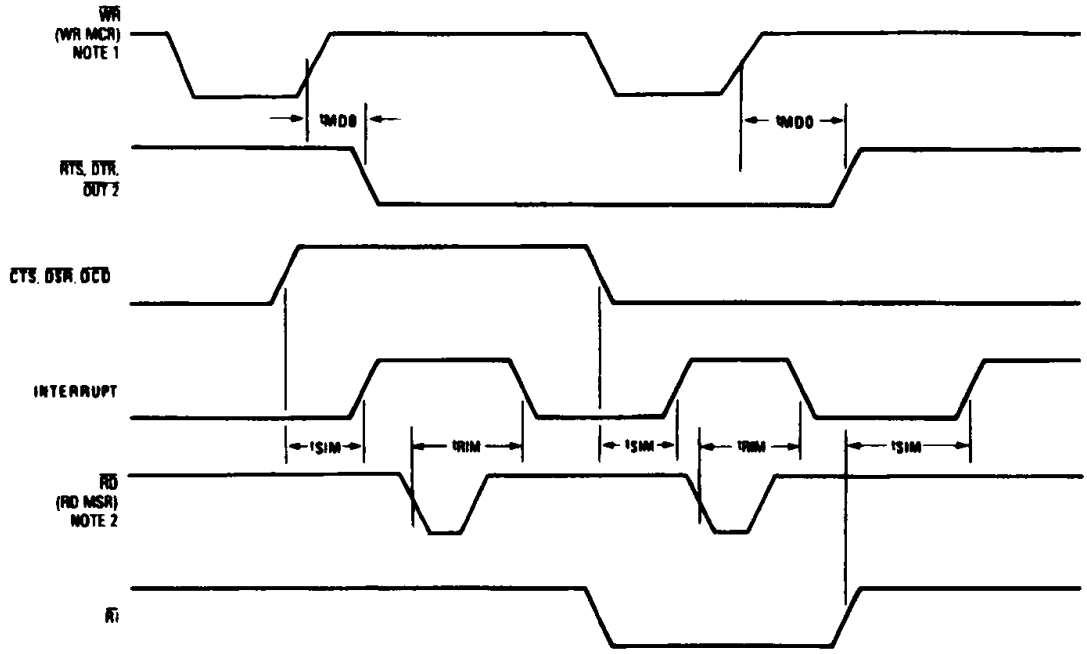
Note 1: See Write Cycle Timing.

Note 2: See Read Cycle Timing.

MODEM Control Timing



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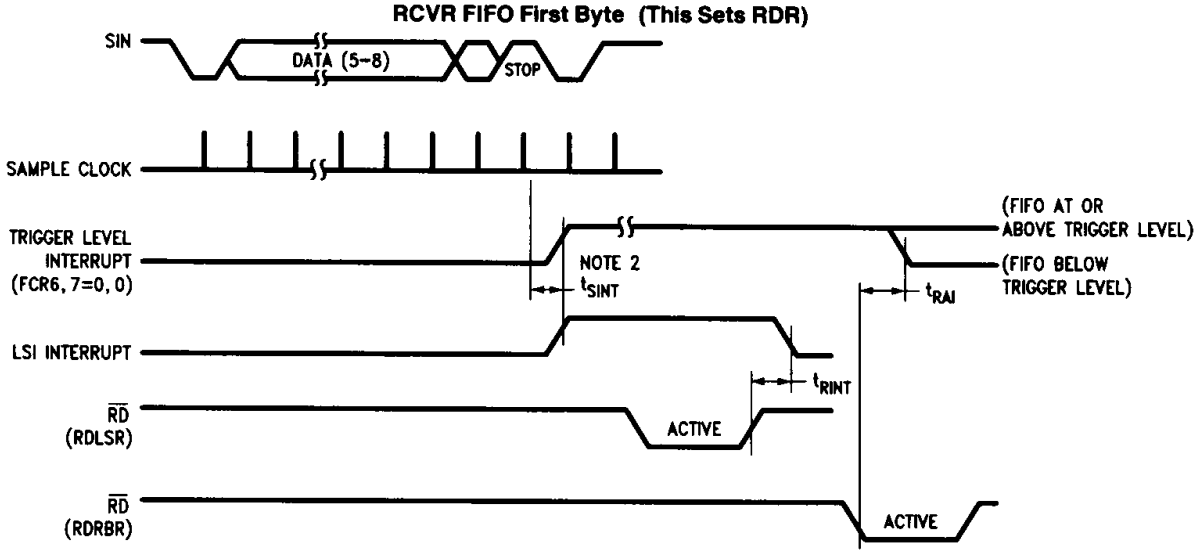
Note 1: See Write Cycle Timing.

Note 2: See Read Cycle Timing.

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

RCVR FIFO First Byte (This Sets RDR)



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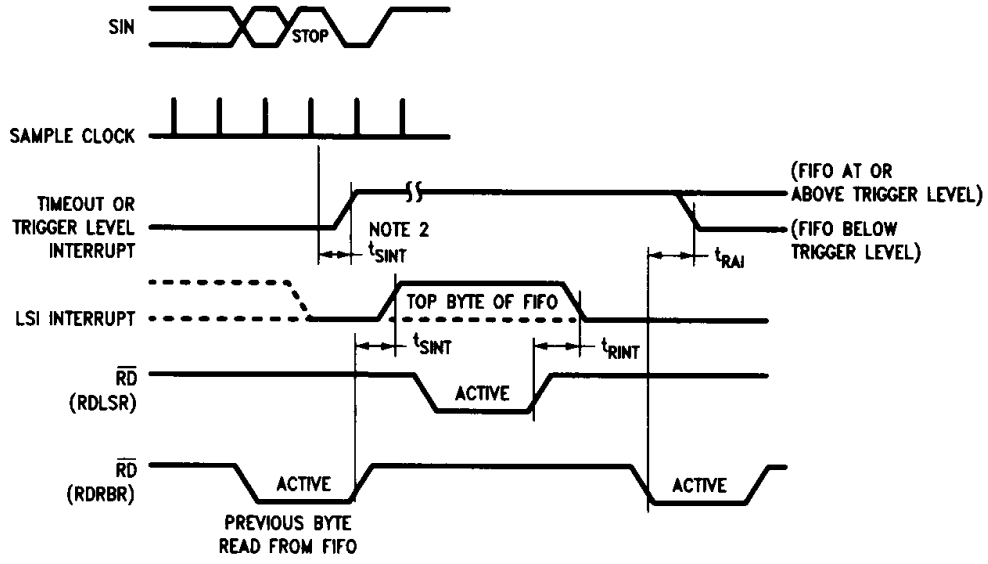
RCVR FIFO Bytes Other than the First Byte (RDR Is Already Set)



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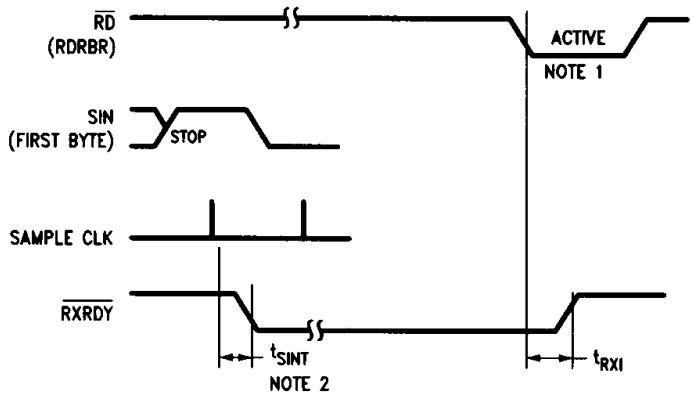
Receiver Ready FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



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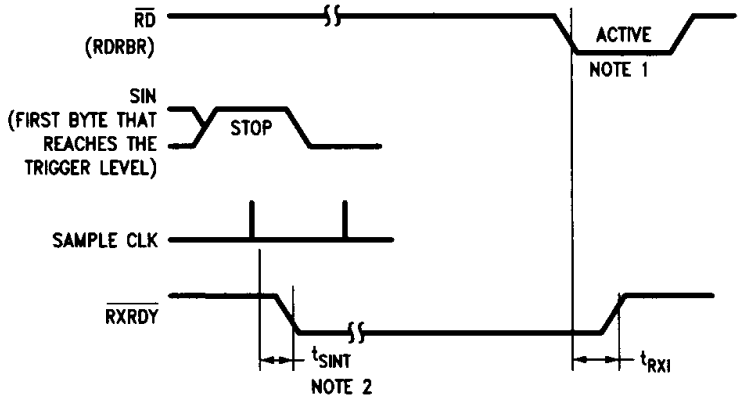
Note 1: This is the reading of the last byte in the FIFO.

Note 2: If FCR0 = 1, then t_{SINT} = 3 RCLKs. For a timeout interrupt, t_{SINT} = 8 RCLKs.

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

Receiver Ready FCR0 = 1 and FCR3 = 1 (Mode 1)



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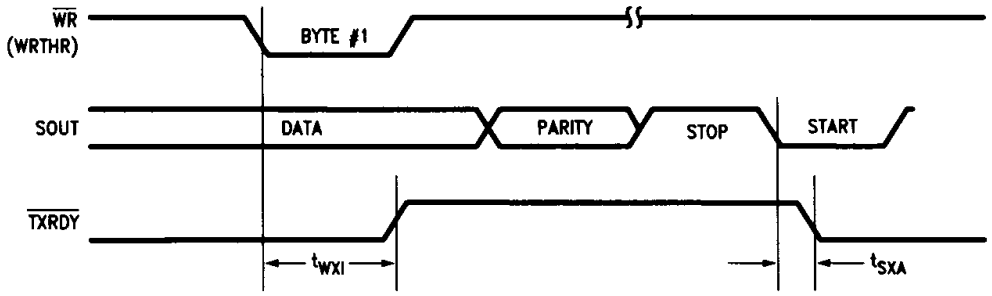
Note 1: This is the reading of the last byte in the FIFO.

Note 2: If FCR0 = 1, t_{SINT} = 3 RCLKs.

Transmitter Ready FCR0 = 0 or FCR0 = 1 and FCR3 = 0 (Mode 0)



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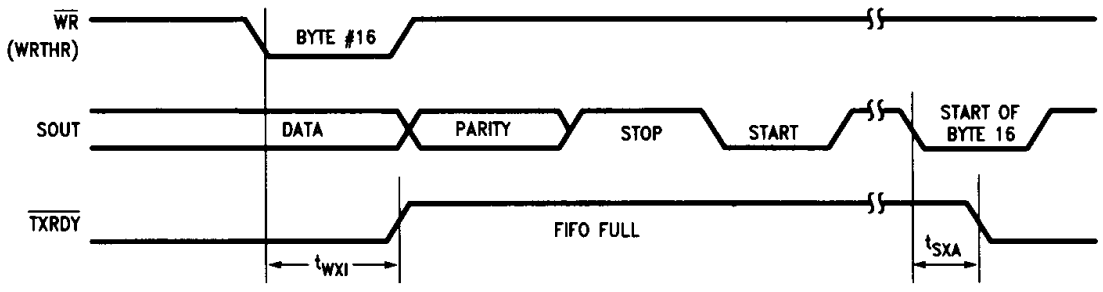
Transmitter Ready FCR0 = 1 and FCR3 = 1 (Mode 1)



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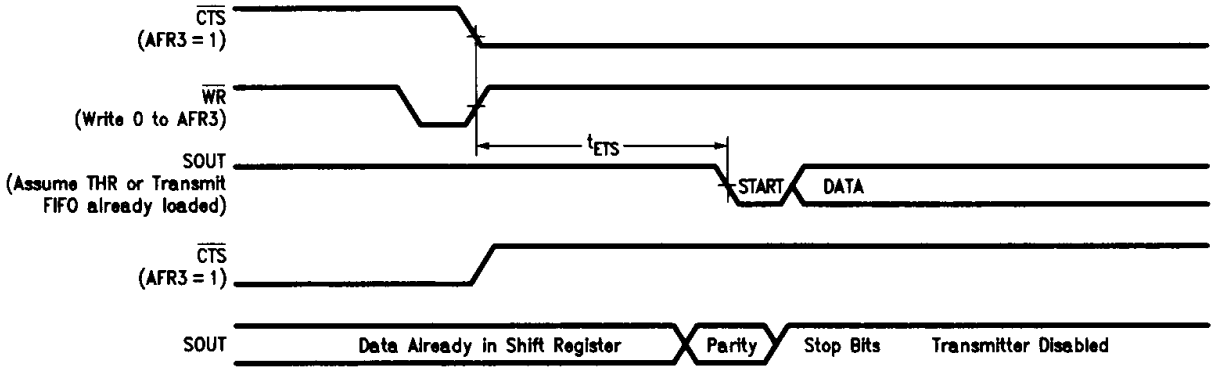
CTS Auto Enable/Disable



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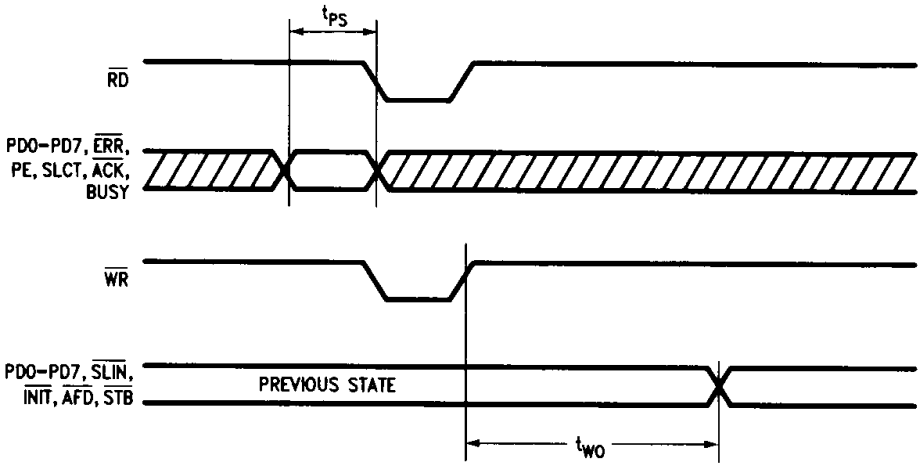
4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

4.3 PARALLEL INTERFACE TIMING

Parallel Port Status and Control Timing



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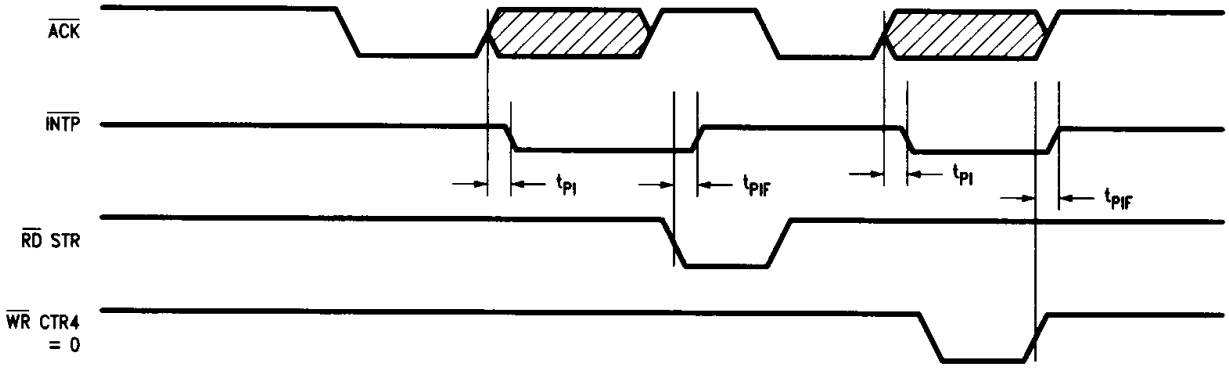
Compatible and Extended Mode Interrupt Timing



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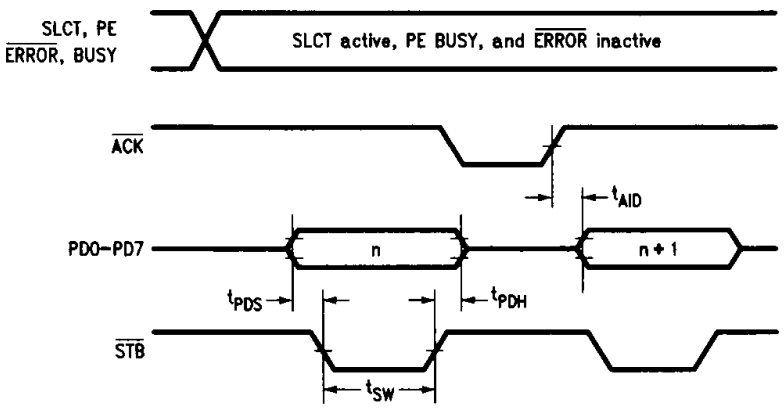
4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

High Performance Write to a Peripheral



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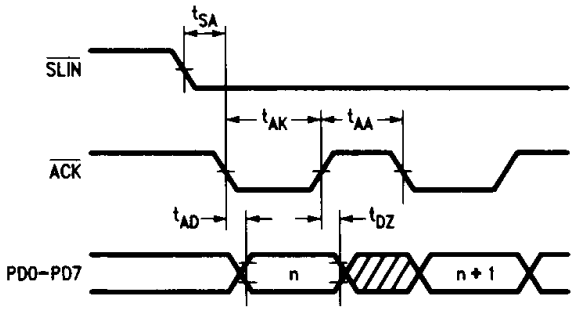
High Performance Read from a Peripheral



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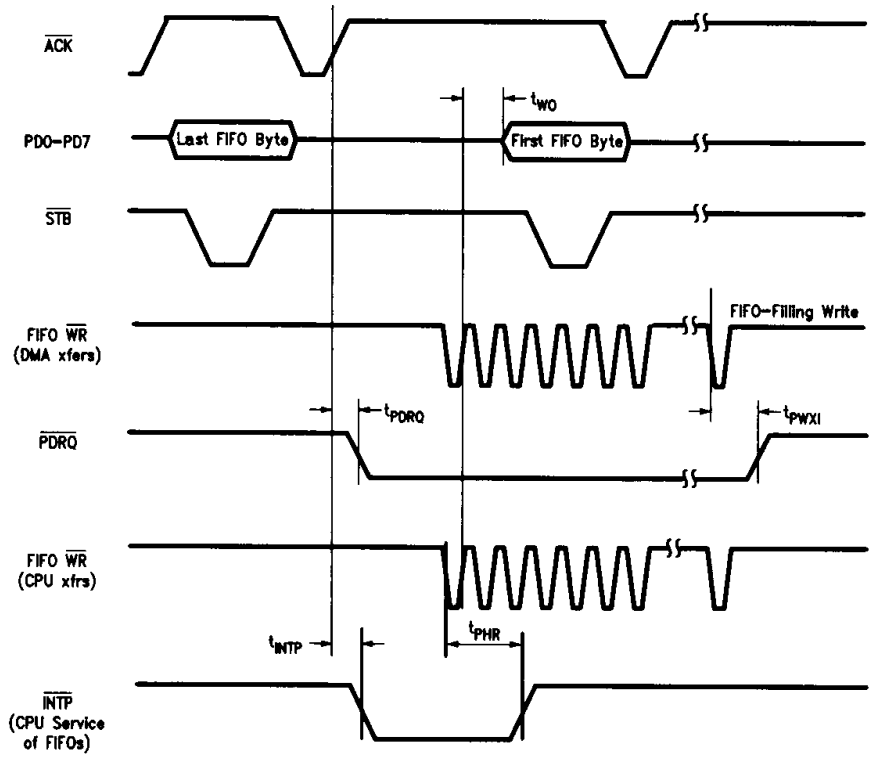
4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

High Performance Mode System CPU and DMA Transfer Timing (Output Direction)



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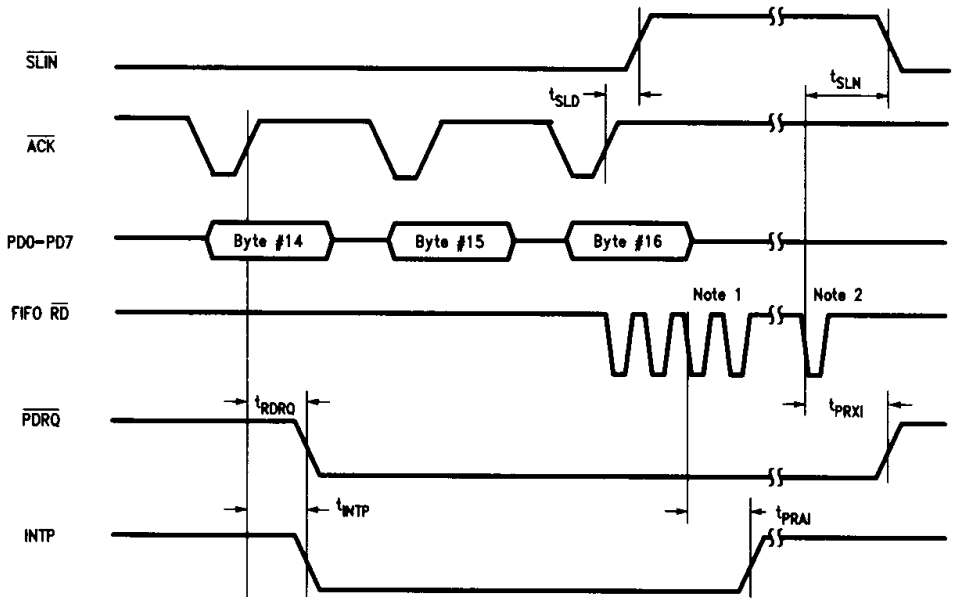
High Performance Mode System DMA and CPU Transfer Timing (Input Direction)



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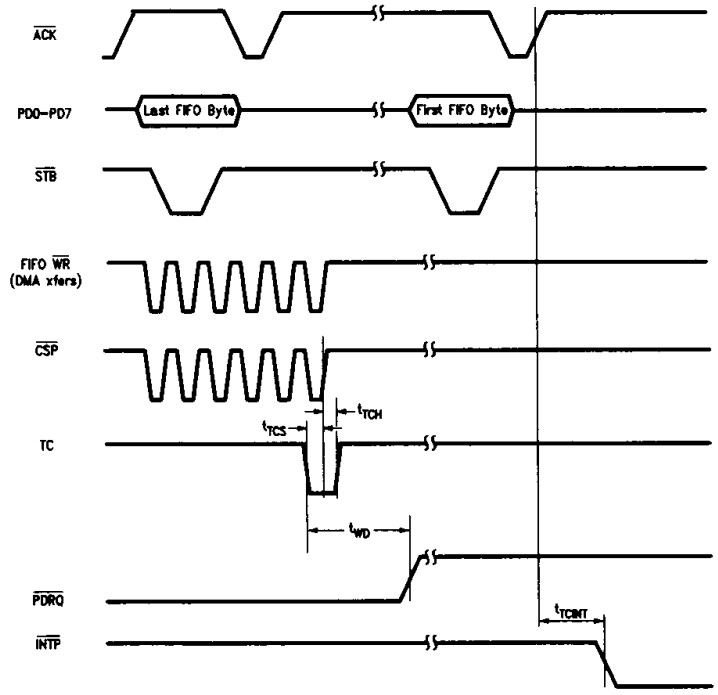
Note 1: This FIFO read drops the data below the 14-byte trigger level.
Note 2: This FIFO read empties the FIFO.

4.0 Timing Waveforms All timings are referenced to valid 0 and valid 1 (Continued)

High Performance Mode DMA End of Transfer Timing (Output Direction)



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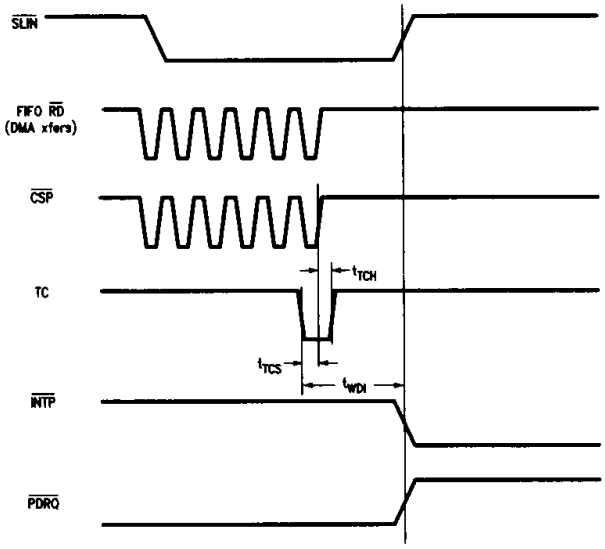
High Performance Mode DMA End of Transfer Timing (Input Direction)



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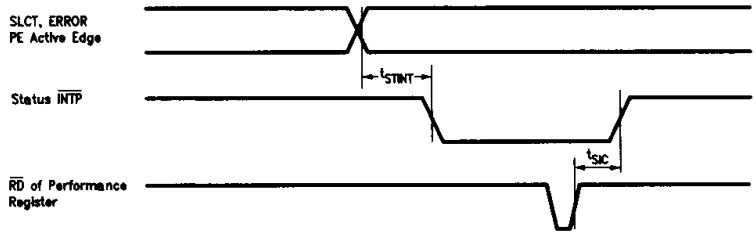
High Performance Mode Status Interrupts



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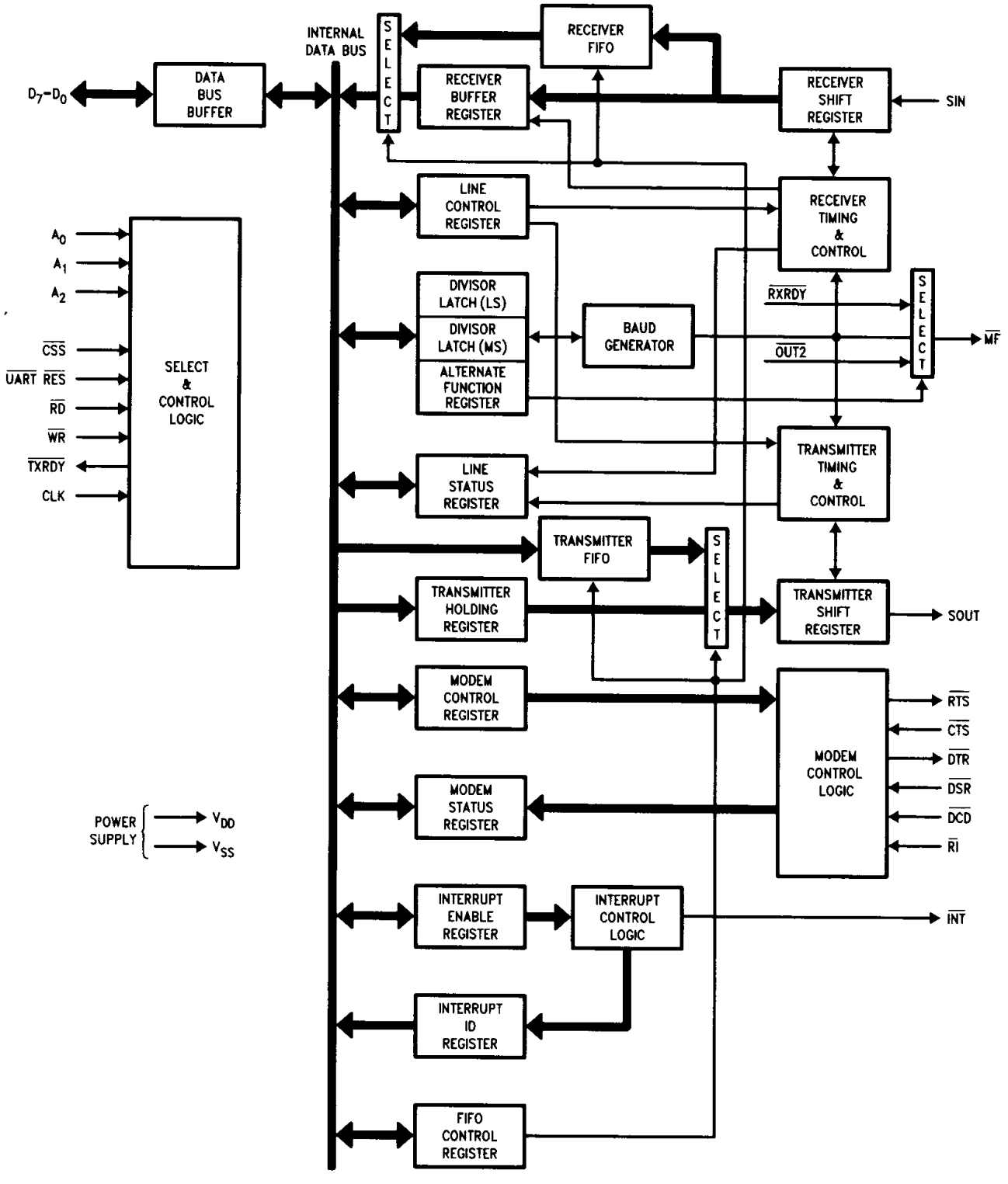
5.0 Block Diagram of a Single Serial Channel



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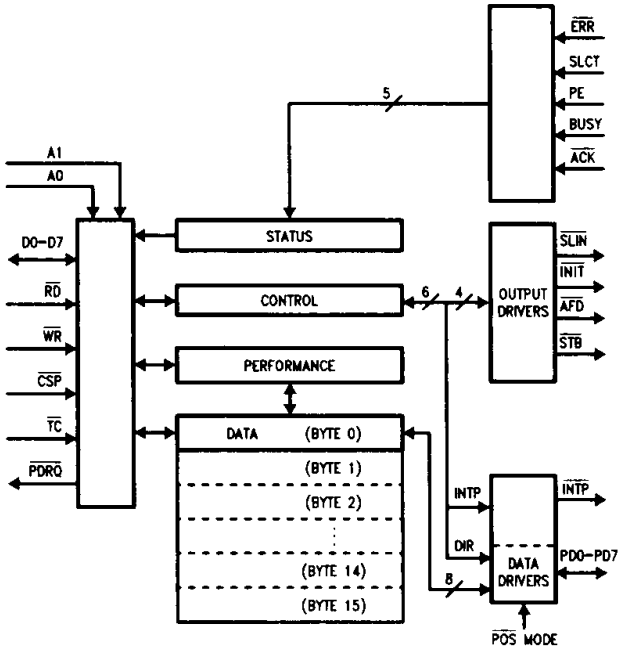
5.0 Block Diagram of a Single Serial Channel (Continued)

Block Diagram of the Parallel Port Logic



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Note: The Performance Register and 16-byte FIFO are additional programmable features to the standard PC, PS/2 and Centronics parallel port.

6.0 Pin Descriptions

The following describes the function of all pins. Some of these descriptions reference internal circuits.

In the following descriptions, a low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

A0, A1, A2 (Register Select), Pins 35, 34, 33: Address signals connected to these 3 inputs select a register for the CPU to read from or write to during data transfer. Tables II and VIII show the registers and their addresses. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain UART registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches and the Alternate Function Register.

$\overline{\text{ACK}}$ (Acknowledge), Pin 68: This input is set low by the printer to indicate that it has received data.

$\overline{\text{AFD}}$ (Automatic Feed XT), Pin 56: When this output is low the printer should automatically line feed after each line printed. This pin requires an external pull-up resistor (4.7 kΩ is recommended).

BUSY (Printer Busy), Pin 66: This input is set high by the printer when it can't accept another character.

CLK (External Clock Input), Pin 4: This input accepts the off-chip clock signal that is used to drive the baud rate generator and the high performance parallel port control logic. Any clock frequency from DC to 24 MHz may be used for the serial port baud generators, but if the high performance parallel port is to be used, the CLK input must be driven at 24 MHz. This insures that the parallel port FIFO timeout period is 4.4 ms and the data-out strobe ($\overline{\text{STB}}$) lasts for 500 ns.

$\overline{\text{CSP}}$ (Chip Select-Parallel Port), Pin 38: When this input is low, the parallel port is selected and will respond to the A1, A0, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals. Valid chip selects should stabilize according to the t_{AW} parameter.

$\overline{\text{CS1}}$, $\overline{\text{CS2}}$ (Chip Select-Serial Port), Pins 32, 3: When this input is low, the serial port is selected and will respond to the A2, A1, A0, $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals. Valid chip selects should stabilize according to the t_{AW} parameter.

$\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$ (Clear to Send), Pins 28, 13: When low, this input indicates that the MODEM or data set is ready to exchange data. The $\overline{\text{CTS}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the $\overline{\text{CTS}}$ signal. $\overline{\text{CTS}}$ can be programmed via the Alternate Function Register Bit 3 to automatically enable and disable serial transmission. If AFR Bit 3 = 0, $\overline{\text{CTS}}$ has no effect on serial transmission. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

D_0–D_7 (Data Bus), Pins 14–21: This bus contains eight TRI-STATE input/output lines. The bus provides bidirectional communications between the UART and the CPU. Data, control words, and status information are transferred via the D_7–D_0 Data Bus. The bus pins feature 24 mA drive capability, allowing direct connection to an AT bus.

$\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$ (Data Carrier Detect), Pins 29, 8: When low, this input indicates that the data carrier has been detected by the MODEM or data set. The $\overline{\text{DCD}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the $\overline{\text{DCD}}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{\text{DCD}}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{\text{DCD}}$ has no effect on the receiver.

Note: Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

6.0 Pin Descriptions (Continued)

$\overline{DSR1}$, $\overline{DSR2}$ (Data Set Ready), Pins 31, 5: When low, this input indicates that the MODEM or data set is ready to establish the communications link with the UART. The $\overline{DSR}$ signal is a MODEM status input whose condition the CPU can test by reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

Note: Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

$\overline{DTR1}$, $\overline{DTR2}$ (Data Terminal Ready), Pins 25, 11: When low, this output indicates to the MODEM or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

$\overline{ERR}$ (Error), Pin 63: This input is set low by the printer when it has detected an error.

$\overline{INIT}$ (Initialize), Pin 57: This output initializes the printer when it is low. This pin requires an external pull-up resistor (4.7 kΩ is recommended).

$\overline{INTP}$ (Parallel Port Interrupt), Pin 59: This active low, TRI-STATE output signals a parallel port interrupt. The signal is enabled by setting Control Register Bit 4 or by entering the High Performance mode. However, enabling the signal does not cause it to leave the TRI-STATE condition. There must also be an active interrupt condition present in the parallel interface. In the Compatible and Extended modes, the pin will change from a TRI-STATE condition to active low on the rising edge of the $\overline{ACK}$ input. See Section 10 for description of the High Performance mode operation. In all cases, the interrupt is reset to a TRI-STATE condition after the appropriate interrupt service, clearing CTR4, clearing PFR0 (High Performance mode) or Parallel port Reset.

$\overline{INT1}$, $\overline{INT2}$ (Serial Port Interrupt), Pins 45, 60: This active low TRI-STATE output signals a serial interrupt. This pin is asserted if a serial interrupt is enabled, the appropriate interrupt condition exists AND the pin is enabled by the OUT 2 bit (MCR bit 3). The serial interrupts are enabled by setting the appropriate bits in the Interrupt Enable Register (IER). Interrupt conditions include: Receiver Error Flag set, Receiver Data Available, Timeout, Transmitter Empty and Modem Status set. The OUT 2 bit enables/disables the pin according to Table VII in Section 8.10.

This pin is in a TRI-STATE condition if there are no active or enabled interrupts and OUT2 has disabled the pin.

$\overline{MF1}$, $\overline{MF2}$ (Multi-Function), Pins 9, 61: This output can be programmed for any one of three signal functions $\overline{OUT\ 2}$, $\overline{BAUDOUT}$ or $\overline{RXRDY}$. Bits 2 and 1 of the Alternate Function Register select which output signal will be present on this pin. $\overline{OUT\ 2}$ is the default signal and it is selected immediately after master reset. $\overline{OUT\ 2}$ can also be selected by programming bits 2 and 1 of the AFR to 00 or 11. If AFR2,1 = 0,0 or 0,1 or 1,0, the OUT 2 bit enables the serial interrupt pin ($\overline{INT1}$ or $\overline{INT2}$) when it is set to 1. If OUT 2 is 0, the associated interrupt pin is forced to a TRI-STATE condition. If AFR2,1 = 1,1, the OUT 2 bit has no affect on the interrupt pins but it is still present on MF.

The $\overline{OUT\ 2}$ signal can be set active low by programming bit 3 (OUT 2) of the associated channel's MODEM Control Register to a 1. A Master Reset operation sets this signal to its inactive (high) state. Loop Mode holds this signal in its inactive state.

The $\overline{BAUDOUT}$ signal is the 16 × clock output that drives the transmitter and receiver logic of the associated serial channel. This signal is the result of the main reference oscillator frequency divided by the value in the Division Latch Registers. The $\overline{BAUDOUT}$ signal for each channel is internally connected to provide the receiver clock (formerly RCLK on the NS16550AF).

The $\overline{RXRDY}$ signal can be used to request a DMA transfer of data from the RCVR FIFO. Details regarding the active and inactive states of this signal are given in Section 8.5, Bit 3.

$\overline{MR}$ (Master Reset), Pin 39: This active low input is decoded with the UART and parallel port chip selects ($\overline{CS1}$, $\overline{CS2}$ and $\overline{CSP}$) to generate either individual block resets or a full chip reset. If all chip selects are inactive, the MR pin acts as a Master Reset and resets the entire chip. Individual resets are generated by asserting the chip select for the functional block to be reset. See Table I for reset decode and see Table V and Section 10 for register and output signal values upon reset. This input is buffered with a TTL-compatible Schmitt Trigger.

PD0–PD7 (Port Data), Pins 53–46: These bidirectional pins transfer data to and from the peripheral data bus. Table IX describes the inputs that control their direction. These pins have high current drive capability (see DC Electrical Characteristics).

$\overline{PDRQ}$ (Parallel Port DMA Request), Pin 44: The High Performance mode parallel port request for DMA service is available on this pin. With the port programmed for the output direction, $\overline{PDRQ}$ is asserted when the output FIFO is empty. It is deasserted when the FIFO is filled, $\overline{TC}$ is asserted or an error condition is detected. With the port programmed for the input mode, $\overline{PDRQ}$ is asserted when a trigger level of 14 bytes is reached in the input FIFO. It is deasserted when the FIFO is emptied, $\overline{TC}$ is asserted, transfer error or timeout occurs.

PE (Paper End), Pin 67: This input is set high by the printer when it is out of paper.

$\overline{POS}$ ($\overline{POS}$ Mode), Pin 1: This input determines the parallel port mode. A high signal on this pin selects the Extended or Performance Mode (this mode allows the parallel port to be bidirectional). A low signal on this pin selects the Compatible Mode. This mode provides compatibility for AT parallel port software.

$\overline{RD}$ (Read), Pin 37: When this input is low while the chip is selected, the CPU can read status information or data from the selected serial or parallel port register.

$\overline{RI1}$, $\overline{RI2}$ (Ring Indicator), Pins 30, 6: When low, this input indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition the CPU can test by reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input **signal** has changed from a low to a high state since the previous reading of the MODEM Status Register.

Note: Whenever the RI **bit** of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

6.0 Pin Descriptions (Continued)

$\overline{RTS1}$, $\overline{RTS2}$ (Request to Send), Pins 24, 12: When low, this output indicates to the MODEM or data set that the UART is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.

SIN1, SIN2 (Serial Input), Pins 41, 62: This input receives serial data from the communications link (peripheral device, MODEM, or data set). In loop mode operation, data input on this pin is disabled.

SLCT (Select), Pin 65: This input is set high by the printer when it is selected.

$\overline{SLIN}$ (Select Input), Pin 58: This output selects the printer when it is low. This pin requires an external pull-up resistor (4.7 kΩ is recommended).

SOUT1, SOUT2 (Serial Output), Pins 26, 10: This output sends composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation, when the transmitter is empty or when in Loop mode. The SOUT pin also programs the state of the Alternate Function Register bit 4 during reset. AFR4 enables/disables a divide-by-13 circuit between the CLK input and the serial port baud generators. A pull up on this pin will enable the divider circuit and a pull down will disable it. The SOUT pin must have a pull up or pull down. See Section 8.3—Serial Baud Generators for description of divider function.

TABLE I. Reset Decode

$\overline{MR}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CSP}$	Block Reset
0	1	1	1	All
0	1	1	0	Parallel Port
0	1	0	1	UART 2
0	1	0	0	UART 2 & Parallel Port
0	0	1	1	UART 1
0	0	1	0	UART 1 & Parallel Port
0	0	0	1	UART 1 & UART 2
0	0	0	0	All
1	X	X	X	None

Note: See Section 4.1 for specified timing

$\overline{STB}$ (Data Strobe), Pin 55: This output indicates to the peripheral that the data at the parallel port is valid. This pin requires an external pull-up resistor (4.7 kΩ is recommended).

$\overline{TC}$ (Terminal Count), Pin 7: This input indicates the termination of a DMA transfer to the High Performance Parallel port. An interrupt is generated and the High Performance mode is automatically disabled. The PC16553 qualifies a general system Terminal Count with the $\overline{CSP}$ input. This insures that only the $\overline{TC}$ directed to the PC16553 will be recognized.

$\overline{TXRDY1}$, $\overline{TXRDY2}$ (Transmitter Ready), Pins 22, 42: Transmitter DMA signalling is available through this output pin. When operating in the FIFO mode, the CPU selects one of two types of DMA transfer via FCR3. When operating as in the NS16450 Mode, only DMA mode 0 is allowed. Mode 0 supports single transfer DMA where a transfer is made between CPU bus cycles. Mode 1 supports multi-transfer DMA where multiple transfers are made continuously until the XMIT FIFO has been filled. Details regarding the active and inactive states of this signal are given in Section 8.5, Bit 3.

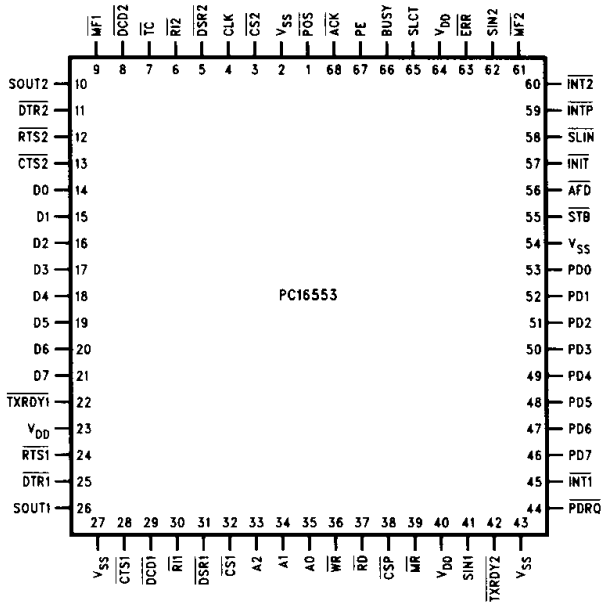
V_{DD} (Power), Pins 23, 40, 64: +5V Supply

V_{SS} (Ground), Pins 2, 27, 43, 54: 0V Reference

$\overline{WR}$ (Write), Pin 36: When this input is low while the chip is selected, the CPU can write control words or data into the selected register.

7.0 Connection Diagram

Chip Carrier Package



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Top View

Order Number PC16553V
See NS Package Number V68A

8.0 UART Registers

TABLE II. UART Register Addresses

DLAB1	$\overline{CS1}$	$\overline{CS2}$	A_2	A_1	A_0	Register	
0	0	1	0	0	0	Receiver Buffer (Read), Transmitter Holding Register (Write)	
0	0	1	0	0	1	Interrupt Enable	C
0	0	1	0	1	0	Interrupt Identification (Read)	H
0	0	1	0	1	0	FIFO Control (Write)	A
X	0	1	0	1	1	Line Control	N
X	0	1	1	0	0	MODEM Control	N
X	0	1	1	0	1	Line Status	E
X	0	1	1	1	0	MODEM Status	L
X	0	1	1	1	1	Scratch	
1	0	1	0	0	0	Divisor Latch (Least Significant Byte)	1
1	0	1	0	0	1	Divisor Latch (Most Significant Byte)	
1	0	1	0	1	0	Alternate Function	
DLAB2	$\overline{CS1}$	$\overline{CS2}$	A_2	A_1	A_0	**Register**	
0	1	0	0	0	0	Receiver Buffer (Read), Transmitter Holding Register (Write)	
0	1	0	0	0	1	Interrupt Enable	C
0	1	0	0	1	0	Interrupt Identification (Read)	H
0	1	0	0	1	0	FIFO Control (Write)	A
X	1	0	0	1	1	Line Control	N
X	1	0	1	0	0	MODEM Control	N
X	1	0	1	0	1	Line Status	E
X	1	0	1	1	0	MODEM Status	L
X	1	0	1	1	1	Scratch	
1	1	0	0	0	0	Divisor Latch (Least Significant Byte)	2
1	1	0	0	0	1	Divisor Latch (Most Significant Byte)	
1	1	0	0	1	0	Alternate Function	

TABLE III. Register Summary for an Individual Channel

Bit No.	Register Address												
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	2	3	4	5	6	7	0 DLAB = 1	1 DLAB = 1	2 DLAB = 1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	FIFO Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Reg-ister	Divisor Latch (LS)	Divisor Latch (MS)	Alternate Function Register
	RBR	THR	IER	IIR	FCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM	AFR
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERDAI)	"0" if Interrupt Pending	FIFO Enable	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8	Concurrent Write
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Interrupt ID Bit	RCVR FIFO Reset	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9	$\overline{\text{BAUDOUT}}$ Select
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit	XMIT FIFO Reset	Number of Stop Bits (STB)	Out 1 Bit	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10	$\overline{\text{RXRDY}}$ Select
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EMSI)	Interrupt ID Bit (Note 2)	DMA Mode Select	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11	$\overline{\text{CTS}}$ Auto Enable/ Disable
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12	Disable ÷ 13 Clock
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13	0
6	Data Bit 6	Data Bit 6	0	FIFOs Enabled (Note 2)	RCVR Trigger (LSB)	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14	0
7	Data Bit 7	Data Bit 7	0	FIFOs Enabled (Note 2)	RCVR Trigger (MSB)	Divisor Latch Access Bit (DLAB)	0	Error in RCVR FIFO (Note 2)	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15	0

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: These bits are always 0 in the NS16450 Mode.

8.0 UART Registers (Continued)

Two identical register sets, one for each channel, are in the PC16553. All register descriptions in this section apply to the register sets in both channels.

8.1 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange and sets the Divisor Latch Access bit via the Line Control Register (LCR). This is a read and write register. Table III shows the contents of the LCR. Details on each bit follow:

Bits 0 and 1: These two bits specify the number of data bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Data Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted with each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit data length is selected, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When parity is enabled and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When parity is enabled and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1 (Mark Parity). If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing state (logic 0). The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator or the Alternate Function Register during a Read or Write operation. It must be set low (logic 0) to access any other register.

Composite Serial Data

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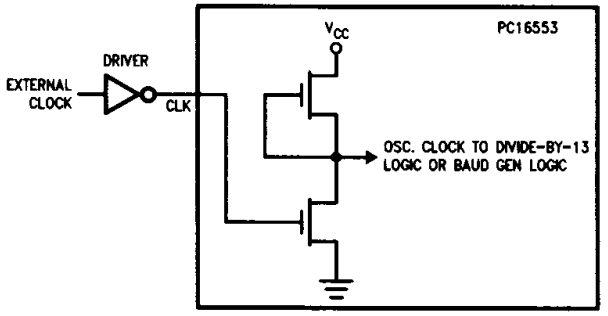
8.2 TYPICAL CLOCK CIRCUITS



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8.3 PROGRAMMABLE BAUD GENERATOR

The PC16553 contains two independently programmable Baud Generators. Each is capable of taking a common clock input from DC to 24.0 MHz and dividing it by any divisor from 1 to $2^{16} - 1$. The highest input clock frequency recommended with a divisor = 1 is 24 MHz. The output frequency of the Baud Generator is 16 × the baud rate, [divisor # = (frequency input) ÷ (baud rate × 16)]. The output of each Baud Generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud Counter is loaded.

Table V provides decimal divisors to use with crystal frequencies of 1.8432 MHz, 3.072 MHz, 18.432 MHz and 24 MHz. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen. Using a divisor of zero is **not** recommended.

To facilitate driving the PC16553 with a 24 MHz oscillator, two independent divide-by-13 circuits are implemented between the CLK input and the serial port baud generators. If the divider circuits are enabled, the baud generators are clocked by an industry standard 1.84 MHz frequency. Disabling the dividers cause the baud generators to be driven by a 24 MHz clock directly, allowing baud rates of up to 1.5M. Bit 4 of the Alternate Function Register enables/disables the divider function. The divider is enabled when AFR4 = 0 and disabled when AFR4 = 1. The bit can be programmed at any time by software. The bit is also hardware programmed during Reset. At the trailing edge of $\overline{MR}$, the state of the SOUT pin is sensed and its complement is latched into AFR4. Thus a pull up resistor (4.7k or greater) on the SOUT pin will enable the divide-by-13 circuit and a pull down will disable the circuit.

8.0 UART Registers (Continued)

TABLE IV. UART Reset Configuration

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	**0000** 0000 (Note 1)
Interrupt Identification Register	Master Reset	00**00** 0001
FIFO Control	Master Reset	00**00** 0000
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	**0000** 0000
Line Status Register	Master Reset	0110 0000
MODEM Status Register	Master Reset	XXXX 0000 (Note 2)
Alternate Function Register	Master Reset	0000 **0000**
SOUT	Master Reset	High
INT (RCVR Errs)	Read LSR/MR	TRI-STATE
INT (RCVR Data Ready)	Read RBR/MR	TRI-STATE
INT (THRE)	Read IIR/Write THR/MR	TRI-STATE
INT (Modem Status Changes)	Read MSR/MR	TRI-STATE
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
RCVR FIFO	MR/FCR1•FCR0/ΔFCR0	All Bits Low
XMIT FIFO	MR/FCR1•FCR0/ΔFCR0	All Bits Low

Note 1: Boldface bits are permanently low.

Note 2: Bits 7–4 are driven by the input signals.

8.4 LINE STATUS REGISTER

This register provides status information to the CPU concerning the data transfer. Table III shows the contents of the Line Status Register. Details on each bit follow:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic 0 by reading all of the data in the Receiver Buffer Register or the FIFO.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that the next character received was transferred into the Receiver Buffer Register before the CPU could read the previously received character. This transfer destroys the previous character. The OE indicator is set to a logic 1 during the character stop bit time when the overrun condition exists. It is reset whenever the CPU reads the contents of the Line Status Register. If the FIFO mode data continues to fill the FIFO beyond the trigger level, an overrun error will occur only after the FIFO is full and the next character has been completely received in the shift register. OE is indicated to the CPU as soon as it happens. The character in the shift register can be overwritten, but it is not transferred to the FIFO.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 during the character Stop bit time when the character has a parity error. It is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register or when the next character is loaded into the Receiver Buffer Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. The FE bit is set to a logic 1 when the serial channel detects a logic 0 during the first Stop bit time. The FE indicator is reset whenever the CPU reads the contents of the Line Status Register or when the next character is loaded into the Receiver Buffer Register. In the FIFO Mode this error is associated with the particular character in the FIFO it applies to. This error is revealed to the CPU when its associated character is at the top of the FIFO. The serial channel will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this "start" bit twice and then takes in the "data".

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register or when the next valid character is loaded into the Receiver Buffer Register. In the FIFO Mode this condition is associated with the particular character in the FIFO it applies to. It is revealed to the CPU when its associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. The next character transfer is en-

8.0 UART Registers (Continued)

abled after SIN goes to the marking state and receives the next valid start bit.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. In the 16450 mode bit 5 indicates that the associated serial channel is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU. In the FIFO mode this bit is set when the XMIT FIFO is empty; it is cleared when at least 1 byte is written to the XMIT FIFO.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmitter FIFO and shift register are both empty.

Bit 7: In the NS16450 Mode this is a 0. In the FIFO Mode LSR7 is set when there is at least one parity error, framing error or break indication in the FIFO. LSR7 is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing. In the FIFO mode the user must load a data byte into the Rx FIFO in order to write to LSR2–4. LSR0 and LSR7 cannot be written to in the FIFO mode.

8.5 FIFO CONTROL REGISTER

This is a write only register at the same location as the IIR (the IIR is a read only register). This register is used to enable the FIFOs, clear the FIFOs, set the RCVR FIFO trigger level, and select the type of DMA signalling.

Bit 0: Writing a 1 to FCR0 enables both the XMIT and RCVR FIFOs. Resetting FCR0 will clear all bytes in both FIFOs.

When changing from FIFO Mode to NS16450 Mode and vice versa, data is automatically cleared from the FIFOs. This bit must be a 1 when other FCR bits are written to or they will not be programmed.

Bit 1: Writing a 1 to FCR1 clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 2: Writing a 1 to FCR2 clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. The 1 that is written to this bit position is self-clearing.

Bit 3: Writing a 1 to FCR3 causes $\overline{\text{RXRDY}}$ and $\overline{\text{TXRDY}}$ operations to change from mode 0 to mode 1 if FCR0 = 1.

RXRDY Mode 0: When in the NS16450 Mode (FCR0 = 0) or in the FIFO Mode (FCR0 = 1, FCR3 = 0) and there is at least 1 character in the RCVR FIFO or RCVR Buffer Register, the $\overline{\text{RXRDY}}$ pin will go low active. Once active the $\overline{\text{RXRDY}}$ pin will go inactive when there are no more characters in the FIFO or Buffer Register.

TABLE Va. Baud Rates, Divisors and Crystals (Internal ÷ 13 Disabled)

Baud Rate	1.8432 MHz Crystal		3.072 MHz Crystal		18.432 MHz Crystal	
	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error
50	2304	—	3840	—	23040	—
75	1536	—	2560	—	15360	—
110	1047	0.026	1745	0.026	10473	—
134.5	857	0.058	1428	0.034	8565	—
150	768	—	1280	—	7680	—
300	384	—	640	—	3840	—
600	192	—	320	—	1920	—
1200	96	—	160	—	920	—
1800	64	—	107	0.312	640	—
2000	58	0.69	96	—	576	—
2400	48	—	80	—	480	—
3600	32	—	53	0.628	320	—
4800	24	—	40	—	240	—
7200	16	—	27	1.23	160	—
9600	12	—	20	—	120	—
19200	6	—	10	—	60	—
38400	3	—	5	—	30	—
56000	2	2.86	—	—	21	2.04
128000	—	—	—	—	9	—

Note: For baud rates of 250k, 300k, 375k, 500k, 750k and 1.5M using a 24 MHz crystal causes minimal error.

8.0 UART Registers (Continued)

TABLE Vb. 24 MHz Baud Rates, Divisors and Crystals (24 MHz Crystal)

Baud Rate	÷ 13 Enabled		÷ 13 Disabled	
	Decimal Divisor for 16 × Clock	Percent Error	Decimal Divisor for 16 × Clock	Percent Error
50	2304	0.1	30000	—
75	1536	—	20000	—
110	1047	—	13636	—
134.5	857	0.4	11152	—
150	768	—	10000	—
300	384	—	5000	—
600	192	—	2500	—
1200	96	—	1250	—
1800	64	—	833	0.042
2000	58	0.5	750	—
2400	48	—	625	—
3600	32	—	417	0.16
4800	24	—	313	0.16
7200	16	—	208	0.16
9600	12	—	156	0.16
19200	6	—	78	0.16
38400	3	—	39	0.16
56000	2	3.0	27	0.79
128000	1	—	12	2.34
250000	—	—	6	—
300000	—	—	5	—
375000	—	—	4	—
500000	—	—	3	—
750000	—	—	2	—
1500000	—	—	1	—

Note: The percent error for all baud rates except when indicated otherwise is 0.2%.

RXRDY Mode 1: In the FIFO Mode (FCR0 = 1) when the FCR3 = 1 and the trigger level or the timeout has been reached, the $\overline{\text{RXRDY}}$ pin will go low active. Once it is activated it will go inactive when there are no more characters in the FIFO.

TXRDY Mode 0: In the NS16450 Mode (FCR0 = 0) or in the FIFO Mode (FCR0 = 1, FCR3 = 0) when there are no characters in the XMIT FIFO or XMIT Holding Register, the $\overline{\text{TXRDY}}$ pin will go low active. Once active the $\overline{\text{TXRDY}}$ pin will go inactive after the first character is loaded into the XMIT FIFO or Holding Register.

TXRDY Mode 1: In the FIFO Mode (FCR0 = 1, FCR3 = 1) and when there are no characters in the XMIT FIFO, the $\overline{\text{TXRDY}}$ pin will go low active. This pin will become inactive when the XMIT FIFO is completely full.

Bit 4, 5: FCR4 to FCR5 are reserved for future use.

Bit 6, 7: FCR6 and FCR7 are used to designate the interrupt trigger level. When the number of bytes in the RCVR FIFO equals the designated interrupt trigger level, a Received Data Available Interrupt is activated. This interrupt must be enabled by setting IER0.

FCR Bits 7 6	RCVR FIFO Trigger Level (Bytes)
0 0	01
0 1	04
1 0	08
1 1	14

8.6 INTERRUPT IDENTIFICATION REGISTER

In order to provide minimum software overhead during data character transfers, each serial channel of the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status.

When the CPU reads the IIR, the associated UART serial channel freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the associated UART serial channel records new interrupts, but does not change its current indication until the access is complete. Table III shows the contents of the IIR. Details on each bit follow:

8.0 UART Registers (Continued)

Bit 0: This bit can be used in a prioritized interrupt environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR identify the highest priority interrupt pending from those shown in Table VI.

Bit 3: In the NS16450 Mode this bit is 0. In the FIFO Mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5: These two bits of the IIR are always logic 0.

Bits 6 and 7: These two bits are set when FCR0 = 1. (FIFO Mode enabled.)

8.7 INTERRUPT ENABLE REGISTER

This register enables five types of interrupts for the associated serial channel. Each interrupt can individually activate the interrupt ($\overline{INT}$) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of the IER register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the $\overline{INT}$ output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table III shows the contents of the IER. Details on each bit follow:

Bit 0: When set to logic 1 this bit enables the Received Data Available Interrupt and Timeout Interrupt in the FIFO Mode.

Bit 1: When set to logic 1 this bit enables the Transmitter Holding Register Empty Interrupt.

Bit 2: When set to logic 1 this bit enables the Receiver Line Status Interrupt.

Bit 3: When set to logic 1 this bit enables the MODEM Status Interrupt.

Bits 4 through 7: These four bits are always logic 0.

8.8 MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table III and are described below:

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit is the $\overline{OUT\ 1}$ bit. It does **not** have an output pin associated with it. It can be written to and read by the CPU. In Local Loopback Mode this bit controls bit 2 of the Modem Status Register.

TABLE VI. Interrupt Control Functions

FIFO Mode Only	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available or Trigger Level Reached	Reading the Receiver Buffer Register or the FIFO Drops below the Trigger Level
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed from or Input to the RCVR FIFO During the Last 4 Char. Times and There is at Least 1 Char. in it During This Time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

8.0 UART Registers (Continued)

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ pin in a manner identical to that described above for bit 0.

The function of this bit is multiplexed on a single output pin with two other functions: $\overline{BAUDOUT}$ and $\overline{RXRDY}$. $\overline{OUT\ 2}$ is the default function of the pin after a master reset. See Section 8.10 for more information about selecting one of these 3 functions via the $\overline{MF}$ pin.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the associated serial channel. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$, and $\overline{DCD}$) are disconnected; the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs; and the MODEM Control output pins are forced to their inactive state (high). In this diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify transmit and receive data paths of the UART.

In this diagnostic mode, the receiver and transmitter interrupts are fully operational. Their sources are external to the part. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

8.9 MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. The latter bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table III and described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 in the MCR.

8.10 ALTERNATE FUNCTION REGISTER

This is a read/write register used to select specific modes of operation. It is located at address 010 when the DLAB bit is set.

Bit 0: When this bit is set the CPU can write concurrently to the same register in both register sets. This function is intended to reduce the UART initialization time. It can be used by a CPU when both channels are initialized to the same state. The CPU can set or clear this bit by accessing either register set. When this bit is set the channel select pin still selects the channel to be accessed during read operations. Setting or clearing this bit has **no** effect on read operations.

The user should ensure that the DLAB bit (LCR7) of both channels are in the same state before executing a concurrent write to register addresses 0, 1 and 2.

Bits 1 and 2: These select the output signal that will be present on the multi-function pin, $\overline{MF}$. These bits are individually programmable for each channel, so that different signals can be selected on each channel. Table VII associates the signal present at the multi-function pin with the bit code.

TABLE VII

AFR2	AFR1	Multi-Function Pin (MFn)	OUT 2 Bit	Serial Interrupt Control
0	0	$\overline{OUT\ 2}$	0	$\overline{INTn}$ Disabled
0	0	$\overline{OUT\ 2}$	1	$\overline{INTn}$ Enabled
0	1	$\overline{BAUDOUT}$	0	$\overline{INTn}$ Disabled
0	1	$\overline{BAUDOUT}$	1	$\overline{INTn}$ Enabled
1	0	$\overline{RXRDY}$	0	$\overline{INTn}$ Disabled
1	0	$\overline{RXRDY}$	1	$\overline{INTn}$ Enabled
1	1	$\overline{OUT\ 2}$	X	$\overline{INTn}$ Enabled

Note: n denotes the specific UART channel (1 or 2)

Bit 3: When this bit is set, the modem input $\overline{CTS}$ automatically controls serial transmission. With this feature enabled and $\overline{CTS}$ = 1, no data will be transferred from the Transmit Holding Register or Transmit FIFO into the shift register, thus halting transmission. Serial transmission is restarted when $\overline{CTS}$ goes active or a 0 is written to this bit.

Bit 4: Setting this bit disables the divide-by-13 circuit implemented between the CLK pin and the serial port baud generators. Disabling the circuit allows a 24 MHz input to generate baud rates up to 1.5M.

Bits 5 through 7: These bits are permanently set to a logic 0.

8.11 SCRATCHPAD REGISTER

This 8-bit Read/Write Register does not control the serial channel in any way. It is intended as a Scratchpad Register to be used by the programmer to hold data temporarily.

9.0 FIFO Mode Operation

Each serial channel has two 16-byte FIFOs associated with it. The operational description that follows is applicable to the FIFOs of both channels.

9.1 FIFO INTERRUPT OPERATION

When the RCVR FIFO and receiver interrupt are enabled (FCR0 = 1, IER0 = 1) Receive Data Available Interrupts will occur as follows:

A. The Receive Data Available Interrupt will be issued to the CPU when the number of bytes in the RCVR FIFO equals the programmed trigger level; it will be cleared as soon as the number of bytes in the RCVR FIFO drops below its programmed trigger level.

B. The IIR Receive Data Available Indication also occurs when the FIFO trigger level is reached, and like the interrupt it is cleared when the FIFO drops below the trigger level.

C. The Receiver Line Status Interrupt (IIR = 06), as before, has higher priority than the Received Data Available (IIR = 04) Interrupt.

D. The data ready bit (LSR0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the RCVR FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts will occur as follows:

A. A RCVR FIFO Timeout Interrupt will occur, if the following conditions exist:

— at least one character is in the RCVR FIFO

— the most recent serial character received was longer than 4 continuous character times ago (if 2 stop bits are programmed the second one is included in this time delay).

— the most recent CPU read of the RCVR FIFO was longer than 4 continuous character times ago.

The maximum time between a received character and a timeout interrupt will be 160 ms at 300 baud with a 12-bit receive character (i.e. 1 START, 8 DATA, 1 PARITY and 2 STOP BITS).

B. Character times are calculated by using the $\overline{\text{BAUDOUT}}$ signal as a clock signal (this makes the delay proportional to the baud rate).

C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.

D. When the timeout interrupt indication is inactive the timeout indication timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO interrupts are enabled (FCR0 = 1, IER1 = 1), XMIT interrupts will occur as follows:

A. The Transmitter Holding Register Empty Interrupt occurs when the XMIT FIFO is empty. It is cleared as soon as the Transmitter Holding Register is written to (1 to 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.

B. The transmitter FIFO empty indications will be delayed 1 character time minus the last Stop bit time whenever the following occurs: THRE = 1 and there have not been at least two bytes at the same time in the transmit FIFO, since the last THRE = 1. The first Transmitter Holding Register Empty Interrupt after changing FCR0 will be immediate, if it is enabled.

This delay prevents the UART from issuing a second Transmitter Holding Register Empty Interrupt as soon as it transfers the first character into the Transmitter Shift Register.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO Empty has the same priority as the current Transmitter Holding Register Empty Interrupt.

9.2 FIFO POLLED OPERATION

With FCR0 = 1 resetting IER0, IER1, IER2, IER3 or all to zero puts the associated serial channel in the FIFO Polled Mode of operation. Since the receiver and transmitter are controlled separately either one or both can be in the polled mode of operation.

In this mode the user's program will check receiver and transmitter status via the LSR. As stated in Section 8.4:

LSR0 will be set as long as there is one byte in the RCVR FIFO.

LSR1 to LSR4 will specify which error(s) has occurred. Character error status is handled the same way as in the interrupt mode.

LSR5 will indicate when the XMIT FIFO is empty.

LSR6 will indicate that both the XMIT FIFO and shift register are empty.

LSR7 will indicate whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are otherwise functional.

10.0 Bidirectional Parallel Port Interface

This parallel interface is designed to provide all of the signals and registers needed to be compatible with the parallel ports designed into IBM PC, XT, AT and PS/2 and compatible machines. In addition it implements a high performance FIFO option.

The Compatible mode features a single byte unidirectional (output) port. Data transfers are controlled through interrupts or polling. Data, control and status are provided by the Data Register (DTR), Control Register (CTR) and Status Register (STR). It is fully compatible with the ports designed into IBM PC, XT and AT and compatible machines.

The Extended mode is enabled via the $\overline{POS}$ pin and features a bidirectional single byte port. Data transfers are controlled through interrupts or polling. Data, control and status are provided by the Data Register (DTR), Control Register (CTR) and Status Register (STR). The Expansion mode is fully compatible with existing IBM PS/2 machines.

The High Performance mode is enabled through software by setting bit 0 in a secondary register called Performance Register (PFR). This mode features a 16-byte bidirectional FIFO, DMA data transfer capability, and automated handshaking to facilitate data transfer to and from the FIFO and peripherals. The PFR is implemented to provide FIFO control and status. When the PFR is activated (see Section 10.4), it replaces the IBM reserved location base+3 in the LPT1, 2 and 3 I/O spaces. In addition, bit 5 of the Control Register (CTR5) and bits 0 and 1 of the Status Register (STR0,1) have new functions.

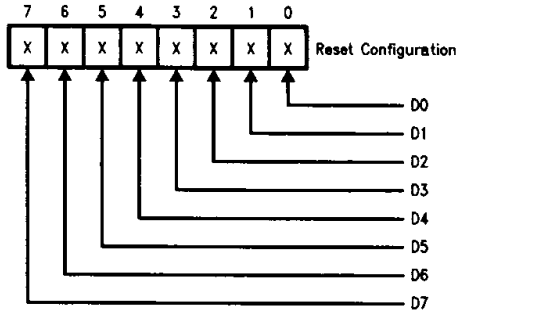
Table VIII illustrates the address assignments for all registers and the following sections describe the register functions.

TABLE VIII

$\overline{CSP}$	$\overline{POS}$	PFR0	A1	A0	Register
COMPATIBLE MODE					
0	0	X	0	0	Data
0	0	X	0	1	Status
0	0	X	1	0	Control
EXTENDED MODE					
0	1	0	0	0	Data
0	1	0	0	1	Status
0	1	0	1	0	Control
HIGH PERFORMANCE MODE					
0	1	1	0	0	Data
0	1	1	0	1	Status
0	1	1	1	0	Control
0	1	1	1	1	Performance (Note 1)

Note 1: This location is only accessible after a 0 is written to the Status Register bit 0 (see Section 10.4).

10.1 DATA REGISTER (DTR)



TL/C/10463-30

This is a bidirectional data port that transfers 8-bit data in the direction determined by the $\overline{POS}$ Mode pin, the Data Port Direction bit (CTR5), and the $\overline{RD}$ and $\overline{WR}$ strobes (see Table IX).

TABLE IX. Data Register Read and Write Modes

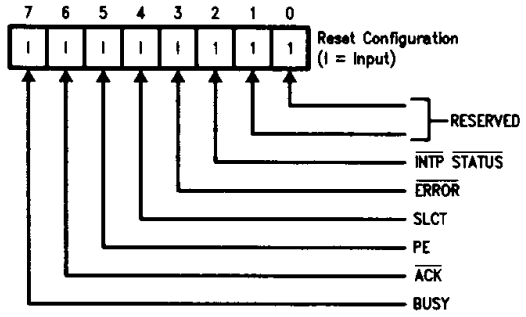
$\overline{POS}$ Mode Pin	Control Register Direction Bit	$\overline{RD}$	$\overline{WR}$	Result
0 (compatible)	X	1	0	Data Written to PD0–PD7
0	X	0	1	Data Previously Written is Read
1 (extended)	0	1	0	Data Written to PD0–PD7
1	1	1	0	Data Written is Latched
1	0	0	1	Data Previously Written is Read
1	1	0	1	Data is Read from PD0–PD7

In compatible mode a write operation to this register causes the data to be presented on pins PD0–PD7. A read operation in this mode causes the register to present the last data written to it by the CPU.

In the extended mode a write operation to this register causes the data to be latched. If the Data Port Direction bit (CTR5) is 0 the latched data is presented to the pins; if it is 1 the data is only latched. In the extended mode with the Data Port Direction bit is 0, a read operation to this register allows the CPU to read the last data it wrote to the port. In the extended mode with the Data Port Direction bit set to 1 (read), a read operation to this register causes the port to present to the CPU the data on pins PD0–PD7.

10.0 Bidirectional Parallel Port Interface (Continued)

10.2 STATUS REGISTER (STR)



TL/C/10463–31

This register provides status for the signals listed below. It is a read only register. Writing to bits 7–1 is an invalid operation that has no effect.

Bit 0, 1: These bits are reserved. See Section 10.4 for alternate functions for Status Register Bits 0 and 1.

Bit 2: This bit ($\overline{\text{INTP STATUS}}$) is latched low when CTR4 = 1 and the printer acknowledge signal, $\overline{\text{ACK}}$, makes a transition from low to high, indicating the printer has received the previously sent data byte. Reading this bit resets it to 1.

Bit 3: This bit ($\overline{\text{ERROR}}$) represents the current state of the printer error signal. The printer sets this bit low when there is a printer error. This bit follows the state of the $\overline{\text{ERR}}$ pin.

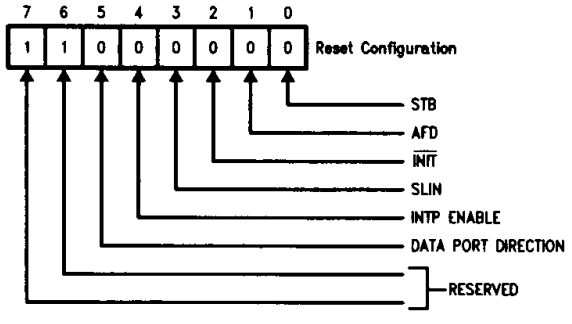
Bit 4: This bit (SLCT) represents the current state of the printer select signal. The printer sets this bit high when it is selected. This bit follows the state of the SLCT pin.

Bit 5: This bit (PE) represents the current state of the printer paper end signal. The printer sets this bit high when it detects the end of the paper. This bit follows the state of the PE pin.

Bit 6: This bit ($\overline{\text{ACK}}$) represents the current state of the printer acknowledge signal. The printer sets this signal to low after it has received a character and is ready to receive another one. This bit follows the state of the $\overline{\text{ACK}}$ pin.

Bit 7: This bit ($\overline{\text{BUSY}}$) represents the current state of the printer busy signal. The printer sets this bit low when it is busy and cannot accept another character. This bit is the inverse of the BUSY pin.

10.3 CONTROL REGISTER (CTR)



TL/C/10463–32

This register provides all output signals to control the printer in the compatible or extended mode. This is a read and write register.

Normally when the Control Register is read, the bit values are provided by the output latch. These bit values can be superseded by the logic level of the $\overline{\text{STB}}$, $\overline{\text{AFD}}$, INIT, and $\overline{\text{SLIN}}$ pins, if these pins are forced high or low by an external voltage. In order to force these pins high or low the corresponding bits should be set to their inactive state (e.g., AFD = STB = SLIN = 0, $\overline{\text{INIT}}$ = 1).

Bit 0: This bit controls the data strobe signal to the printer via the $\overline{\text{STB}}$ pin. This bit is the inverse of the $\overline{\text{STB}}$ pin.

Bit 1: This bit controls the automatic feed XT signal to the printer via the $\overline{\text{AFD}}$ pin. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the $\overline{\text{AFD}}$ pin.

Bit 2: This bit controls the signal to initialize the printer via the $\overline{\text{INIT}}$ pin. Setting this bit to low initializes the printer. This bit follows the $\overline{\text{INIT}}$ pin.

Bit 3: This bit directly controls the select in signal to the printer via the $\overline{\text{SLIN}}$ pin. Setting this bit high selects the printer. This bit is the inverse of the $\overline{\text{SLIN}}$ pin.

Bit 4: This bit enables the parallel port interrupt. When this bit is set high, the INTP signal follows the $\overline{\text{ACK}}$ signal and latches a 0 to 1 transition. Setting this bit low, puts INTP into TRI-STATE and clears any pending interrupts.

Bit 5: This bit controls the direction of the data port in the Extended (bidirectional) Mode (see Table IX and Performance Mode). This is a write-only bit in Extended Mode but is readable and writable in Performance Mode.

Bit 6, 7: These bits are reserved.

10.4 PERFORMANCE REGISTER AND THE HIGH PERFORMANCE MODE

This programmable high performance cell allows the parallel port to transfer multiple bytes of data to or from a peripheral without the CPU having to affect each transfer. These transfers are supported by:

1. An on-chip bidirectional FIFO that can store 16 bytes of data.
2. A DMA request strobe, $\overline{\text{PDRQ}}$ which facilitates DMA servicing of data transfer requests from the parallel port.
3. An automated handshake capability (Centronics compatible) for transfer of FIFO data to and from the attached peripheral.

Data may be loaded into or unloaded from the FIFO by the CPU (interrupt or polling modes) or by the system DMA controller. These functions greatly reduce software overhead associated with parallel port I/O.

To maintain compatibility with existing IBM and compatible PC parallel port interfaces, the Performance Register is hidden and the High Performance mode is disabled after system power up. The Performance Register (PFR) is only available after a 0 is written to the Status Register bit 0. It occupies the reserved location base+3 in the IBM parallel port I/O spaces. The FIFO and automatic transfers (High Performance mode) can then be enabled by writing a 1 to Performance bit 0 (Performance Enable). Writing a 0 to STR0 also enables new functions for bits CTR5 and STR1. CTR5 is the Data Direction bit and is changed from write-only in the Extended Mode to being readable. STR1 is reserved in the Compatible and Extended Modes but becomes a FIFO Overrun bit in Performance Mode.

10.0 Bidirectional Parallel Port Interface (Continued)

The existence of the High Performance mode within a parallel port interface can be identified by reading the Status Register I/O location following a write of 0 to the same register's bit 0. The Status register is replaced, for one read only, by an ID byte of A7h. Further accesses to the Status Register location will produce the standard Status Register bits with the addition of a FIFO Overrun error indication in Bit 1.

Procedure for initializing high performance cell:

— program Data Direction bit (CTR5)

— write 0 to STR0

— read back value in STR

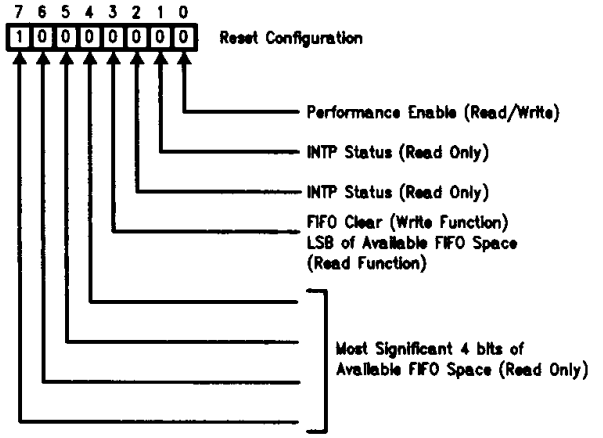
— if value = A7h, proceed with initialization

— write a 1 to the Performance Register bit 0 (FIFO Enable) enabling FIFOs and automatic handshaking.

Writing a 1 to STR0 hides the Performance Register but does not disable the High Performance mode. The mode can only be disabled by clearing the FIFO Enable bit in the Performance Register.

Note: The ID byte in the Status Register location does NOT present itself if a 1 is written to STR0.

Performance Register



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This register provides control and status bits for parallel port data transfers in the High Performance mode. Access to this register is only allowed after a 0 is written to STR0. Different status and control functions are provided by bits 1, 2, and 3 depending on the direction of the data transfer. Therefore, the software should program the Data Port Direction bit (CTR5) before accessing the Performance Register. Note that Performance Register bits 1–7 are accessible regardless of whether the High Performance Mode is enabled (PFR0 = 1)

Bit 7–3: Reading these 5 bits provide a binary representation of the number of open spaces in the FIFO. The FIFO is 16 bytes deep. The number of bytes in the FIFO can be determined by subtracting the decimal equivalent of these bits from 16 (the maximum number of bytes in the FIFO).

Bit 3: The write function of this bit is FIFO Clear. Writing a 1 to this bit clears the FIFO of its contents. Input FIFO Service and Timeout interrupts are also cleared. This is a self-clearing bit.

Bit 2, 1: These bits indicate the interrupt status and are indicated in order of priority with 00 being the highest priority and 11 being the lowest.

Bit 0: Setting the Performance Enable bit generates the following actions:

1. The Data Register is replaced by the 16-byte FIFO.
2. Automatic handshaking and data transfers between an attached peripheral and the FIFO begins (see Parallel Port Operation).
3. If in DMA mode (CTR4 INTP Enable bit = 0), the DMA request strobe $\overline{\text{PDRQ}}$ is enabled (conditions for assertion of $\overline{\text{PDRQ}}$ are described in the following material).
4. SLCT, ERROR and PE interrupts are automatically enabled.
5. Timeout and Overrun interrupts are enabled if in input mode (CTR5 = 1).
6. If CTR4 INTP Enable bit = 1 (Interrupt Mode), the FIFO Service interrupt is enabled. If CTR4 INTP Enable bit = 0 (DMA mode), the TC interrupt is enabled.

The bit is automatically cleared (High Performance mode exited) if a Status, Overrun or TC interrupt occurs. Note that these conditions do NOT clear the FIFO contents.

Interrupt Definitions

Bit 2	Bit 1	Interrupt
0	0	No Interrupt
0	1	Status/Overrun
1	0	Timeout
1	1	FIFO Service (Interrupt Mode) TC (DMA Mode)

No Interrupt: No interrupts are pending from the parallel port.

Status/Overrun: When the parallel port direction is set for output, this code indicates that a Status interrupt has occurred. When the direction is set for input, the code indicates a Status or an Input FIFO Overrun error. The Status interrupts are automatically enabled in High Performance mode (Control Register bit 4, INTP Enable, is ignored) and are generated by the active edges of the SLCT, ERROR or PE input signals. The Overrun interrupt is also automatically

10.0 Bidirectional Parallel Port Interface (Continued)

enabled in the input mode and occurs if greater than 16 bytes are transferred to the FIFO by the peripheral without any service from the system. The byte causing the Overrun error is not loaded into the FIFO and is lost. The source of the Status/Overrun interrupt can be determined by reading the Status Register. Bit 1 is cleared if an overrun has occurred and the states of the SLCT, $\overline{\text{ERROR}}$ and PE pins will determine the source of a Status error.

The Status and Overrun interrupts are cleared by reading the Performance Register.

Timeout: This interrupt is only valid for the input direction and is asserted when there is data in the FIFO and no transfers in or out of the FIFO have occurred during the last 4.4 ms.

The interrupt is cleared by setting the FIFO Clear bit (PFR3) or by the first read of the input FIFO.

FIFO Service/TC: In Interrupt Mode (CTR4 = 1), this interrupt indicates that the CPU should either load or remove data from the FIFO depending on the port direction. In DMA Mode this interrupt indicates that the port has received a terminal count (TC) from the servicing DMA controller channel. See DMA End of Transfer timing diagrams for details on the TC interrupt.

In the Interrupt mode, output direction, the interrupt is cleared by reading the PFR or by the first write to the output FIFO. In interrupt mode, input direction, the interrupt is cleared by reading the input FIFO until the data level is below the trigger level or by setting the FIFO Clear bit (PFR3). In DMA mode, the TC interrupt is cleared by reading the Performance Register.

Performance Port Operation

The following sections describe in more detail the operation of the High Performance port. Refer also to the attached flowcharts. Data flow through the High Performance port is summarized by Table X.

When the Data Port Direction bit is 0 (output) and the FIFO Enable bit is set, data requests issued to the host and subsequent transfers to the peripheral will be done by the parallel port automatically. The cell will output the next byte in the FIFO to pins PD0–PD7 and strobe pin $\overline{\text{STB}}$ in response to a 0 to 1 transition on the $\overline{\text{ACK}}$ pin. A byte will be output only if BUSY, $\overline{\text{ERR}}$ and PE are inactive and SLCT is active. The cell requests FIFO service from the system CPU or DMA controller when the FIFO is empty. The Status Register and the Control Register may be read or written by the CPU. However, the $\overline{\text{STB}}$ bit in the Control Register has no function when the FIFO Enable bit is set. The cell will also request CPU service if $\overline{\text{ERR}}$, PE or SLCT are asserted by the peripheral during data transfers. In DMA mode, a TC indication will cause an interrupt to be generated but only after the last byte in the output FIFO has been transferred. PFR0 will also be cleared at this point.

When the Data Port Direction bit is 1 (input) and the FIFO Enable bit is set, requests for data from the host and subsequent data transfers from a peripheral to the host will be done by the parallel port automatically. Two signals are used to transfer the data. The $\overline{\text{SLIN}}$ pin will be asserted by the host system to indicate to the peripheral that the parallel port is ready to accept data. The $\overline{\text{ACK}}$ pin will be used by the peripheral to strobe the data into the input FIFO. When the input FIFO reaches a trigger level of 14, the cell requests FIFO service from the system CPU or DMA controller. In DMA mode, a TC indication generates an interrupt and clears PFR0 immediately.

Note: The trigger level is not programmable. It defaults to 14 bytes.

If the FIFO is not serviced before it fills to 16 bytes, the cell stops further transfers from the peripheral by automatically deasserting $\overline{\text{SLIN}}$. $\overline{\text{SLIN}}$ will go active again when the input FIFO is empty. The CPU may read either the Status register or the Control register during automatic transfers. However, writing to these registers has no effect other than to change the Data Port direction or the INTP Enable state.

The INTP Enable bit in the Control register (CTR4) defines whether FIFO service requests are made with an interrupt ($\overline{\text{INTP}}$) or with a DMA request ($\overline{\text{PDRQ}}$). Setting CTR4 enables interrupts while clearing it (default condition) enables DMA. The programmer must have the system prepared to handle a DMA request or an interrupt immediately upon setting the Performance Enable bit if the data direction is output. Since the output FIFO is initially empty, the DMA request strobe $\overline{\text{PDRQ}}$ or the interrupt pin $\overline{\text{INTP}}$ will go active immediately after the Performance Enable bit is set.

The Performance Enable bit is cleared (Performance mode disabled) if a Status, Overrun or End of Transfer (TC active) interrupt is generated.

A timeout period of 4.4 ms is calculated on chip. The timer is used during input operations and exists so that data which is below the 14-byte threshold will be able to trigger a CPU interrupt. This interrupt notifies the CPU that there has been data in the Input FIFO longer than 4.4 ms with no further data from the peripheral being loaded. Note that a 24 MHz input on the CLK pin is required to create the 4.4 ms period.

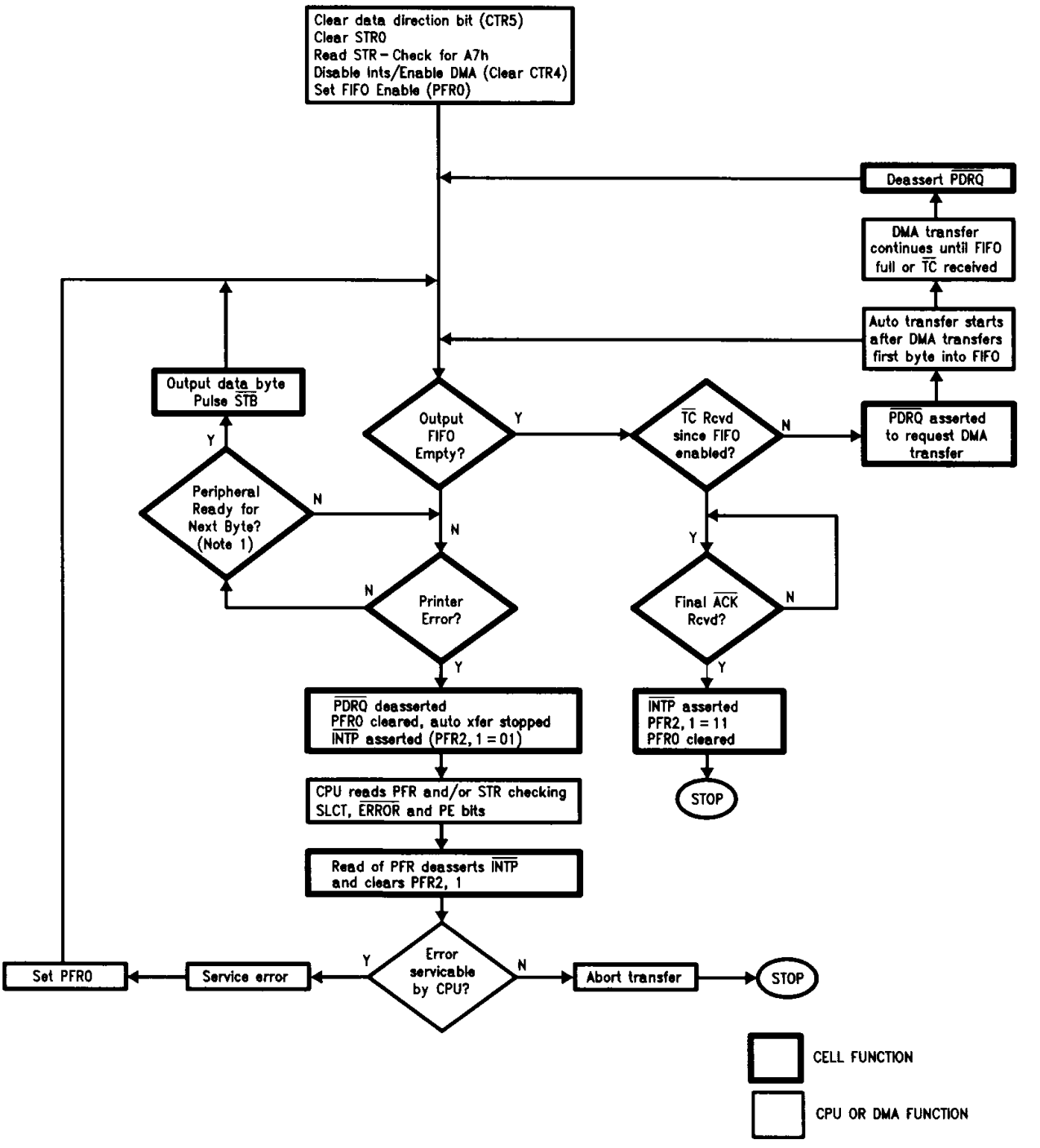
TABLE X. Data Port Direction in High Performance Mode

Perf. En. Bit (PFR0)	Direction Bit (CTR5)	$\overline{\text{RD}}$	$\overline{\text{WR}}$	Direction
1	0	1	0	Data is written to output FIFO and automatically transferred via PD0–7
1	0	0	1	Reserved Operation
1	1	1	0	Reserved Operation
1	1	0	1	Data automatically received from PD0–7 is read from the input FIFO

10.0 Bidirectional Parallel Port Interface (Continued)

10.5 OPERATION FLOWCHARTS

High Performance Parallel Port
(DMA Output Transfers)



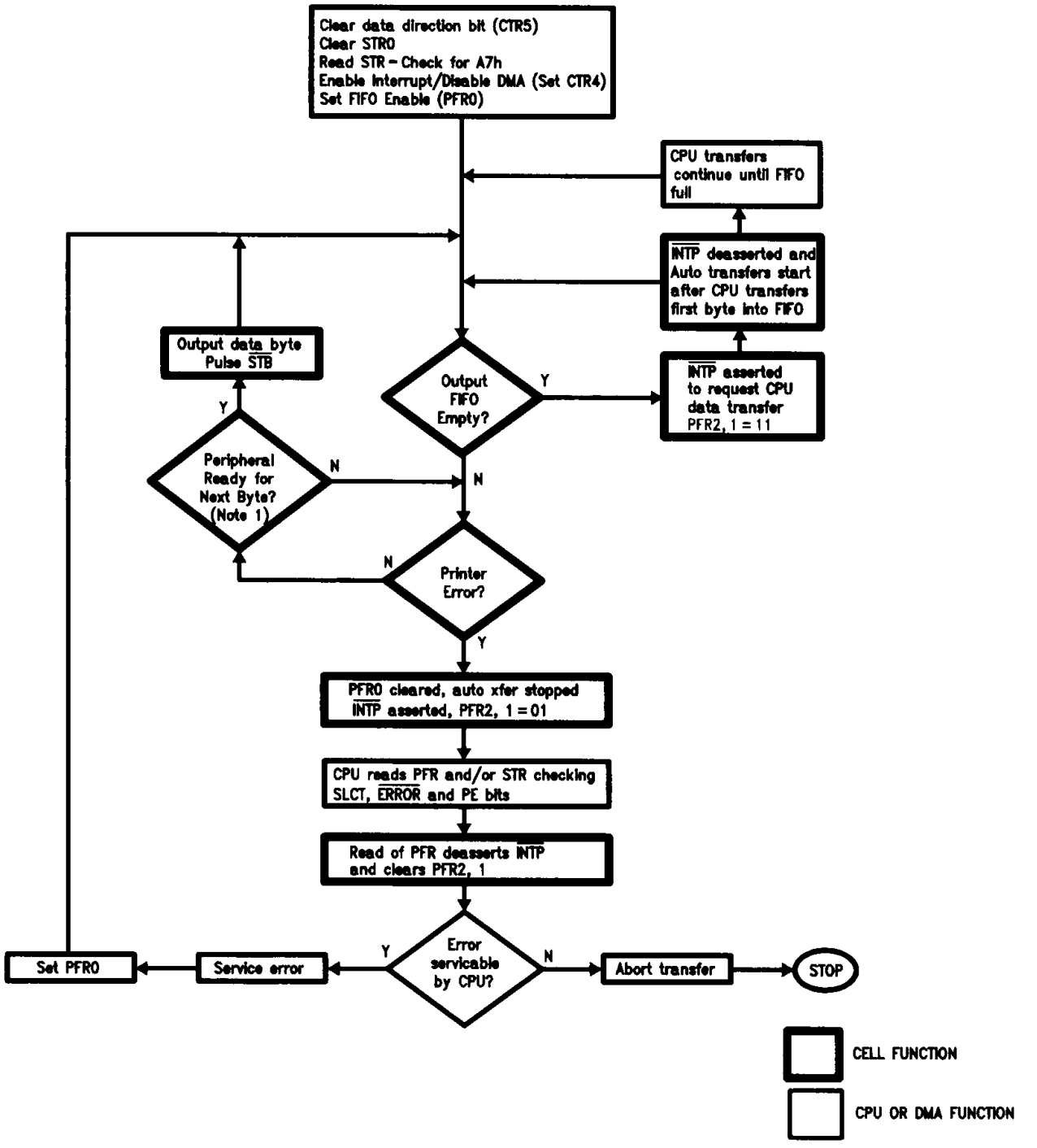
TL/C/10463–44

Note 1: Peripheral is ready when BUSY = 0, PE = 0, $\overline{ERR}$ = 1 and SLCT = 1.

10.0 Bidirectional Parallel Port Interface (Continued)

10.5 OPERATION FLOWCHARTS (Continued)

High Performance Parallel Port
(CPU Output Transfers)



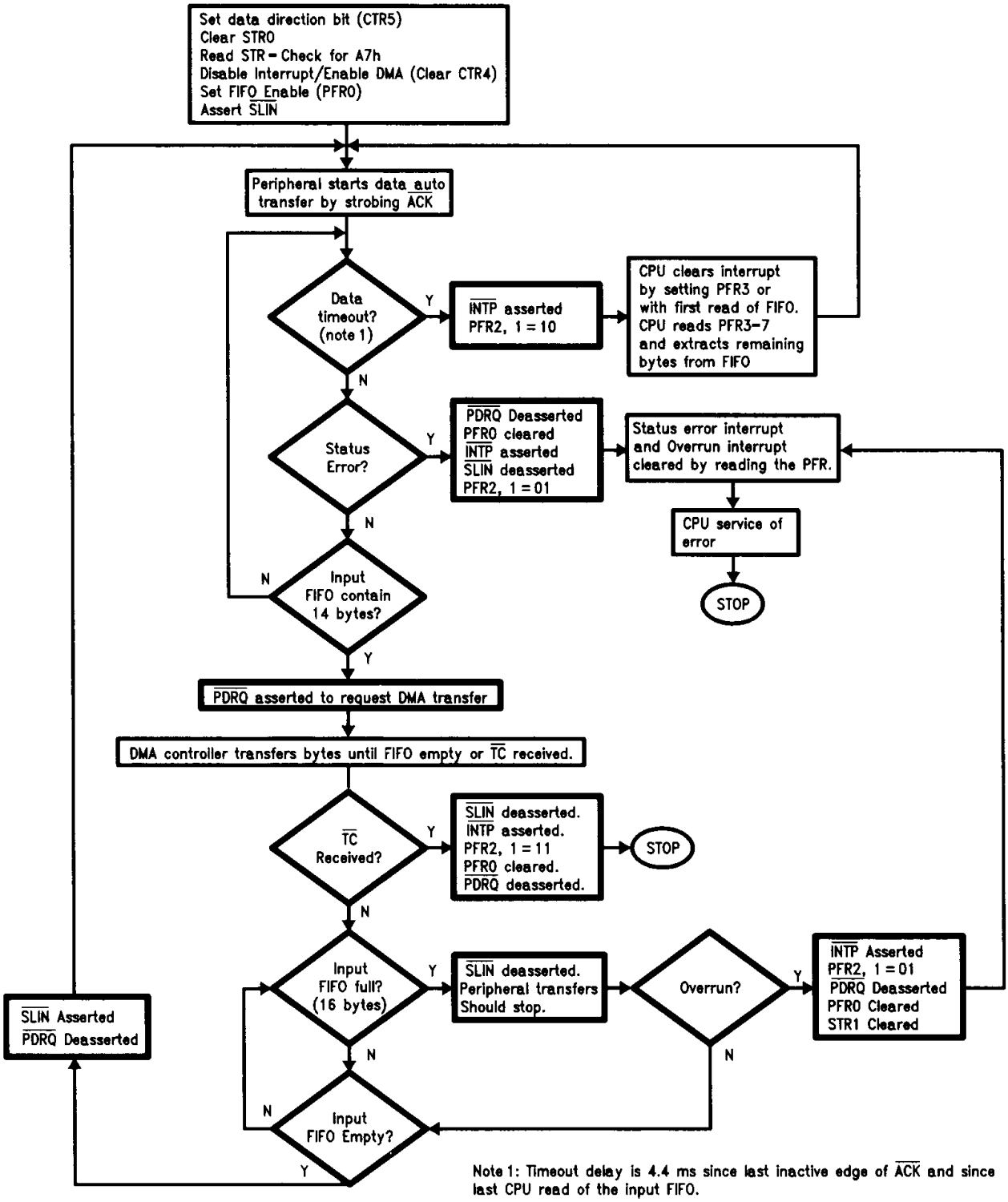
TL/C/10463–45

Note 1: Peripheral is ready when BUSY = 0, PE = 0, $\overline{ERR}$ = 1 and SLCT = 1.

10.0 Bidirectional Parallel Port Interface (Continued)

10.5 OPERATION FLOWCHARTS (Continued)

High Performance Parallel Port
(DMA Input Transfers)



Note 1: Timeout delay is 4.4 ms since last inactive edge of ACK and since last CPU read of the input FIFO.

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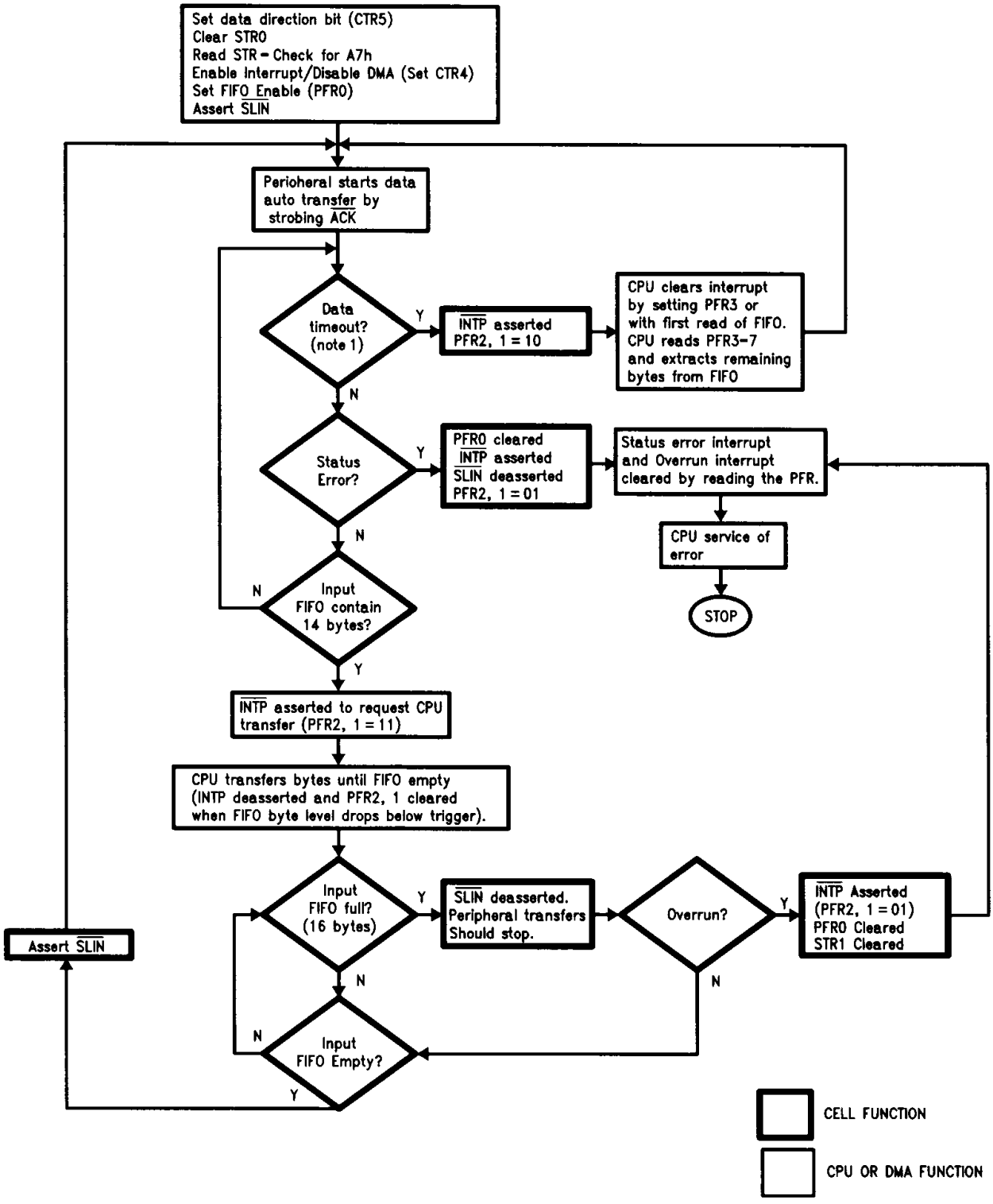
10.0 Bidirectional Parallel Port Interface (Continued)

10.5 OPERATION FLOWCHARTS (Continued)

High Performance Parallel Port
CPU Input Transfers



TL/C/10463–47

Note 1: Timeout delay is 4.4 ms since last inactive edge of $\overline{ACK}$ and since last CPU read of the input FIFO.

11.0 Ordering Information

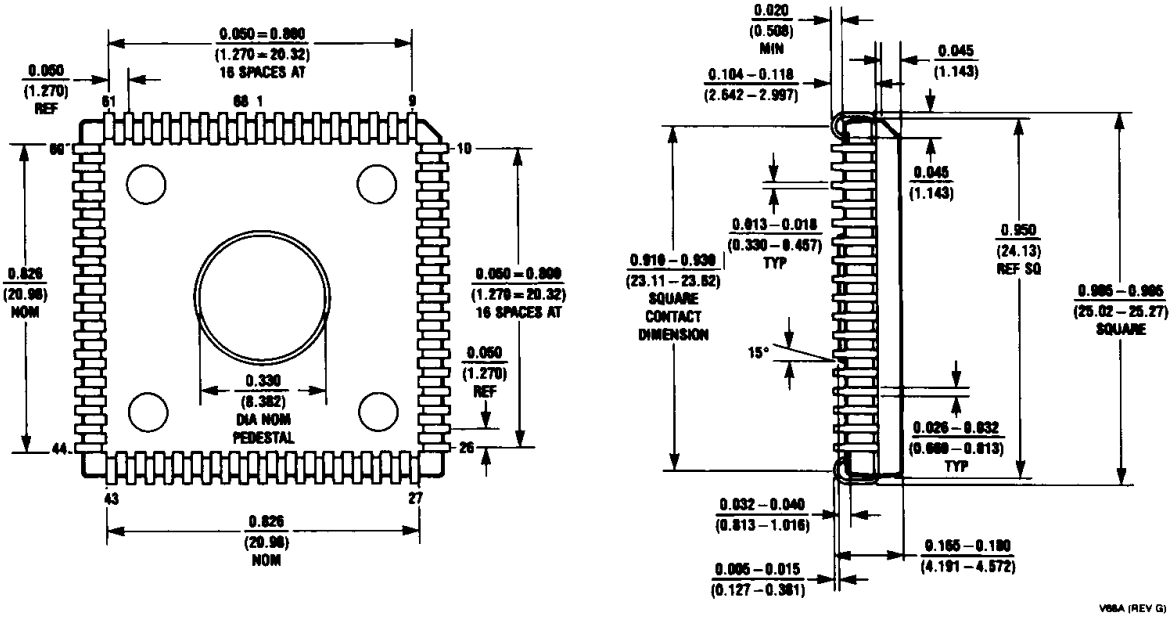
NS16C553XX

- /A* = A* RELIABILITY SCREENING
- V = PLASTIC LEADED CHIP CARRIER (PLCC)

TL/C/10463-33

12.0 Physical Dimensions inches (millimeters)

Lit. # 112908



68-Lead Plastic Chip Carrier (V)
Order Number PC16553V
NS Package Number V68A

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