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*Advance Information*

# Ignition Control

# MC33094

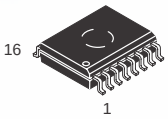
## IGNITION CONTROL

**SEMICONDUCTOR TECHNICAL DATA**

Designed for automotive ignition applications in 12 V systems, the MC33094DW provides outstanding control of the ignition coil when used with an appropriate Motorola Power Darlington Transistor. Engine control systems utilizing these devices for ignition coil control exhibit exceptional fuel efficiency and low exhaust emissions. The device is designed to be controlled from a single–ended Hall Sensor input. The circuit is built using high–density Integrated–Injection Logic (IIL) processing incorporating high current–gain PNP and NPN transistors.

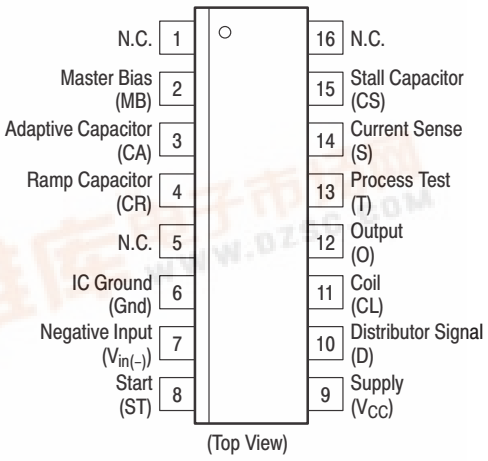
The MC33094DW is packaged in an economical surface mount package and specified over an ambient temperature of –40°C to 125°C with a maximum junction temperature of 150°C.

- External Capacitors Program the Devices Timing Characteristics
- Overvoltage Shutdown Protection
- Auto Start–Up Capability After Overvoltage Condition Ceases
- Allows for Push Start–Up in Automotive Applications
- Ignition Coil Current Limiting
- Ignition Coil Voltage Limiting
- Band Gap Reference for Enhanced Stability Over Temperature
- Negative Edge Filter for Hall Sensor Input Transient Protection
- Hall Sensor Inputs for RPM and Position Sensing
- –40°C ≤ $T_A$ ≤ 125°C Ambient Operating Temperature




**DW SUFFIX**
PLASTIC PACKAGE
CASE 751G
(SO–16L)

**PIN CONNECTIONS**




(Top View)

**MAXIMUM RATINGS** (All voltages are with respect to ground, unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 28.6 | V |
| Junction Temperature | $T_J$ | 150 | °C |
| Operating Ambient Temperature<br>Continuous<br>Limited | $T_A$ | <br>–30 to 105<br>–40 to 125 | °C |
| Storage Temperature | $T_{stg}$ | –55 to 150 | °C |
| Operating Frequency Range | $f_{op}$ | 1.0 to 400 | Hz |
| Soldering Temperature<br>SO–16L (for 10 seconds) | $T_{solder}$ | 270 | °C |
| Thermal Resistance<br>Junction–to–Ambient (SO–16L) | $R_{\theta JA}$ | 97 | °C/W |

**NOTE:** ESD data available upon request.

**ORDERING INFORMATION**

| Device | Operating Temperature Range | Package |
|---|---|---|
| PC33094DW | $T_A$ = –40° to +125°C | SO–16L |

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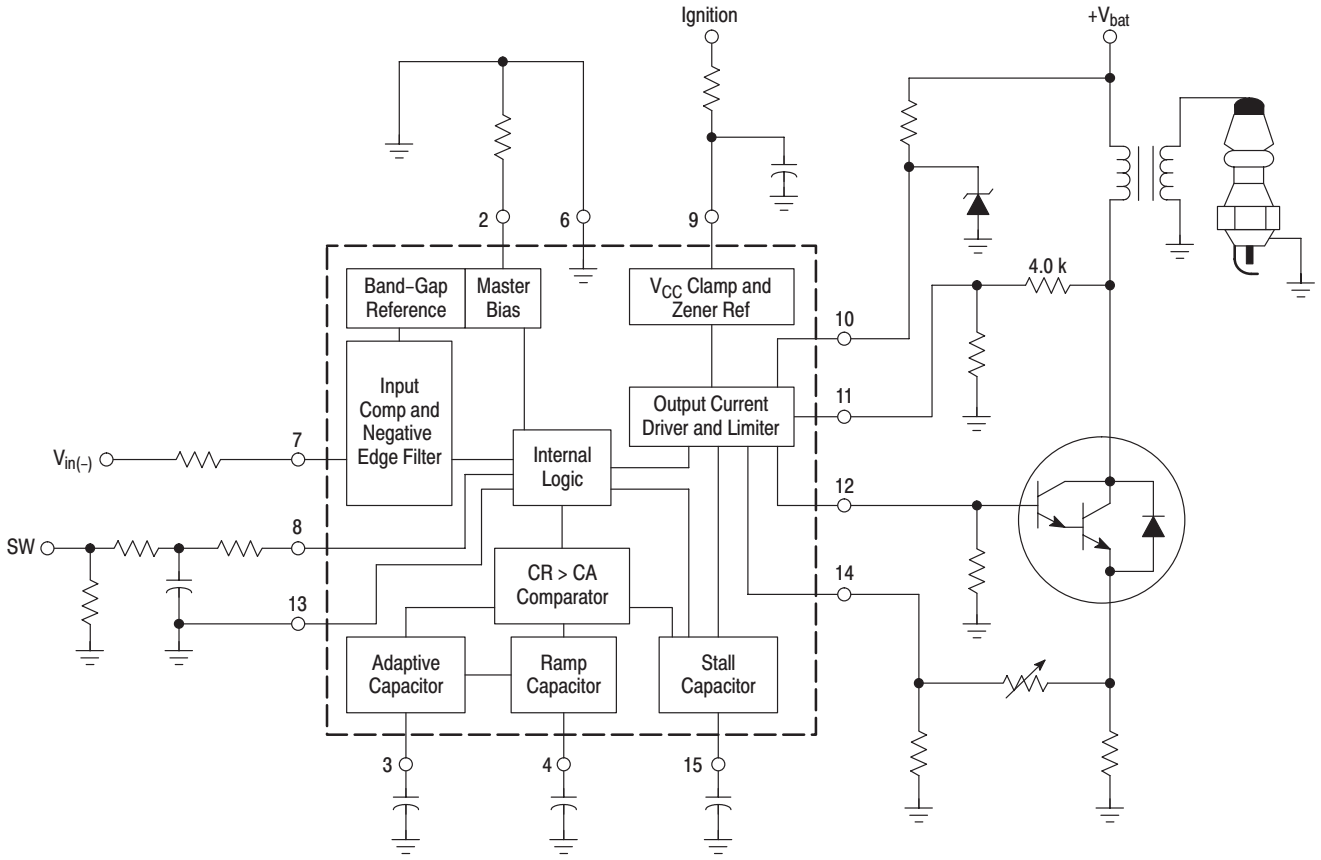
This document contains information on a new product. Specifications and information herein are subject to change without notice.

**Simplified Ignition Circuit**




This device contains ??? active transistors.

**ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions 6.0 V ≤ $V_D$ = $V_{CC}$ ≤ 16 V, –40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values are specified for $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **SUPPLY AND MASTER BIAS** | | | | | |
| Supply Current ($V_{CC}$ = 16 V, $V_{in(–)}$ = 0 V, $V_D$ = 3.0 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = $V_{ST}$ = Open) (Note 1) | $I_{CC}$ | 5.0 | 8.4 | 18 | mA |
| Overvoltage Shutdown ($V_{in(–)}$ = 0 V, $V_{CA}$ = $V_{CR}$ = Open, $V_{CS}$ = 3.0 V, $V_{ST}$ = 28 V) (Note 2) | $V_{CC3}$ | 23.7 | 27.5 | 31 | V |
| Start–$V_{CC}$ Latch ($V_{in(–)}$ = 0 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = Open, $V_{ST}$ = 25 V, $V_D$ = 14 V, $I_{ST}$ = 40 mA) | $V_{CC5}$ | 8.0 | 16.1 | – | V |
| Adaptive Dwell High Supply Voltage ($V_{in(–)}$ = 11 V, $V_{CA}$ = Open, $V_{CR}$ = 3.0 V, $V_{CS}$ = 3.0 V, $V_{ST}$ = 6.0 V, $V_D$ = 13 V)<br>Threshold (Note 3)<br>Hysteresis (Note 4) | <br><br>$V_{CC1}$<br>$V_{CC2(hys)}$ | <br><br>16.5<br>0.2 | <br><br>18.9<br>0.5 | <br><br>19.5<br>0.8 | V |
| Master Bias Voltage ($V_{CC}$ = 16 V, $V_{in(–)}$ = 0 V, $V_D$ = 3.0 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = $V_{ST}$ = Open) (Note 5) | $V_{MB}$ | 1.12 | 1.2 | 1.32 | V |

**NOTES:** 1. Current sourced into Supply pin.
2. Ramp up $V_{CC}$ from 24 to 31 V in 0.1 V increments and note the supply voltage, $V_{CC}$, which causes $V_O$ to fall below 1.0 V.
3. Ramp up $V_{CC}$ from 14 to 20 V in 0.1 V increments and measure $V_{CC}$ when $I_{CA}$ ≤ 2.0 μA.
4. Ramp up $V_{CC}$ from 20 to 14 V and measure $V_{CC}$ when $I_{CA}$ ≥ 2.0 μA and compute hysteresis difference from $V_{CC1}$.
5. Voltage measured at Master Bias pin.

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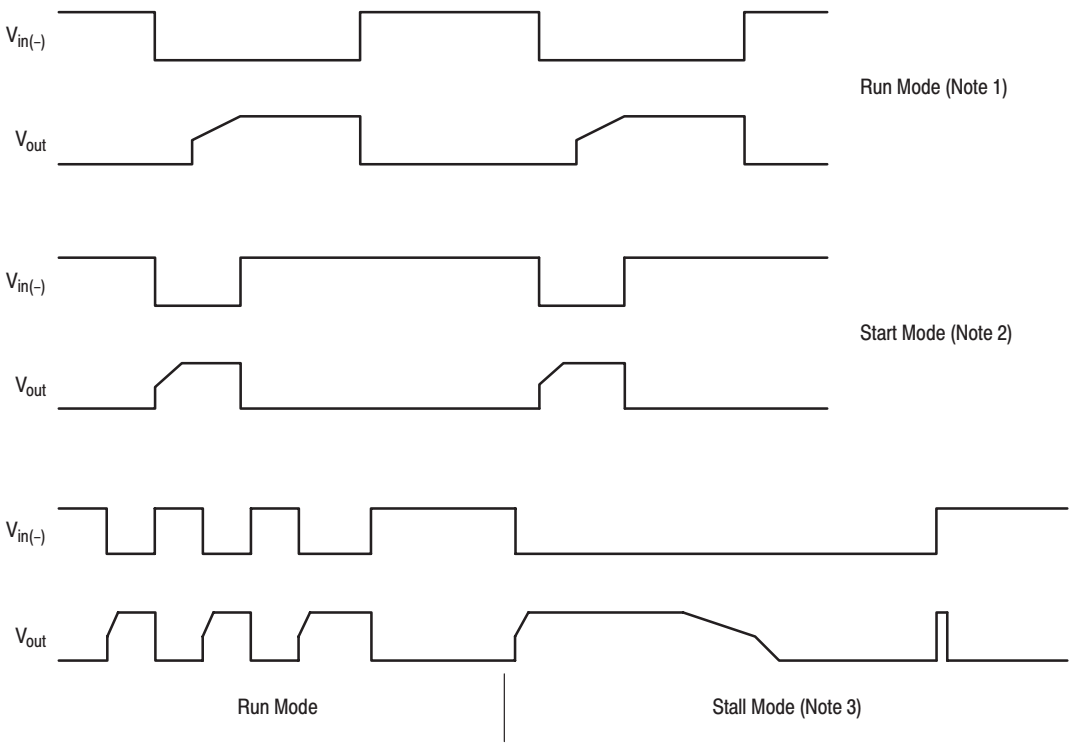
**ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions 6.0 V ≤ $V_D = V_{CC}$ ≤ 16 V, –40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values are specified for $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **INPUTS** | | | | | |
| Input Positive Threshold Voltage ($V_{CC}$ = 6.0 V, $V_{CA} = V_{CR}$ = Open, $V_{CS}$ = 1.0 V, $V_{ST}$ = 6.0 V) (Note 1) | $V_{in(–)(th)A}$ | 50 | 54 | 65 | $\%V_{CC}$ |
| Input Positive Threshold Voltage ($V_{CC}$ = 16 V, $V_{CA} = V_{CR}$ = Open, $V_{CS}$ = 1.0 V, $V_{ST}$ = 10 V) (Note 2) | $V_{in(–)(th)B}$ | 50 | 54 | 65 | $\%V_{CC}$ |
| Input Hysteresis ($V_{CC}$ = 6.0 V, $V_{CA} = V_{CR} = V_{CS}$ = Open, $V_{ST}$ = 6.0 V) (Note 3) | $V_{in(–)(hys)A}$ | 0.6 | 0.72 | 1.2 | V |
| Input Hysteresis ($V_{CC}$ = 16 V, $V_D$ = 3.0 V, $V_{CA} = V_{CR} = V_{CS}$ = Open, $V_{ST}$ = 10 V) (Note 4) | $V_{in(–)(hys)B}$ | 1.6 | 2.23 | 3.2 | V |
| Input Impedance ($V_{CC}$ = 14 V , $V_{in(–)}$ = 10 V , $V_D$ = 3.0 V, $V_{CA} = V_{CR} = V_{CS} = V_{ST}$ = Open) (Note 5) | $Z_I$ | 70 | 94 | 250 | kΩ |

**NOTES:** 1. Ramp up $V_{in(–)}$ from 1.0 to 5.0 V in 0.1 V increments. Record $V_{in(–)}$ when $I_{CR}$ goes positive and convert to % of $V_{CC}$ by dividing by $V_{CC}$.
2. Ramp up $V_{in(–)}$ from 3.0 to 10 V in 0.1 V increments. Record $V_{in(–)}$ when $I_{CR}$ goes positive and convert to % of $V_{CC}$ by dividing by $V_{CC}$.
3. Ramp up $V_{in(–)}$ from $V_{in(–)(th)A}$ in 0.01 V increments. Record $V_{in(–)}$ when $I_{CA}$ goes positive. $V_{in(–)(hys)A} = V_{in(–)(th)A} – (V_{in(–)})$.
4. Ramp up $V_{in(–)}$ from $V_{in(–)(th)B}$ in 0.01 V increments. Record $V_{in(–)}$ when $I_{CA}$ goes positive. $V_{in(–)(hys)B} = V_{in(–)(th)B} – (V_{in(–)})$.
5. Measure $I_{in(–)}$ into Pin 7; $Z_I = 10\ V/I_{in(–)}$.

**Figure 1. Basic Timing Diagrams**




**NOTES:** 1. The falling edge of the $V_{in(–)}$ signals a charge command, while the rising edge signals a spark command.
2. During start mode, stall conditions are prevented.
3. During a stall, the coil is discharged slowly and a quick charge and spark occur on the next spark command.

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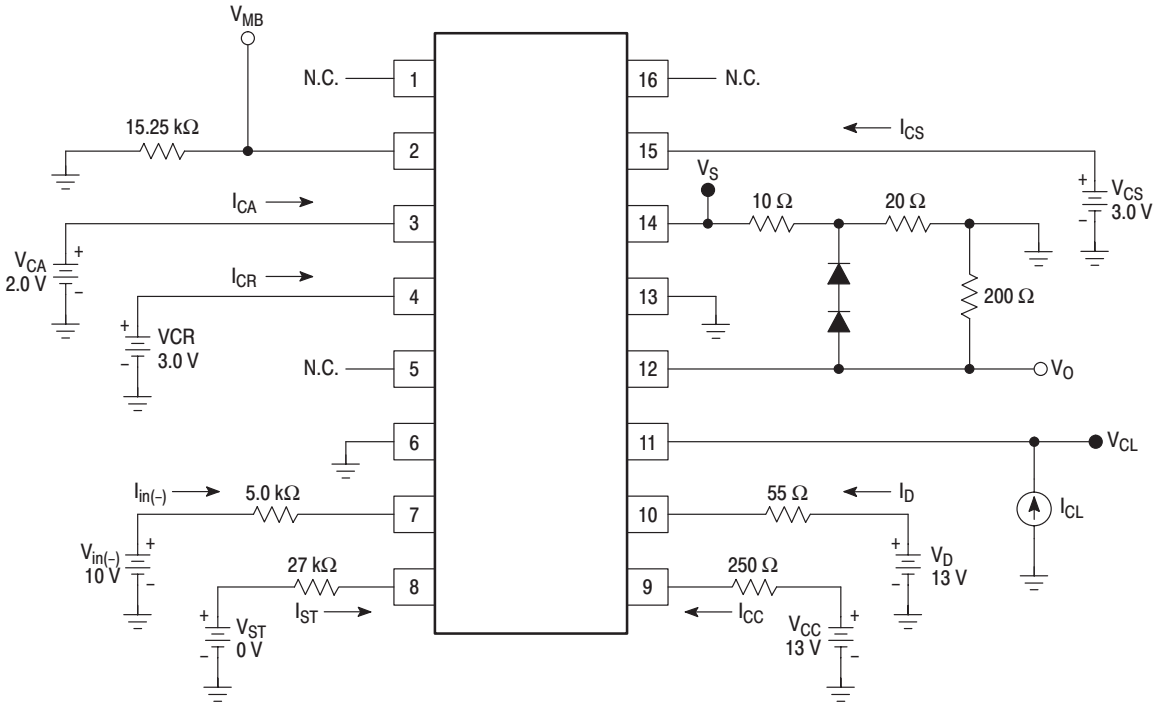
**Figure 2. Test Circuit**




**ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions 6.0 V ≤ $V_D$ = $V_{CC}$ ≤ 16 V, –40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values are specified for $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OUTPUT AND DWELL** | | | | | |
| Output Current ($V_{in(–)}$ = 0 V, $V_{CA}$ = $V_{CR}$ = Open, $V_{CS}$ = 3.0 V, $V_{ST}$ = 10 V, $V_O$ = 2.1 V) (Note 1) | | | | | mA |
| Normal Condition ($V_{CC}$ = 14 V, $V_D$ = 6.0 V) | $I_{O1}$ | 40 | 52 | 65 | |
| High Voltage Condition ($V_{CC}$ = 14 V, $V_D$ = 22 V ) | $I_{O2}$ | 40 | 55 | 65 | |
| Output Leakage Current ($V_{CC}$ = 14 V, $V_{in(–)}$ = 10 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = Open, $V_{ST}$ = 10 V, $V_S$ = 0 V, $V_D$ = 18, $V_O$ = 0 V) (Note 2) | $I_{O3}$ | 1.0 | –1.33 | 100 | µA |
| Output Clamp Voltage ($V_{CC}$ = 14 V, $V_{in(–)}$ = 10 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = Open, $V_{ST}$ = 10 V, $V_D$ = 14 V, $V_O$ = 0 V, $V_{CL}$ = 20 V, $I_{CL}$ = 10 mA) (Note 3) | $V_{CL}$ | 13.7 | 14.52 | 15.58 | V |
| Output Clamp Dynamic Impedance ($V_{CC}$ = 14 V, $V_{in(–)}$ = 10 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = Open, $V_{ST}$ = 10 V, $V_D$ = 14 V, $V_O$ = 0 V, $I_{CL}$ = 12 mA, $\Delta I_{CL}$ = 2.0 mA) (Note 4) | $Z_{CL}$ | 10 | 37 | 75 | Ω |
| Dwell (Note 5) | | | | | % |
| Normal Condition: D1 = ($I_{CA2}$/$I_{CA1}$) x CR Data from $I_{CA2}$, $I_{CA1}$, and CR characteristics | D1 | 14.5 | 17.6 | 20.5 | |
| High Voltage Condition: D2 = ($I_{CA3}$/$I_{CA1}$) x CR Data from $I_{CA3}$, $I_{CA1}$, and CR characteristics | D2 | 4.1 | 5.3 | 5.9 | |

**NOTES:** 1. Capability measured by forcing the Output to 2.0 V with Current Sense pin (IS) open while measuring the Output current to ground.
2. Measured by clamping the output to that output voltage with IS pin to ground; then increasing $V_D$ from 6.0 to 18 V and measuring output leakage current to ground.
3. Output Clamp voltage with reference to ground while forcing 10 mA into the Dynamic Clamp pin (CL).
4. Output Clamp impedance measured with $I_{CL}$ = 11 ± 1.0 mA into the Dynamic Clamp pin (CL) and noting the corresponding Output Clamp Voltage change ($Z_{CL}$ = $\Delta V_{CL}/\Delta I_{CL}$).
5. Dwell is defined as Run Mode Down Current divided by the Run Mode Up Current times the Ramp Control Current Ratio and is calculated from other measured characteristics as defined above.
6. Set the $V_{CR}$ voltage to 1.5 V; Ramp $V_{CR}$ voltage from 1.8 to 2.2 V in 0.02 V increments and note the Ramp voltage ($V_{CR}$) which causes the Output voltage to go > 1.0 V; $V_{CRO}$ = 2.0 V – $V_{CR}$.

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**ELECTRICAL CHARACTERISTICS (continued)** (Characteristics noted under conditions 6.0 V ≤ $V_D$ = $V_{CC}$ ≤ 16 V, –40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values are specified for $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OUTPUT AND DWELL** | | | | | |
| Adaptive Dwell Logic, Ramp Threshold ($V_{CC}$= 14 V, $V_{in(–)}$ = 10 V, $V_{CA}$ = $V_{CS}$ = Open, $V_{ST}$ = 0 V, $V_D$ = 10 V, $V_S$ = 0 V) (Note 6) | $V_{CRO}$ | –60 | 0 | 60 | mV |
| Soft Shutdown Voltage ($V_{CC}$ = 6.0 V, $V_{in(–)}$ = 10 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = Open, $V_{ST}$ = 0 V) Measure $V_S$ | $V_{SS}$ | 0 | 1.48 | 16.7 | mV |

**NOTES:** 1. Capability measured by forcing the Output to 2.0 V with Current Sense pin (IS) open while measuring the Output current to ground.
2. Measured by clamping the output to that output voltage with IS pin to ground; then increasing $V_D$ from 6.0 to 18 V and measuring output leakage current to ground.
3. Output Clamp voltage with reference to ground while forcing 10 mA into the Dynamic Clamp pin (CL).
4. Output Clamp impedance measured with $I_{CL}$ = 11 ± 1.0 mA into the Dynamic Clamp pin (CL) and noting the corresponding Output Clamp Voltage change ($Z_{CL} = \Delta V_{CL}/\Delta I_{CL}$).
5. Dwell is defined as Run Mode Down Current divided by the Run Mode Up Current times the Ramp Control Current Ratio and is calculated from other measured characteristics as defined above.
6. Set the $V_{CR}$ voltage to 1.5 V; Ramp $V_{CR}$ voltage from 1.8 to 2.2 V in 0.02 V increments and note the Ramp voltage ($V_{CR}$) which causes the Output voltage to go > 1.0 V; $V_{CRO}$ = 2.0 V – $V_{CR}$.

**ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions 6.0 V ≤ $V_D$ = $V_{CC}$ ≤ 16 V, –40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values are specified for $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **ADAPTIVE CAPACITOR** | | | | | |
| Run Mode, Adaptive Capacitor, Charge Current ($V_{CC}$ = 6.0 V, $V_{in(–)}$ = 5.0 V, $V_{CA}$ = Open, $V_{CR}$ = 3.0 V, $V_{CS}$ = 3.0 V, $V_{ST}$ = 6.0 V) (Note 1) | $I_{CA1}$ | –7.91 | –6.53 | –5.62 | µA |
| Run Mode, Adaptive Capacitor, Discharge Current ($V_{CA}$ = Open, $V_{CS}$ = 3.0 V, $V_{CR}$ = 3.0 V, $V_{ST}$ = 6.0 V) | | | | | µA |
| Normal Condition ($V_{CC}$ = 6.0 V, $V_{in(–)}$ = 10 V) | $I_{CA2}$ | 3.7 | 4.77 | 5.63 | |
| High Voltage Condition ($V_{CC}$ = 22 V, $V_{in(–)}$ = 17 V, $V_D$ = 13 V) | $I_{CA3}$ | 1.05 | 1.43 | 1.82 | |
| Start Mode, Adaptive Capacitor Currents ($V_{CA}$ = $V_{CR}$ = $V_{CS}$ = Open, $V_{ST}$ = 10 V) | | | | | µA |
| Charge Current ($V_{CC}$ = 5.0 V, $V_{in(–)}$ = 10 V) (Note 2) | $I_{CA4}$ | –112 | –87 | –80 | |
| Discharge Current ($V_{CC}$ = 6.0 V, $V_{in(–)}$ = 0 V) (Note 3) | $I_{CA5}$ | 67.6 | 89.4 | 109 | |
| Start Mode, Adaptive Capacitor, Clamp Voltage ($V_{CC}$ = 6.0 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = Open, $V_{ST}$ = 10 V) | | | | | V |
| High Clamp Voltage ($V_{in(–)}$ =10 V) | $V_{CA1}$ | 2.23 | 2.39 | 2.65 | |
| Low Clamp Voltage ($V_{in(–)}$ = 0 V) | $V_{CA2}$ | 0.95 | 1.1 | 1.26 | |
| Adaptive Gain ($V_{CC}$ = 14 V, $V_{in(–)}$ = 11 V, $V_{ST}$ = 6.0 V, $V_{CA}$ = Open, $V_{CR}$ = 3.0 V, $V_{CS}$ = 3.0 V , $V_D$ = 13 V) (Note 4) | AG | 0.85 | 0.99 | 1.15 | Times |

**NOTES:** 1. Open $V_{CR}$ initially then force $V_{CR}$ = 3.0 V and measure $I_{CA1}$.
2. Start Mode Adaptive Control sourcing current.
3. Start Mode Adaptive Control sink current.
4. Measure $I_{CA}$. Calculate: AG = $I_{CR1}/I_{CA}$.

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**ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions 6.0 V ≤ $V_D$ = $V_{CC}$ ≤ 16 V, –40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values are specified for $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **STALL CAPACITOR** | | | | | |
| Start Mode, Stall Control, Charge Current ($V_{CC}$ = 5.0 V, $V_{in(–)}$ = 0 V, $V_{CA}$ = $V_{CR}$ = Open, $V_{CS}$ = 1.0 V, $V_{ST}$ = 10 V) | $I_{CS1}$ | –2.7 | –2.33 | –2.13 | µA |
| Run Mode, Stalled, Stall Control, Discharge Current ($V_{CC}$ = 14 V, $V_{in(–)}$ = 0 V, $V_{CA}$ = $V_{CR}$ = Open, $V_{CS}$ = 1.0 V, $V_{ST}$ = 0 V) | $I_{CS2}$ | 7.5 | 9.69 | 13.2 | µA |
| Run Mode, Stall Control, Charge Current ($V_{CC}$ = 14 V, $V_{in(–)}$ = 10 V, $V_{CA}$ = 2.0 V, $V_{CR}$ = 3.0 V, $V_{CS}$ = 1.0 V, $V_{ST}$ = 0 V) | $I_{CS3}$ | –33.1 | –27 | –23.5 | µA |
| Run Mode, Stall Control, Discharge Current ($V_{CC}$ = 14 V, $V_{in(–)}$ = 10 V, $V_{CA}$ = 2.0 V, $V_{CR}$ = Open, $V_{CS}$ = 1.0 V, $V_{ST}$ = 0 V, $V_{MB}$ = 0 V) | $I_{CS4}$ | 0.76 | 1.02 | 1.26 | µA |
| Stall Control Threshold Voltage ($V_{CC}$ = 14 V, $V_{in(–)}$ = 0 V, $V_{CA}$= $V_{CR}$ = Open, $V_{ST}$ = 0 V) (Note 1) | $V_{CS1}$ | 1.95 | 2.06 | 2.45 | V |
| Stall Control Saturation Voltage ($V_{CC}$ = 14 V, $V_{in(–)}$ = 0 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = Open, $V_{ST}$ = 0 V) (Note 2) | $V_{CS2}$ | 20 | 35.3 | 165 | mV |

**NOTES:** 1. Ramp $V_{CS}$ from 1.5 to 2.5 V in 20 mV steps. Record $V_{CS}$ when $I_{CS}$ goes negative.
2. Set $V_{ST}$ = 10 V, $V_{CS}$ = 1.0 V, Fail if output is on.
Set $V_{CS}$ = 3.0 V, Fail if output is off.

**ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions 6.0 V ≤ $V_D$ = $V_{CC}$ ≤ 16 V, –40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values are specified for $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **RAMP CAPACITOR** | | | | | |
| Ramp Control Current Ratio ($V_{CC}$ = 14 V, $V_{in(–)}$ = 0 V, $V_{CR}$ = 3.0 V, $V_{ST}$ = 0 V, $V_{CA}$ = $V_{CS}$ = Open) (Note 1) | CR | 22 | 24.3 | 28 | % |
| Ramp Capacitor Reset Hysteresis ($V_{CC}$ = 14 V, $V_{in(–)}$ = 10 V, $V_{CA}$ = 2.0 V, $V_{CS}$ = 3.0 V, $V_{ST}$ = 6.0 V) (Note 2) | $V_{CR(hys)}$ | 6.0 | 19.19 | 180 | mV |

**NOTES:** 1. Set $V_{CA}$ to 0.5 V, then open $V_{CA}$. Set $V_{CR}$ to 0.9 V. Percent ratio of CR Up Current as compared to the CR Down Current; ($I_{CR1}$/($I_{CR1}$ – $I_{CR2}$) x 100).
2. Open $V_{CR}$, Force $V_{CR}$ = 1.3 V. Ramp $V_{CR}$ down in 3.0 mV steps until $I_{CR}$ goes negative, $V_{CR1}$. Ramp $V_{CR}$ up in 3.0 mV steps, toggle input between steps, until $I_{CR}$ goes positive, $V_{CR2}$. $V_{CR(hys)}$ = $V_{CR2}$ – $V_{CR1}$.

**ELECTRICAL CHARACTERISTICS** (Characteristics noted under conditions 6.0 V ≤ $V_D$ = $V_{CC}$ ≤ 16 V, –40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values are specified for $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **TIMING** | | | | | |
| Negative Edge Filter, Falling Edge Time Constant ($V_{CC}$ = 16 V, $V_{in(–)}$ = 0 V, $V_{CA}$ = $V_{CR}$ = $V_{CS}$ = Open, $V_{ST}$ = 10 V) (Note 1) | $t_1$ | 400 | 613.65 | 1000 | µs |
| Propagation Delay Time ($V_{CC}$ = 14 V, $V_{in(–)}$ = 10 V, $V_{CA}$ = $V_{CS}$ = Open, $V_{CR}$ = 3.0 V, $V_{ST}$ = 0 V) (Note 2) | $t_2$ | 0 | 3.45 | 15 | µs |
| Start Delay, Positive Edge (Data from $I_{CA4}$, $V_{CA1}$, $V_{CA2}$) (Note 3) | $t_{sdp}$ | 1.15 | 1.46 | 1.71 | ms |
| Start Delay, Negative Edge (Data from tests $V_{CA1}$, $I_{CA5}$, $V_{CA2}$, $t_1$) (Note 4) | $t_{sdn}$ | 1.19 | 2.06 | 2.8 | ms |
| Start to Output Disable Time (Note 5) | $t_{sod}$ | 71 | 87 | 107 | ms |
| Stall to Spark Output Propagation Delay (Data from tests $I_{CS3}$, $V_{CS1}$, $V_{CS2}$) (Note 6) | $t_{ssd}$ | 4.6 | 7.48 | 8.8 | ms |

**NOTES:** 1. Measure time until $V_O$ > 0.2 V. The Negative Edge Filter prevents multiple output sparks caused by switching transients present at the input by disabling the once used input for the filter time t.
2. Propagation delay time measurement of input to output response; Step change $V_{in(–)}$ from 0 to 10 V. Measure the time required for $V_O$ < 1.5 V.
3. $t_{sdp}$ = ($V_{CA1}$ – $V_{CA2}$) x CA/$I_{CA4}$; CA = 0.1 µF.
4. $t_{sdn}$ = [($V_{CA1}$ – $V_{CA2}$) x CA/$I_{CA5}$] + $t_1$; CA = 0.1 µF.
5. $t_{sod}$ = ($V_{CS1}$ – $V_{CS2}$) x CS/$I_{CS1}$; CS = 0.1 µF.
6. $t_{ssd}$ = ($V_{CS1}$ – $V_{CS2}$) x CS/$I_{CS3}$; CS = 0.1 µF.
7. $t_{sst}$ = ($V_{CS1}$ – $V_{CS2}$) x CS/$I_{CS2}$; CS = 0.1 µF.
8. $f_{ss}$ = 1/[(5.4/$V_{in(+)(th)}$) + (4.3/$I_{CS4}$) + (2/$I_{CS2}$)] x CS; CS = 0.1 µF.
9. $t_{bit}$ = [($V_{CS}$ – 0.7 V)/$I_{CS1}$] x CS; CS 0.1 µF.

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**ELECTRICAL CHARACTERISTICS (continued)** (Characteristics noted under conditions 6.0 V ≤ $V_D$ = $V_{CC}$ ≤ 16 V, –40°C ≤ $T_A$ ≤ 125°C, unless otherwise noted. Typical values are specified for $T_A$ = 25°C.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **TIMING** | | | | | |
| Stall Shutdown Time (Data from $I_{CS2}$, $V_{CS1}$, $V_{CS2}$) (Note 7) | $t_{sst}$ | 13.6 | 20.9 | 26.5 | ms |
| Stall Frequency (Note 8) | $f_s$ | 1.69 | 2.26 | 2.8 | Hz |
| Battery Interrupt Time ($V_{CC}$ = $V_{in(–)}$ = $V_{ST}$ = 0 V, $V_{CA}$ = $V_{CR}$ = Open, $V_{CS}$ = 6.0 V) (Note 9) | $t_{bit}$ | 25 | 66.65 | 200 | ms |

**NOTES:** 1. Measure time until $V_O$ > 0.2 V. The Negative Edge Filter prevents multiple output sparks caused by switching transients present at the input by disabling the once used input for the filter time t.
2. Propagation delay time measurement of input to output response; Step change $V_{in(–)}$ from 0 to 10 V. Measure the time required for $V_O$ < 1.5 V.
3. $t_{sdp}$ = ($V_{CA1}$ – $V_{CA2}$) x CA/$I_{CA4}$; CA = 0.1 µF.
4. $t_{sdn}$ = [($V_{CA1}$ – $V_{CA2}$) x CA/$I_{CA5}$] + $t_1$; CA = 0.1 µF.
5. $t_{sod}$ = ($V_{CS1}$ – $V_{CS2}$) x CS/$I_{CS1}$; CS = 0.1 µF.
6. $t_{ssd}$ = ($V_{CS1}$ – $V_{CS2}$) x CS/$I_{CS3}$; CS = 0.1 µF.
7. $t_{sst}$ = ($V_{CS1}$ – $V_{CS2}$) x CS/$I_{CS2}$; CS = 0.1 µF.
8. $f_{ss}$ = 1/[(5.4/$V_{in(+)(th)}$) + (4.3/$I_{CS4}$) + (2/$I_{CS2}$)] x CS; CS = 0.1 µF.
9. $t_{bit}$ = [($V_{CS}$ – 0.7 V)/$I_{CS1}$] x CS; CS 0.1 µF.

**Figure 3. Input Positive Threshold Voltage versus Temperature**

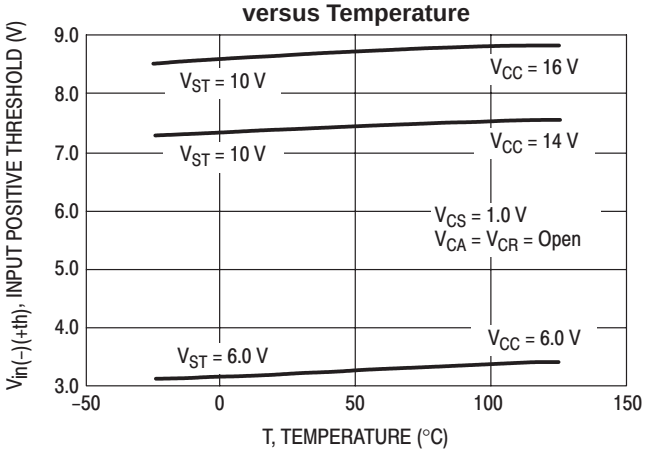


**Figure 4. Input Negative Threshold Voltage versus Temperature**

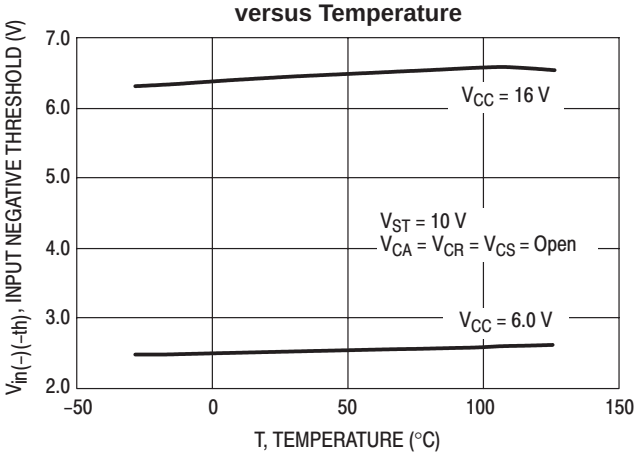


**Figure 5. Output Current Change versus Temperature**

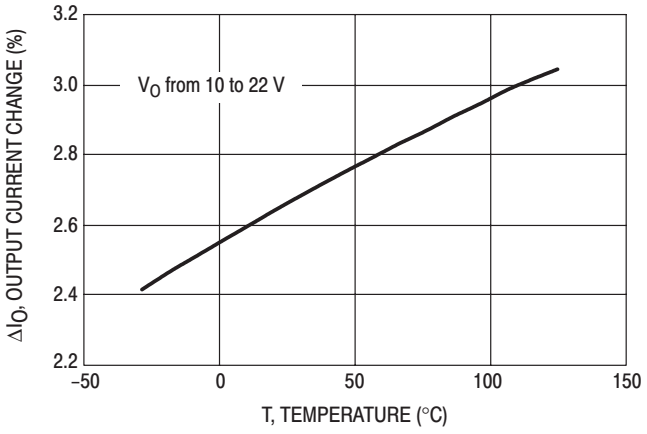


**Figure 6. Input Impedance versus Temperature**

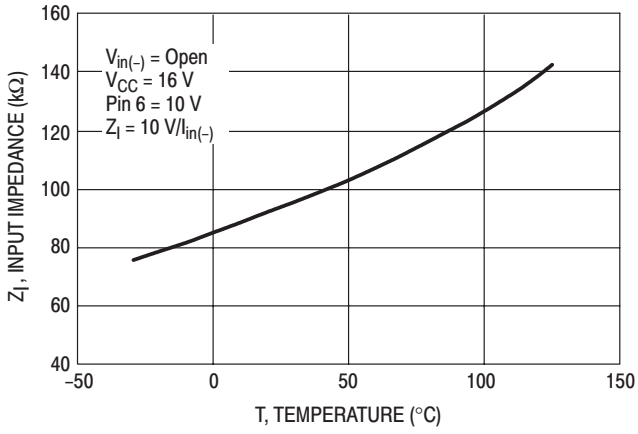


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**Figure 7. Output Clamp Voltage versus Temperature**

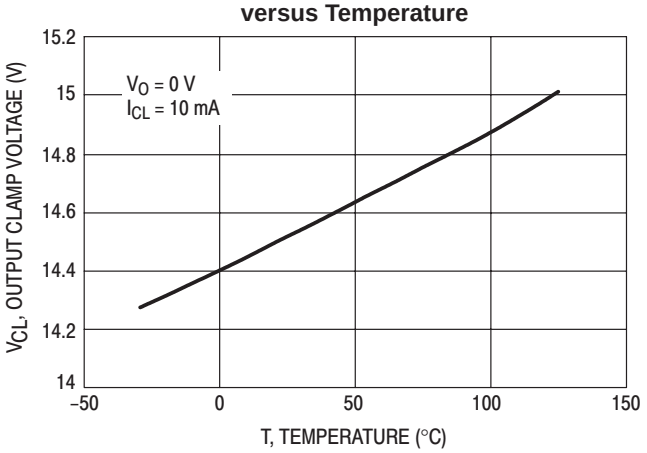



**Figure 8. Output Clamp Dynamic Impedance versus Temperature**

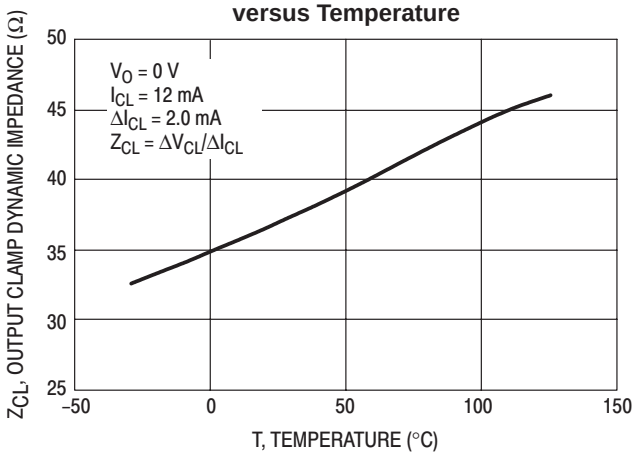
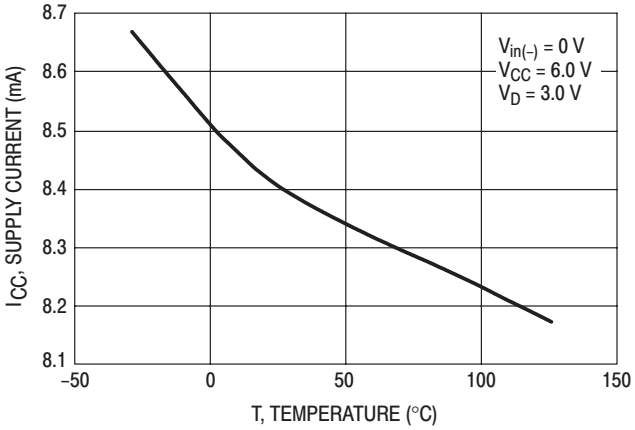



**Figure 9. Supply Drain Current versus Temperature**




**Block Diagram Description** (Figure 10)

The Band–Gap Reference generates a nominal 1.2 V having very good stability with temperature variations. The Band–Gap Reference conceptually provides a low temperature drift voltage by summing a strongly negative Temperature Coefficient (TC) voltage with an equally strong positive TC voltage. The negative TC voltage element is a result of a transistor emitter–to–base voltage while the positive TC voltage is developed as a result of a positive TC current imposed across a resistor. The positive TC current relies on the matching of currents in different sizes of transistors. The result is a very stable reference voltage independent of temperature variations. The Band–Gap Reference voltage provides a thermally stable voltage reference for critically sensitive circuits within the IC. It also sets the master bias current for all precision currents on the IC.

The $V_r$ Zener Reference block contains a 6.75 V zener regulator, which also exhibits a very low temperature coefficient.

The $V_{CC}$ Comparator and Clamp block limits the $V_{CC}$ voltage to one $V_{be}$ plus three zener drops in addition to comparing the $V_{CC}$ voltage to 15 and 22 V. When the $V_{CC}$ voltage is greater than either of these two values, the IC changes the adaptive capacitor discharge rate and when above 22 V the IC forces the coil current to shutdown. The minimum $V_{CC}$ value the IC will operate at is 4.0 V and $V_{bat}$ of 5.0 V. Below 7.5 V, the $V_r$ reference is no longer maintained, and the IC consumes excess power and excess voltage is dropped in the external $V_{CC}$ resistor.

The Master Bias Current Reference block generates precise currents used throughout the IC. The MB pin is held at 1.2 V by a differential amplifier with feedback. Capacitive loading on the MB pin reduces the effectiveness of the internal dominant pole, and loading as modest as 200 pF may cause the differential amplifier to oscillate.

The Input Voltage Comparator block requires an input signal between ground and $V_{bat}$ and detects the swing in the input signal. The thresholds for the input comparator are approximately 56.2% of $V_{bat}$ for rising signals and 36% of $V_{bat}$ for falling signals. The input signal may come from a Hall effect sensor or reluctor sensor on the distributor.

The Negative Edge Filter block is an inverting buffer for the signal from the Input Voltage Comparator and has a time constant of approximately 0.1 μs for rising edges and 500 μs for falling edges.

The Adaptive Capacitor Charging and Sensing block charges, discharges, and senses the adaptive capacitor voltage. The adaptive capacitor has a single charge rate of 8.4 μA and two discharge rates. The 1.688 μA slow discharge rate is used only during very high $V_{CC}$ operation and

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represents an effort to reduce excess dwell and therefore power dissipation during high voltage operation. The 5.88 μA discharge rate is used under normal $V_{CC}$ operating conditions. Under a start mode, this block will discharge the adaptive capacitor forcing an enhanced start mode dwell. The start/run modes are set internally by detecting the engine frequency, which corresponds to the ramp capacitor voltage.

The Stall Capacitor Charging and Sensing block controls the charging and discharging rates of the stall capacitor. The charging rate is 31.5 μA, and the two discharging rates are 1.0 μA and 7.0 μA. The stall capacitor potential commands the IC to maintain or reduce the coil current. When the engine is turning very slowly (or stalled), the stall capacitor will have enough time to discharge below threshold and thereby reduce coil current. The output current limiter (see Output Current Driver and Limiter block description below) forces the coil current to be proportional to the stall capacitor voltage when the stall capacitor voltage is less than 2.0 V.

The Ramp Capacitor Charging and Sensing block charges the ramp capacitor at approximately 8.4 μA and discharges it at about 33.6 μA. The charging circuit is always on and sources current during the “not 25%” part of the engine cycle. The discharging circuit is only on and sinking current during the “25%” part of the engine cycle. The positive edge of the distributor input signal sets the 25% mode, and the ramp comparator output clears this mode.

The CR > CA Adaptive Comparator block signals the point where the ramp capacitor voltage is greater than the adaptive capacitor voltage. The point at which the two capacitor voltages are equal is the point where charging of the coil is begun. The adaptive algorithm used in the IC maintains the required excess dwell throughout all reasonable accelerations and decelerations without causing excess coil power dissipation, in addition, it insures that more than adequate spark energy is available for very high engine speeds, when excess dwell is impossible.

The Output Current Driver and Limiter block sources a limited supply current of about 50 mA to the base of the Darlington power transistor. The Darlington will cause the coil to conduct to about 6.5 amps and the voltage drop on the IS pin of the IC will rise to the threshold of the current limiter. The current limiter will then hold the coil current at that level until either a spark is commanded by the logic block, or the engine begins to stall (causing the coil to slowly discharge).

The Internal Logic block performs the required memory and gating functions on the IC to implement the adaptive ignition control algorithm.

**Figure 10. Block Diagram**

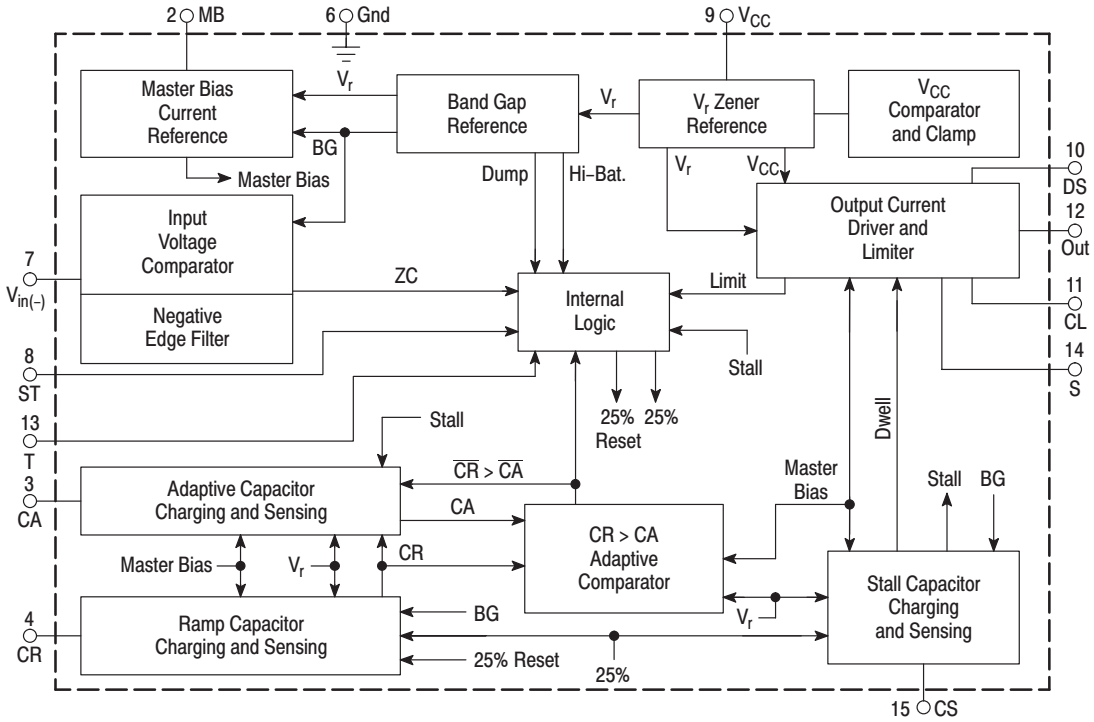


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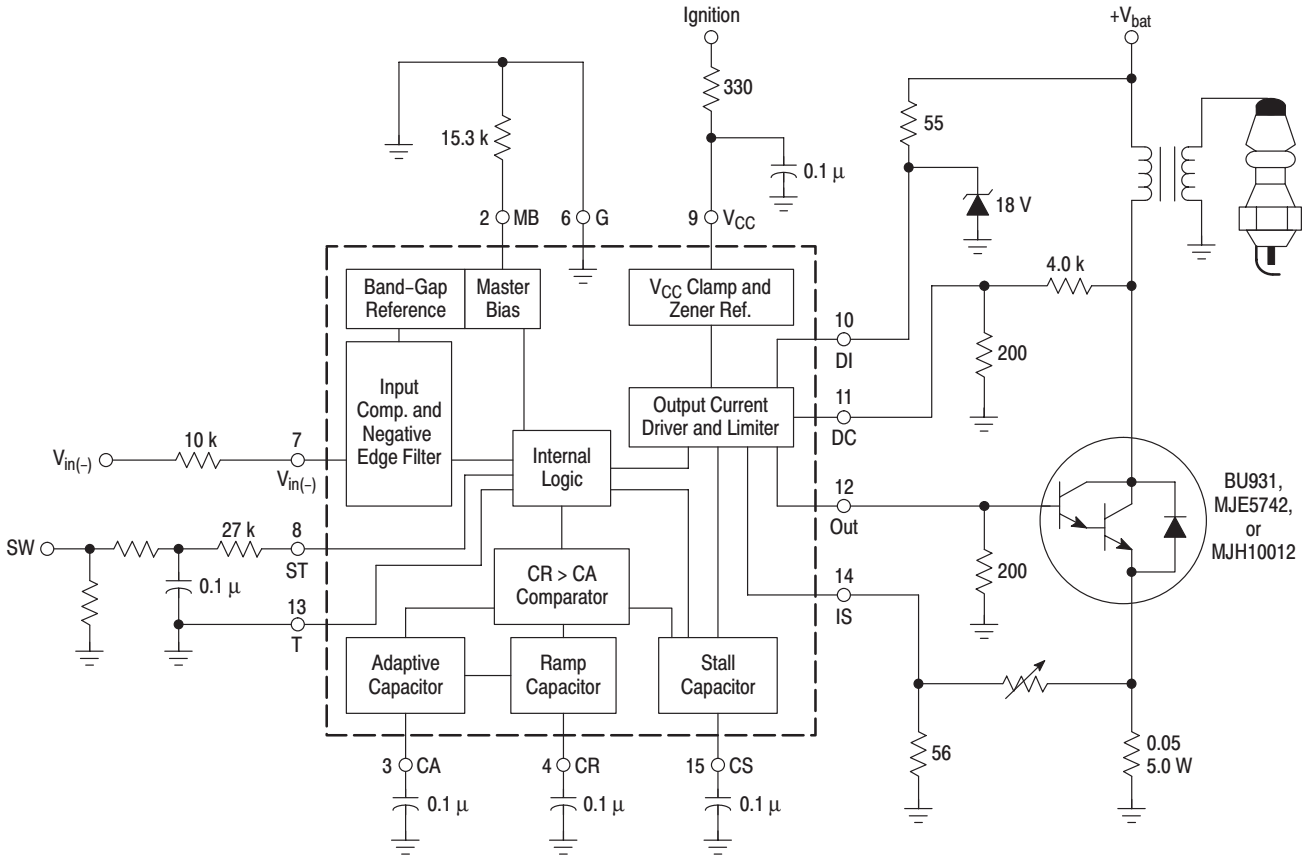
**Figure 11. Typical Ignition Circuit**




**Introduction**

The MC33094DW is designed for engine compartment use in 12 V automotive ignition applications to provide high performance control of the ignition coil when used with an appropriate Motorola Power Darlington Transistor. Engine control systems utilizing these devices for ignition coil control exhibit superior fuel efficiency and lower exhaust emissions over predecessor systems. The device is designed for single input control from a Hall sensor to determine crankshaft position.

The device, a bipolar linear integrated circuit, is built using high–density Integrated–Injection Logic (IIL) processing incorporating high current–gain PNP and NPN transistors. All module inputs are transient voltage protected through the use of resistors, capacitors, and/or zener diodes working in conjunction with internal protection elements. These elements provide protection of critical circuitry from externally induced high–voltage transients which may degrade the devices operational performance. At the module level, it is recommended the $V_{CC}$ pin of the device be transient decoupled using an external resistor and capacitor to work in conjunction with the on–chip internal zener string to provide robust module protection of the device power pin. The D input of module should be protected from transients through the use of an external resistor and zener diode. The Start Wire of the module should be decoupled through the use of two resistors and a capacitor to work in conjunction with the on–chip internal clamp (Figure 11).

The output of the device incorporates a high current–gain PNP designed to drive an external power Darlington transistor to provide control of the ignition coil. The output drive is carefully synchronized with the output from the distributor. The charging and discharging of three capacitors, external to the device, provide timing signals which program the dwell and charge time control of the ignition coil over a wide rpm range.

The timing and charge/discharge rates of the three external capacitors are accurately controlled by internal circuitry acted upon by sensor and distributor signal detection of the device.

A feedback path from the emitter of the external power Darlington transistor to the device provide monitoring of the ignition coil current. An internal comparitor of the device senses and limits the maximum ignition coil current to approximately 6.5 amps. Other circuitry within the device provides an interruption of the coil current so as to generate the spark, or slowly discharges the coil in a controlled manner so as to prevent a spark and limit the total module energy dissipation.

When the external Darlington is switched off, the Darlington collector will instantly experience a dramatic increase in voltage as a result of the collapsing field of the ignition coil (inductive kick). The external voltage divider working in conjunction with the internal device zener string and power PNP form a dynamic clamp which limits the inductive kick voltage to less than 350 V. This feature protects the Darlington transistor from damaging stress or breakdown.

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**Ignition Circuit Operation Description**

When initially powered up, all module capacitors start discharged (0 V). The $V_{CC}$ capacitor will power up first, and the IC's internal logic latches are indeterminate. The following conditions will hold: STALL = 1, because the stall capacitor voltage is less than 2.0 V; 25% = 0, because the ramp capacitor is less than the Band Gap Reference voltage ($V_{bg}$); and $I_{coil}$ = 0 amps, because the stall capacitor is at 0 V.

Because 25% = 0, the ramp capacitor charges towards $V_r$. At cranking frequencies, the ramp capacitor always exceeds the start mode threshold at the input (ZC), and therefore the stall signal resets the start mode latch upon the first ac signal (this causes the adaptive capacitor to be discharged). With the adaptive capacitor held low, very high rates of acceleration are possible. If the adaptive capacitor were allowed to adapt the dwell at low frequencies, severe limitations to engine acceleration would occur.

See Figure 13. At point A, a spark from the previous cycle occurs as the field around the coil collapses rapidly. At the same time ZC (ZC (input) = high(1)) will set the 25% clock signal which commands the adaptive and ramp capacitors to discharge and the stall capacitor to charge. At point B, as the ramp capacitor voltage crosses the 1.2 V ($V_{bg}$) level, the 25% clock is cleared and the polarities and amplitude of the ramp and stall capacitor currents change to their appropriate levels. At this point the adaptive capacitor is discharged and begins to float. At point C, the coil turns on and ramps until the coil current is limited to 6.5 amps. The adaptive capacitor, at point D, remains discharged and the dwell is maximized to 6.5 amps because the start/run latch has yet to be set. At point E, ZC (ZC = high) turns the coil off causing a spark to occur and at which point a new cycle begins. As the engine frequency increases, the peak voltage on the ramp capacitor at the ac signal will fall below the start mode enable threshold level. The start mode enable detector then sets the start/run latch to the run mode ($CA_{DUMP}$ = 0) by clocking a zero into the start/run latch at the zero cross. At this time the adaptive algorithm is evoked and the adaptive capacitor is allowed to charge and discharge according to it's other logical inputs. After normal run mode operation is entered, the start mode may not be reentered even though the ramp capacitor voltage again exceeds the start mode enable threshold. A start mode may only be evoked by a STALL signal transition from logic 1 to 0. The STALL signal transition occurs at a ZC frequency of approximately 2.0 Hz.

The IC and circuit provides for other than normal starting procedures such as push starting the engine. Since the stall capacitor will be discharged in this low frequency mode, the IC will provide a spark timing with a maximum retardation of about 6.5 ms.

After the start mode operation is exited, the normal operation algorithm is entered and a different sequence of events dominate the IC's performance. See Figures 14, 15, and 16. At point A, the spark from the previous cycle occurs and the 25% part of the cycle begins. During this part of the cycle, the stall capacitor will charge and the ramp and adaptive capacitors will discharge. At point B, the "not 25%" part of the cycle, also called the 75% part of the cycle, begins. The stall capacitor discharges, while the ramp capacitor charges. During this part of the cycle the adaptive capacitor floats. At point C, the ramp capacitor voltage equals the voltage on the adaptive capacitor. At this time, the coil turns on and the coil current ramps to the point where it is limited. When the coil current reaches the limit, point D, the adaptive capacitor begins to charge, until zero cross (ZC = 1logic(high)), point E. This turns the coil off and induces a spark. The 75% part of the cycle lasts until point E, at which time the cycle begins again.

The adaptive dwell algorithm causes the engine to maintain a fixed percent of excess dwell time (if possible). The mechanism that permits this involves the floating nature of the adaptive capacitor. During engine deceleration, the initial coil turn–on might occur early, but the next coil turn–on will be retarded to it's correct location due to the % adjusted adaptive capacitor charge time. During acceleration, the coil may not charge up as early as desired the first time, however, the spark will still be correctly slaved to the distributor. The side effect of this is that the adaptive capacitor will not receive as much charge time for that cycle and will have a lower average value the next cycle, thus starting the coil charging sooner, as can be seen in Figure 16. In this figure, the output voltage rises before the adaptive capacitor charge signal occurs.

See Figure 12. In the Stall mode the output is slaved by the stall capacitor. The stall capacitor can discharge completely, but starting at point X it charges during the 25% of the engine cycle (duration of when ZC is logic high = 1). At the same time a spark from the previous cycle occurs. The DWELL signal will be high as long as the engine is in stall, but falls gradually preventing a spark at point Y when the STALL goes low starting at 2.4 V. The coil will be slaved to the stall capacitor, and at point Z the coil will charge to 6.5 amps as the stall capacitor charges to 2.0 V. At that time the STALL comparator will trip (STALL = 0) and the DWELL signal will fall, triggering a reduced spark with some retardation (6.5 ms). At this point a new cycle begins.

Each of the three different modes (Stall, Start, and Run) have their own differences. The Stall capacitor controls the output in the stall mode, however is disabled in both the start and run modes. The output is clamped longer in the start mode as compared to the run mode due to the more energy/current in the coil causing a longer/bigger spark.

Other less likely operating sequences are possible. For example, there is a possibility of $V_{CC}$ exceeding 15 V during engine operation (High battery = logic 1). Above about 17 V on $V_{bat}$, the excess current limit percentage falls to 5% to conserve IC and circuit power dissipation. Above 25 V, current to the coil is disabled. Care was placed in this design to account for all possible operating modes.

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**Figure 12. Stall Mode 60 RPM (Frequency: 2.0 Hz @ 100 ms)**

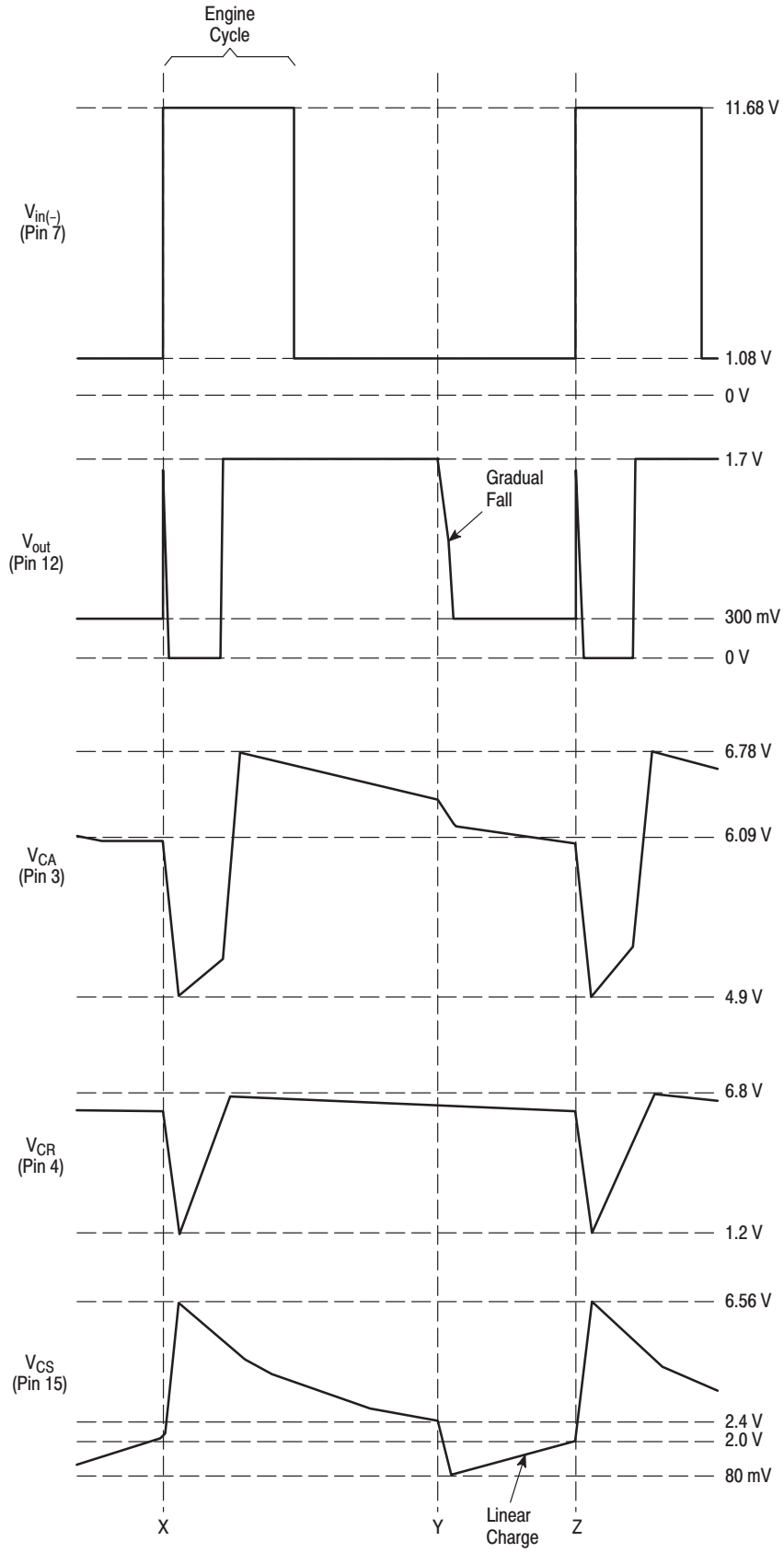


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Figure 13. Start Mode 300 RPM (Frequency: 10 Hz @ 20 ms)

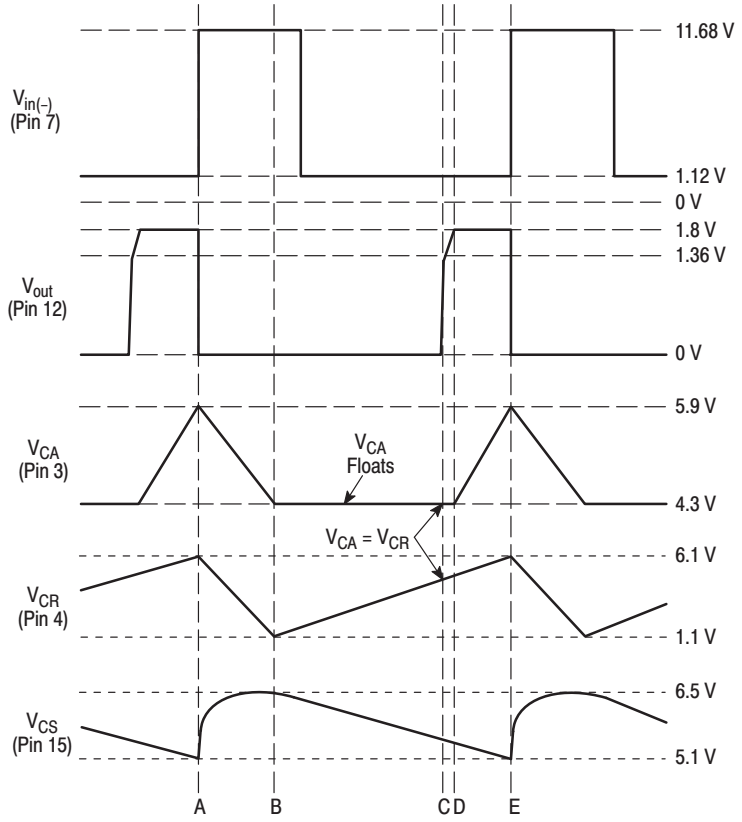


Figure 14. Run Mode 900 RPM (Frequency: 30 Hz @ 10 ms)

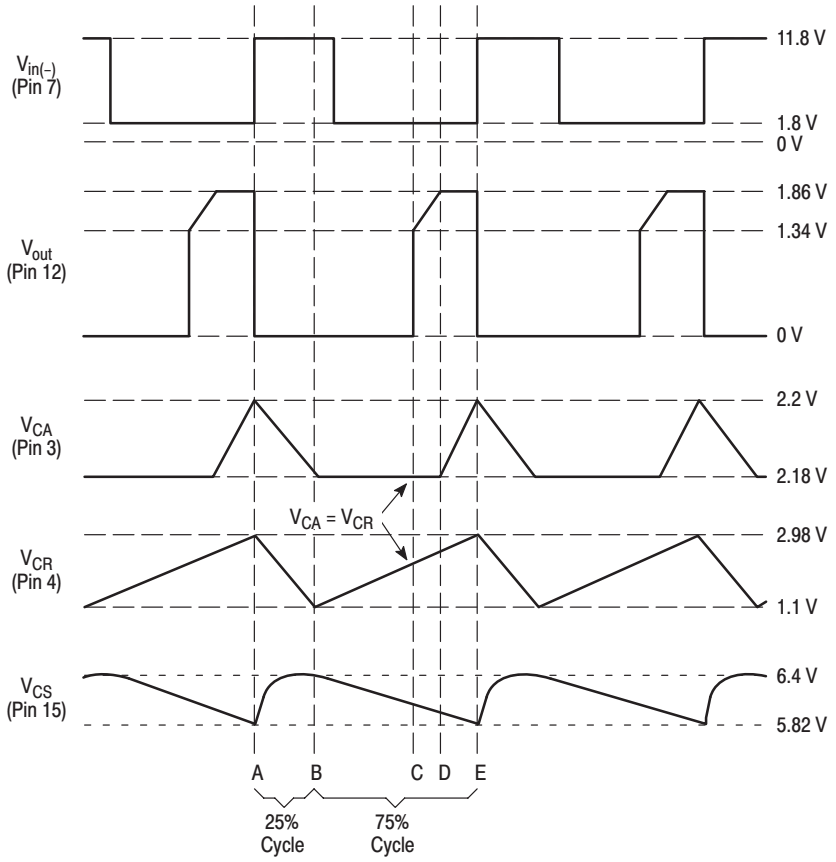


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**Figure 15. Run Mode 2000 RPM (Frequency: 66.67 Hz @ 5.0 ms)**

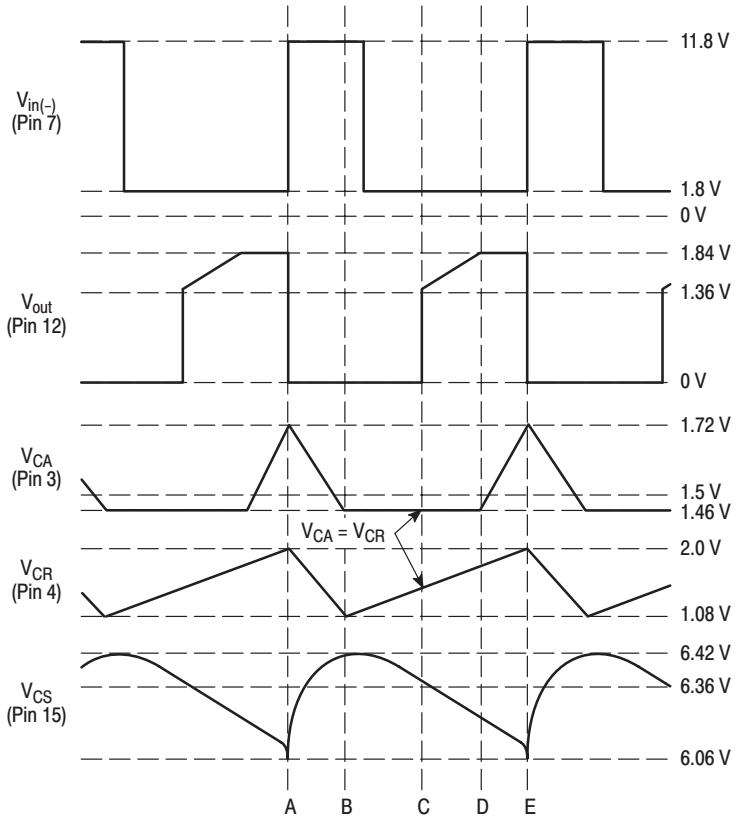
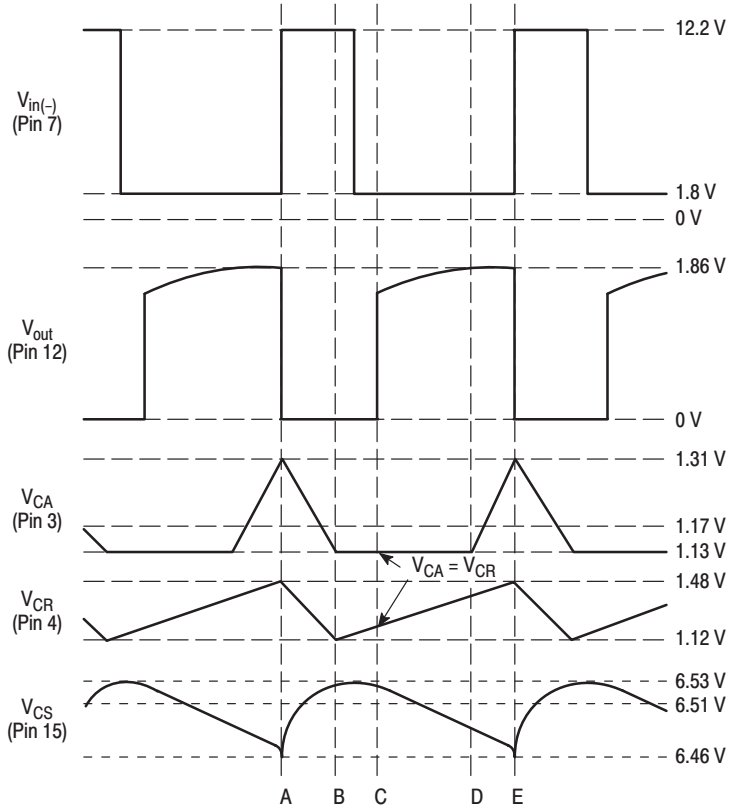



**Figure 16. Run Mode 5000 RPM (Frequency: 166.67 Hz @ 2.0 ms)**

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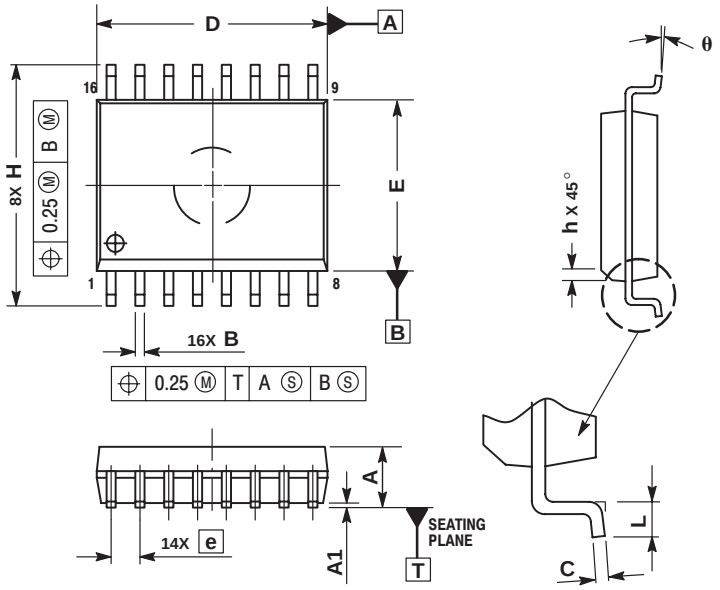
## OUTLINE DIMENSIONS

**DW SUFFIX**
PLASTIC PACKAGE
CASE 751G–03
ISSUE B




NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 10.15 | 10.45 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

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