National Semiconductor

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PC87310 (SuperI/O™) Dual UART with Floppy Disk Controller and Parallel Port†

General Description

The PC87310 incorporates two full function UARTs, a floppy disk controller (FDC) with analog data separator, one parallel port, game port decode, hard disk controller decode, standard XT/AT address decoding for on-chip functions, and a Configuration Register in one chip. Thus it offers a single chip solution to the most commonly used IBM®PC, XT, and AT peripherals. The floppy disk controller is fully compatible with the industry standard 765 architecture, but it includes many more advanced options such as a high performance data separator, extended track range to 4096, implied seek command, scan command, and both standard IBM formats as well as ISO 3.5″ formats. The UARTs are compatible with either the INS8250N-B or the NS16450. The parallel port, hard disk select, and game port select logic maintain complete compatibility with the IBM XT and AT. Hardware selects XT or AT compatibility.

The Configuration Register is one byte wide and can be programmed via hardware or software. Through its control, the user can assign standard AT addresses and disable any major on-chip function (e.g., the FDC, either UART, or the parallel port) independently of the others. This allows for flexibility in system configuration when adapter cards contain duplicate functions.

Features

- 100% compatible to the IBM PC, XT and AT architectures
- Software compatible to the INS8250N-B, INS8250A and NS16450 UARTs
- 100% compatible to the industry standard 765A architecture
- On-chip analog data separator operates up to 1 Mb/s
- Implements all DP8473 Floppy Disk Controller functions
- Bidirectional parallel port for printer or scanner operation. Provides all standard Centronics and IBM PC, XT, and AT interface signals.
- Decoding and chip selects for an IDE hard disk interface
- Address decoding and strobe generation for a game port
- Fabricated in NSC's 1.5 μ M2CMOS process
- Low power CMOS with a power down mode
- 100-pin EIAJ plastic flatpak package
- Integrates all PC-XT®, PC-AT® logic
  - — On chip 24 MHz crystal oscillator
  - — DMA enable logic
  - — IBM compatible address decode of A0–A9
  - — 24 mA μP bus interface buffers
  - — 40 mA floppy drive interface buffers
  - — Data rate and drive control registers
- Precision analog data separator
  - — Self-calibrating PLL and delay line
  - — Automatically chooses one of three filters
  - — Intelligent read algorithm
- Two pin programmable precompensation modes
- Other enhancements
  - — Implied seek up to 4000 tracks
  - — IBM or ISO formatting
- Separate interrupt request lines for the parallel and serial ports
- Adds or deletes standard asynchronous communication bits (start, parity, and stop) to or from the serial data
- Independently controlled transmit, receive, line status, and data set interrupts
- Programmable baud generators for each UART channel divide the input clock by 1 to ($2^{16} - 1$) and generate the internal 16 × sample clock
- MODEM control functions for each UART channel (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial-interface characteristics:
  - — 5, 6, 7, or 8 bit characters
  - — Even, odd, or no parity generation and detection
  - — 1, 1½, or 2 stop bit generation
- High current drive capability for the parallel port

†**Note:** This part is patented.

PC87310 (SuperI/O) Dual UART with Floppy Disk Controller and Parallel Port

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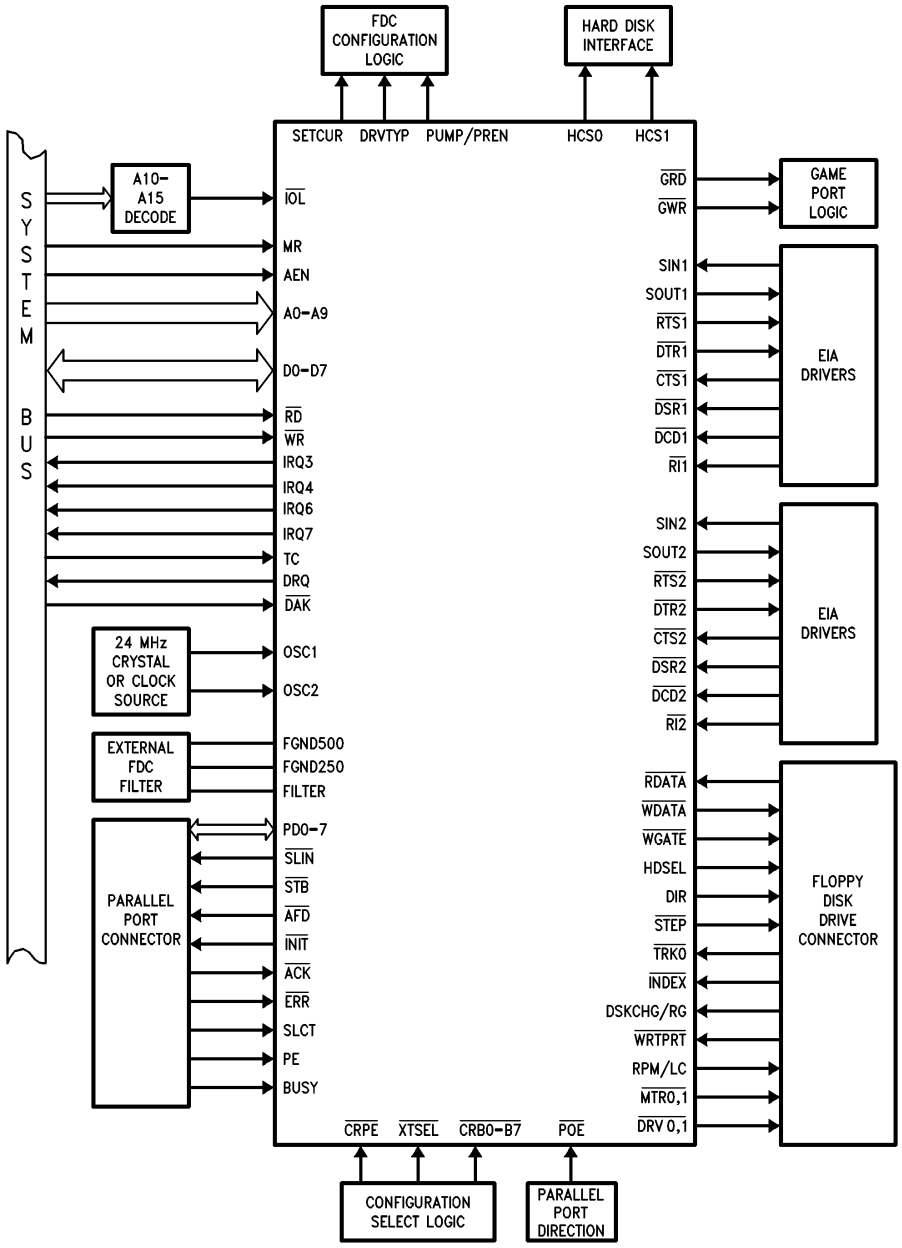
Basic Configuration



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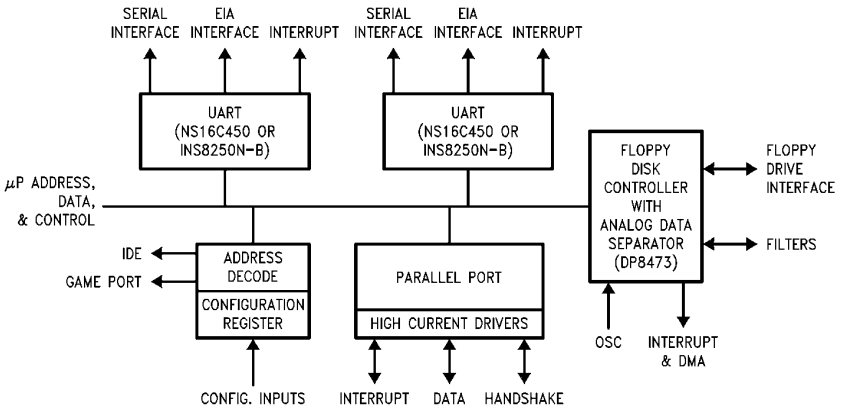
1.0 Block Diagram



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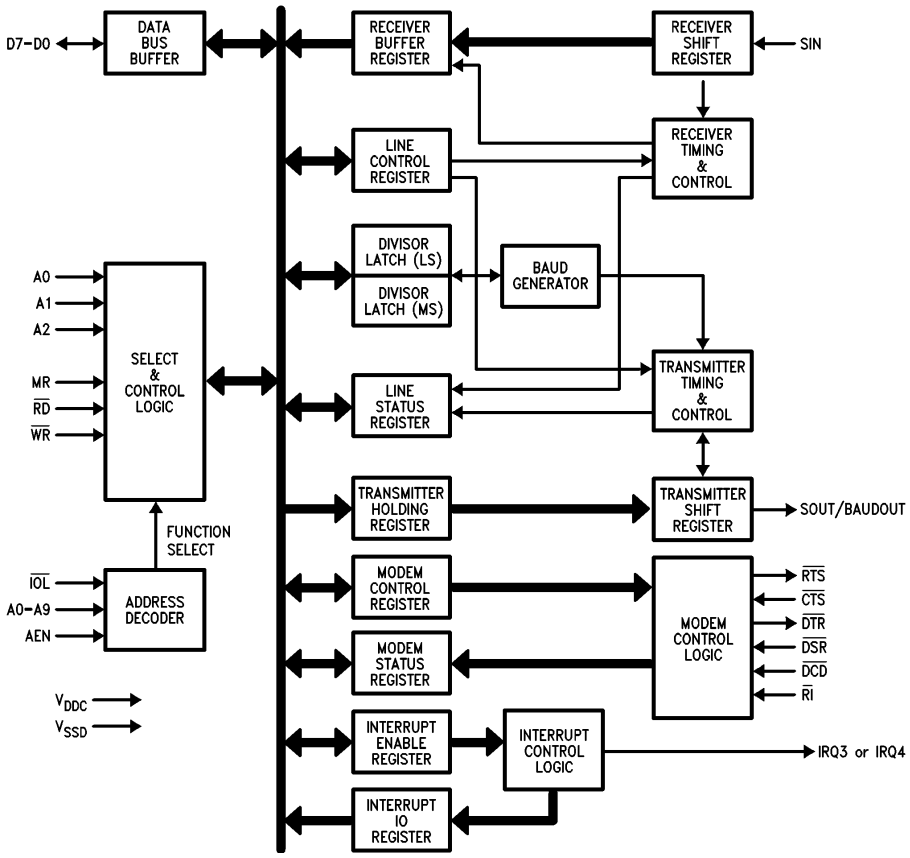
1.1 BLOCK DIAGRAM OF A SERIAL PORT



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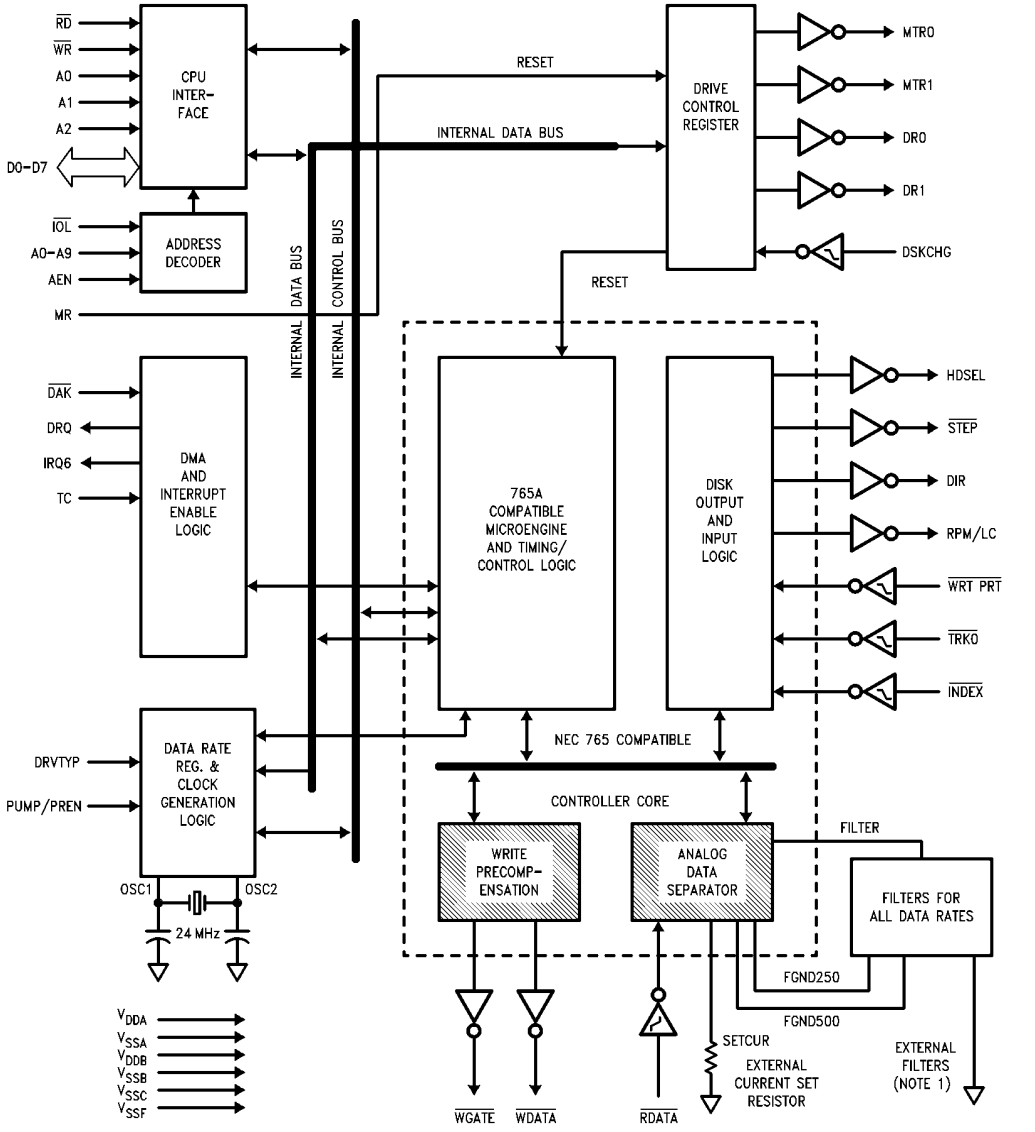
1.0 Block Diagram (Continued)

1.2 BLOCK DIAGRAM OF THE FLOPPY DISK CONTROLLER



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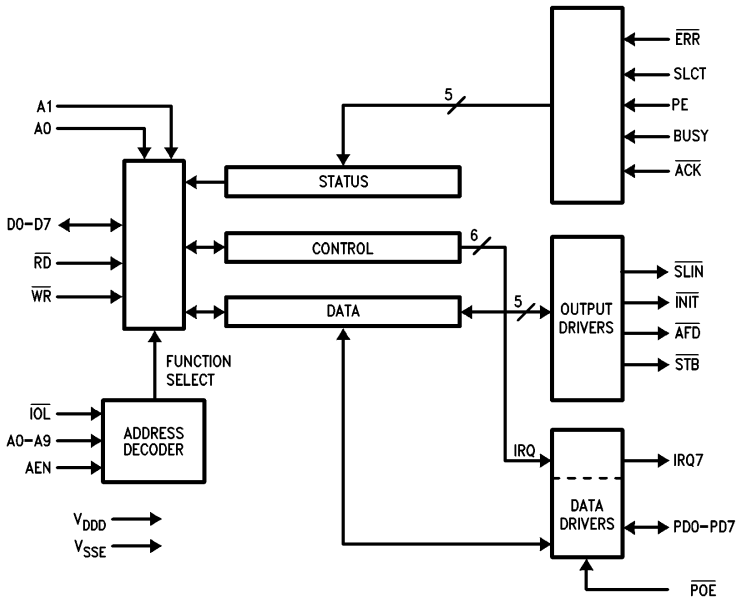
Note 1: See *Figure 3* for filter description.

1.0 Block Diagram (Continued)

1.3 BLOCK DIAGRAM OF THE PARALLEL PORT



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1.4 I/O ADDRESS DECODE

TABLE 1-1

Address Range	Function
278H–27FH	Parallel Port 3
378H–37FH	Parallel Port 2
3BCH–3BEH	Parallel Port 1
3F8H–3FFH	Serial Port 1
2F8H–2FFH	Serial Port 2
320H–324H (XT) HCS0 Active 1F0H–1F7H, 3F6H, 7* (AT) HCS0, HCS1 Active	Hard Disk Select
3F2H, 4, 5, 7*	Floppy Disk
201	Game Port Select
3F3H**	Configuration Port

*READ D7 from FDC, D0–D6 from HDD; WRITE D0–D7 to FDC

**Write only register that requires two consecutive writes to change the data

2.0 Pin Descriptions

The following describes the function of all pins. A low represents a logic 0 (0V nominal) and a high represents a logic 1 (+2.4V nominal).

Pin Symbol	Pin Number	Description
A0–A9 (I/O Address)	11–2	Address signals connected to these inputs select the active register during a CPU read or write. Details on each register are given in the device section associated with that register (e.g., UART, FDC, parallel port, etc.).
$\overline{\text{ACK}}$ (Acknowledge)	31	This input is set low by the printer to indicate that it has received data.
AEN (Address Enable)	12	This input disables function selection via A0–A9 when it is high.
$\overline{\text{AFD}}$ (Automatic Feed XT)	35	When this output is low the printer should automatically line feed after each line printed. This pin will be in a TRI-STATE® condition 10 ns after a zero is loaded into the corresponding Control Register bit position. The system should pull this pin high using a 4.7 kΩ resistor.
BOUT1, 2 (Baud Rate Output)	57, 41	This multi-function output pin provides the associated serial channel Baudout signal, after data of 10 hex has been written to the TCR. This pin provides the composite serial data output signal for the associated channel after a reset or after 00 is written to the TCR. (See SOUT1, 2 and CRB0, 7 for further information on these pins.)
BUSY (Printer Busy)	32	This input is set high by the printer when it can't accept another character.
$\overline{\text{CRPE}}$ (Configuration Register Program Enable)	17	This multi-function pin is used to select between internal or external default values for the Configuration Register and whether the Configuration Register can be initialized via hardware or software. The chip checks this pin during reset, at that time it acts as an input. If it is low during reset, the Configuration Register will default to the complement of the $\overline{\text{CPB}}$0–4, 6, 7 pin states. If it is high, the Configuration Register will default to 00. A 47 kΩ (Note 1) resistor can be used to pull this pin to the required signal level. This pin will be driven by the chip when not in reset. Regardless of the initial polarity of this pin the Configuration Register can be programmed whenever Master Reset is inactive. This pin must always have a pull up or pull down resistor attached to it. (See $\overline{\text{HCS}}$1 and $\overline{\text{GWR}}$ for further information on pin 17 when the chip is NOT being reset.) **Note 1:** If the minimum reset time of 100 ns is required these resistors will have to be reduced to <10 kΩ to stabilize the input signal during the reset pulse. The exact resistor value is a function of the signal capacitive loading.
$\overline{\text{CRB}}$0–4, 6, 7 (Configuration Register Bits)	41, 43, 44, 54, 55, 16, 57	These dual function pins act as inputs during reset (if $\overline{\text{CRPE}}$ = 0) to determine the state of the Configuration Register bits. The bits of the Configuration Register will be the complement of these inputs. A 47 kΩ (Note 1) resistor can be used to pull these pins to the required signal levels. These pins will be outputs when the chip is not in reset. These pins have the following dual functions SOUT2/$\overline{\text{CRB}}$0, $\overline{\text{RTS}}$2/$\overline{\text{CRB}}$1, $\overline{\text{DTR}}$2/$\overline{\text{CRB}}$2, $\overline{\text{DTR}}$1/$\overline{\text{CRB}}$3, $\overline{\text{RTS}}$1/$\overline{\text{CRB}}$4, $\overline{\text{HCS}}$0/$\overline{\text{CRB}}$6, SOUT1/$\overline{\text{CRB}}$7. **Note 1:** If the minimum reset time of 100 ns is required these resistors will have to be reduced to <10 kΩ to stabilize the input signal during the reset pulse. The exact resistor value is a function of the signal capacitive loading.
$\overline{\text{CTS}}$1, 2 (Clear to Send)	51, 48	When low, this input indicates that the MODEM or data set is ready to exchange data. The $\overline{\text{CTS}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 4 (CTS) of the MODEM Status Register for the appropriate channel. Bit 4 is the complement of the $\overline{\text{CTS}}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{\text{CTS}}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{\text{CTS}}$ has no effect on the transmitter. **Note:** Whenever the DCTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
D0–D7 (Data Bus)	60–64, 66–68	This bus contains eight TRI-STATE input/output lines. The bus provides bidirectional communications between this chip and the CPU. Data, control words, and status information are transferred via the D0–D7 Data Bus.
$\overline{\text{DAK}}$ (DMA Acknowledge)	70	Active low input to acknowledge the DMA request and enable the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ inputs. This signal is enabled when D3 of the Drive Control Register is set. However, the specify command must be used to enable the DMA mode.

2.0 Pin Descriptions (Continued)

Pin Symbol	Pin Number	Description
$\overline{\text{DCD}}$1, 2 (Data Carrier Detect)	52, 47	When low, this input indicates that the data carrier has been detected by the MODEM or data set. The $\overline{\text{DCD}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the DCD signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{\text{DCD}}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{\text{DCD}}$ has no effect on the receiver. **Note:** Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
DIR (Direction)	91	This output determines the direction of the head movement (low = step in, high = step out). When in the write or read modes, this output will be high. This is a high drive open drain output.
$\overline{\text{DR}}$0, 1 (Drive)	93, 92	These are active low drive select outputs for drive 0 and drive 1. They are ANDed with the corresponding motor enable lines. This is a high drive open drain output. These pins contain encoded drive select information if bit 7 of the Configuration Register is set (see Configuration Register for detailed information on the encoding).
DRQ (DMA Request)	69	Active high output to signal the DMA controller that a data transfer is needed. This signal is enabled when D3 of the Drive Control Register is set. However, the specify command must be used to enable the DMA mode.
DRVTYP (Drive Type)	84	This is an input used by the controller to enable the 300 kb/s mode. This enables the use of floppy drives with either dual or single speed spindle motors. For dual speed spindle motors, this pin is tied low. When low, and 300 kb/s data rate is selected in the data rate register, the PLL actually uses 250 kb/s. This pin is tied high for single speed spindle motor drives (standard AT drive). When this pin is high and 300 kb/s is selected 300 kb/s is used. (See also RPM/LC pin.)
DSKCHG/RG (Disk Change/Read Gate)	73	This disk interface input indicates when the disk drive door has been opened. The active high state of this input is read from bit D7 of address 3F7 hex. When the RG bit in the Mode Command is set, this pin functions as a Read Gate signal. When low it forces the data separator to lock to the crystal, and when high it locks to the data for diagnostic purposes.
$\overline{\text{DSR}}$1, 2 (Data Set Ready)	53, 46	When low, this input indicates that the MODEM or data set is ready to establish the communications link with the UART. The $\overline{\text{DSR}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 5 ($\overline{\text{DSR}}$) of the MODEM Status Register. Bit 5 is the complement of the $\overline{\text{DSR}}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{\text{DSR}}$ input has changed state since the previous reading of the MODEM Status Register. **Note:** Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
$\overline{\text{DTR}}$1, 2 (Data Terminal Ready)	54, 44	When low, this output indicates to the MODEM or data set that the UART is ready to establish a communications link. The $\overline{\text{DTR}}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state, if the $\overline{\text{XTSEL}}$ pin is high during reset. If the $\overline{\text{XTSEL}}$ pin is low during reset, the associated pin state is controlled by the MCR0 bit during loop mode operation. These are dual function pins; see CRB2 and CRB3 for detailed operation during reset.
$\overline{\text{ERR}}$ (Error)	28	This input is set low by the printer when it has detected an error.
FILTER	82	This pin is the output of the charge pump and the input to the VCO. One or more filters are attached between this pin and the VSSA, FGND250 and FGND500 pins.
FGND250 (Filter Ground 250 kb/s)	80	This pin connects the PLL filter for 250k(MFM)/125k(FM) b/s or 300k(MFM)/150k(FM) b/s to ground. This is a low impedance open drain output.
FGND500 (Filter Ground 500 kb/s)	79	This pin connects the PLL filter for 500k(MFM)/250k(FM) b/s to ground. This is a low impedance open drain output.

2.0 Pin Descriptions (Continued)

Pin Symbol	Pin Number	Description
$\overline{\text{GPEN}}$ (Game Port Enable)	18	This multi-function output provides an active low signal if I/O address 201 hex is selected and the $\overline{\text{XTSEL}}$ pin was high during reset. It can be used as a decoded chip select for external logic that implements the game port function in an AT system. (See $\overline{\text{GRD}}$ and $\overline{\text{XTSEL}}$ for additional details about the operation of this pin.)
$\overline{\text{GRD}}$ (Game Read)	18	This multi-function output provides an active low signal if I/O address 201 hex is selected, the read pin is low, and the $\overline{\text{XTSEL}}$ pin was low during reset. It can be used as a decoded read signal for external logic that implements the game port function in an XT system. (See $\overline{\text{GPEN}}$ and $\overline{\text{XTSEL}}$ for additional details about the operation of this pin.)
$\overline{\text{GWR}}$ (Game Write)	17	This multi-function output provides an active low signal if I/O address 201 hex is selected, the write pin is low, and the $\overline{\text{XTSEL}}$ pin was low during reset. It can be used as a decoded write signal for external logic that implements the game port function in an XT system. (See $\overline{\text{HCS}}$1 and $\overline{\text{CPPE}}$ for additional details about the operation of this pin.)
$\overline{\text{HSC}}$0, 1 (Hard Disk Chip Select)	16, 17	These dual and multi-function outputs provide a hard disk enable signal when the addresses shown in Table 1-1 are present on A0–A9 during a read or write access. Using minimal hardware, these signals will control and interface between the CPU and a hard disk drive that has a controller. $\overline{\text{HSC}}$0 is always used for this function after reset. $\overline{\text{HSC}}$1 can be used for this function after reset, if $\overline{\text{XTSEL}}$ was high during reset. (See $\overline{\text{CRB}}$6, $\overline{\text{GWR}}$ and $\overline{\text{CRPE}}$ for further information on these pins, and Table 1-1.)
HDSEL (Head Select)	96	This output determines which disk drive head is active. Low = Head 1, Open (high) = Head 0. This is a high drive open drain output.
$\overline{\text{IOL}}$ (I/O Address Low)	13	This input pin should be driven low by external decode logic when all I/O address bits 10–15 are low. This signal is gated inside the PC87310 to ensure that the I/O bus is fully decoded.
$\overline{\text{INIT}}$ (Initialize)	36	This output initializes the printer when it is low. This pin will be in a TRI-STATE condition 10 ns after a one is loaded into the corresponding Control Register bit position. The system should pull this pin high using a 4.7 kΩ resistor.
$\overline{\text{INDEX}}$	98	This active low Schmitt input signals the beginning of a track.
IRQ3, 4 (Interrupt Request 3, 4)	40, 58	These outputs signal serial port interrupts. The appropriate interrupt goes high whenever it is enabled via the IER and any of the following serial interrupt conditions are active: Receiver Error Flag set, Receiver Data Available, Transmitter Holding Register Empty or Modem Status set. The interrupt is reset low after the appropriate interrupt service, disabling through IER or a Master Reset. IRQ4 presents the interrupt signal if the serial channel is designated COM1. IRQ3 presents the interrupt signal if the serial channel is designated COM2. Both IRQ3 and IRQ4 can be disabled by resetting OUT 2 low.
IRQ6 (Interrupt Request 6)	72	Active high output to signal that a floppy disk controller operation requires the attention of the microprocessor. The action required depends on the current function of the controller. This signal is enabled when D3 of the Drive Control Register is set.
IRQ7 (Interrupt Request 7)	39	This output signals parallel port interrupts. When enabled (Control Register bit 4 = 1), the appropriate interrupt signal will follow the $\overline{\text{ACK}}$ signal input.
MR (Master Reset)	1	When this input is high, it clears all registers, except the parallel port data and status registers; the UART Receiver Buffer, Transmitter Holding, and Divisor Latch Registers. In the floppy disk controller it resets all disk drive output lines to their disabled state. Reset clears the Drive Control Register, sets the Data Rate Register to 250 kb/s, and sets the Main Status Register to 80. The Mode register default values are given in the Mode Register description. To prevent glitches from activating the reset sequence, attach a 1000 pF capacitor to this pin.

2.0 Pin Descriptions (Continued)

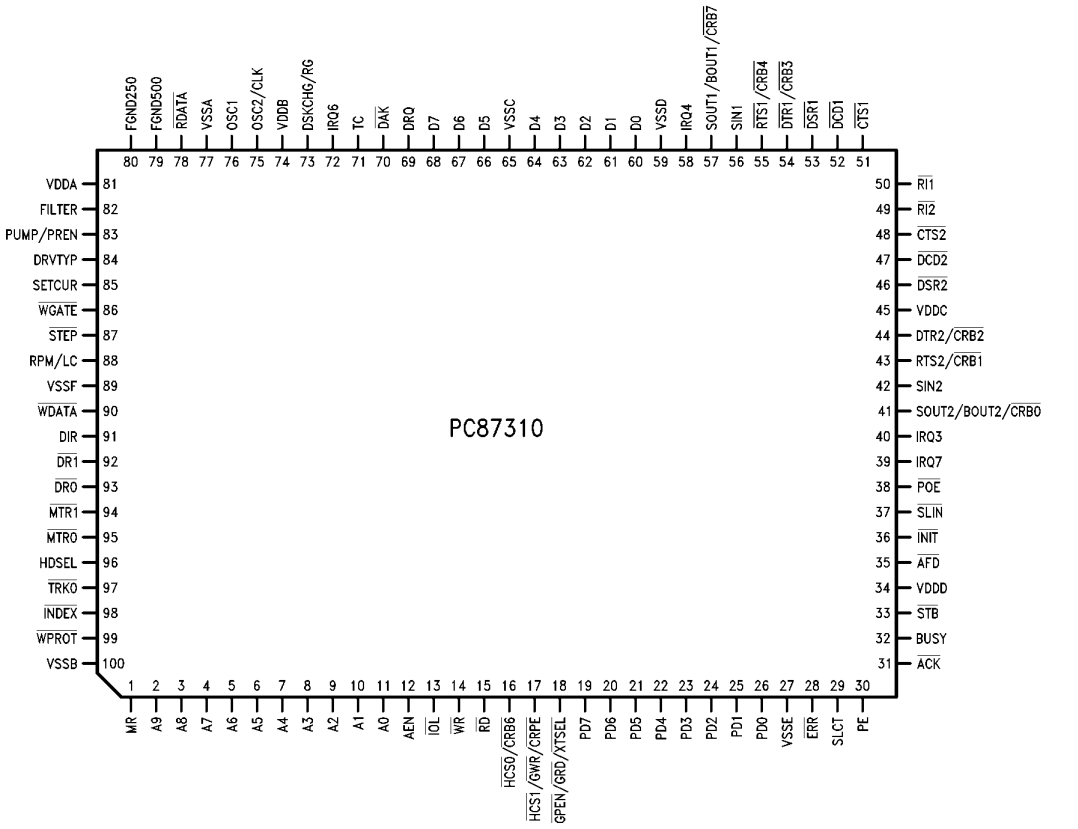
Pin Symbol	Pin Number	Description
$\overline{\text{MTR}}$0, 1 (Motor)	95, 94	These are active low motor enable outputs for drive 0 and drive 1. This is a high drive open drain output. These pins contain encoded drive select information if bit 7 of the Configuration Register is set (see Configuration Register for detailed information on the encoding). Otherwise they are controlled through bits in the Drive Control Register.
OSC1 (Oscillator)	76	One side of an external 24 MHz crystal is attached here. This pin is tied low if an external clock is used.
OSC2/CLK (Oscillator/Clock)	75	One side of the external 24 MHz crystal is attached here. If a crystal is not used, a TTL or CMOS compatible clock is connected to this pin.
PD0–PD7 (Port Data)	26–19	These bidirectional pins transfer data to and from the peripheral data bus. These pins have high current drive capability. (See DC Electrical Characteristics.)
PE (Paper End)	30	This input is set high by the printer when it is out of paper.
$\overline{\text{POE}}$ (Port Output Enable)	38	When this input is low, data written to the parallel port data register is output through PD0–PD7. When this input is high, PD0–PD7 are in a high impedance state and act as inputs. This pin is usually tied low for printer operation.
PUMP/PREN (Pump/Precompensation Enable)	83	When the PU bit is set in Mode Command this pin is an output that indicates when the charge pump is making a correction. Otherwise this pin is an input that sets the precomp mode as shown in Table 4-13. If pin is configured as PUMP, PREN is assumed high.
$\overline{\text{RD}}$ (Read)	15	When this input is low while the chip is selected, the CPU can read status information or data from the selected register.
$\overline{\text{RDATA}}$ (Read Data)	78	The active low raw data read from the disk is connected here. This is a Schmitt input.
$\overline{\text{RI}}$1, 2 (Ring Indicator)	50, 49	When low, this input indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{\text{RI}}$ signal is a MODEM status input whose condition the CPU can test by reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{\text{RI}}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{\text{RI}}$ input signal has changed from a low to a high state since the previous reading of the MODEM Status Register. **Note:** Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.
RPM/LC (Revolutions per Minute/Low Current)	88	This high drive open drain output pin has two functions based on the selection of the DRVTYP pin. 1. When using a dual speed spindle motor floppy drive (DRVTYP pin low), this output is used to select the spindle motor speed, either 300 RPM or 360 RPM. In this mode this output goes low when 250/300 kb/data rate is chosen in the data rate register, and high when 500 kb/s is chosen. 2. When using single speed spindle motor floppy drive (DRVTYP pin high), this pin indicates when to reduce the write current to the drive. This output is high for high density media (when 500 kb/s is chosen).
$\overline{\text{RTS}}$1, 2 (Request to Send)	55, 43	When low, this output indicates to the MODEM or data set that the UART is ready to exchange data. The $\overline{\text{RTS}}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state, if the $\overline{\text{XTSEL}}$ is high during reset. If the $\overline{\text{XTSEL}}$ pin is low during reset, MCR bit 1 controls the associated pin during loop mode operation. (See CRB4 and CRB1 for further information on these pins.)
SETCUR (Set Current)	85	An external resistor connected from this pin to analog ground programs the amount of charge pump current that drives the external filters. The PLL Filter Design section shows how to determine the values.
SIN1, 2 (Serial Input)	56, 42	This input receives composite serial data from the communications link (peripheral device, MODEM, or data set).

2.0 Pin Descriptions (Continued)

Pin Symbol	Pin Number	Description
SLCT (Select)	29	This input is set high by the printer when it is selected.
$\overline{\text{SLIN}}$ (Select Input)	37	This output selects the printer when it is low. This pin will be in a TRI-STATE condition 10 ns after a zero is loaded into the corresponding Control Register bit position. The system should pull this pin high using a 4.7 kΩ resistor.
SOUT1, 2 (Serial Output)	57, 41	This output sends composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation. (See BOUT1, 2 and CRB0, 7 for further information on these pins.)
$\overline{\text{STB}}$ (Data Strobe)	33	This output indicates to the peripheral that the data at the parallel port is valid. This pin will be in a TRI-STATE condition 10 ns after a zero is loaded into the corresponding Control Register bit position. The system should pull this pin high using a 4.7 kΩ resistor.
$\overline{\text{STEP}}$	87	This active low open drain high drive output will produce a pulse at a software programmable rate to move the head during a seek operation.
TC (Terminal Count)	71	Active high input to indicate the termination of a DMA transfer. This signal is enabled when the DMA Acknowledge pin is active.
$\overline{\text{TRK0}}$ (Track 0)	97	This active low Schmitt input tells the controller that the head is at track zero of the selected disk drive.
V_{DD} A, B, C, D (Power)	81, 74, 45, 34	+5V Supply to the FDC analog, FDC digital, serial ports, and parallel port circuitry, respectively.
V_{SS} A, B, C, D, E, F (Ground)	77, 100, 65, 59, 27, 89	0V Reference for the FDC analog, FDC digital, CPU interface, serial ports, parallel port, and disk interface output drive circuitry, respectively.
$\overline{\text{WDATA}}$ (Write Data)	90	This is the active low open drain write precompensated serial data to be written onto the selected disk drive. This is a high drive open drain output.
$\overline{\text{WGATE}}$ (Write Gate)	86	This active low open drain high drive output enables the write circuitry of the selected disk drive. This output has been designed to prevent glitches during power up and power down. This prevents writing to the disk when power is cycled.
$\overline{\text{WPROT}}$ (Write Protect)	99	This active low Schmitt input indicates that the disk is write protected. Any command that writes to that disk drive is inhibited when a disk is write protected.
$\overline{\text{WR}}$ (Write)	14	When this input is low while the chip is selected, the CPU can write control words or data into the selected register.
$\overline{\text{XTSEL}}$ (XT Select)	18	When this input is low during reset the chip will operate in the XT compatible mode. When this input is high during reset this chip will operate in the AT compatible mode. This pin must always have a pull down or pull up resistor attached to it. (See $\overline{\text{GPEN}}$ and $\overline{\text{GRD}}$ for further information on this pin.)

3.0 Connection Diagram

Plastic Quad Flatpak, EIAJ



TL/C/10591–6

Order Number PC87310VF
See NS Package Number VF100B

4.0 Functional Description

This section provides the descriptions for each of the major functional blocks of the PC87310. Each functional block is described as independently of the other blocks as is possible. Software can address all blocks independently of each other, except for the Configuration Port and low power mode operation. The Configuration Register affects all other blocks by determining which ones the address decoder can activate. The low power mode is enabled and disabled via the floppy disk controller mode command. Enabling low power mode will stop the 24 MHz crystal and clock oscillation to all logic blocks. Software should ensure that both UARTs and the floppy disk controller are idle and will continue to be idle while the low power mode is enabled.

4.1 ADDRESS DECODER

This decodes address signals A0–A9, qualifies them and if they qualify it activates the appropriate function block. The $\overline{\text{XTSEL}}$ pin determines whether function blocks respond to the industry standard XT or AT address.

Before activating the block it qualifies the address with $\overline{\text{IOL}}$, AEN, and the Configuration Register enable signals for each function. If $\overline{\text{IOL}}$ is low (active), then an external decoder has determined that address bits A10–A15 are all zero and this is an I/O access. If AEN is low (active), then this is a CPU (not DMA) access and the addressed register can respond. If the configuration bit for the addressed function is 0, that function is active on this particular device and can respond.

There are no pin selects for the functions on this device, so the designer must use the on-chip address decoder to select any function. Each function, except for the hard disk select, can be disabled via hardware or software. The hard disk select can only be disabled via software.

4.2 CONFIGURATION PORT

This port consists of a one byte register that the system can program via hardware (voltage levels on certain pins during reset) or software (two consecutive writes to I/O address 03f3 hex). When programming the Configuration Register via software, the data sent during both writes to 03f3 hex should be the correct bit pattern and there should be no I/O write strobes between these 03f3 hex accesses. Furthermore, system interrupts should be disabled to prevent interrupt service routines from issuing I/O write strobes between the 03f3 hex accesses. Through this register, the system can enable, disable, or reassign addresses to the on-chip functions.

One pin ($\overline{\text{CRPE}}$) determines whether the default value of this register will be 00 (all functions enabled) or a value latched in during reset from the $\overline{\text{CRB}}$x pins. If $\overline{\text{CRPE}}$ is low during reset, the **complement** of the $\overline{\text{CRB}}$x pins will be loaded into the bits of the Configuration Register.

Bit 5, Hard Drive Chip Select does not have an external pin associated with it and will always default to the enabled state. If $\overline{\text{CRPE}}$ is high during reset, then 00 will be loaded into the Configuration Register. After reset, the value of this register can be changed by software regardless of the state of $\overline{\text{CRPE}}$.

The Configuration Register bits are defined in Table 4-1. An example of the initial condition after reset if 00 is loaded into the Configuration Register is:

1. The parallel port responds to address range 378–37A (LPT2).
2. Serial Port 1 responds to 3F8–3FF (COM1).
3. Serial Port 2 responds to 2F8–2FF (COM2).
4. The hard disk selects are enabled.
5. The floppy disk controller is enabled.
6. The floppy disk controller drive and motor pins can drive the disk interface directly (no encoded information is presented).

TABLE 4-1. Configuration Register Bit Definitions

B7	B6	B5	B4	B3	B2	B1	B0	Result	
						0	0	Parallel port at LPT2 (378–37F)	
						0	1	Parallel port at LPT1 (3BC–3BE)	
						1	0	Parallel port at LPT3 (278–27F)	
						1	1	Parallel port disabled	
								UART1	**UART2**
			0	0	0			COM1 (3F8–3FF)	COM2 (2F8–2FF)
			0	0	1			disabled	COM2
			0	1	0			COM1	disabled
			0	1	1			disabled	disabled
			1	0	0			COM2	COM1
			1	0	1			disabled	COM1
			1	1	0			COM2	disabled
			1	1	1			disabled	disabled
		0						Hard disk select enabled	
		1						Hard disk select disabled	
	0							Floppy disk controller enabled	
	1							Floppy disk controller disabled	
0								DR0, DR1, MTR0, and MTR1 pins select drive 0, drive 1, motor 0, motor 1, respectively	
1								DR0, DR1, MTR0, and MTR1 pins contain the encoded drive and motor information shown in Table 4-2.	

4.0 Functional Description (Continued)

TABLE 4-2. Encoded Drive and Motor Pin Information (Configuration Register Bit 7 = 1)

Drive Control Register Bits								Drive Control Pins				Decoded Function
7	6	5	4	3	2	1	0	$\overline{DR1}$	$\overline{DR0}$	$\overline{MTR1}$	$\overline{MTR0}$	
X	X	0	1			0	0	1	1	1	0	Activate Drive 0 and Motor 0
X	X	1	0			0	1	1	0	0	1	Activate Drive 1 and Motor 1
X	X	0	0			1	0	0	1	1	1	Activate Drive 2 and Motor 2
X	X	0	0			1	1	0	0	1	1	Activate Drive 3 and Motor 3

The pin states shown in Table 4-2 are the direct results of the bit patterns shown. All other bit patterns produce pin states that should NOT be decoded to enable any drive or motor. In other words all other bit patterns except the four shown in Table 4-2 are invalid and should disable all drives and motors, when Configuration Register bit 7 = 1.

4.3 SERIAL PORTS

4.3.1 Introduction

Each of these serial ports function as a data input/output interface in a microcomputer system. The system software determines the functional configuration of the UARTs via a TRI-STATE 8-bit bidirectional data bus.

The UARTs are completely independent. They perform serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of either UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).

The UARTs have programmable baud rate generators that are capable of dividing the timing reference clock input by divisors of 1 to ($2^{16}-1$), and producing a 16 $\times$ clock for driving the internal transmitter logic. Provisions are also included to use this 16 $\times$ clock to drive the receiver logic. The UARTs have complete MODEM-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

The UARTs can operate in the INS8250-B mode (XT) or the NS16450 mode (AT) depending on the state of the $\overline{XTSEL}$ pin during reset.

4.3.2 Serial Port Registers

TABLE 4-3. Register Addresses ($\overline{IOL}$ = 0, AEN = 0)

DLAB1	CHSL	A2	A1	A0	Register	
0	1	0	0	0	Receiver Buffer (Read), Transmitter Holding (Write)	UART 1
0	1	0	0	1	Interrupt Enable	
X	1	0	1	0	Interrupt Identification (Read)	
X	1	0	1	0	Test Control (Write)	
X	1	0	1	1	Line Control	
X	1	1	0	0	MODEM Control	
X	1	1	0	1	Line Status	
X	1	1	1	0	MODEM Status	
X	1	1	1	1	Scratch (Note 1)	
1	1	0	0	0	Divisor Latch (Least Significant Byte)	
1	1	0	0	1	Divisor Latch (Most Significant Byte)	
DLAB2	**CHSL**	**A2**	**A1**	**A0**	**Register**	
0	0	0	0	0	Receiver Buffer (Read), Transmitter Holding (Write)	UART 2
0	0	0	0	1	Interrupt Enable	
X	0	0	1	0	Interrupt Identification (Read)	
X	0	0	1	0	Test Control (Write)	
X	0	0	1	1	Line Control	
X	0	1	0	0	MODEM Control	
X	0	1	0	1	Line Status	
X	0	1	1	0	MODEM Status	
X	0	1	1	1	Scratch (Note 1)	
1	0	0	0	0	Divisor Latch (Least Significant Byte)	
1	0	0	0	1	Divisor Latch (Most Significant Byte)	

Note 1: This register is only present when operating in the AT, NS16450, mode ($\overline{XTSEL}$ is high during reset).

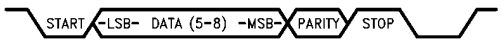
4.0 Functional Description (Continued)

4.3.2 Serial Port Registers

Two identical register sets, one for each channel, are in the DUART. All register descriptions in this section apply to the register sets in both channels.

LINE CONTROL REGISTER

The system programmer uses the Line Control Register (LCR) to specify the format of the asynchronous data communications exchange and set the Divisor Latch Access bit. This is a read and write register. Table 4-4 shows the contents of the LCR. Details on each bit follow:



TL/C/10591–7

FIGURE 1. Composite Serial Data

Bits 0 and 1: These two bits specify the number of data bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Data Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits transmitted with each serial character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit data length is selected, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The receiver checks the first Stop bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When parity is enabled and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When parity is enabled and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked as a logic 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a logic 0 then the Parity bit is transmitted and checked as a logic 1 (Mark Parity). If bit 5 is a logic 0 Stick Parity is disabled.

Bit 6: This bit is the Break Control bit. It causes a break condition to be transmitted to the receiving UART. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing state (logic 0). The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has no effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator or the Alternate Function Register during a Read or Write operation. It must be set low (logic 0) to access any other register.

4.0 Functional Description (Continued)

TABLE 4-4. Register Summary for an Individual UART Channel

Bit No.	Register Address											
	0 DLAB=0	0 DLAB=0	1 DLAB=0	2	2	3	4	5	6	7	0 DLAB=1	1 DLAB=1
	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Ident. Register (Read Only)	Test Control Register (Write Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register (Note 4)	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	TCR	LCR	MCR	LSR	MSR	SCR	DLL	DLM
0	Data Bit 0 (Note 1)	Data Bit 0	Enable Received Data Available Interrupt (ERDAI)	"0" if Interrupt Pending	Reserved 0	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETHREI)	Interrupt ID Bit	Reserved 0	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit	Reserved 0	Number of Stop Bits (STB)	Out 1 (Note 3)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EMSI)	0	Reserved 0	Parity Enable (PEN)	IRQ Enable (Note 3)	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	$\overline{\text{BAUDOUT}}$ Select	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Reserved 0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Reserved 0	Set Break	0	Transmitter Empty (TEMT) (Note 2)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Reserved 0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Note 3: This bit no longer has a pin associated with it.

Note 4: When operating in the XT mode, this register is not available.

4.0 Functional Description (Continued)

TABLE 4-5. DUART Reset Configuration

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	**0000** 0000 (Note 1)
Interrupt Identification Register	Master Reset	00**00** 0001
Test Control	Master Reset	**000**0 **0000**
Line Control Register	Master Reset	0000 0000
MODEM Control Register	Master Reset	**0000** 0000
Line Status Register	Master Reset	0110 0000
MODEM Status Register	Master Reset	XXXX 0000 (Note 2)
SOUT	Master Reset	High
INTR (RCVR Errs)	Read LSR/MR	Low/TRI-STATE
INTR (RCVR Data Ready)	Read RBR/MR	Low/TRI-STATE
INTR (THRE)	Read IIR/Write THR/MR	Low/TRI-STATE
INTR (Modem Status Changes)	Read MSR/MR	Low/TRI-STATE
$\overline{\text{OUT 2}}$ Bit	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High

Note 1: Boldface bits are permanently low.

Note 2: Bits 7–4 are driven by the input signals.

PROGRAMMABLE BAUD GENERATOR

The DUART contains two independently programmable Baud Generators. The 24 MHz crystal oscillator frequency input is divided by 13, resulting in a frequency of 1.8462 MHz. This is sent to each Baud Generator and divided by the divisor for the associated UART. The output frequency of the Baud Generator is 16 × the baud rate, [divisor # = (frequency input) ÷ (baud rate × 16)]. The output of each Baud Generator drives the transmitter and receiver sections of the associated serial channel. Two 8-bit latches per channel store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization to ensure proper operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud Counter is loaded.

Table 4-6 provides decimal divisors to use with crystal frequencies of 24 MHz. The oscillator input to the chip should always be 24 MHz to ensure that the Floppy Disk Controller timing is accurate and that the UART divisors are compatible with existing software. Using a divisor of zero is **not** recommended.

LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. Table 4-4 shows the contents of the Line Status Register. Details on each bit follow:

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

TABLE 4-6. Divisors, Baud Rates and Clock Frequencies

Divisor Baud Rate	1.8462 MHz Clock	
	Decimal Divisor for 16 × Clock	Percent Error (Note 1)
50	2304	0.1
75	1536	
110	1047	
134.5	857	0.4
150	768	
300	384	
600	192	
1200	96	
1800	64	
2000	58	0.5
2400	48	
3600	32	
4800	24	
7200	16	
9600	12	
19200	6	
38400	3	
56000	2	3.0

Note 1: The percent error for all Baud Rates, except where indicated otherwise, is 0.2%.

4.0 Functional Description (Continued)

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is set to a logic 1 upon detection of an overrun condition and reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is a logic 0 (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status Register. The UART will try to resynchronize after a framing error. To do this it assumes that the framing error was due to the next start bit, so it samples this ''start'' bit twice and then takes in the ''data''.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status Register. Restarting after a break is received, requires the SIN pin to be logical 1 for at least ½ bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 whenever the CPU loads the Transmitter Holding Register.

Bit 6: This bit changes its function depending on whether the device is operating in the XT or AT mode. When operating in the AT mode, this bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character. When operating in the XT mode this bit is set whenever the Transmitter Shift Register is empty. It is cleared whenever a byte is loaded into the Transmit Shift Register.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is only used for factory testing.

INTERRUPT IDENTIFICATION REGISTER

In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels and records these in the Interrupt Identification Register. The four levels of interrupt conditions in order of priority are Receiver Line Status; Received Data Ready; Transmitter Holding Register Empty; and MODEM Status.

When the CPU accesses the IIR, the UART freezes all interrupts and indicates the highest priority pending interrupt to the CPU. While this CPU access is occurring, the UART records new interrupts, but does not change its current indication until the access is complete. Table 4-4 shows the contents of the IIR. Details on each bit follow:

Bit 0: This bit can be used in an interrupt environment to indicate whether an interrupt condition is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 4-7.

Bits 3 through 7: These five bits of the IIR are always logic 0.

TEST CONTROL REGISTER

This 8-bit write only register provides for the control of UART test and alternate functions.

Bits 0–3, 5–7: These seven bits are reserved.

Bit 4: This bit selects whether the /Baudout (TCR4 = 1) or SOUT (TCR4 = 0) signal will be presented at the output pin assigned to the corresponding UART channel.

INTERRUPT ENABLE REGISTER

This register enables the four types of UART interrupts. Each interrupt can individually activate the appropriate interrupt (IRQ3 or IRQ4) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, setting bits of this register to a logic 1, enables the selected interrupt(s). Disabling an interrupt prevents it from being indicated as active in the IIR and from activating the interrupt output signal. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. Table 4-4 shows the contents of the IER. Details on each bit follow.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register (MCR) are indicated in Table 4-4 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1. In local loopback mode, this bit controls bit 5 of the MODEM Status Register.

Note: The $\overline{DTR}$ and $\overline{RTS}$ output of the UART may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

4.0 Functional Description (Continued)

TABLE 4-7. Interrupt Control Functions

Interrupt Identification Register			Priority Level	Interrupt Set and Reset Functions		
Bit 2	Bit 1	Bit 0		Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1		None	None	
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0. In local loopback mode, this bit controls bit 4 of the MODEM Status Register.

Bit 2: This bit is the OUT1 bit. It does not have an output pin associated with it. It can be written to and read by the CPU. In local loopback mode, this bit controls bit 6 of the Modem Status Register.

Bit 3: This bit enables the interrupt when set. No external pin is associated with this bit. In local loopback mode, this bit controls bit 7 of the MODEM Status Register.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is ''looped back'' into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{DSR}$, $\overline{CTS}$, $\overline{RI}$ and $\overline{DCD}$) are disconnected; and the DTR, RTS, OUT1, IRQ ENABLE bits in MCR are internally connected to DSR, CTS, RI and DCD in MSR respectively. When operating in the AT mode the MODEM Control output pins are forced to their high (inactive) states. When operating in the XT mode the Modem Control output pins remain connected to their corresponding bits in the MCR. In the loopback mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit-and-received-data paths of the serial port.

In the loopback mode, the receiver and transmitter interrupts are fully operational. The MODEM Status Interrupts are also operational, but the interrupts' sources are the lower four bits of MCR instead of the four MODEM control inputs. Writing a 1 to any of them will cause an interrupt. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

Table 4-4 shows the contents of the MSR. Details on each bit follow.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This bit is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loopback) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to IRQ ENABLE in the MCR.

SCRATCHPAD REGISTER

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily. When operating in the XT mode, this register is unavailable.

4.0 Functional Description (Continued)

4.4 FLOPPY DISK CONTROLLER

4.4.1 Introduction

This device contains a full featured floppy disk controller that is software compatible with the μPD765A and the DP8473. It includes many hardware and software enhancements. Among these enhancements is additional logic specifically required for an IBM PC, PC-XT, or PS/2 design.

This controller incorporates a precision analog data separator, that includes a self trimming delay line and VCO. Up to three external filters are switched automatically depending on the data rate selected. This provides optimal performance at the standard PC data rates fo 250/300 kb/s, and 500 kb/s. It also enables optimum performance at 1 Mb/s (MFM). These features combine to provide the lowest possible PLL bandwidth, with the greatest lock range, and hence the widest window margin.

This controller has write precompensation circuitry. A shift register is used to provide a fixed 125 ns early-late precompensation for all tracks at 500k/300k/250 kb/s (83 ns for 1 MB/s), or a precompensation value that scales with the data rate, 83 ns/125 ns/208 ns/250 ns for data rates of 1.0M/500k/300k/250 kb/s respectively.

Specifically to support the PC-AT and PC-XT design, the Floppy Disk Controller PLUS-2 includes address decode for the A0–A2 address lines, the motor/drive select register, data rate register for selecting 250/300/500 kb/s, Disk Changed status, dual speed spindle motor control, low write current and DMA/interrupt sharing logic. The controller also supports direct connection to the μP bus via internal 24 mA buffers. The controller also can be connected directly to the disk drive via internal open drain high drive outputs, and Schmitt inputs.

In addition to this logic the controller includes many features to ease design of higher performance drives and future controller upgrades. These include 1.0 Mb/s data rate, extended track range to 4096, Implied seeking, working Scan Commands, motor control timing, both standard IBM formats as well as Sony 3.5″ (ISO) formats, and other enhancements.

4.4.2 765A Compatible Micro-Engine

The core of the FDC is a μPD765A and DP8473 compatible microcoded engine. This engine consists of a sequencer, program ROM, and disk/misc registers. This core is clocked by either a 4 MHz, 4.8 MHz or 8 MHz clock selected in the Data Rate Register. Upon this core is added all the glue logic used to implement a PC-XT or AT, or PS/2 floppy controller, as well as the data separator and write precompensation logic.

The controller consists of a microcoded engine that controls the entire operation of the chip including coordination of data transfer with the CPU, controlling the drive controls, and actually performing the algorithms associated with reading and writing data to/from the disk. This includes the read algorithm for the data separator.

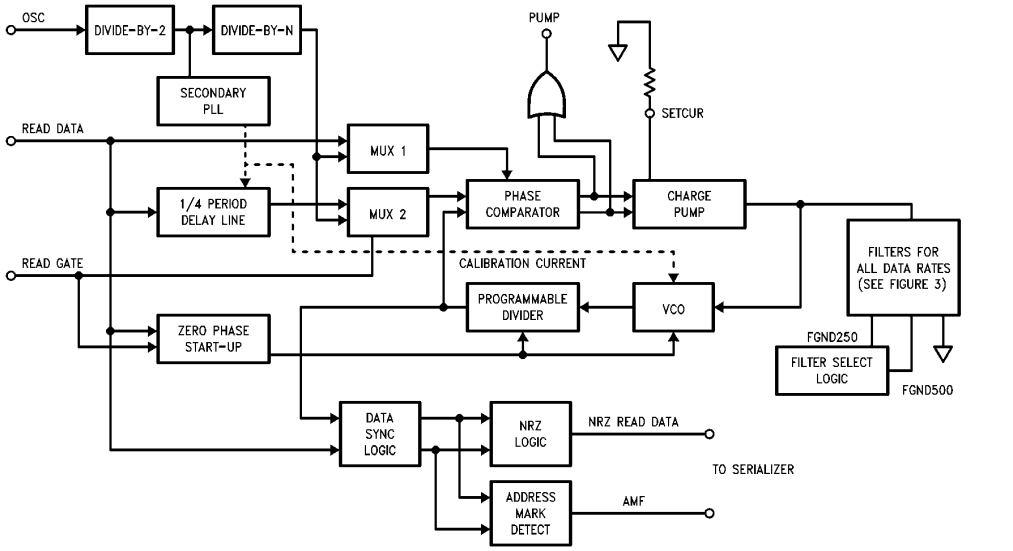
Like the μPD765A, this controller takes commands and returns data and status through the Data Register in a byte serial fashion. Handshake for command/status I/O is provided via the Main Status Register. All of the μPD765A commands are supported, as are many other enhanced commands.

DATA SEPARATOR

The internal data separator consists of an analog PLL and its associated circuitry. The PLL synchronizes the raw data signal read from the disk drive. The synchronized signal is used to separate the encoded clock and data pulses. The data pulses are de-serialized into bytes and then sent to the μP by the controller.

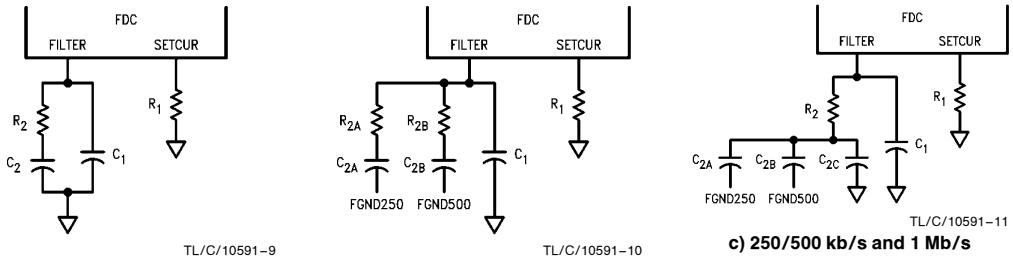
The main PLL consists of four main components, a phase comparator, a filter, a voltage controlled oscillator (VCO), and a programmable divider. The phase comparator detects the difference between the phase of the divider's output and the phase of the raw data being read from the disk. This phase difference is converted to a current which either charges or discharges one of the three external filters. The resulting voltage on the filter changes the frequency of the VCO and the divider output to reduce the phase difference between the input data and the divider's output. The PLL is ''locked'' when the frequency of the divider is exactly the same as the average frequency of the data read from the disk. A block diagram of the data separator is shown in *Figure 2.*

4.0 Functional Description (Continued)



TL/C/10591–8

FIGURE 2. Block Diagram of the Data Separator



TL/C/10591–9

a) Single Data Rate

TL/C/10591–10

b) 250/500 kb/s Filter

TL/C/10591–11

c) 250/500 kb/s and 1 Mb/s

Note: For all filter configurations, 250 kb/s and 300 kb/s share the same filter.

FIGURE 3. Typical Configuration for Loop Filters for the FDC Showing Component Labels

To ensure optimal performance, the data separator incorporates several additional circuits. The quarter period delay line is used to determine the center of each bit cell. A secondary PLL is used to automatically calibrate the quarter period delay line. The secondary PLL also calibrates the center frequency of the VCO.

To eliminate the logic associated with controlling multiple data rates the floppy disk controller (FDC) supports the connection of three filters to the chip via the FGND250, and FGND500 pins (filter ground switches). The controller chooses which filter components to use based on the value loaded in the Data Rate Register. If 500 k(MFM) is being used then the FGND500 is enabled (FGND250 is disabled). If 250 k(MFM) or 300 k(MFM) is being used the FGND250 pin is enabled, and FGND500 is disabled. For 1 Mb/s (MFM) both FGND pins are disabled.

Note for FM encoding: Sometimes, after a reset, the FDC will consistently return an error in the Result Phase after an FM read command. If this occurs, simply reset the FDC and retry the operation. This may have to be done more than once, as many as five times. Resetting and repeating will prevent soft errors being reported prematurely. This technique is used by MS-DOS.

Figure 3 shows several possible filter configurations. For a filter to cover all data rates *(Figure 3c)*, the FDC has a 1 Mb/s filter always connected and other capacitor filter components for the other data rates are switched in parallel to this filter. The actual loop filter for 500 kb/s is the parallel combination of the two capacitors, C_{2C} and C_{2B}, attached to the FGND500 pin and to ground. The 250/300 kb/s filter is the parallel combination of the capacitors, C_{2C} and C_{2A}, attached to the FGND250, and ground. If 1 Mb/s need not be supported then the filter configuration of *Figure 3b* can be used. This configuration allows more optimal performance for both 500k and 250/300 kb/s. *Figure 3a* is a simple filter configuration primarily for a single data rate (or multiple data rates with a performance compromise). Table 4-8 shows some typical filter values. Other filter configurations and values are possible, these result in good general performance.

While the controller and data separator support both FM and MFM encoding, the filter switch circuitry only supports the IBM standard MFM data rates. To provide both FM and MFM filters external logic may be necessary.

4.0 Functional Description (Continued)

The controller takes best advantage of the internal data separator by implementing a sophisticated ID search algorithm. This algorithm, shown in *Figure 4,* enhances the PLL's lock characteristics by forcing the PLL to relock to the crystal any time the data separator attempts to lock to a non-preamble pattern. This algorithm ensures that the PLL is not thrown way out of lock by write splices or bad data fields.

TABLE 4-8. Typical Filter Values for the Various Data Rates (Assuming ±6% Capture Range)

Data Rate (MFM b/s)	C_2	R_2	C_1	R_1
Filter Values when Using All 3 Data Rates				
1.0M 500k 250/300k	C_{2C} = 0.012 µF C_{2B} = 0.015 µF C_{2A} = 0.033 µF	560Ω	510 pF	5.6 kΩ
Filter Values when Using 250/300 and 500 kb/s				
500k 250/300k	C_{2B} = 0.027 µF C_{2A} = 0.047 µF	560Ω 560Ω	1000 pF	5.6 kΩ
Filter Using Only One Data Rate				
1.0M	C_2 = 0.012 µF	560Ω	510 pF	5.6 kΩ
500k	C_2 = 0.027 µF	560Ω	1000 pF	5.6 kΩ
300/250k	C_2 = 0.047 µF	560Ω	2000 pF	5.6 kΩ

(These values are preliminary and thus are subject to change.)

TABLE 4-9. Data Rates (MFM) versus VCO Divide-By Factor

Data Rate	N
1 Mb/s	4
500 kb/s	8
300 kb/s	16
250 kb/s	16

PLL DIAGNOSTIC MODES

In addition, the FDC has two diagnostic modes to enable filter optimization, 1) enabling the Charge Pump output signal onto the PUMP/PREN pin, and 2) providing external control of the Read Gate signal to the data separator. Both modes are enabled in the last byte of the Mode Command.

The Pump output signal indicates when the charge pump is making a phase correction, and hence whether the loop is locked or not.

The Read Gate function, when enabled, allows the designer to manually force the data separator to lock to the incoming data or back to the reference clock. This enables easy verification of the lock characteristics of the PLL, by monitoring the FILTER pin, and the Pump signal.

PLL FILTER DESIGN

This section provides information to enable design of the data separator's external filter and charge pump set resistor. This discussion is for a single data rate filter, and can be easily extrapolated to the other filters of *Figure 3.* Table 4-8 shows some typical filter component values, but if a custom filter is desired, the following parameters must be considered:

R_1: Charge pump current setting resistor. The current set by this resistor is multiplied by the charge pump gain, K_P which is ~2.5. Thus the charge pump current is:

I_{PUMP} = (2.5) 1.2V/R_1. R_1 should be set to between 3–12 kΩ. This resistor determines the gain of the phase detector, which is $K_D = I_{PUMP}/2\pi$.

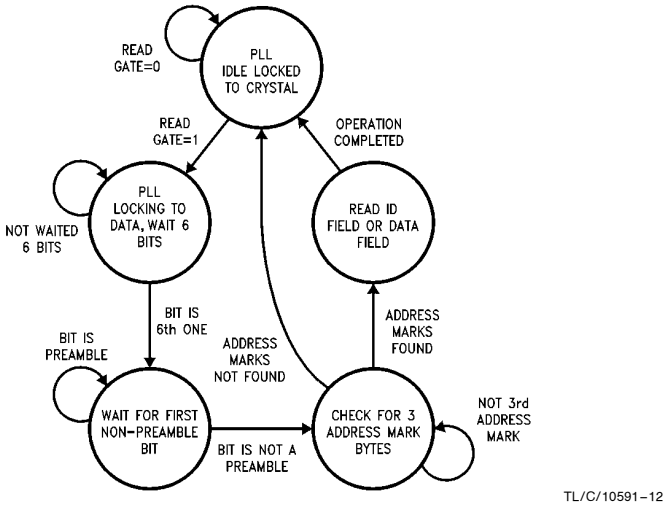


FIGURE 4. Read Algorithm-State Diagram for Data

4.0 Functional Description (Continued)

C_2: Filter capacitor in series with R_2. With pump current this determines loop bandwidth.

R_2: Filter resistor. Determines the PLL damping factor.

C_1: This filter capacitor improves the performance of the PLL by providing additional filtering of bit jitter and noise.

K_{VCO}: The ratio of the change in the frequency of the VCO output due to a voltage change at the VCO input. $K_{VCO} \approx 25$ Mrad/s/V. The VCO is followed by a divider to achieve the desired frequency for each data rate. VCO center frequency is 4 MHz for data rates of 1 Mb/s, 500 kb/s, and 250 kb/s (MFM), and is 4.8 MHz for 300 kb/s (MFM).

K_{PLL}: This is the gain of the internal PLL circuitry, and is the product of $V_{REF} \times K_{VCO} \times K_P$. This value is specified in the Phase Locked Loop Characteristics table.

ω_n: This is the bandwidth of the PLL, and is given by,

$$\omega_n = \sqrt{\frac{K_{PLL}}{2\pi C_2 N R_1}}$$

where N is the number of VCO cycles between two phase comparisons. The value of N for the various data rates are shown in Table 4-9.

ζ: The damping factor is set to 0.7 to 1.2 and is given by,

$$\zeta = \frac{\omega_n R_2 C_2}{2}$$

The trade off, when choosing filter components is between acquisition time while the PLL is locking and jitter immunity while reading data. To select the proper components for a standard floppy disk application the following procedure can be used:

1. Choose FM or MFM, and data rate. Determine N from Table 4-9. Determine preamble length (MFM = 12). The PLL should lock within ½ the preamble time.

2. Determine loop bandwidth (ω_n) required, and set the charge pump resistor R_1.

3. Calculate C_2 using:

$$C_2 = \frac{K_{PLL}}{2\pi R_1 N \omega_n^2}$$

4. Choose R_2 using:

$$R_2 = \frac{2\zeta}{\omega_n C_2}$$

6. Select C_1 to be about 1/20th of C_2.

The above procedure will yield adequate loop performance. If optimum loop performance is required, or if the nature of the loop performance is very critical, then some additional consideration must be given to choosing ω_n and the damping factor. (For a detailed description on how to choose ω_n and ζ, see: **AN-505 Floppy Disk Data Separator Design Guide for the DP8473).**

WRITE PRECOMPENSATION

The FDC incorporates a single fixed 3-bit shift register. This shift register outputs are tapped and multiplexed onto the write data output. The taps are selected by a standard precompensation algorithm. This precompensation value can be selected from the PUMP/PREN pin. When this pin is low 125 ns precomp is used for all data rates except 1 Mb/s which uses 83 ns. When PREN is tied high, the precompensation-value scales with data rate at 250 kb/s its 250 ns, for 300 kb/s its 208 ns, at 500 kb/s its 125 ns, and at 1.0 Mb/s its 83 ns. These values are shown in Table 4-13.

PC-AT AND PC-XT LOGIC BLOCKS

This section describes the major functional blocks of the PC logic that have been integrated on the controller. Refer back to the block diagram 1.2.

DMA Enable Logic: This is gating logic that disables the DMA lines and the Interrupt output, under the control of the DMA Enable bit in the Drive control register. When the DMA Enable bit is 0 then the INT, and DRQ are held TRI-STATE, and $\overline{DAK}$ is disabled.

Drive Output Buffers/Input Receivers: The drive interface output pins can drive 150Ω ±10% termination resistors. This enables connection to a standard floppy drive. All drive interface inputs are TTL compatible schmitt trigger inputs with typically 250 mV of hysteresis. *The MTR2 and 3, and DR2 and 3 pins have been removed in order to accommodate the 100 pin package.*

Bus Interface-Address Decode: The address decode circuit allows software access to the controller, Drive Control Register, and Data Rate Register (see Table 4-10 for the memory map) using the same address map as is used in the XT, AT, or PS/2. The decoding is provided for A0–A2, so only a single address decoder connected to the chip select is needed to complete the decode. The bus interface logic includes the 8-bit data bus and DRQ/INT signals. The output drive for these pins is 24 mA.

TABLE 4-10. Address Memory Map for DP8473

I/O Addr.	A2	A1	A0	R/W	Register
03F0	0	0	0	X	None (Bus TRI-STATE)
03F1	0	0	1	X	None (Bus TRI-STATE)
03F2	**0**	**1**	**0**	**W**	**Drive Control (DCR)**
03F3	0	1	1	X	None (Bus TRI-STATE)
03F4	**1**	**0**	**0**	**R**	**Main Status (MSR)**
03F5	**1**	**0**	**1**	**R/W**	**Data (DR)**
03F6	1	1	0	X	None (Bus TRI-STATE)
03F7	**1**	**1**	**1**	**W**	**Data Rate (DRR)**
03F7	**1**	**1**	**1**	**R**	**Disk Changed Bit (DKR)***

*When this location is accessed only bit D7 is driving, all others are held in TRI-STATE.

Drive Control Register: This 8-bit write only register controls the drive selects, motor enables, DMA enable, and Reset. See Register Description.

Reset Logic: The reset input pin is active high, and directly feeds the Drive Control Register and the Data Rate Register. After a hardware reset the Drive Control Register is reset to all zeros, and the Data Rate Register is set to 250 kb/s data rate. The controller is held reset until the software sets the Drive Control reset bit, after which the controller may be initialized. A software reset to the controller core can be issued by resetting then setting this bit. A software reset does not reset the Drive Control Register, or the Data Rate Register.

Data Rate Register and Clock Logic: This is a two bit register that controls the data rate that the controller uses. See Register Description. This register feeds logic that selects the data rates by programming a prescaler that divides the crystal or clock input by either 3, 5, or 6. This causes

4.0 Functional Description (Continued)

either 4 MHz, 4.8 MHz and 8 MHz to be input as the master clock for the controller core. If the Drive Type pin is high and a 300 kb/s data rate is chosen, 4.8 MHz is used to generate 300 kb/s, but when the DRVTYP pin is low and 300 kb/s is selected, 4 MHz is used, and the actual data rate is 250 kb/s. See Table 4-12.

Low Power Mode Logic: This logic is an enhancement over the standard XT, AT, PS/2 design. In the Low Power Mode the crystal oscillator, the FDC, both UARTs, and all linear circuitry are turned off. The internal FDC circuitry is disabled while the oscillator is off because the internal circuitry is driven from this clock. The oscillator will turn back on automatically after it detects a read or a write to the Main Status or Data Registers. It may take a few milli-seconds for the oscillator to stabilize and the μP will be prevented from trying to access the Data Register during this time through the normal Main Status Register protocol. (The Request for Master bit in the Main Status Register will be inactive.) During the oscillator stabilization period the software should poll the Main Status Register until the Request for Master bit is set. The low power mode is programmed through the Mode Command.

The Data Rate Register and the Drive Control Register are unaffected by the power down mode. They will remain active. It is up to the user to ensure that the Motor and Drive select signal are turned off. The ESDI interface will be inactive. All of the registers will remain unchanged.

The UART registers are unaffected by the power down mode, however their serial data sections will be inoperative. The parallel port, address decoder and configuration register are unaffected by the power down mode.

Note: In addition to the manual low power mode, an automatic low power mode is incorporated on this part. This automatic low power mode is unsupported by NSC and we recommend that it not be used, because it may result in lost data during UART operation.

TABLE 4-11. Truth Table for Drive Control Register (Configuration Register Bit 7 = 0)

D7	D6	D5	D4	D1	D0	Function
X	X	X	1	0	0	Drive 0 Selected (DR0 = 0)
X	X	1	X	0	1	Drive 1 Selected (DR1 = 0)
X	1	X	X	1	0	Not Available
1	X	X	X	1	1	Not Available

Crystal Oscillator: The FDC is clocked by a single 24 MHz signal. An on-chip oscillator is provided, to enable the attachment of a crystal, or a clock. If a crystal is used, a 24 MHz fundamental mode, parallel resonant crystal should be used. This crystal should be specified to have less than 50Ω series resistance, and shunt capacitance of less than 7 pF.

If an external oscillator circuit is used, it must have a duty cycle of 40–60%, and minimum input levels of 2.4V and 0.4V. The controller should be configured so that the clock is input into the OSC2 pin, and OSC1 is tied to ground.

Crystal: SaRonix: SRX 3164

TABLE 4-12. Summary of FDC Registers

Bits / Register	7	6	5	4	3	2	1	0
DCR (W)	MTR3 Enable	MTR2 Enable	MTR1 Enable	MTR0 Enable	DMA Enable	Software Reset	Drive Select 1	Drive Select 0
MSR (R)	Request for Master	Expected Data Direction	Non-DMA Execution	Command in Progress	Drive 3 Seeking	Drive 2 Seeking	Drive 1 Seeking	Drive 0 Seeking
DR (R/W)	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
DRR (W)	X	X	X	X	X	X	Data Rate Bit 1	Data Rate Bit 0
DKR (R)	DSKCHG Pin Inverse	Z	Z	Z	Z	Z	Z	Z
ST0	Data IRQ6 Code	Data IRQ6 Code	Seek End	No Track 0	0	Head Addr	DRV 1 (Exec.)	DRV 0 (Exec.)
ST1	EOT Bit No TC	0	CRC Error	Data Overrun	0	No Data	WRT PRT	Missing Address Mark
ST2	0	Control Mark	CRC Error in Data Fld	WRG Track #	Scan Equal Hit	Scan Not Satisfied	Bad Track	Missing Address Mark in Data Fld
ST3	0	Write Protect Status	1	Track 0 Status	0	Head Select Status	DRV 1 (Exec.)	DRV 0 (Exec.)

4.0 Functional Description (Continued)

4.4.3 Register Description

This section describes the register bits for all the registers that are directly accessible to the μP. Table 4-10 shows the memory map for these registers. Note that in the PC some of the registers are partially decoded, this is not the case here. All registers occupy only their documented addresses.

MAIN STATUS REGISTER (Read Only)

The read only Main Status Register indicates the current status of the disk controller. The Main Status Register is always available to be read. One of its functions is to control the flow of data to and from the Data Register. The Main Status Register indicates when the disk contoller is ready to send or receive data. It should be read before each byte is transferred to or from the Data Register except during a DMA transfer. No delay is required when reading this register after a data transfer.

D7 Request for Master: Indicates that the Data Register is ready to send or receive data from the μP. This bit is cleared immediately after a byte transfer and will become set again as soon as the disk controller is ready for the next byte.

D6 Data Direction: Indicates whether the controller is expecting a byte to be written to (0) or read from (1) the Data Register.

D5 Non-DMA Execution: Bit is set only during the Execution Phase of a command if it is in the non-DMA mode. In other words, if this bit is set, the multiple byte data transfer (in the Execution Phase) must be monitored by the μP either through interrupts, or software polling as described in the Processor Software Interface section.

D4 Command in Progress: Bit is set after the first byte of the Command Phase is written. Bit is cleared after the last byte of the Result Phase is read. If there is no result phase in a command, the bit is cleared after the last byte of the Command Phase is written.

D3 Drive 3 Seeking: Set after the last byte of the Command Phase of a Seek or Recalibrate command is issued for drive 3. Cleared after reading the first byte in the Result Phase of the Sense Interrupt Command for this drive.

D2 Drive 2 Seeking: Same as above for drive 2.

D1 Drive 1 Seeking: Same as above for drive 1.

D0 Drive 0 Seeking: Same as above for drive 0.

DATA REGISTER (Read/Write)

This is the location through which all commands, data and status flow between the CPU and the FDC. During the Command Phase the μP loads the controller's commands into this register based on the Status Register Request for Master and Data Direction bits. The Result Phase transfers the Status Registers and header information to the μP in the same fashion.

DRIVE CONTROL REGISTER (Write Only)

D7 Motor Enable 3: This controls the Motor for drive 3, MTR3. When 0 the output is inactive, when 1 the output is active. (Note this signal is not output to a pin.) This bit and DCR bit 6 provide information that controls the MTR1 and 0 pins, respectively when bit 7 of the Configuration Register is set. See Tables 4-2 and 4-11.

D6 Motor Enable 2: Same function as D7 except for drive 2's motor. (Note this signal is not brought out to a pin.)

D5 Motor Enable 1: This bit controls the Motor for drive 1's motor. When this bit is 0 the MTR1 output is high.

D4 Motor Enable 0: Same as D5 except for drive 0's motor.

D3 DMA Enable: When set to a 1 this enables the DRQ, DAK, INT pins. A zero disables these signals.

D2 Reset Controller: This bit when set to a 0 resets the controller, and when a 1 enables normal operation. It does not affect the Drive Control or Data Rate Registers which are reset only by a hardware reset.

D1–D0 Drive Select: These two pins are encoded for the four drive selects, and are gated with the motor enable lines, so that only one drive is selected when it's Motor Enable is active. (See Table 4-11.)

DATA RATE REGISTER (Write Only)

D7–D2: Not used.

D1, D0 Data Rate Select: These bits set the data rate and the write precompensation values for the disk controller. After a hardware reset these bits are set to 10 (250 kb/s). They are encoded as shown in Table 4-13.

DISK CHANGED REGISTER (Read Only)

D7 Disk Changed: This bit is the latched complement of the Disk Changed input pin. If the DSKCHG input is low this bit is high.

TABLE 4-13. Data Rate and Precompensation Programming Values

D1	D0**	DRVTYP Pin	Data Rate MFM (kb/s)	Normal Precomp* (ns)	Alternate Precomp* (ns)	FGND Pin Enabled	RPM/LC Pin Level
0	0	X	500	125	125	FGND500	High
0	1	0	250	125	250	FGND250	Low
0	1	1	300	208	208	FGND250	Low
1	0	0	250	125	250	FGND250	Low
1	0	1	250	125	250	FGND250	Low
1	1	0	1000	83	83	None	High
1	1	1	1000	83	83	None	Low

*Normal values when PUMP/PREN pin set low; Alternate values when PUMP/PREN pin set high.

**D0 and D1 are Data Rate Control Bits.

4.0 Functional Description (Continued)

D6–D0: These bits are reserved for use by the hard disk controller, thus during a read of this register, these bits are TRI-STATE.

4.4.4 Result Phase Status Registers

The Result Phase of a command contains bytes that hold status information. The format of these bytes are described below. Do not confuse these register bytes with the Main Status Register which is a read only register that is always available. The Result Phase status registers are read from the Data Register only during the Result Phase.

STATUS REGISTER 0 (ST0)

D7–D6 Interrupt Code:

00 = Normal Termination of Command.

01 = Abnormal Termination of Command. Execution of Command was started, but was not successfully completed.

10 = Invalid Command Issue. Command Issued was not recognized as a valid command.

11 = Ready changed state during the polling mode.

D5 Seek End: This bit is set after a Seek or Recalibrate Command is completed by the Controller. (Used during Sense Interrupt command.)

D4 Equipment Check: This bit is set if a Recalibrate Command or a Track 0 signal failed to occur. (Used during Sense Interrupt command.)

D3 Not Used: 0

D2 Head Number: (at end of Execution Phase).

D1, D0 Drive Select: (at end of Execution Phase).

00 = Drive 0 selected. 01 = Drive 1 selected.

10 = Drive 2 selected. 11 = Drive 3 selected.

STATUS REGISTER 1 (ST1)

D7 End of Track: This bit is set when the controller transferred the last byte of the last sector without the TC pin becoming active. The last sector is the End Of Track sector number programmed in the Command Phase.

D6 Not Used: 0

D5 CRC Error: If this bit is set and bit 5 of ST2 is clear, then there was a CRC error in the Address Field of the correct sector. If bit 5 of ST2 is set, then there was a CRC error in the Data Field.

D4 Over Run: This bit is set when the controller was not serviced by the μP soon enough during a data transfer in the Execution Phase.

TABLE 4-14. Maximum Time Allowed to Service an Interrupt or Acknowledge a DMA Request in Execution Phase

Data Rate	Time to Service
125	62.0 μs
250	30.0 μs
500	14.0 μs
1000	6.0 μs

Time from rising edge of DRQ or INT to trailing edge of $\overline{DAK}$ or $\overline{RD}$ or $\overline{WR}$.

D3 Not Used: 0

D2 No Data: This bit is set for any of three possible problems: 1) Controller cannot find the sector specified in the Command Phase during the execution of a Read, Write, or Scan command. An address mark was found however so it is not a blank disk. 2) Controller cannot read any Address Fields without a CRC error during Read ID command. 3) Controller cannot find starting sector during execution of Read A Track command.

D1 Not Writable: This bit is set if the Write Protect pin is active when a Write or Format command is issued.

D0 Missing Address Mark: If this bit is set and if bit 0 of ST2 is clear then the disk controller cannot detect any Address Field Address Mark after two disk revolutions. If bit 0 of ST2 is set then the disk controller cannot detect the Data Field Address Mark.

STATUS REGISTER 2 (ST2)

D7 Not Used: 0

D6 Control Mark: This bit is set if the controller tried to read a sector which contained a deleted data address mark during execution of Read Data or Scan commands. Or, if a Read Deleted Data command was executed, a regular address mark was detected.

D5 CRC Error in Data Field: This bit is set if the controller detected a CRC error in the Data Field. Bit 5 of ST1 is also set.

D4 Wrong Track: This bit is only set if the desired sector is not found, and the track number recorded on any sector of the current track is different from that stored in the Track Register.

D3 Scan Equal Hit: This bit is set if the ''Equal'' condition satisfied during any Scan Command.

D2 Scan Not Satisfied: This bit is set if the controller cannot find a sector on the track which meets the desired condition during Scan Command.

D1 Bad Track: This bit is only set if the desired sector is not found, and the track number recorded on any sector on the track is different from that stored in the Track Register and the recorded track number is FF.

D0 Missing Address Mark in Data Field: This bit is set if the controller cannot find the Data Field Address Mark during Read/Scan command. Bit 0 of ST1 is also set.

STATUS REGISTER 3 (ST3)

D7 Not Used: 0

D6 Write Protect Status: This bit is the complement of the associated FDC interface pin for the drive selected in the DCR.

D5 Not Used: 1

D4 Track 0 Status: This bit is the complement of the associated FDC interface pin for the drive selected in the DCR.

D3 Not Used: 0

D2 Head Select Status: This bit shows the status of the associated bit in the Sense Drive Status Command Phase.

D1, D0 Drive Selected (at end of Execution Phase): These bits show the status of the associated bits in the Sense Drive Status Command Phase. These bits show the same status as ST0 bits 1, 0.

00 = Drive 0 selected. 01 = Drive 1 selected.

10 = Drive 2 selected. 11 = Drive 3 selected.

4.0 Functional Description (Continued)

4.4.5 Processor Software Interface

Bytes are transferred to and from the disk controller in different ways for the different phases in a command.

COMMAND SEQUENCE

The disk controller can perform various disk transfer, and head movement commands. Most commands involve three separate phases.

Command Phase: The μP writes a series of bytes to the Data Register. These bytes indicate the command desired and the particular parameters required for the command. All the bytes must be written in the order specified in the Command Description Table. The Execution Phase starts immediately after the last byte in the Command Phase is written. Prior to performing the Command Phase, the Drive Control and Data Rate Registers should be set.

Execution Phase: The disk controller performs the desired command. Some commands require the μP to read or write data to or from the Data Register during this time. Reading data from a disk is an example of this.

Result Phase: The μP reads a series of bytes from the data register. These bytes indicate whether the command executed properly and other pertinent information. The bytes are read in the order specified in the Command Description Table.

A new command may be initiated by writing the Command Phase bytes after the last bytes required from the Result Phase have been read. If the next command requires selecting a different drive or changing the data rate the Drive Control and Data Rate Registers should be updated. If the command is the last command, then the software should deselect the drive. *(Note as a general rule the operation of the controller core is independent of how the μP updates the Drive Control and Data Rate Registers. The software must ensure that manipulation of these registers is coordinated with the controller operation.)*

During the Command Phase and the Result Phase, bytes are transferred to and from the Data Register. The Main Status Register is monitored by the software to determine when a data transfer can take place. Bit 6 of the Main Status Register must be clear and bit 7 must be set before a byte can be written to the Data Register during the Command Phase. Bits 6 and 7 of the Main Status Register must both be set before a byte can be read from the Data Register during the Result Phase.

If there is information to be transferred during the Execution Phase, there are three methods that can be used. The DMA mode is used if the system has a DMA controller. This allows the μP to do other things during the Execution Phase data transfer. If DMA is not used, an interrupt can be issued for each byte transferred during the Execution Phase. If interrupts are not used, the Main Status Register can be polled to indicate when a byte transfer is required.

DMA MODE

If the DMA mode is selected, a DMA request will be generated in the Execution Phase when each byte is ready to be transferred. To enable DMA operations during the Execution Phase, the DMA mode bit in the Specify Command must be enabled, and the DMA signals must be enabled in the Drive Control Register. The DMA controller should respond to the DMA request with a DMA acknowledge and a read or write strobe. The DMA request will be cleared by the active edge of the DMA acknowledge. After the last byte is transferred, an interrupt is generated, indicating the beginning of the Result Phase. During DMA operations the Chip Select input must be held high. TC is asserted to terminate an operation. Due to the internal gating TC is only recognized when the $\overline{DAK}$ input is low.

INTERRUPT MODE

If the non-DMA mode is selected, an interrupt will be generated in the Execution Phase when each byte is ready to be transferred. The Main Status Register should be read to verify that the interrupt is for a data transfer. Bits 5 and 7 of the Main Status Register will be set. The interrupt will be cleared when the byte is transferred to or from the Data Register. The μP should transfer the byte within the time allotted by Table 4-14. If the byte is not transferred within the time allotted, an Overrun Error will be indicated in the Result Phase when the command terminates at the end of the current sector.

An interrupt will also be generated after the last byte is transferred. This indicates the beginning of the Result Phase. Bits 7 and 6 of the Main Status Register will be set and bit 5 will be clear. This interrupt will be cleared by reading the first byte in the Result Phase.

Interrupt Type	Reg. Bits =	μP Clearing Action
Result Phase Start	MSR7, 6, 5 = 1, 1, 0	Read 1 status byte from the Data Register (Result)
Data Write	MSR7, 6, 5 = 1, 0, 1	Write 1 data byte to the Data Register (Execution)
Data Read	MSR7, 6, 5 = 1, 1, 1	Read 1 data byte from the Data Register (Execution)
Reset (Note)	MSR7, 6, 5 = 1, 0, 0	Issue a Sense Interrupt command after reset
Seek (Note)	MSR7, 6, 5 = 1, 0, 0	Issue a Sense Interrupt command after a Seek
Recalibrate (Note)	MSR7, 6, 5 = 1, 0, 0	Issue a Sense Interrupt command after a Recalibrate

Note: These 3 interrupts are identified by reading Status Register 0 after issuing a sense-interrupt command.

4.0 Functional Description (Continued)

SOFTWARE POLLING

If the non-DMA mode is selected and interrupts are not suitable, the μP can poll the Main Status Register during the Execution Phase to determine when a byte is ready to be transferred. In the non-DMA mode, bit 7 of the Main Status Register reflects the state of the interrupt pin. Otherwise, the data transfer is similar to the Interrupt Mode described above.

4.4.6 Command Description Table

See Section 4.4.7 for a detailed description of each command.

Note: Mnemonic Definitions

DRn = Drive to Select (encoded)
ETR = Extended Track Range
HD = Head Number
IAF = Index Address Field
IPS = Implied Seek (In individual commands this bit is a don't care unless the IPS bit in the mode command is set.)
LW PR = Low Power Mode
MFM = Data Encoding Scheme
MSB = Selects whether the most significant or least significant byte of the track is read. 1 = MSB.
MSN PTN = Most Significant Nibble Present Track Number
MT = Multi-Track
PU = Enables Charge Pump PUMP signal to be output on the PUMP/PREN pin.
RG = Enables the Read Gate Input on the DSKCHG pin for the Data Separator. (Write = 1).
$\overline{R}$/W = Selects whether the track is written or read (Read = 0).
SK = Skip Sector
TMR = Motor/Head Timer Mode
WLD = Wildcard in Scan
X = DON'T CARE

READ DATA

From specified sectors in logical order on a track (optional Implied Seek)

Command Phase

MT	MFM	SK	0	0	1	1	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Number of Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Note 1

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

READ ID

From the first address field that is found

Command Phase

0	MFM	0	0	1	0	1	0
X	X	X	X	X	HD	DR1	DR0

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

FORMAT A TRACK

Write header and data patterns to the specified track

Command Phase

0	MFM	0	0	1	1	0	1
X	X	X	X	X	HD	DR1	DR0
Number of Bytes per Sector							
Number of Sectors per Track							
Intersector Gap Length							
Data Pattern							

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

4.0 Functional Description (Continued)

READ DELETED DATA

Based on the specified address and the deleted data mark

Command Phase

MT	MFM	SK	0	1	1	0	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Number of Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

WRITE DATA

To specified sectors in logical order on a track (optional Implied Seek)

Command Phase

MT	MFM	0	0	0	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Number of Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

SCAN EQUAL

Compare on a byte-by-byte basis the μP and disk data from the specified sector, match on $=$

Command Phase

MT	MFM	SK	1	0	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Number of Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

READ A TRACK

Read all sectors on the specified track in physical order

Command Phase

0	MFM	SK	0	0	0	1	0
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Number of Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

WRITE DELETED DATA

Based on the address and the Deleted Data Mark

Command Phase

MT	MFM	0	0	1	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Number of Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Data Length							

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

SCAN LOW OR EQUAL

Compare on a byte-by-byte basis the μP and disk data from the specified sector, match on $<=$

Command Phase

MT	MFM	SK	1	1	0	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Number of Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

4.0 Functional Description (Continued)

SCAN HIGH OR EQUAL

Compare on a byte-by-byte basis the μP and disk data from the specified sector, match on $>=$

Command Phase

MT	MFM	SK	1	1	1	0	1
IPS	X	X	X	X	HD	DR1	DR0
Track Number							
Drive Head Number							
Sector Number							
Number of Bytes per Sector							
End of Track Sector Number							
Intersector Gap Length							
Sector Step Size							

Result Phase

Status Register 0
Status Register 1
Status Register 2
Track Number
Head Number
Sector Number
Bytes/Sector

SENSE DRIVE STATUS

Read the ready status of the specified drive

Command Phase

0	0	0	0	0	1	0	0
X	X	X	X	X	HD	DR1	DR0

Result Phase

Status Register 3

SPECIFY

The step, head load, and unload times

Command Phase

0	0	0	0	0	0	1	1
Step Rate Time				Motor Off Time			
Motor On Time							DMA

SEEK

The specified track by reading the address field and stepping the head

Command Phase

0	0	0	0	1	1	1	1
X	X	X	X	X	X	DR1	DR0
New Track Number							
MSB of Track				0	0	0	0

Note 2

MODE

Select various controller options (e.g., motor timer, low power, implied seek, etc.)

Command Phase

0	0	0	0	0	0	0	1
TMR	IAF	IPS	0	LW	PR	1	ETR
0	0	0	0	0	0	0	0
1	1	0	WLD	Head Settle			
0	0	0	0	0	RG	0	PU

Note 3

RECALIBRATE

Move the head to Track 0 (max. steps 77, extd. 3917)

Command Phase

0	0	0	0	0	1	1	1
0	0	0	0	0	0	DR1	DR0

SET TRACK

Set the current track register to the most recent track read

Command Phase

0	$\overline{R}$/W	1	0	0	0	0	1
0	0	1	1	0	MSB	DR1	DR0
New Track Number							

Result Phase

Value

Note 3

SENSE INTERRUPT

Read the interrupt status

Command Phase

0	0	0	0	1	0	0	0

Result Phase

Status Register 0				
Present Track Number (PTN)				
MSN PTN	0	0	0	0

Note 2

INVALID COMMAND

Has been specified

Command Phase

Invalid Op Codes

Result Phase

Status Register 0

Note 1: The IPS bit is only enabled if the IPS bit in the mode command is set. Otherwise this bit is a don't care.

Note 2: Shaded byte only written or read if the extended track range mode is enabled in the Mode Command (ET) = 1.

Note 3: These commands are additional enhanced commands.

4.0 Functional Description (Continued)

4.4.7 Command Descriptions

READ DATA

The Read Data op-code is written to the data register followed by 8 bytes as specified in the Command Description Table. After the last byte is written, the controller starts looking for the correct sector header. Once the sector is found the controller sends the data to the μP. After one sector is finished, the Sector Number is incremented by one and this new sector is searched for. If MT (Multi-Track) is set, both sides of one track can be read. Starting on side zero, the sectors are read until the sector number specified by End of Track Sector Number is reached. Then, side one is read starting with sector number one.

In DMA mode the Read Data command continues to read until the TC pin is set. This means that the DMA controller should be programmed to transfer the correct number of bytes. TC could be controlled by the μP and be asserted when enough bytes are received. An alternative to these methods of stopping the Read Data command is to program the End of Track Sector Number to be the last sector number that needs to be read. The controller will stop reading the disk with an error indicating that it tried to access a sector number beyond the end of the track.

The Number of Data Bytes per Sector parameter is defined in Table 4-15. If this is set to zero then the Data Length parameter determines the number of bytes that the controller transfers to the μP. If the data length specified is smaller than 128 the controller still reads the entire 128 byte sector and checks the CRC, though only the number of bytes specified by the Data Length parameter are transferred to the μP. Data Length should not be set to zero. If the Number of Bytes per Sector parameter is not zero, the Data Length parameter has no meaning and should be set to FF (hex).

If the Implied Seek Mode is enabled by both the Mode command and the IPS bit in this command, a Seek will be performed to the track number specified in the Command Phase. The controller will also wait the Head Settle time if the implied seek is enabled.

After all these conditions are met, the controller searches for the specified sector by comparing the track number, head number, sector number, and number bytes/sector given in the Command Phase with the appropriate bytes read off the disk in the Address Fields.

If the correct sector is found, but there is a CRC error in the Address Field, bit 5 of ST1 (CRC Error) is set and an abnormal termination is indicated. If the correct sector is not found, bit 2 of ST1 (No Data) is set and an abnormal termination is indicated. In addition to this, if any Address Field track number is FF, bit 1 of ST2 (Bad Track) is set or if any Address Field track number is different from that specified in the Command Phase, bit 4 of ST2 (Wrong Track) is set.

After finding the correct sector, the controller reads that Data Field. If a Deleted Data Mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (Control Mark) is set, and the next sector is searched for. If a deleted data mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (Control Mark) is set, and the read terminates with a normal termination. If a CRC error is detected in the Data Field, bit 5 is set in both ST1 and ST2 (CRC Error) and an abnormal termination is indicated.

If no problems occur in the read command, the read will continue from one sector to the next in logical order (not physical order) until either TC is set or an error occurs.

If a disk has not been inserted into the disk drive, there are many opportunities for the controller to appear to hang up. It does this if it is waiting for a certain number of disk revolutions for something. If this occurs, the controller can be forced to abort the command by writing a byte to the Data register. This will place the controller into the Result Phase for the current command that is being executed. The software should, then execute the Result Phase activity (i.e., for the Read Data Command it should read 7 status bytes).

TABLE 4-15. Sector Size Selection

Bytes/Sector Code	Number of Bytes in Data Field
0	128
1	256
2	512
3	1024
4	2048
5	4096
6	8192

An interrupt will be generated when the Execution Phase of the Read Data command terminates. The values that will be read back in the Result Phase are shown in Table 4-16. If an error occurs, the result bytes will indicate the sector being read when the error occurred.

READ DELETED DATA

This command is the same as the Read Data command except for its treatment of a Deleted Data Mark. If a Deleted Data Mark is read, the sector is read normally. If a Regular Data Mark is found and the SK bit is set, the sector is not read, bit 6 of ST2 (Control Mark) is set, and the next sector is searched for. If a Regular Data Mark is found and the SK bit is not set, the sector is read, bit 6 of ST2 (Control Mark) is set, and the read terminates with a normal termination.

4.0 Functional Description (Continued)

TABLE 4-16. Result Phase Termination Values with No Error

MT	HD	Last Sector	ID Information at Result Phase			
			Track	Head	Sector	B/S
0	0	< EOT	NC	NC	S+1	NC
0	0	= EOT	T+1	NC	1	NC
0	1	< EOT	NC	NC	S+1	NC
0	1	= EOT	T+1	NC	1	NC
1	0	< EOT	NC	NC	S+1	NC
1	0	= EOT	NC	1	1	NC
1	1	< EOT	NC	NC	S+1	NC
1	1	= EOT	T+1	0	1	NC

EOT = End of Track Sector Number from Command Phase

NC = No Change in Value

S = Sector Number last operated on by controller

T = Track Number programmed in Command Phase

WRITE DATA

The Write Data command is very similar to the Read Data command except that data is transferred from the μP to the disk rather than the other way around. If the controller detects the Write Protect signal, bit 1 of ST1 (Not Writable) is set and an abnormal termination is indicated.

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Mark is written at the beginning of the Data Field instead of the normal Data Mark.

READ A TRACK

This command is similar to the Read Data command except for the following. The controller starts at the index hole and reads the sectors in their physical order, not their logical order.

Even though the controller is reading sectors in their physical order, it will still perform a comparison of the header ID bytes with the Data programmed in the Command Phase. The exception to this is the sector number. Internally, this is initialized to a one, and then incremented for each successive sector read. Whether or not the programmed Address Field matches that read from the disk, the sectors are still read in their physical order. If a header ID comparison fails, bit 2 of ST1 (No Data) is set, but the operation will continue. If there is a CRC error in the Address Field or the Data Field, the read will also continue.

The command will terminate when it has read the number of sectors programmed in the EOT parameter.

READ ID

This command will cause the controller to read the first Address Field that it finds. The Result Phase will contain the header bytes that are read. There is no data transfer during the Execution Phase of this command. An interrupt will be generated when the Execution Phase is completed.

FORMAT A TRACK

This command will format one track on the disk. After the index hole is detected, data patterns are written on the disk including all gaps, address marks, Address Fields, and Data Fields. The exact details of the number of bytes for each field is controlled by the parameters given in the Format A Track command, and the IAF (Index Address Field) bit in the Mode command. The Data Field consists of the Fill Byte specified in the command, repeated to fill the entire sector.

To allow for flexible formatting, the μP must supply the four Address Field bytes (track, head, sector, number of bytes) for each sector formatted during the Execution Phase. In other words, as the controller formats each sector, it will request four bytes through either DMA requests or interrupts. This allows for non-sequential sector interleaving. Some typical values for the programmable GAP size are shown in Table 4-17.

The Format Command terminates when the index hole is detected a second time, at which point an interrupt is generated. Only the first three status bytes in the Result Phase are significant.

TABLE 4-17

Format Table for Sector Size and Data Rate

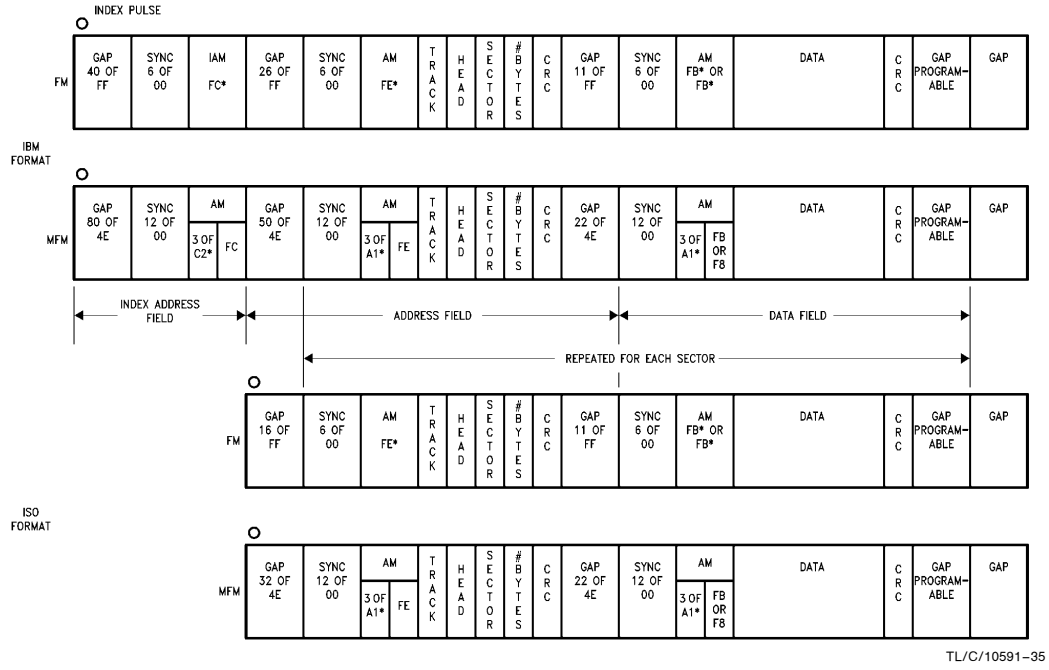
Mode	Sector Size	Sector Code	EOT	Sector Gap	Format Gap
	Decimal	Hex	Hex	Hex	Hex
FM 125 kb/s	128	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM 250 kb/s	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	512	02	09	1B	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
FM 250 kb/s	128	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM 500 kb/s	256	01	1A	0E	36
	512	02	0F	1B	54
	512	02	12	1B	6C
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF

Format Table for PC Compatible Diskette Media

Media Type	Sector Size	Sector Code	EOT	Sector Gap	Format Gap
	Decimal	Hex	Hex	Hex	Hex
360k	512	02	09	2A	50
1.2M	512	02	0F	1B	54
720k	512	02	09	1B	50
1.44M	512	02	12	1B	6C

Note: Format Gap is the gap length used only for the Format command.

4.0 Functional Description (Continued)



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Notes:

FE* = Data pattern of FE, Clock pattern of C7
FC* = Data pattern of FC, Clock pattern of D7
FB* = Data pattern of FB, Clock pattern of C7
F8* = Data pattern of F8, Clock pattern of C7
A1* = Data pattern of A1, Clock pattern of 0A
C2* = Data pattern of C2, Clock pattern of 14

All byte counts in decimal.

All byte values in hex.

CRC uses standard polynomial $x^{16} + x^{12} + x^5 + 1$.

FIGURE 5. IBM and ISO Formats Supported by the Format Command

SCAN COMMANDS

The Scan Commands allow data read from the disk to be compared against data sent from the μP on a byte-by-byte basis. There are three Scan Commands to choose from:

Scan Equal	Disk Data = μP Data
Scan Less Than or Equal	Disk Data ≤ μP Data
Scan Greater Than or Equal	Disk Data ≥ μP Data

Each sector is interpreted with the most significant bytes first. If the Wildcard mode is enabled from the Mode command, an FF(hex) from either the disk or the μP is used as a don't care byte that will always match equal. If after each sector is read, the desired condition has not been met, the next sector is read. The next sector is defined as the current sector number plus the Sector Step Size specified. The Scan command will continue until the scan condition has been met, or the End of Track Sector Number has been reached, or if TC is asserted.

If the SK bit is set, sectors with deleted data marks are ignored. If all sectors read are skipped, the command will terminate with D3 of ST2 set (Scan Equal Hit). The result phase of the command is shown in Table 4-18.

TABLE 4-18. Scan Command Termination Values

Command	Status Register 2		Conditions
	D2	D3	
Scan Equal	0	1	Disk = μP
	1	0	Disk ≠ μP
Scan Low or Equal	0	1	Disk = μP
	0	0	Disk < μP
	1	0	Disk > μP
Scan High or Equal	0	1	Disk = μP
	0	0	Disk > μP
	1	0	Disk < μP

4.0 Functional Description (Continued)

SEEK

There are two ways to move the disk drive head to the desired track number. Method One is to enable the Implied Seek Mode. This way each individual Read or Write command will automatically move the head to the track specified in the command.

Method Two is using the Seek Command. During the Execution Phase of the Seek Command, the track number to seek to is compared with the present track number and a step pulse is produced to move the head one track closer to the desired track number. This is repeated at the rate specified by the Specify Command until the head reaches the correct track. At this point an interrupt is generated and a Sense Interrupt Command is required to clear the interrupt.

During the Execution Phase of the Seek Command the only indication via software that a Seek Command is in progress is bits 0–3 (Drive Busy) of the Main Status Register. Bit 4 of the Main Status Register (Command in Progress) is not set. The internal microengine is capable of executing seeks on more than one drive at a time. However, since the active drive is selected by the system software and there is no way to coordinate this selection with the microengine step pulses, only one seek command should be issued by the software at a time. No other command except the Sense Interrupt Command should be issued while a Seek Command is in progress.

If the extended track range mode is enabled, a fourth byte should be written in the Command Phase to indicate the four most significant bits of the desired track number. Otherwise, only three bytes should be written.

RECALIBRATE

The Recalibrate Command is very similar to the Seek Command. It is used to step a drive head out to track zero. Step pulses will be produced until the track zero signal from the drive becomes true. If the track zero signal does not go true before 77 step pulses are issued, an error is generated. If the extended track range mode is enabled, an error is not generated until 3917 pulses are issued.

Recalibrations on more than one drive at a time should not be issued for the same reason as explained in the Seek Command. No other command except the Sense Interrupt Command should be issued while a Recalibrate Command is in progress.

SENSE INTERRUPT STATUS

An interrupt is generated by the controller when any of the following conditions occur:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read Deleted Data Command
   c. Write Data Command
   d. Write Deleted Data Command
   e. Read a Track Command
   f. Read ID Command
   g. Format Command
   h. Scan Commands
2. During data transfers in the Execution Phase while in the Non-DMA mode
3. Internal Ready signal changes state (only occurs immediately after a hardware or software reset).
4. Seek or Recalibrate Command termination

An interrupt generated for reasons 1 and 2 above occurs during normal command operations and are easily discernible by the μP. During an execution phase in Non-DMA Mode, bit 5 (Execution Mode) in the Main Status Register is set to 1. Upon entering Result Phase this bit is set to 0. Reasons 1 and 2 do not require the Sense Interrupt Status command. The interrupt is cleared by reading or writing information to the data register.

Interrupts caused by reasons 3 and 4 are identified with the aid of the Sense Interrupt Status Command. This command resets the interrupt when the command byte is written. Use bits 5, 6 and 7 of ST0 to identify the cause of the interrupt as shown in Table 4-19.

TABLE 4-19. Status Register 0 Termination Codes

Status Register 0			Cause
Interrupt Code		Seek End	
D7	D6	D5	
1	1	0	Internal Ready Went True
0	0	1	Normal Seek Termination
0	1	1	Abnormal Seek Termination

TABLE 4-20. Step, Head Load and Unload Timer Definitions (500 kb/s MFM)

Timer	Mode 1		Mode 2		Unit
	Value	Range	Value	Range	
Step Rate	(16 − N)	1–16	(16 − N)	1–16	ms
Head Unload	N × 16	0–240	N × 512	0–7680	ms
Head Load	N × 2	0–254	N × 32	0–4064	ms

Issuing a Sense Interrupt Status Command without an interrupt pending is treated as an invalid command.

If the extended track range mode is enabled, a third byte should be read in the Result Phase which will indicate the four most significant bits of the Present Track Number. Otherwise, only two bytes should be read.

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The timer programming values are shown in Table 4-20.

The Head Load and Head Unload timers are artifacts of the μPD765A. These timers determine the delay from loading the head until a read or write command is started, and unloading the head sometime after the command was completed. Since the FDC's head load signal is now from the software controlled Motor lines in the Drive Control Register, these timers only provide some delay from the initiation of a command until it is actually started. These times can be extended by setting the TMR bit in the Mode Command.

The Step Rate Time defines the time interval between adjacent step pulses during a Seek, Implied Seek, or Recalibrate Command.

The times stated in the table are affected by the Data Rate. The values in the table are for 500 kb/s MFM (250 kb/s FM) and 1 Mb/s MFM (500 kb/s FM). For a 300 kb/s MFM data

4.0 Functional Description (Continued)

rate (150 kb/s FM) these values should be multiplied by 1.6667, and for 250 kb/s MFM (125 kb/s FM) these values should be doubled.

The choice of DMA or Non-DMA operation is made by the NON-DMA bit. When this bit is 1 then Non-DMA mode is selected, and when this bit is 0, the DMA mode is selected.

This command does not generate an interrupt.

SENSE DRIVE STATUS

This two byte command obtains the status of a disk drive. Status Register 3 is returned in the result phase and contains the drive status. This command does not generate an interrupt.

MODE

This command is used to select the special features of the controller. The bits for the command phase bytes are shown in the command description table, and their function is described below. The defaults after a hardware or software reset are shown by the ''bullets'' to the left of each item.

- **TMR = 0 (motor TiMeR):** Timers for motor on and motor off are defined for Mode 1. (See Specify Command)
  TMR = 1: Timers for motor on and motor off are defined for Mode 2. (See Specify Command)

LW PR (LoW PoweR)

- 00 Disable the low power mode. (default)
  01 Reserved (Do Not Use)
  10 Enable low power mode.
  11 Reserved (Do Not Use)
- **IAF = 0 (Index Address Format):** The controller will format tracks with the Index Address Field included. (IBM Format)

  IAF = 1: The controller will format tracks without including the Index Address Mark Field. (ISO Format)
- **IPS = 0 (ImPlied Seek):** The implied seek bit in the command is ignored.

  IPS = 1: The implied seek bit in the command is enabled so that if the bit is set in the command, a Seek will be performed automatically.
- **ETR = 0 (Extended Track Range):** Header format is the IBM System 34 (double density) or System 3740 (single density).

  ETR = 1: Header format is the same as above but there are 12 bits of track number. The MSB's of the track number are in the upper four bits of the head number byte.
- **WLD = 0 (scan WiLD card):** An FF(hex) from either the μP or the disk during a Scan Command is interpreted as a wildcard character that will always match true.

  WLD = 1: The Scan commands do not recognize FF(hex) as a wildcard character.

  Head Settle: Time allowed for head to settle after an Implied Seek. Time = N $\times$ 4 ms, (0 ms–60 ms). (Based on 500 kb/s and 1 Mb/s MFM data rates. Double for 250 kb/s.)

  PU (PUMP Pulse Output): When set enables a signal that indicates when the Data Separator's charge pump is making a phase correction. This is a series of pulses. This signal is output on the PUMP/PREN pin when this bit is set.

  This is intended as a test mode to aid in evaluation of the Data Separator. (Default mode is off)

  RG (Read Gate): Like the PUMP output, when this bit is set it enables a pin (the DSKCHG pin) to act as an external Read Gate signal for the Data Separator. This is intended as a test mode to aid in evaluation of the Data Separator. (Default mode is off)

SET TRACK

This command is used to inspect or change the value of the internal Present Track Register. This could be useful for recovery from disk mis-tracking errors, where the real current track could be read through the Read ID command and then the Set Track Command can set the internal present track register to the correct value.

The first byte of the command contains the command opcode and the R/W bit. If the R/W bit is low, a track register is to be read. In this case, the result phase contains the value in the internal register specified, and the third byte of the command is a dummy byte.

If the R/W bit is high, data is written to a track register. In this case the 3rd byte of the command phase is forced into the specified internal register, and the result phase contains the new byte value written.

The particular track register chosen to operate on is determined by the least significant 3 bits of the second byte of the command. The two LSB's select the drive (DR1, DR0), and the next bit (MSB) determines whether the least significant byte (MSB = 0) or the most significant byte (MSB = 1) of the track register is to be read/written. When not in the extended track range mode, only the LSB track register need be updated. In this instance, the MSB bit is set to 0.

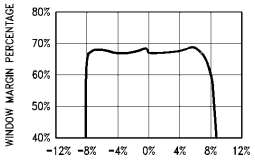
This command does not generate an interrupt.

INVALID COMMAND

If an invalid command (i.e., a command not defined) is received by the controller, the controller will respond with ST0 in the Result Phase. The Controller does not generate an interrupt during this condition. Bits 6 and 7 in the Main Status Register are both set to one's indicating to the processor that the Controller is in the Result Phase and the contents of ST0 must be read. When the system reads ST0 it will find an 80(hex) indicating an invalid command was received.

4.4.8 Typical Performance Characteristics

Typical Window Margin Performance Characteristics at 250 kb/s MFM



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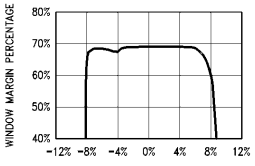
Typical Window Margin Performance Characteristics at 500 kb/s MFM



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4.0 Functional Description (Continued)

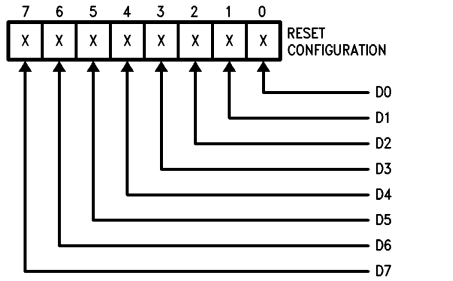
4.5 PARALLEL PORT

This parallel interface is designed to provide all of the signals and registers needed to communicate through a standard parallel printer port as found in the IBM PC, XT, AT, and Centronics systems. The address decoding of the registers utilizing A0 and A1 is shown in Table 4-21. Table 4-22 shows the Reset states of Parallel port registers and pin signals. All bits in the registers are located in the same positions and have the same functions as the registers of the systems listed above. These registers are shown below.

TABLE 4-21. Parallel Interface Register Addresses

$\overline{CSP}$	A1	A0	Address	Register	Read/Write
0	0	0	0	Data	Read/Write
0	0	1	1	Status	Read
0	1	0	2	Control	Read/Write
0	1	1	3	TRI-STATE	—

DATA REGISTER (DTR)



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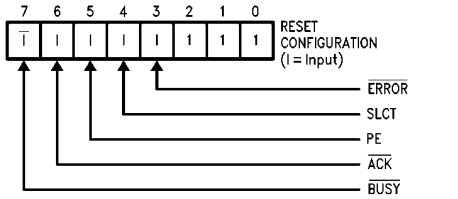
This is a bidirectional data port that transfers 8-bit data in the direction determined by the logic state of $\overline{POE}$ pin and the $\overline{RD}$ and $\overline{WR}$ strobes.

STATUS REGISTER (STR)



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This register provides status for the signals listed below. It is a read only register. Writing to it is an invalid operation that has no effect.

Bits 0, 1, 2: These bits are always 1.

Bit 3: This bit represents the current state of the printer error signal ($\overline{ERROR}$). The printer sets this bit low when there is a printer error. This bit follows the state of the $\overline{ERR}$ pin.

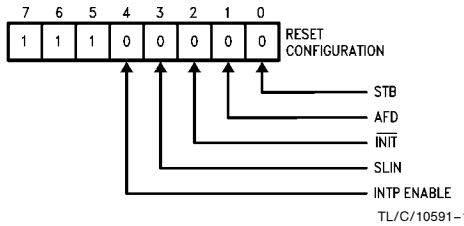
Bit 4: This bit represents the current state of the printer select signal (SLCT). The printer sets this bit high when it is selected. This bit follows the state of the SLCT pin.

Bit 5: This bit represents the current state of the printer paper end signal (PE). The printer sets this bit high when it detects the end of the paper. This bit follows the state of the PE pin.

Bit 6: This bit represents the current state of the printer acknowledge signal ($\overline{ACK}$). The printer sets this signal to low after it has received a character and is ready to receive another one. This bit follows the state of the $\overline{ACK}$ pin.

Bit 7: This bit represents the current state of the printer busy signal (BUSY). The printer sets this bit low when it is busy and cannot accept another character. This bit is the inverse of the (BUSY) pin.

CONTROL REGISTER (CTR)



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This register provides all output signals to control the printer. This is a read and write register.

Bit 0: This bit directly controls the data strobe signal to the printer via the $\overline{STB}$ pin. This bit is the inverse of the $\overline{STB}$ pin.

Bit 1: This bit directly controls the automatic feed XT signal to the printer via the $\overline{AFD}$ pin. Setting this bit high causes the printer to automatically feed after each line is printed. This bit is the inverse of the $\overline{AFD}$ pin.

Bit 2: This bit directly controls the signal to initialize the printer via the $\overline{INIT}$ pin. Setting this bit to low initializes the printer. This bit follows the $\overline{INIT}$ pin.

Bit 3: This bit directly controls the select in signal to the printer via the $\overline{SLIN}$ pin. Setting this bit high selects the printer. This bit is the inverse of the $\overline{SLIN}$ pin.

Bit 4: This bit enables the parallel port interrupt. When this bit is set high, the INTP signal follows the $\overline{ACK}$ signal transitions.

Bits 5, 6, 7: These bits are always 1.

TABLE 4-22. Parallel Port Reset Functions

Register/ Signal	Reset Control	Reset State
$\overline{SLIN}$ Pin	$\overline{MR}$	High
$\overline{INIT}$ Pin	$\overline{MR}$	High
$\overline{AFD}$ Pin	$\overline{MR}$	High
$\overline{STB}$ Pin	$\overline{MR}$	High
IRQ7 Pin	$\overline{MR}$	TRI-STATE

Normally when the Control Register is read, the bit values are provided by the output latch. These bit values can be superseded by the logic level of the $\overline{STB}$, $\overline{AFD}$, INIT, and $\overline{SLIN}$ pins, if these pins are forced high or low by an external voltage. In order to force these pins high or low the corresponding bits should be set to their inactive state (e.g. AFD = STB = SLIN = 0, $\overline{INIT}$ = 1).

4.6 IDE HARD DISK INTERFACE CIRCUIT USING THE PC87310 SUPER I/O CONTROLLER

The PC87310 SuperI/O controller is designed to provide a higher level of integration when interfacing to commonly used peripherals such as a floppy disk drive and communications port. Another key interface design that is facilitated

4.0 Functional Description (Continued)

through use of the PC87310 is the **IDE (I**ntelligent **D**rive **E**lectronics) Hard Disk interface. The SuperI/O provides the two hard disk chip selects required for this interface. Using the SuperI/O, only five other chips are required to construct the IDE Hard Disk Interface circuit (see *Figure 7*). The circuit shown provides the address decoding, buffers, and control and data signals for the hard disk IDE interface.

The IDE interface is essentially the AT bus ported to the hard drive. The hard disk controller resides on the hard drive itself. So the IDE interface circuit must provide the AT bus signals, including data bits D15–D0, address lines A3–A0, as well as the common control signals. These signals are contained on the 40-pin IDE interface header (see *Figure 7*).

When in the PC-AT mode. The PC87310 SuperI/O controller provides the two hard disk chip selects for the IDE interface. The $\overline{HCS0}$ output is active low when the 1F0–1F7 (hex) I/O address space is chosen and corresponds to the 1FX signal on the IDE header. The $\overline{HCS1}$ output is active low when the 3F6 or 3F7 I/O addresses are chosen, and corresponds to 3FX on the IDE header. These are the two address blocks used in the PC-AT hard disk controller. The table below summarizes the addresses used by the PC-AT hard disk controller.

Looking at the IDE interface circuit in more detail, the LS244 provides buffering of the control and address lines. The 16L8 PAL provides the necessary control signals to enable the data lines for the correct addresses. These four control signals, $\overline{ENHI}$, $\overline{ENLO}$, $\overline{D7RD}$, and $\overline{D7WR}$ are active low based on the PAL equations (see *Figure 6*).

To summarize the function of these PAL control signals, $\overline{ENHI}$ enables the LS245 octal bus transceiver for the upper data lines (D15–D8) for 16-bit read and write operations at addresses 1F0–1F7. $\overline{ENHI}$ will activate the LS245 only if the $\overline{IOCS16}$ output from the hard drive is active. $\overline{ENLO}$ enables the other LS245 octal bus transceiver for the lower data lines (D7–D0) for 1F0–1F7 reads and writes, and for 3F6 writes and 3F7 reads. In addition, the $\overline{D7RD}$ and $\overline{D7WR}$ control lines from the PAL insure that the D7 data line is disabled for address 3F7 (this bit is used for the Disk Changed register on the floppy disk controller). The two LS245 chips are used to enable or TRI-STATE these data signals. The LS125 is used to buffer or TRI-STATE the D7 data line and the $\overline{HCS0}$ chip select.

PC-AT Hard Disk Controller Registers

Address	Read Function	Write Function
1F0	Data Register	Data Register
1F1	Error Register	Write Precomp Register
1F2	Sector Count	Sector Count
1F3	Sector Number	Sector Number
1F4	Cylinder Low	Cylinder Low
1F5	Cylinder High	Cylinder High
1F6	SDH Register	SDH Register
1F7	Status Register	Command Register
3F6	Not Used. Data Bus TRI-STATE	Digital Output Register
3F7	Drive Address Register (Note)	Not Used. Data Bus TRI-STATE

Note: Data bit D7 is used by the Floppy Disk Controller at address 3F7. D7 must be TRI-STATED by the IDE interface circuit at this address.

```
module SIOpal;
flag '-r2';

title
          'Address decode PAL for SuperI/O demo board, PC87310EB 2.0
          Steve Horeff, PC Peripherals 12/89'

SIO5 device 'P16L8';

VCC, GND                    PIN 20, 10;
RESET, _XTSEL, _HCS0, _HCS1 PIN 1, 2, 3, 4;
_IOR, _IOW, A0, _IO16CS     PIN 5, 6, 7, 8;
_D7WR, _D7RD                PIN 18, 19;
_ENLO, _ENHI                PIN 12, 13;
EN, _RESET                  PIN 11, 17;
equations

_RESET = !(RESET);
_D7RD  = !(EN * (!_IOR * !_HCS0));
_D7WR  = !(EN * (!_IOW *((!_HCS1 * !A0) + !_HCS0)));
_ENHI  = !(EN * ((!_IO16CS * !_HCS0) * (!_IOR + !_IOW)));
_ENLO  = !(EN * ((!_HCS0 * (!_IOR + !_IOW)) +
         (!_HCS1 * ((A0 * !_IOR) + (!A0 * !_IOW)))));
end SIO; pal;
```

FIGURE 6. PAL (16R4) Pin Definitions Equations

4.0 Functional Description (Continued)

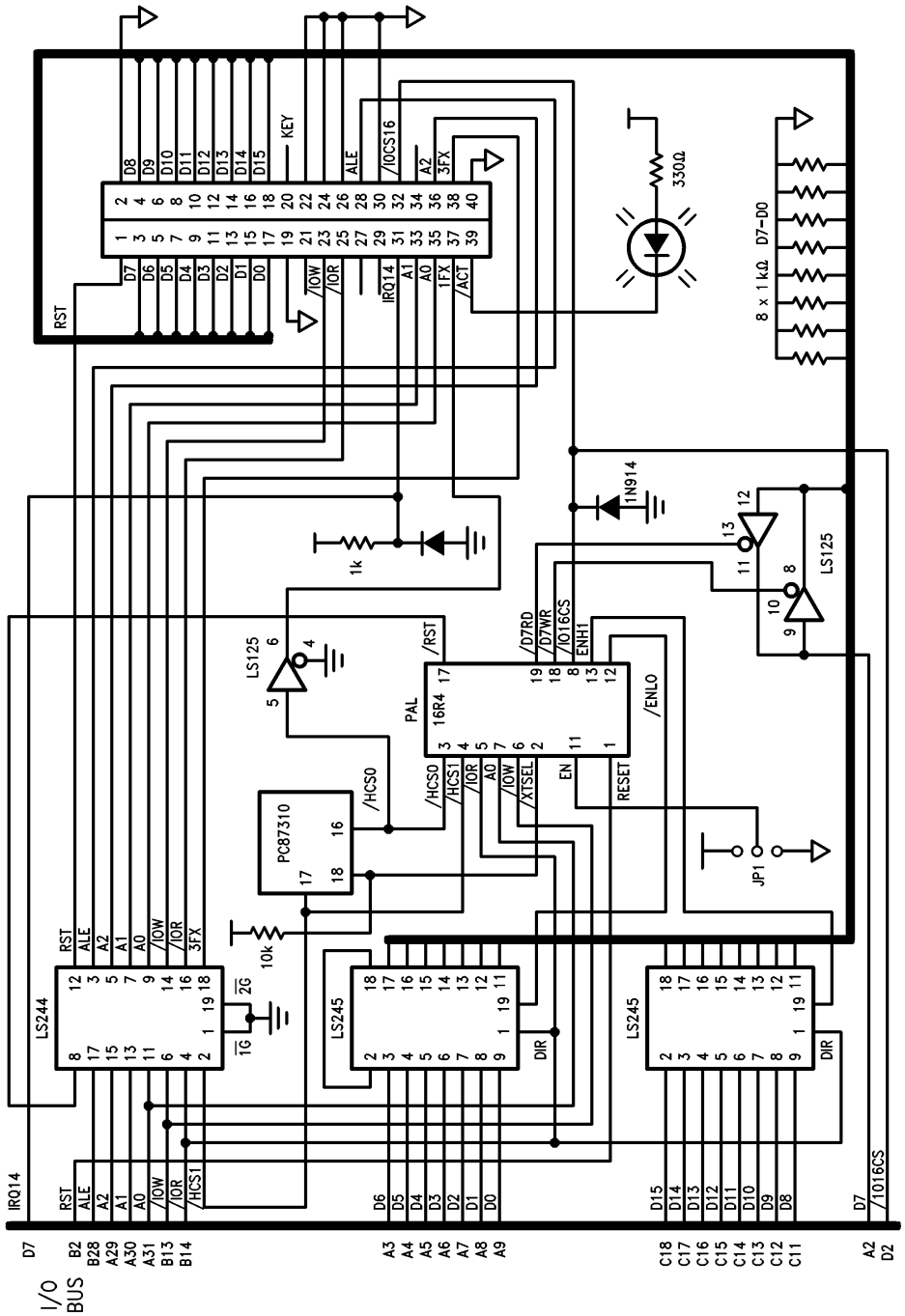


FIGURE 7. Interface between the PC87310 and the (IDE) Cable

4.0 Functional Description (Continued)

4.7 GAME PORT

4.7.1 PC87310 Interface to the AT Game Port

To interface with the game port, all that is required is the logic shown in *Figure 8* and the qualification of the read and write signals. Since the PC87310 provides the game port chip select ($\overline{GPEN}$, pin 18), the game read and game write signals can be easily qualified by gating $\overline{GPEN}$ with $\overline{IOR}$ and $\overline{IOW}$. A typical game port circuit is shown below. (The game port is implemented by using a 74LS244 buffer, NE558 Quad Timer, and some resistors and capacitors.)

4.7.2 PC87310 Interface to the XT Game Port

This interface is essentially the same as for the AT, except that the game port read and write signals are qualified on the PC87310. These qualified read and write signals are provided from the PC87310 via the $\overline{GRD}$ and $\overline{GWR}$ signals directly. This eliminates the need for 2 OR gates in the external game port logic.

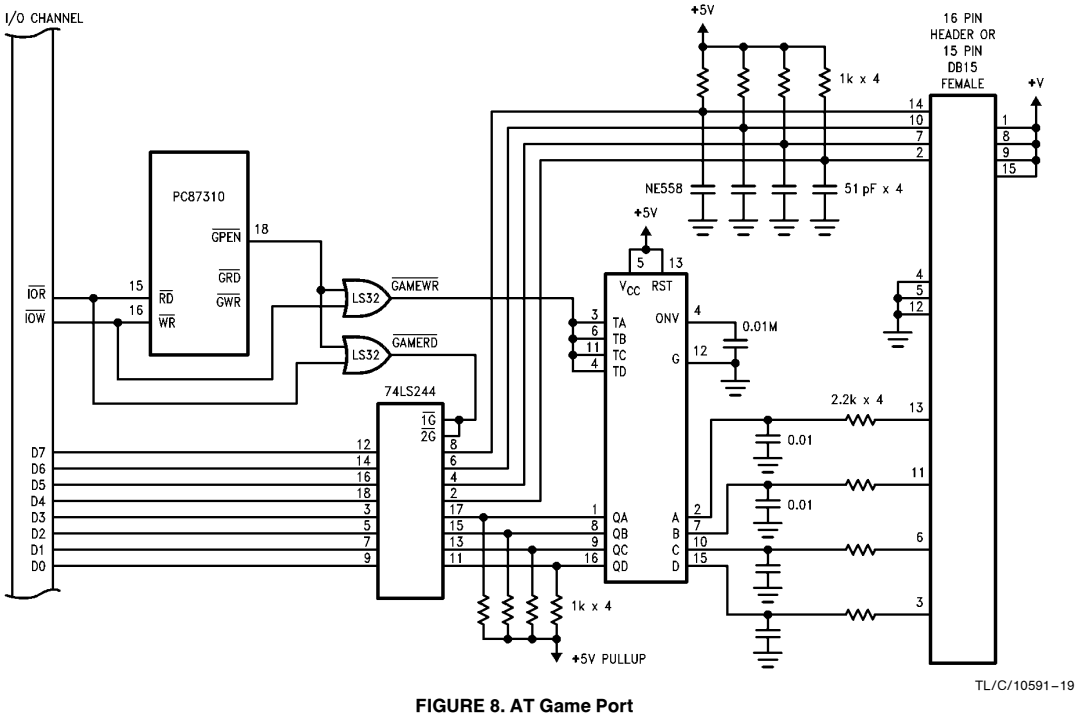


FIGURE 8. AT Game Port

5.0 Absolute Maximum Ratings

(Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +7V
All Input and Output Voltages with Respect to V_{SS}	−0.5V to V_{CC} + 0.5V
Storage Temperature Range (T_{STG})	−65°C to +150°C
Package Power Dissipation (P_D)	750 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
$\lvert V_{CC}-V_{CCA}\rvert$	0.6V

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD})	4.5	5.5	V
Operating Temperature (T_A)	0	+70	°C

ESD Rating is to be determined.

6.0 DC Electrical Characteristics

V_{DD} = 5V ±10%, V_{SS} = 0V, unless otherwise specified (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage	(except OSC2/CLK) (Note 5)	2.0	V_{CC}	V
V_{IL}	Low Level Input Voltage	(except OSC2/CLK)	−0.5	0.8	V
I_{IN}	Input Current (except OSC pins)	V_{IN} = V_{DD} or GND		±1.0	μA
I_{CCA}	Average V_{DDA} Supply Current	V_{IN} = 2.4V or 0.5V, I_O = 0 mA (Note 4)		10	mA
	Quiescent V_{DDA} Supply Current in Low Power Mode	V_{IN} = V_{DD} or GND, I_O = 0 mA (Note 4)		400	μA
I_{CC}	Combined Average V_{DD} Supply Current	V_{DD} = 5.5V, No Loads on the Outputs; $\overline{RD}$, $\overline{WR}$, SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2V; All Other Inputs = 0.8V or 2.4V; CLK = 24 MHz; DIVISOR = EFFF		35	mA
	Quiescent V_{DD} Supply Current in Low Power Mode	V_{IN} = V_{DD} or GND, I_O = 0 mA (Note 4)		950	μA
OSCILLATOR PINS (OSC2/CLK)					
I_{OSC}	OSC2 Input Current	OSC1 = GND, V_{IN} = V_{DD} or GND	±1.2		mA
V_{IH}	OSC2 High Level Input Voltage	OSC1 = GND	2.4		V
V_{IL}	OSC2 Low Level Input Voltage	OSC1 = GND		0.4	V
DISK DRIVE INTERFACE PINS (MTR0–3, DR0–3, WDATA, WGATE, RDATA, DIR, HDSEL, TRK0, WRTPRT, RPM, STEP, DSKCHG, INDEX)					
V_H	Input Hysteresis		250 Typical		mV
V_{OL}	Low Level Output Voltage	I_{OUT} = 48 mA		0.4	V
I_{LKG}	Output High Leakage Current	V_{OUT} = V_{DD} or GND		±100	μA
V_{IH}	High Level Input Voltage		2.2		V
V_{IL}	Low Level Input Voltage			0.8	V

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: These DC Electrical Characteristics are measured statically, and not under dynamic conditions.

Note 4: I_{CC} is measured with a 0.1 μF supply decoupling capacitor to ground.

Note 5: $\overline{CRB0-7}$, $\overline{XTSEL}$, and $\overline{CRPE}$ are NOT TTL compatible. Pull-up resistors must be used if this is a requirement.

6.0 DC Electrical Characteristics

V_{DD} = 5V ±10%, V_{SS} = 0V, unless otherwise specified (Note 3) (Continued)

Symbol	Parameter	Conditions	Min	Max	Units
MICROPROCESSOR AND PARALLEL PORT PINS					
V_{OL}	Output Low Voltage	I_{OL} = 24 mA on D0–D7 I_{OL} = 16 mA on PD0–PD7 I_{OL} = 12 mA on All Other Outputs		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −6 mA on D0–D7 I_{OH} = −6 mA on PD0–PD7 I_{OH} = −1 mA On $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$ and $\overline{SLIN}$ (Note 5) I_{OH} = −0.2 mA on All Other Outputs	2.4		V
I_{IL}	Input Leakage	V_{DD} = 5.5V, V_{SS} = 0V All Other Pins Floating		±10	μA
I_{OZ}	Output TRI-STATE Leakage	V_{DD} = 5.5V, V_{SS} = 0V, V_{OUT} = 0V, 5.5V		±20	μA

6.1 PHASE LOCKED LOOP CHARACTERISTICS V_{CC} = 5V ±10%, F_{XTAL} = 24 MHz unless otherwise specified

Symbol	Parameter	Conditions	Typ		Units
V_{REF}	SETCUR Pin Reference Voltage	R_1 = 5.6 kΩ, V_{CC} = 5V	1.1		V
K_{VCO}	VCO Gain (Note 1)	t_{DATA} = 1 μs ±10%	25		Mrad/s/V
R_1	Recommended Pump Resistor Range		3–12		kΩ
$K_{P(UP)}$	Charge Pump Up Current Gain ($I_{REF}/I_{P(UP)}$) (Note 2)	R_1 = 5.6 kΩ	2.50		(none)
$K_{P(DWN)}$	Charge Pump Down Current Gain ($I_{REF}/I_{P(DWN)}$) (Note 2)	R_1 = 5.6 kΩ	2.25		(none)
K_{PLL}	Internal Phase Locked Loop Gain (Note 3)	(R_1 = 5.6 kΩ) Pump Up Pump Down	75 70		Mrad Mrad
T_{SW}	Static Window (Note 4)		**Early**	**Late**	
		(R_1 = 5.6 kΩ) 250 kb/s 500 kb/s 1.0 Mb/s	 1075 530 259	 872 440 234	 ns ns ns
T_{DW}	Dynamic Window Margin	(Note)	70		%

Note: Measurements made with a repeating ''DB6'' data pattern with reverse write precompensation, using recommended filter values for the configuration shown in *Figure 3c.* 25°C, 5.0V, 0% MSV.

Note 1: The VCO gain is measured at the 1.0 Mb/s data rate by forcing the data period over a range from 900 ns to 1100 ns, and measuring the resulting voltage on the filter pin. The best straight line gain is fit to the measured points.

Note 2: This is the current gain of the charge pump, which is defined as the output current divided by the current through R_1.

Note 3: This is the product of: $V_{REF} \times K_P \times K_{VCO}$. The total variation in this specification indicates the total loop gain variation contributed by the internal circuitry. The K_{VCO} portion of this specification is measured at the 1.0 Mb/s data rate by forcing the data period over a range of 900 ns to 1100 ns, and measuring the resultant K_{VCO}. K_P is measured by forcing the Filter pin to 2.1V and measuring the ratio of the charge pump current over the input current.

Note 4: The FDC is guaranteed to correctly decode a single shifted clock pulse at the end of a long series of non-shifted preamble bits as long as the single shifted pulse is shifted less than the amount specified in T_{SW}. The length of the preamble is long enough for the PLL to lock. The filter components used are those in Table 4-8.

Note 5: $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$ and $\overline{SLIN}$ are open collector output pins that require pull-up resistors (4.7 kΩ) to V_{DD}.

6.2 CAPACITANCE T_A = 25°C, V_{DD} = V_{SS} = 0V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	f_c = 1 MHz Unmeasured Pins Returned to V_{SS}		5	7	pF
C_{OUT}	Output Capacitance			6	8	pF
$C_{I/O}$	Input/Output Capacitance			10	12	pF

7.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$

Symbol	Parameter	Conditions	Min	Max	Units
CPU INTERFACE					
t_{AR}	Delay from Address to $\overline{RD}$		19		ns
t_{AW}	Delay from Address to $\overline{WR}$		19		ns
t_{CH}	Duration of Clock High Pulse	External Clock (24 MHz Max)	16		ns
t_{CL}	Duration of Clock Low Pulse	External Clock (24 MHz Max)	16		ns
t_{DH}	Data Hold Time		10		ns
t_{DS}	Data Setup Time		19		ns
t_{HZ}	$\overline{RD}$ to Floating Data Delay	(Note 1)	13	25	ns
t_{MR}	Master Reset Pulse Width		100		ns
t_{PH}	Port Hold		25		ns
t_{PS}	Port Setup		18		ns
t_{RA}	Address Hold Time from $\overline{RD}$		0		ns
t_{RC}	Read Cycle Update		36		ns
t_{RD}	$\overline{RD}$ Strobe Width		60		ns
t_{RI}	Read Strobe to Clear IRQ6			52	ns
t_{RVD}	Delay from $\overline{RD}$ to Data			39	ns
t_{WA}	Address Hold Time from $\overline{WR}$		0		ns
t_{WC}	Write Cycle Update		36		ns
t_{WI}	Write Strobe to Clear IRQ6			52	ns
t_{WO}	Write to Output			41	ns
t_{WR}	$\overline{WR}$ Strobe Width		60		ns
RC	Read Cycle $= t_{AR} + t_{RD} + t_{RC}$		115		ns
WC	Write Cycle $= t_{AW} + t_{WR} + t_{WC}$		115		ns

Note 1: Charge and discharge time is determined by V_{OL}, V_{OH} and the external loading.

Note 2: All AC timings can be met with current loads that don't exceed 3.2 mA or $-80\ \mu A$ at 100 pF capacitive loading.

Note 3: For capacitive loads that exceed 100 pF the following typical derating factors should be used:

$100\ pF < C_L \leq 150\ pF$, $t = (0.1\ ns/pF)\ (C_L - 100\ pF)$ typical
$150\ pF < C_L \leq 200\ pF$, $t = (0.08\ ns/pF)\ (C_L - 100\ pF)$ and
$t = (0.5\ ns/mA)\ (I_{SINK}\ mA)$ or
$t = -(0.5\ ns/mA)\ (I_{SOURCE\ mA})$
I_{SOURCE} is always negative, $I_{SINK} \leq 4.8$ mA, $I_{SOURCE} \leq -120\ \mu A$, $C_L \leq 250$ pF

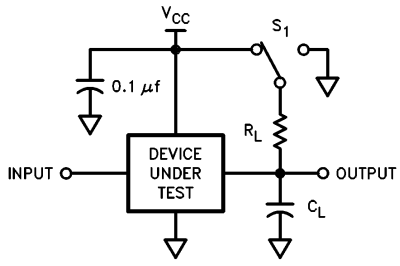
AC Test Conditions (Notes 1, 2, 3)

Input Pulse Levels	GND to 3V
Input Rise and Fall Times	6 ns
Input and Output Reference Levels	1.3V
TRI-STATE Reference Levels	Active High − 0.5V Active Low + 0.5V

Note 1: $C_L = 100$ pF, includes jig and scope capacitance.

Note 2: S1 = open for push-pull outputs. S1 = V_{CC} for high impedance to active low and active low to high impedance measurements. S1 = GND for high impedance to active high and active high to high imepedance measurements. $R_L = 1.0\ k\Omega$ for μP interface pins.

Note 3: For the Open Drain Drive Interface Pins S1 = V_{CC} and $R_L = 150\Omega$.



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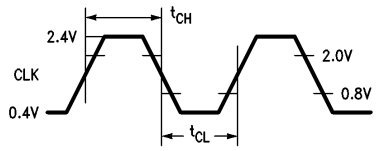
7.0 AC Electrical Characteristics All timings are referenced to valid 0 and valid 1

External Clock Input (24 MHz)



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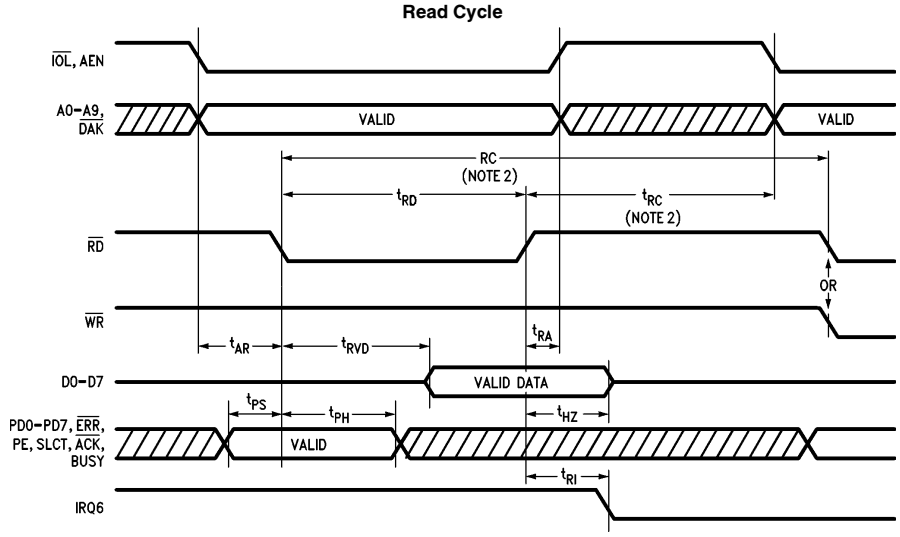
Note 1: The 2.4V and 0.4V levels are the voltages that the inputs are driven to during AC testing.

CPU INTERFACE

Read Cycle



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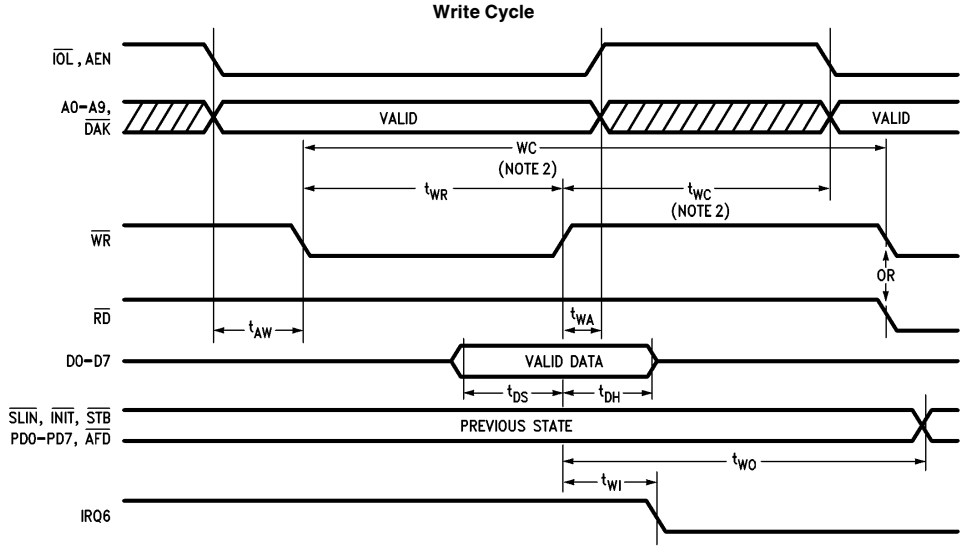
Write Cycle



Note 2: These parameters are only valid during UART accesses.

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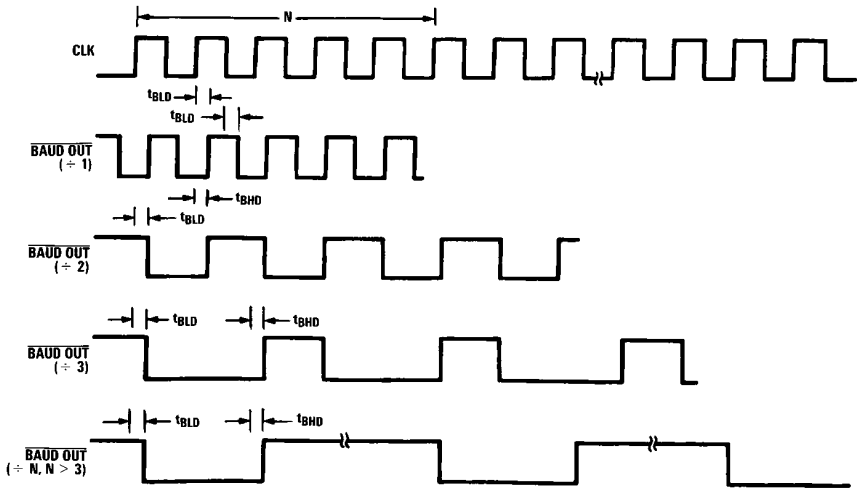
7.0 AC Electrical Characteristics All timings are referenced to valid 0 and valid 1 (Continued)

SERIAL INTERFACE BAUD GENERATOR

Symbol	Parameter	Conditions	Min	Max	Units
N	Baud Divisor		1	$2^{16} - 1$	
t_{BHD}	Baud Output Positive Edge Delay	CLK = 24 MHz ÷ 2, 100 pF Load		56	ns
t_{BLD}	Baud Output Negative Edge Delay	CLK = 24 MHz ÷ 2, 100 pF Load		56	ns

$\overline{\text{BAUDOUT}}$ Timing



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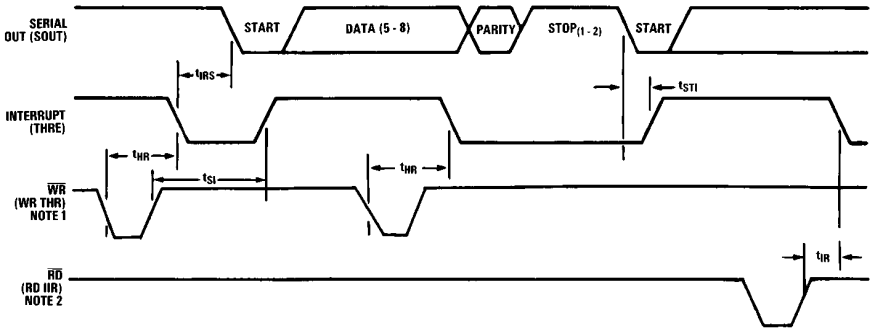
7.0 AC Electrical Characteristics All timings are referenced to valid 0 and valid 1 (Continued)

TRANSMITTER

Symbol	Parameter	Conditions	Min	Max	Units
t_{HR}	Delay from $\overline{WR}$ (WR THR) to Reset Interrupt			50	ns
t_{IR}	Delay from $\overline{RD}$ (RD IIR) to Reset Interrupt (THRE)			50	ns
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		8	24	BAUDOUT Cycles
t_{SI}	Delay from Initial Write to Interrupt		16	24	BAUDOUT Cycles
t_{STI}	Delay from Start to Interrupt (THRE)			8	BAUDOUT Cycles

Transmitter Timing



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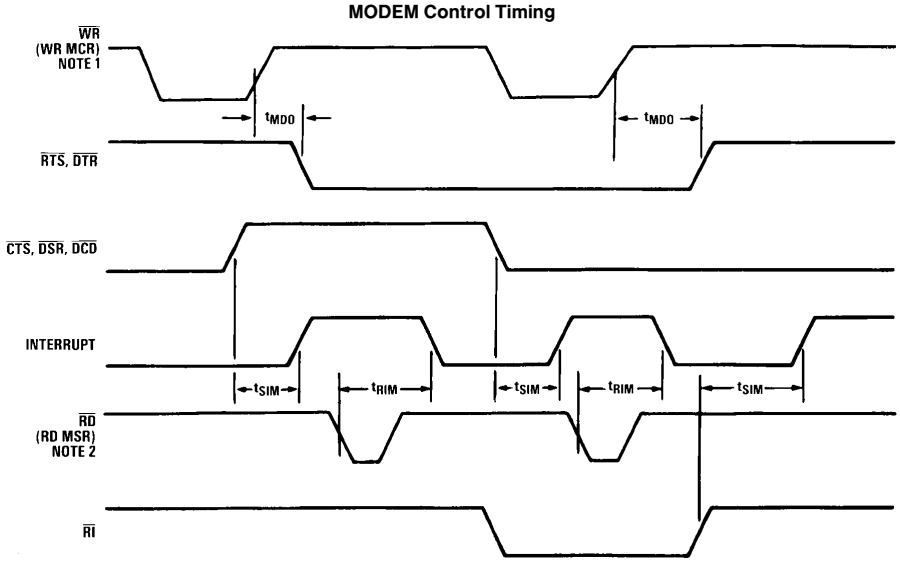
7.0 AC Electrical Characteristics All timings are referenced to valid 0 and valid 1 (Continued)

MODEM CONTROL

Symbol	Parameter	Conditions	Min	Max	Units
t_{MDO}	Delay from $\overline{WR}$ (WR MCR) to Output			50	ns
t_{RIM}	Delay to Reset Interrupt from $\overline{RD}$ (RD MSR)			98	ns
t_{SIM}	Delay to Set Interrupt from MODEM Input			65	ns

MODEM Control Timing



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Note 1: See Write Cycle timing.

Note 2: See Read Cycle timing.

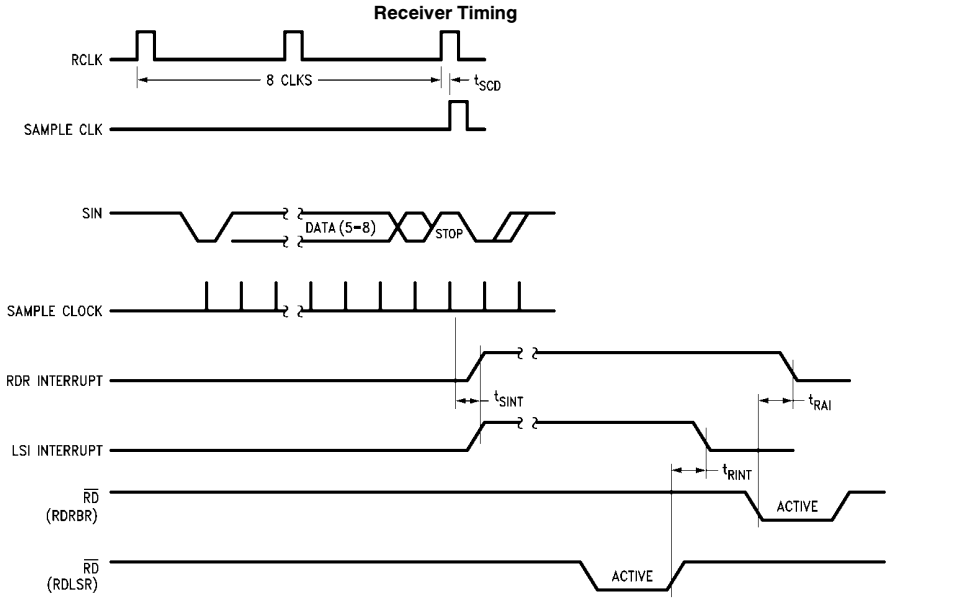
7.0 AC Electrical Characteristics All timings are referenced to valid 0 and valid 1 (Continued)

RECEIVER

Symbol	Parameter	Conditions	Min	Max	Units
t_{RAI}	Delay from Active Edge of $\overline{RD}$ to Reset Interrupt			98	ns
t_{RINT}	Delay from Inactive Edge of $\overline{RD}$ (RD LSR) to Reset Interrupt			60	ns
t_{SCD}	Delay from R_{CLK} to Sample Time	(Note 1)		41	ns
t_{SINT}	Delay from Stop to Set Interrupt			2	BAUDOUT Cycles

Note 1: This is an internal timing and therefore is not tested.

Receiver Timing



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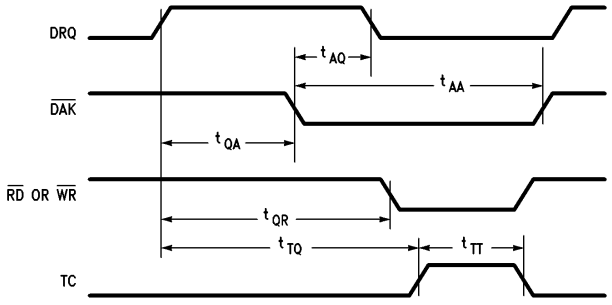
7.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$ (Continued)

DMA TIMING (Note 1)

Symbol	Parameter	Min	Max	Units
t_{AA}	DAK Pulse Width	60		ns
t_{AQ}	End of DRQ from DAK		92	ns
t_{QA}	DAK Assertion from DRQ	8		ns
t_{QR}	DRQ to Read or Write Strobe	8		ns
t_{TQ}	Time after Last DRQ That TC Must Be Asserted By		(Note 2)	
t_{TT}	TC Strobe Width	40		ns

Note 1: DMA Acknowledge is sufficient to acknowledge a data transfer. Read or Write Strobes are neccessary only if data is to be presented to the data bus. If Read/Write Strobes are applied, then they and the Acknowledge must be removed within 1 μs of each other.

Note 2: TC is is the terminal count pin which terminates the data transfer operation. There are several constraints placed on the timing of TC. 1) TC is enabled by $\overline{DAK}$, so TC must be pulsed while $\overline{DAK}$ is low. 2) TC must occur before ((1/data rate x 8) − 1 μs). Data rate is the exact data transfer rate being used.



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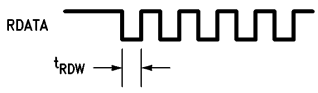
DRIVE READ TIMING

Symbol	Parameter	Min	Max	Units
t_{RDW}	Read Data Pulse Width	25		ns



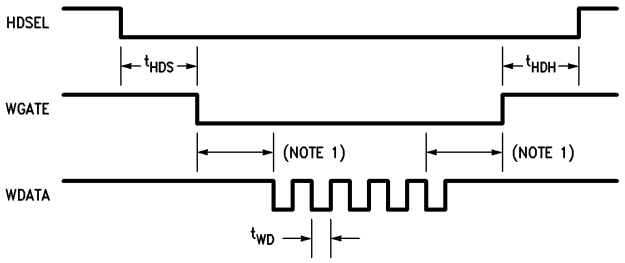
TL/C/10591–29

7.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$ (Continued)

DRIVE WRITE TIMING

Symbol	Parameter	Conditions	Min	Max	Units
t_{WD}	Write Data Pulse Width	250 kb/s (MFM)	500		ns
		300 kb/s (MFM)	416		ns
		500 kb/s (MFM)	250		ns
		1000 kb/s(MFM)	225		ns
t_{HDS}	Head Select Setup to Write Gate Assertion		40		μs
t_{HDH}	Head Select Hold from Write Gate		12		μs

Note 1: Whenever WGATE is asserted the WDATA line is active. At the end of each write one dummy byte is written before WGATE is deasserted.



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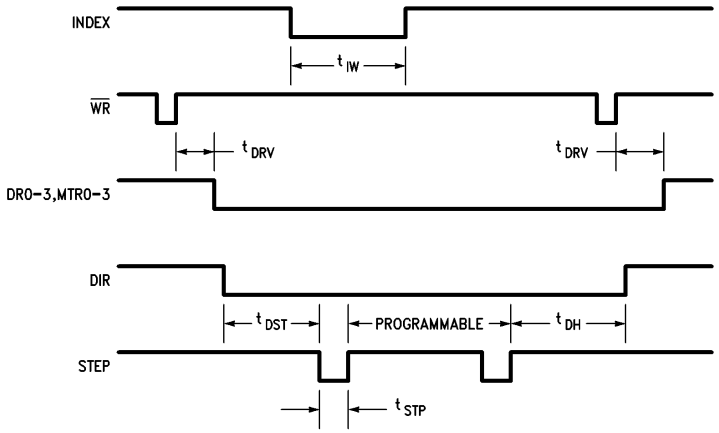
DRIVE TRACK ACCESS TIMING

Symbol	Parameter	Min	Max	Units
t_{DH}	Direction Hold from End of Step	1 Step Time		
t_{DRV}	Drive Select or Motor Time from Write Strobe		100	ns
t_{DST}	Direction Setup prior to Step	6		μs
t_{IW}	Index Pulse Width	100		ns
t_{STP}	Step Pulse Width	8		μs



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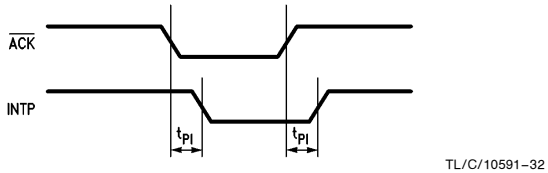
7.0 AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{DD} = +5V \pm 10\%$ (Continued)

PARALLEL INTERFACE

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PDH}	Port Data Hold	(Note 1)	500		ns
t_{PDS}	Port Data Setup	(Note 1)	500		ns
t_{PI}	Port Interrupt			38	ns
t_{SW}	Strobe Width	(Note 1)	500		ns

Note 1: These numbers are system dependent and therefore are not tested.

Interrupt Timing



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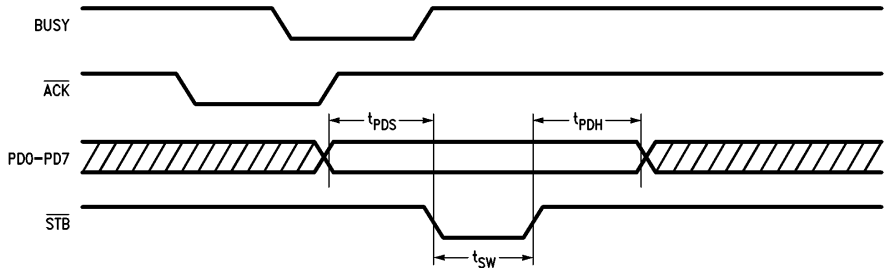
Typical Peripheral Data Exchange



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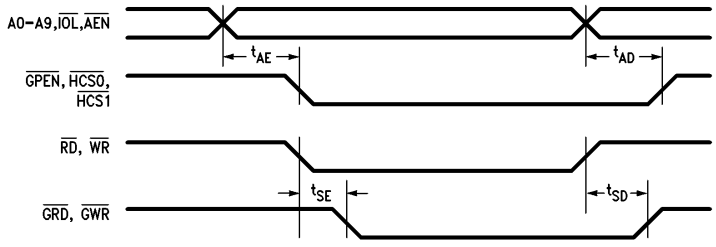
IDE AND GAME PORT TIMING

Symbol	Parameter	Conditions	Min	Max	Units
t_{AD}	Delay from Address to Disable Strobe			25	ns
t_{AE}	Delay from Address to Enable Strobe			25	ns
t_{SD}	Delay from CPU Strobe to Disable Game Strobe			25	ns
t_{SE}	Delay from CPU Strobe to Enable Game Strobe			25	ns



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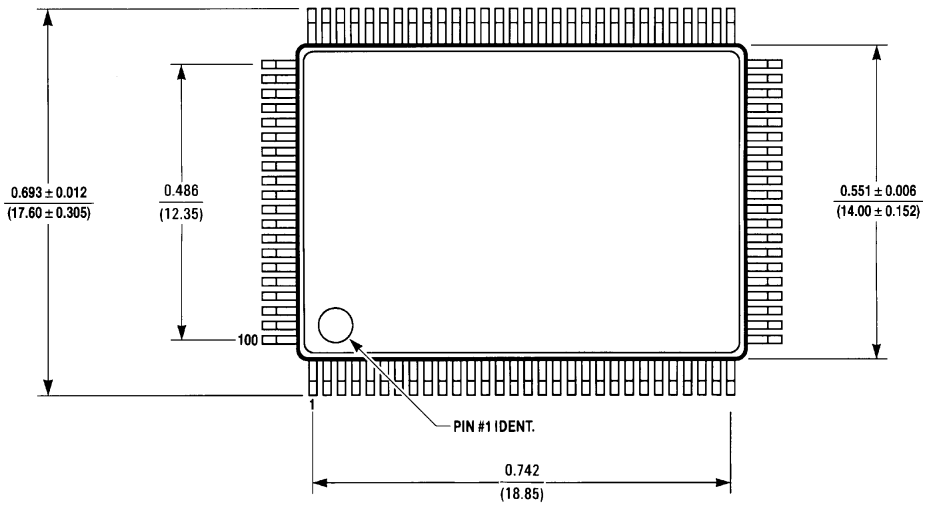
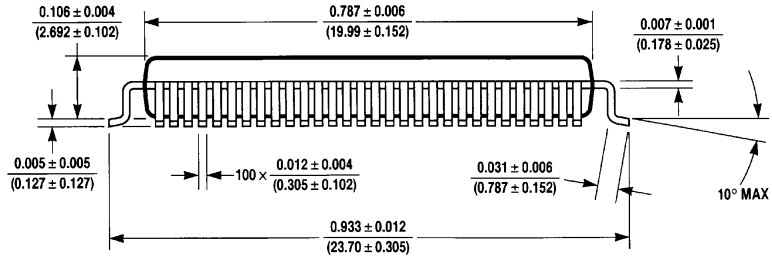
9.0 Physical Dimensions inches (millimeters)





VF100B (REV C)

Plastic Quad Flatpak, EIAJ (VF)
Order Number PC87310VF
NS Package Number VF100B

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