

PC912X

Ultra-high Speed Response OPIC Photocoupler

■ Features

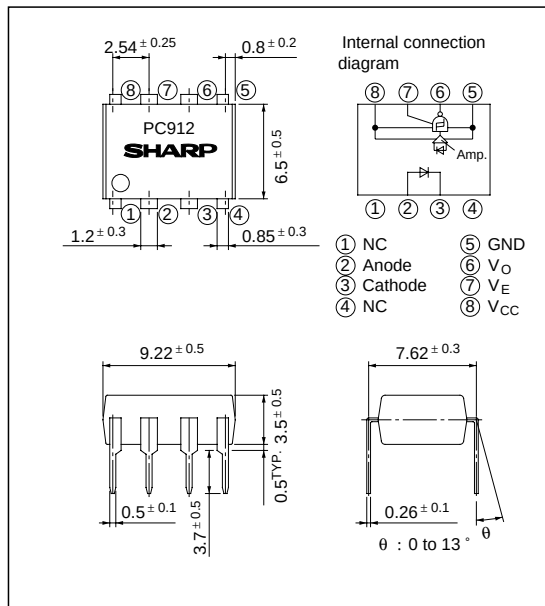
1. Ultra-high speed response
(t_{PHL} , t_{PLH} : TYP. 40ns)
2. High instantaneous common mode rejection voltage (CM_H : MIN. 3kV/ μ s)
3. Capable of high speed digital transmission
(Transmission speed : MAX. 20Mb/s)
(NRZ signal)

■ Applications

1. Personal computers
2. Electrical music instruments

■ Outline Dimensions

(Unit : mm)



* “OPIC” (Optical IC) is a trademark of the SHARP Corporation.
An OPIC consists of a light-detecting element and signal-processing circuit integrated onto a single chip.

■ Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

	Parameter	Symbol	Rating	Unit
Input	*1 Forward current	I_F	20	mA
	Reverse voltage	V_R	5	V
	*1 Power dissipation	P	40	mW
Output	Supply voltage	V_{CC}	7	V
	*2 Enable voltage	V_E	7	V
	High level output current	I_{OH}	- 8	mA
	Low level output current	I_{OL}	25	mA
	*1, 3 Collector power dissipation	P_O	40	mW
	*4 Isolation voltage	V_{iso}	2.5	kV _{rms}
	Operating temperature	T_{opr}	0 to + 70	$^\circ\text{C}$
	Storage temperature	T_{stg}	- 55 to + 125	$^\circ\text{C}$
	*5 Soldering temperature	T_{sol}	260	$^\circ\text{C}$

*1 $T_a = 0$ to 70°C *2 It shall not exceed 500mV or more over supply voltage (V_{CC}).*3 Applied to output terminal (V_O)

*4 AC for 1 minute, 40 to 60% RH

*5 For 10 seconds

■ Electro-optical Characteristics

(Unless specified : Ta = 0 to 70°C)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input	Forward voltage		V _F	Ta = 25°C, I _F = 10mA	-	1.6	1.9	V	
	Reverse current		I _R	Ta = 25°C, V _R = 5V	-	-	10	μ A	
	Terminal capacitance		C _t	Ta = 25°C, V _F = 0V f = 1MHz	-	60	120	pF	
Output	High level output voltage		V _{OH}	V _{CC} = 4.5V, I _{OH} = - 2mA I _F = 0.25mA, V _E = 2.0V	2.4	-	-	V	
	Low level output voltage		V _{OL}	V _{CC} = 4.5V, V _E = 2.0V I _F = 5mA, I _{OL} = 13mA	-	0.3	0.6	V	
	High level enable voltage		V _{EH}	V _{CC} = 5.5V	2.0	-	-	V	
	Low level enable voltage		V _{EL}	V _{CC} = 5.5V	-	-	0.8	V	
	High level enable current		I _{EH}	V _{CC} = 5.5V, V _E = 5.5V	-	-	100	μ A	
	Low level enable current		I _{EL}	V _{CC} = 5.5V, V _E = 0.5V	-	- 0.2	- 0.4	mA	
	High level supply current		I _{CCH}	V _{CC} = 5.5V, I _F = 0mA V _E = 2.0V	-	13	23	mA	
	Low level supply current		I _{CCL}	V _{CC} = 5.5V, I _F = 10mA V _E = 2.0V	-	15	25	mA	
	High impedance supply current		I _{CCZ}	V _{CC} = 5.5V, V _E = 0V	-	16	26	mA	
	Output leak current		I _{OH}	V _{CC} = 5.5V, V _E = 2.0V V _O = 5.5V, I _F = 0.25mA	-	-	100	μ A	
	High impedance output current		I _{OZH}	V _{CC} = 5.5V, V _E = 0.4V	-	-	100	μ A	
	Output short-circuit current		I _{OS}	V _{CC} = 5.5V, V _O = 0V I _F = 0mA 10ms or less	- 10	-	- 50	mA	
	Transfer charac- teristics	“High→Low” threshold input current		I _{FHL}	V _{CC} = 5V V _E = 2.0V	-	2.5	5	mA
“Low→High” threshold input current		I _{FLH}	0.5	1.9		-	mA		
Hysteresis		I _{FLH} / I _{FHL}	0.55	-		0.95	-		
Isolation resistance		R _{ISO}	Ta = 25°C, DC = 500V 40 to 60% RH	5 x 10 ¹⁰	10 ¹¹	-	Ω		
Floating capacitance		C _f	Ta = 25°C, V = 0V f=1MHz	-	0.6	5	pF		
Response time		“ High→Low ” propagation delay time		t _{PHL}	Ta = 25°C V _{CC} = 5V C _L = 15pF I _F = 7.5mA *6	-	40	55	ns
		“ Low→High ” propagation delay time		t _{PLH}		-	40	55	ns
		Pulse width distortion t _{PHL} - t _{PLH}		Δ T _w		-	-	15	ns
		Rise/fall time		t _r , t _f		-	15	30	ns
		“ High→Low ” enable propagation delay time		t _{EHL}		-	40	70	ns
		“ Low→High ” enable propagation delay time		t _{ELH}		-	40	70	ns
CMR		Instantaneous common mode rejection voltage (High level output)		CM _H	Ta = 25°C, V _{CC} = 5V V _{CM} = 50V, I _F = 0mA V _O (Min) = 2V, *8	3 000	10 000	-	V/ μ s
		Instantaneous common mode rejection voltage (Low level output)		CM _L	Ta = 25°C, V _{CC} = 5V V _{CM} = 50V, I _F = 5mA V _O (Max) = 0.8V, *8	- 3 000	10 000	-	V/ μ s

*6 Refer to Fig. 1 *7 Refer to Fig. 2 *8 Refer to Fig. 3

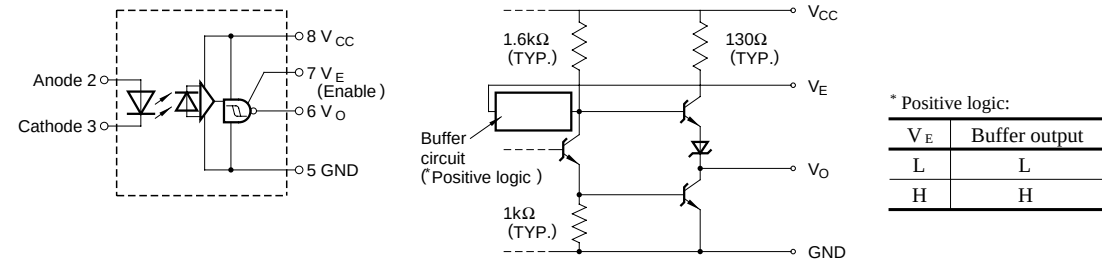
 All typical values are at Ta = 25°C, $V_{CC} = 5\text{V}$.

Recommended Operating Conditions

Parameter	Symbol	MIN.	MAX.	Unit
Low level input current	I_{FL}	0	250	μA
High level input current	I_{FH}	7	15	mA
High level enable voltage	V_{EH}	2.0	V_{CC}	V
Low level enable voltage	V_{EL}	0	0.8	V
Supply voltage	V_{CC}	4.5	5.5	V
Fan out (TTL load)	N	-	8	-
Operating temperature	T_{opr}	0	70	$^{\circ}C$

- 1. When the enable input is not used, please connect to V_{CC} .
- 2. It is necessary to connect a by-pass ceramic capacitor (0.01 to 0.1 μF) between V_{CC} and GND at the position within 1cm from pin.

Block Diagram

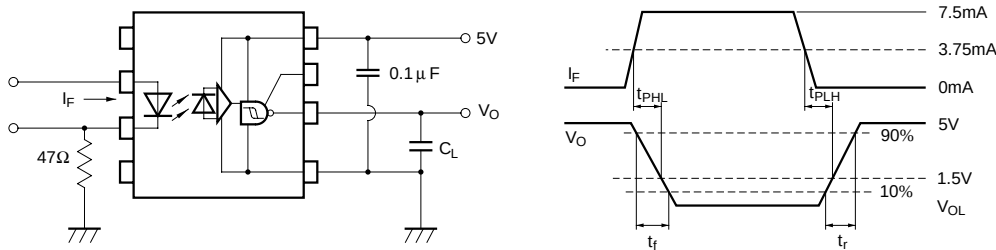


Truth Table

Input	Enable	Output
H	H	L
L	H	H
H	L	Z
L	L	Z

L : Logic (0)
H : Logic (1)
Z : High impedance

Fig. 1 Test Circuit for t_{PHL} , t_{PLH} , t_r and t_f



* C_L includes the probe and wiring capacitance.

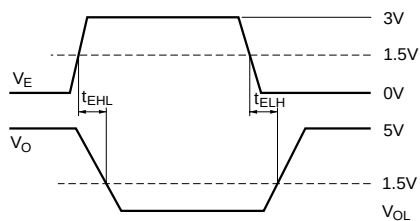
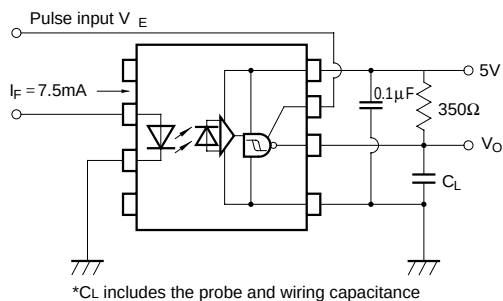
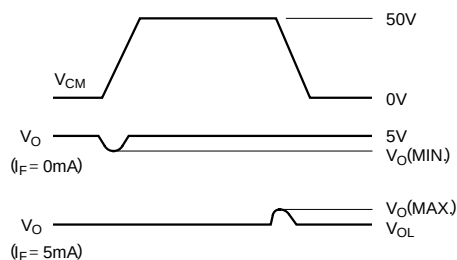
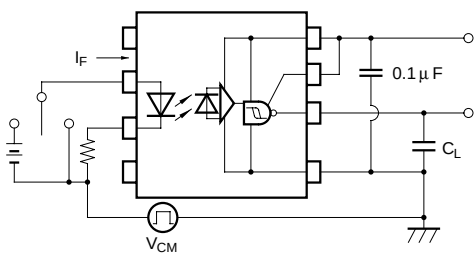
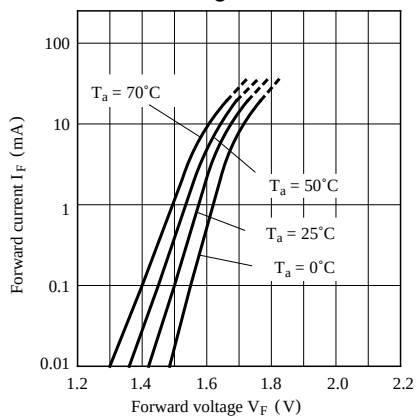
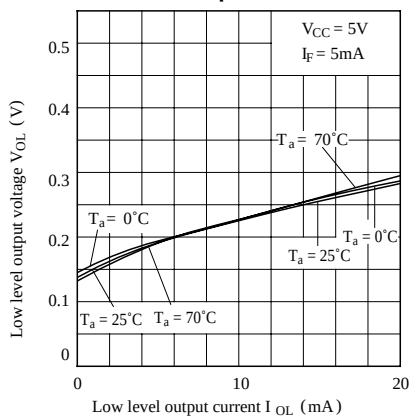
Fig. 2 Test Circuit for t_{EHL} and t_{ELH} Fig. 3 Test Circuit for CM_H and CM_L Fig. 4 Forward Current vs.
Forward VoltageFig. 5 Low Level Output Voltage vs.
Low Level Output Current

Fig. 6 High Level Output Voltage vs. High Level Output Current

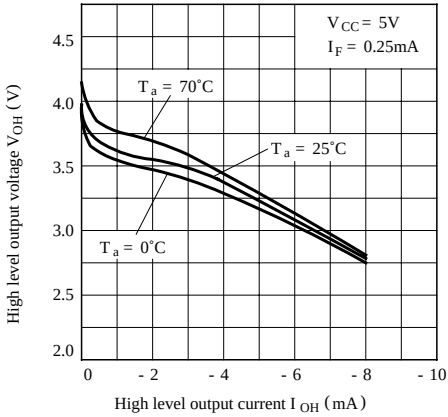


Fig. 7 Propagation Delay Time vs. Ambient Temperature

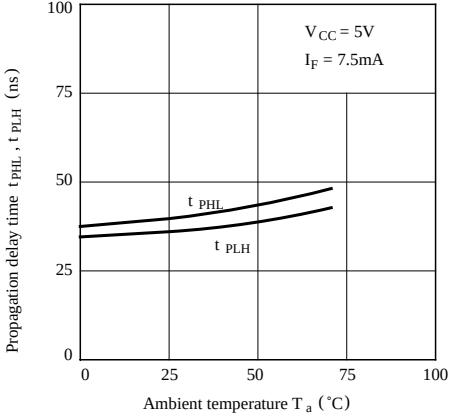
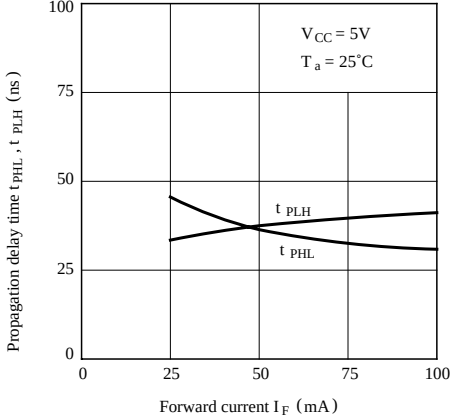


Fig. 8 Propagation Delay Time vs. Forward Current



● Please refer to the chapter “Precautions for Use ”