INTEGRATED CIRCUITS

DATA SHEET

PCA3354C; PCD3354A

8-bit microcontrollers with DTMF generator and 256 bytes EEPROM

Product specification   1996 Dec 18

Supersedes data of 1996 May 09

File under Integrated Circuits, IC03

CONTENTS

8-bit microcontrollers with DTMF generator and 256 bytes EEPROM

PCA3354C; PCD3354A

1 FEATURES

- 8-bit CPU, ROM, RAM, EEPROM and I/O; all in a 44-lead quad flat package
- 8 kbytes ROM; 256 bytes RAM
- 256 bytes Electrically Erasable Programmable Read Only Memory (EEPROM)
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 36 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 8-bit reloadable Timer 2
- Three single-level vectored interrupts:
  - external
  - 8-bit programmable Timer/event counter 1
  - derivative; triggered by reloadable Timer 2
- Two test inputs, one of which also serves as the external interrupt input
- DTMF, modem, musical tone generator
- Reference for supply and temperature-independent tone output
- Filtering for low output distortion (CEPT compatible)
- Melody output for ringer application
- Programmable DTMF clock divider
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF tone output and EEPROM erase/write from 2.5 V)
- CPU clock frequency: 1 to 16 MHz (3.58 MHz or 10.74 MHz for DTMF)
- Operating ambient temperature:
  - −25 to +70 °C (PCD3354A)
  - 0 to 50 °C (PCA3354C)
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

This data sheet details the specific properties of the PCA3354C and PCD3354A. The shared properties of the PCD33xxA family of microcontrollers are described in the *"PCD33xxA family"* data sheet, which should be read in conjunction with this publication.

The PCA3354C and PCD3354A are microcontrollers oriented towards telephony applications. They include 8 kbytes ROM, 256 bytes RAM, 36 I/O lines, and an on-chip generator for dual tone multifrequency (DTMF), modem and musical tones. In addition to dialling, the generated frequencies can be made available as square waves for melody generation, providing ringer operation.

The PCA3354C and PCD3354A also incorporate 256 bytes of EEPROM, permitting data storage without battery backup. The EEPROM can be used for storing telephone numbers, particularly for implementing redial functions.

The differences between PCA3354C and PCD3354A are shown in Table 1.

The instruction set is similar to the MAB8048 and is a sub-set of that listed in the *"PCD33xxA family"* data sheet.

Table 1 Differences: PCA3354C and PCD3354A

TYPE	V_{POR}	AMBIENT TEMP. RANGE
PCA3354C	fixed at 2.0 V ±0.3 V	0 to 50 °C
PCD3354A	(1.2 to 3.6 V) ±0.5 V[1]	−25 to +70 °C

Note

1. See Chapter 13, Table 24.

3 ORDERING INFORMATION (see note 1)

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA3354CH	QFP44	plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 × 14 × 2.2 mm	SOT205-1
PCD3354AH			

Note

1. Please refer to the Order Entry Form (OEF) for this device for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

4 BLOCK DIAGRAM

Fig.1 Block diagram.

8-bit microcontrollers with DTMF generator and 256 bytes EEPROM

PCA3354C; PCD3354A
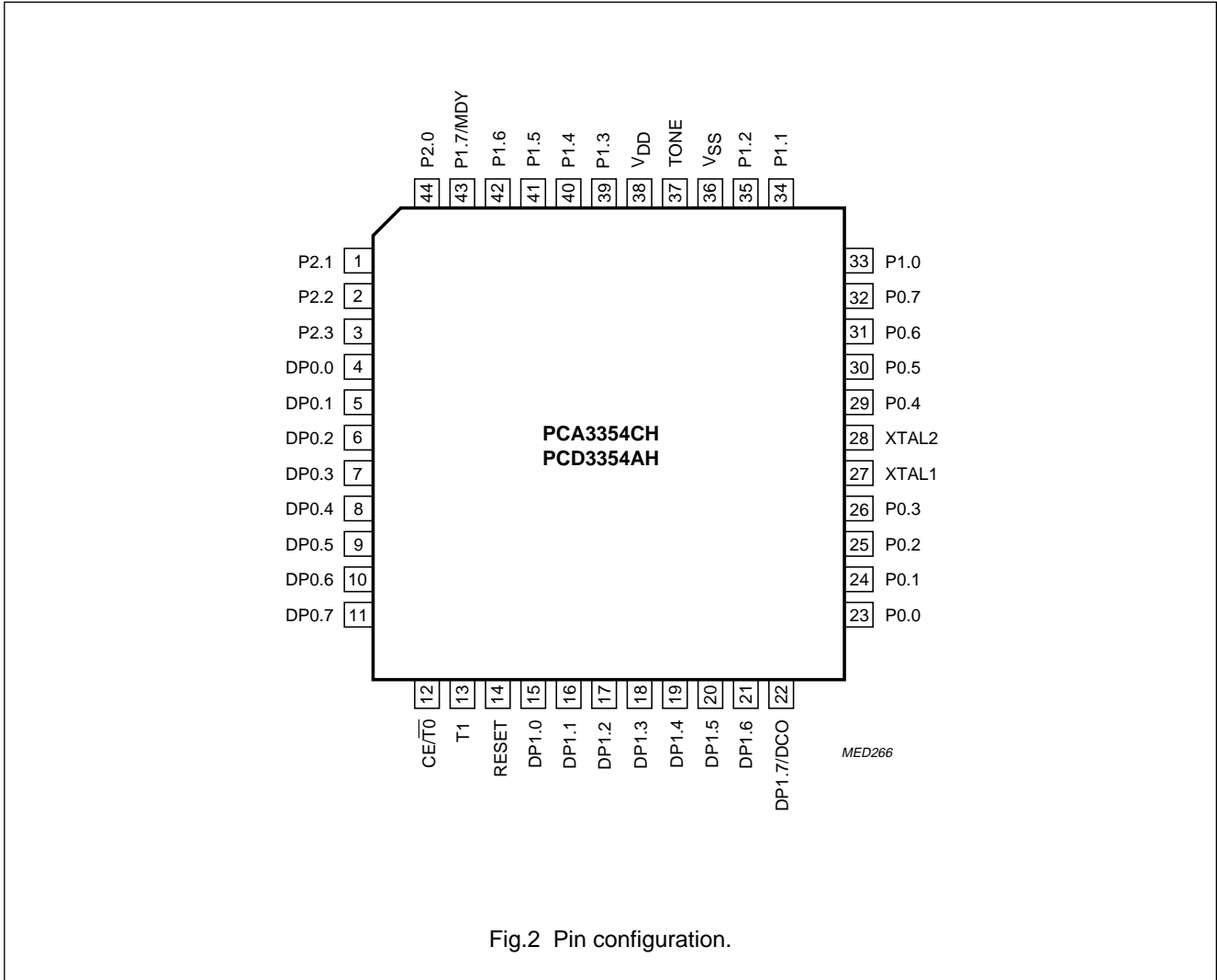
5 PINNING INFORMATION

5.1 Pinning

Fig.2 Pin configuration.

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

5.2   Pin description

Table 2   SOT205-1 package (for information on parallel I/O ports, see Chapter 13)

SYMBOL	PIN	TYPE	DESCRIPTION
P2.1 to P2.3	1 to 3	I/O	3 bits of Port 2: 4-bit quasi-bidirectional I/O port
DP0.0 to DP0.7	4 to 11	I/O	Derivative Port 0: 8-bit quasi-bidirectional I/O port
CE/$\overline{\text{T0}}$	12	I	Chip Enable or Test 0 input
T1	13	I	Test 1/count input of 8-bit Timer/event counter 1
RESET	14	I	reset input
DP1.0 to DP1.6	15 to 21	I/O	7 bits of Derivative Port 1: 8-bit quasi-bidirectional I/O port
DP1.7/DCO	22	I/O	1 bit of Derivative Port 1: 8-bit quasi-bidirectional I/O port; or DTMF clock output
P0.0 to P0.3	23 to 26	I/O	4 bits of Port 0: 8-bit quasi-bidirectional I/O port
XTAL1	27	I	crystal oscillator/external clock input
XTAL2	28	O	crystal oscillator output
P0.4 to P0.7	29 to 32	I/O	4 bits of Port 0: 8-bit quasi-bidirectional I/O port
P1.0 to P1.2	33 to 35	I/O	3 bits of Port 1: 8-bit quasi-bidirectional I/O port
V$_{SS}$	36	P	ground
TONE	37	O	DTMF output
V$_{DD}$	38	P	positive supply voltage
P1.3 to P1.6	39 to 42	I/O	4 bits of Port 1: 8-bit quasi-bidirectional I/O port
P1.7/MDY	43	I/O	1 bit of Port 1: 8-bit quasi-bidirectional I/O port; or melody output
P2.0	44	I/O	1 bit of Port 2: 4-bit quasi-bidirectional I/O port

6 FREQUENCY GENERATOR

A versatile frequency generator section with built-in programmable clock divider is provided (see Fig.3). The clock divider allows the DTMF section to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = \frac{1}{3} \times f_{xtal}$) depending on the state of the divider control bit DIV3 (see Table 5). The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available. Their frequencies are provided either in purely sinusoidal form on the TONE output or as a square wave on the port line P1.7/MDY. The latter is typically for ringer applications in telephone sets. If no frequency output is selected the TONE output is in 3-state mode.

6.1 Frequency generator derivative registers

6.1.1 HIGH AND LOW GROUP FREQUENCY REGISTERS

Table 3 gives the addresses, symbols and access types of the High Group Frequency (HGF) and Low Group Frequency (LGF) registers, used to set the frequency output.

Table 3 Hexadecimal addresses, symbols, access types and bit symbols of the frequency registers

REGISTER ADDRESS	REGISTER SYMBOL	ACCESS TYPE	BIT SYMBOLS							
			7	6	5	4	3	2	1	0
11H	HGF	W	H7	H6	H5	H4	H3	H2	H1	H0
12H	LGF	W	L7	L6	L5	L4	L3	L2	L1	L0

6.1.2 CLOCK AND MELODY CONTROL REGISTER (MDYCON)

Table 4 Clock and Melody Control Register, MDYCON (address 13H; access type R/W)

7	6	5	4	3	2	1	0
0	0	0	0	0	EDCO	DIV3	EMO

Table 5 Description of MDYCON bits

| BIT	SYMBOL	DESCRIPTION
7 to 3	–	These bits are set to a logic 0.
2	EDCO	Enable DTMF clock output. If bit EDCO = 0, then DP1.7/DCO is a general purpose derivative port line. If bit EDCO = 1, then DP1.7/DCO is the DTMF clock output. EDCO = 1 does not inhibit the port instructions for DP1.7/DCO. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by derivative port instructions. However, the port flip-flop of DP1.7/DCO must remain set to avoid conflicts between DTMF clock and port outputs.
1	DIV3	Enable DTMF clock divider. If bit DIV3 = 0, then the DTMF clock $f_{DTMF} = f_{xtal}$. If bit DIV3 = 1, then $f_{DTMF} = \frac{1}{3} \times f_{xtal}$.
0	EMO	Enable Melody Output. If bit EMO = 0, then P1.7/MDY is a standard port line. If bit EMO = 1, then P1.7/MDY is the melody output. EMO = 1 does not inhibit the port instructions for P1.7/MDY. Therefore the state of both port line and flip-flop may be read in and the port flip-flop may be written by port instructions. However, the port flip-flop of P1.7/MDY must remain set to avoid conflicts between melody and port outputs. When the HGF contents are zero while EMO = 1, P1.7/MDY is in the HIGH state.
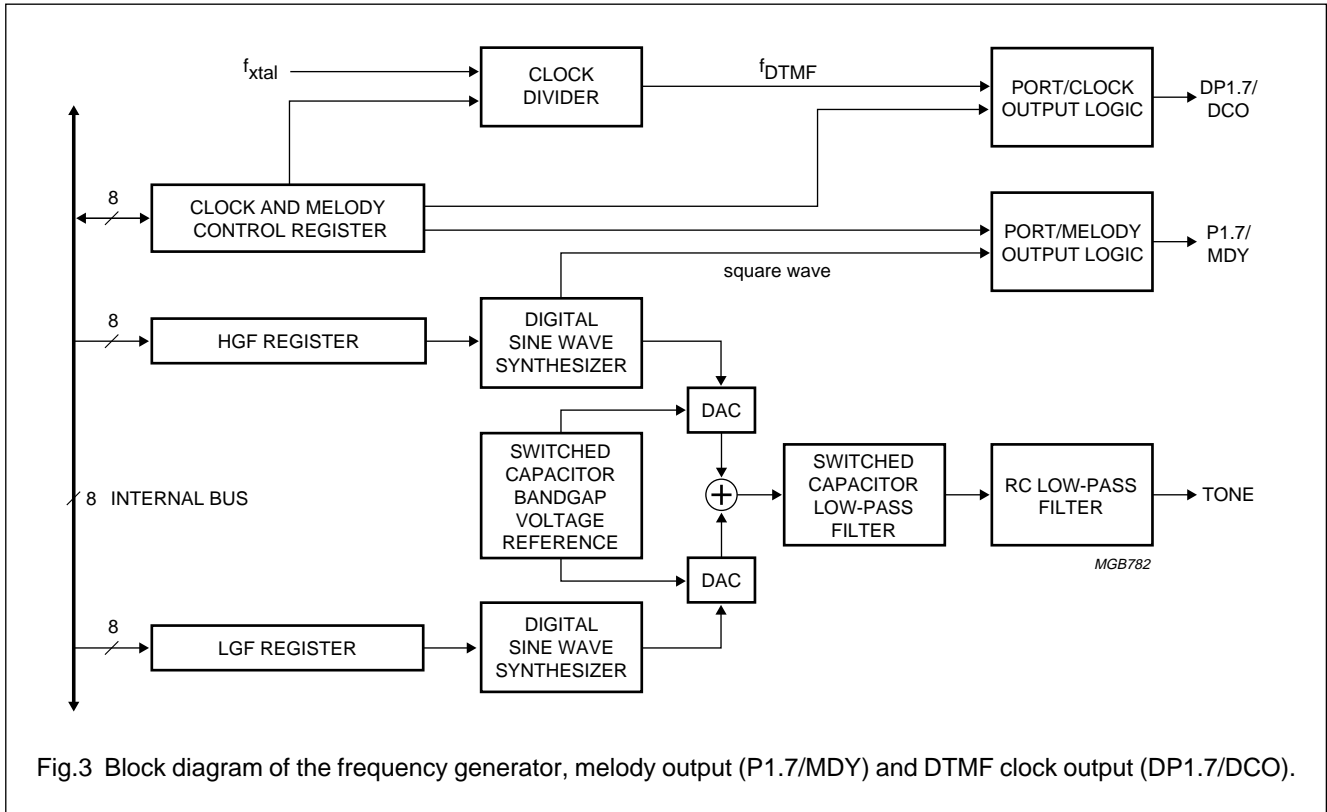
Fig.3 Block diagram of the frequency generator, melody output (P1.7/MDY) and DTMF clock output (DP1.7/DCO).

6.2 Melody output (P1.7/MDY)

The melody output (P1.7/MDY) is very useful for generating musical notes when a purely sinusoidal signal is not required, such as for ringer applications.

The square wave (duty cycle = $^{12}/_{23}$ or 52%) will include the attenuated harmonics of the base frequency, which is defined by the contents of the HGF register (Table 3). However, even higher frequency notes may be produced since the low-pass filtering on the TONE output is not applied to the P1.7/MDY output. This results in the minimum decimal value x in the HGF register (see equation in Section 6.4) being 2 for the P1.7/MDY output, rather than 60 for the TONE output. A sinusoidal TONE output is produced at the same time as the melody square wave, but due to the filtering, the higher frequency sine waves with x < 60 will not appear at the TONE output.

Since the melody output is shared with P1.7, the port flip-flop of P1.7 has to be set HIGH before using the melody output. This is to avoid conflicts between melody and port outputs. The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 13, Table 24.

6.3 DTMF clock divider and output (DP1.7/DCO)

The DTMF clock divider allows the DTMF part to run either with the main clock frequency ($f_{DTMF} = f_{xtal}$) or with a third of it ($f_{DTMF} = \frac{1}{3} \times f_{xtal}$) depending on the state of the divider control bit DIV3 in register MDYCON.

For low power applications, a 3.58 MHz quartz crystal or PXE resonator can be chosen together with the divide-by-one function of the clock divider.

For other applications a 10.74 MHz quartz crystal or PXE resonator may be chosen together with the divide-by-three function of the clock divider. This triples the program speed of the microcontroller, thereby keeping the assumed DTMF frequency of 3.58 MHz.

Since a 3.58 MHz clock is needed for peripheral telephony circuits such as the analog voice scrambler/descrambler PCD4440T, a switchable DTMF clock output is provided depending on the state of the enable clock output bit EDCO in register MDYCON.

8-bit microcontrollers with DTMF generator and 256 bytes EEPROM

PCA3354C; PCD3354A

If EDCO = 1 and DIV3 = 1 in the MDYCON register: a square wave with the frequency $f_{DTMF} = \frac{1}{3} \times f_{xtal}$ is output on the derivative port line DP1.7/DCO. If EDCO = 1 and DIV3 = 0: a square wave with the frequency $f_{DTMF} = f_{xtal}$ is output on the derivative port line DP1.7/DCO.

The melody output drive depends on the configuration of port P1.7/MDY, see Chapter 13, Table 24.

6.4 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures tone output levels independent of supply voltage and temperature. The amplitude of the Low Group Frequency sine wave is attenuated by 2 dB compared to the amplitude of the High Group Frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency 'f' of the sine wave generated from either of the frequency registers is a function of the clock frequency 'f_{xtal}' and the decimal value 'x' held in the register. The equation relating these variables is:

$$f = \frac{f_{xtal}}{[\,23\,(x+2)\,]}; \text{ where } 60 \le x \le 255.$$

The frequency limitation given by $x \ge 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.5 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 6.

The relationship between telephone keyboard symbols, DTMF frequency pairs and the corresponding frequency register contents are given in Table 7.

Table 6 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 7 Dialling symbols, corresponding DTMF frequency pairs and frequency register contents

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

6.6 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz,
the standard modem frequencies can be implemented as
in Table 8. It is suggested to define the frequency by the
HGF register while the LGF register contains 00H,
disabling Low Group Frequency generation.

Table 8 Standard modem frequencies and their
implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.7 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones
can be realized, again assuming an oscillator frequency
f_{xtal} = 3.58 MHz (Table 9). It is suggested to define the
frequency by the HGF register while the LGF contains
00H, disabling Low Group Frequency generation.

Table 9 Musical scale frequencies and their
implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7   EEPROM AND TIMER 2 ORGANIZATION

The PCA3354C; PCD3354A have 256 bytes of Electrically Erasable Programmable Read Only Memory (EEPROM). Such non-volatile storage provides data retention without the need for battery backup. In telecom applications, the EEPROM is used for storing redial numbers and for short dialling of frequently used numbers. More generally, EEPROM may be used for customizing microcontrollers, such as to include a PIN code or a country code, to define trimming parameters, to select application features from the range stored in ROM.

The most significant difference between a RAM and an EEPROM is that a bit in EEPROM, once written to a logic 1, cannot be cleared by a subsequent write operation. Successive write accesses actually perform a logical OR with the previously stored information. Therefore, to clear a bit, the whole byte must be erased and re-written with the particular bit cleared. Thus, an erase-and-write operation is the EEPROM equivalent of a RAM write operation.

Whereas read access times to an EEPROM are comparable to RAM access times, write and erase accesses are much slower at 5 ms each. To make these operations more efficient, several provisions are available in the PCA3354C; PCD3354A.

First, the EEPROM array is structured into 64 four-byte pages (see Fig.4) permitting access to 4 bytes in parallel (write page, erase/write page and erase page). It is also possible to erase and write individual bytes.

Finally, the EEPROM address register provides auto-incrementing, allowing very efficient read and write accesses to sequential bytes.

To simplify the erase and write timing, the derivative 8-bit down-counter (Timer 2) with reload register is provided. In addition to EEPROM timing, Timer 2 can be used for general real-time tasks, such as for measuring signal duration and for defining pulse widths.
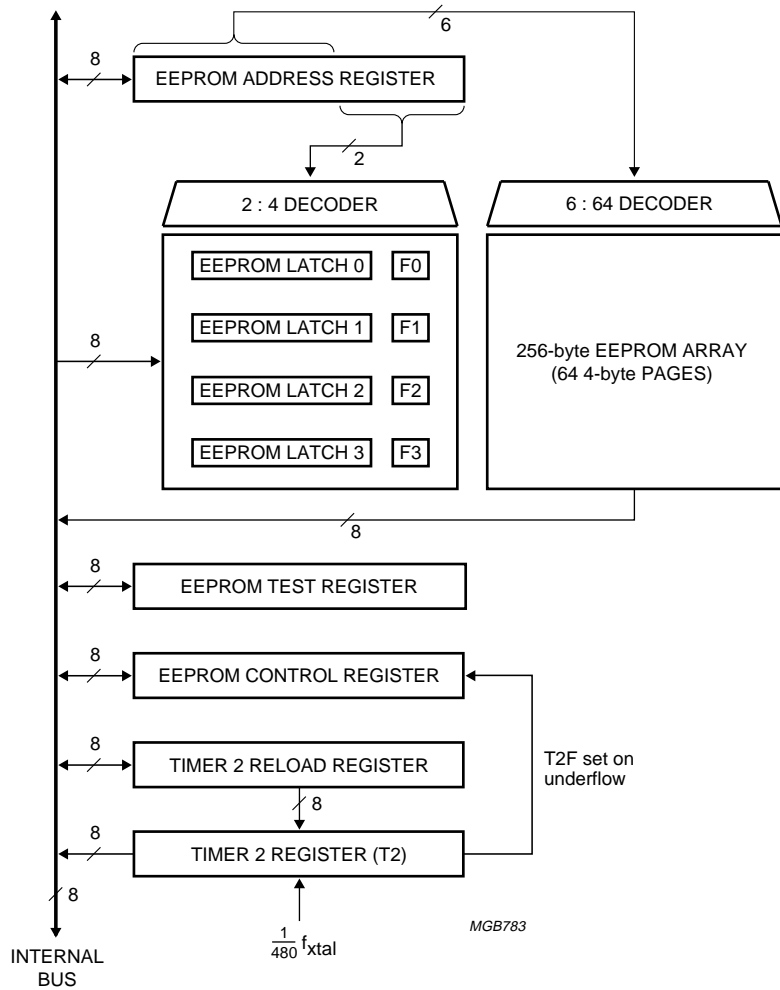
Fig.4 Block diagram of the EEPROM and Timer 2.

7.1 EEPROM registers

7.1.1 EEPROM CONTROL REGISTER (EPCR)

The behaviour of the EEPROM and Timer 2 section is defined by the EEPROM Control Register. See Tables 10, 11 and 12.

Table 10 EEPROM Control Register (address 04H, access type R/W)

7	6	5	4	3	2	1	0
STT2	ET2I	T2F	EWP	MC3	MC2	MC1	0

Table 11 Description of the EPCR bits

BIT	SYMBOL	DESCRIPTION
7	STT2	Start T2. If STT2 = 0, then Timer 2 is stopped; T2 value held. If STT2 = 1, then T2 decrements from reload value.
6	ET2I	Enable T2 interrupt. If ET2I = 0, then T2F event cannot request interrupt. If ET2I = 1, then T2F event can request interrupt.
5	T2F	Timer 2 flag. Set when T2 underflows (or by program); reset by program.
4	EWP	Erase or write in progress (EWP). Set by program (EWP starts EEPROM erase and/or write and Timer 2). Reset at the end of EEPROM erase and/or write.
3	MC3	Mode control 3 to 1. These three bits in conjunction with bit EWP select the mode as shown in Table 12.
2	MC2	
1	MC1	
0	–	This bit is set to a logic 0.

Table 12 Mode selection; X = don't care

EWP	MC3	MC2	MC1	DESCRIPTION
0	0	0	0	read byte
0	0	1	0	increment mode
1	0	1	X	write page
1	1	0	0	erase/write page
1	1	1	1	erase page
X	0	0	1	not allowed
X	1	0	1	
X	1	1	0	

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

7.1.2   EEPROM ADDRESS REGISTER (ADDR)

The EEPROM Address Register determines the EEPROM location to which an EEPROM access is directed.

As a whole, ADDR auto-increments after read and write cycles to EEPROM, but remains fixed after erase cycles. This behaviour generates the correct ADDR contents for sequential read accesses and for sequential write or erase/write accesses with intermediate page setup. Overflow of the 8-bit counter wraps around to zero.

Table 13 EEPROM Address Register (address 01H, access type R/W)

7	6	5	4	3	2	1	0
0	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Table 14 Description of ADDR bits

BIT	SYMBOL	DESCRIPTION
7	–	This bit is set to a logic 0.
6 to 2	AD6 to AD2	AD2 to AD6 select one of 32 pages.
1 to 0	AD1 to AD0	AD1 and AD0 are irrelevant during erase and write cycles. For read accesses, AD0 and AD1 indicate the byte location within an EEPROM page. During page setup, finally, AD0 and AD1 select EEPROM Latch 0 to 3 whereas AD2 to AD6 are irrelevant. If increment mode (Table 12) is active during page setup, the subcounter consisting of AD0 and AD1 increments after every write to an EEPROM latch, thus enhancing access to sequential EEPROM latches. Incrementing stops when EEPROM Latch 3 is reached, i.e. when AD0 and AD1 are both a logic 1.

7.1.3   EEPROM DATA REGISTER (DATR)

Table 15 EEPROM Data Register (address 03H; access type R/W)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Table 16 Description of DATR bits

BIT	SYMBOL	DESCRIPTION
7 to 0	D7 to D0	The EEPROM Data Register (DATR) is only a conceptual entity. A read operation from DATR, reads out the EEPROM byte addressed by ADDR. On the other hand, a write operation to DATR, loads data into the EEPROM latch (see Fig.4) defined by bits AD0 and AD1 of ADDR.

7.1.4   EEPROM TEST REGISTER (TST)

The EEPROM Test register is used for testing purposes during device manufacture. It must not be accessed by the device user.

7.2　EEPROM latches

The four EEPROM latches (EEPROM Latch 0 to 3; Fig.4)
cannot be read by user software. Due to their construction,
the latches can only be preset, but not cleared. Successive
write operations through DATR to the EEPROM latches
actually perform a logical OR with the previously stored
data in EEPROM. The EEPROM latches are reset at the
conclusion of any EEPROM cycle.

7.3　EEPROM flags

The four EEPROM flags (F0 to F3; Fig.4) cannot be
directly accessed by user software. An EEPROM flag is
set as a side-effect when the corresponding EEPROM
latch is written through DATR. The EEPROM flags are
reset at the conclusion of any EEPROM cycle.

7.4　EEPROM macros

The instruction sequence used in an EEPROM access
should be treated as an indivisible entity. Erroneous
programs result if ADDR, DATR, RELR or EPCR are
inadvertently changed during an EEPROM cycle or its
setup. Special care should be taken if the program may
asynchronously divert due to an interrupt. A new access to
the EEPROM may only be initiated when no write, erase or
erase/write cycles are in progress. This can be verified by
reading bit EWP (register EPCR).

For write, erase and erase/write cycles, it is assumed that
the Timer 2 Reload Register (RELR) has been loaded with
the appropriate value for a 5 ms delay, which depends on
f_{xtal} (see Table 23). The end of a write, erase or erase/write
cycle will be signalled by a cleared EWP and by a Timer 2
interrupt provided that ET2I = 1 and that the derivative
interrupt is enabled.

7.5　EEPROM access

One read, one write, one erase/write and one erase
access are defined by bits EWP and MC1 to MC3 in the
EPCR register; see Table 10.

Read byte retrieves the EEPROM byte addressed by
ADDR when DATR is read. Read cycles are
instantaneous.

Write and erase cycles take 5 ms, however. Erase/write is
a combination of an erase and a subsequent write cycle,
consequently taking 10 ms.

As their names imply, **write page, erase page and
erase/write page** are applied to a whole EEPROM page.
Therefore, bits AD0 and AD1 of register ADDR (see
Table 13), defining the byte location within an EEPROM

page, are irrelevant during write and erase cycles.
However, write and erase cycles need not affect all bytes
of the page. The EEPROM flags F0 to F3 (see Fig.4)
determine which bytes within the EEPROM page are
affected by the erase and/or write cycles. A byte whose
corresponding EEPROM flag is zero remains unchanged.

With erase page, a byte is erased if its corresponding
EEPROM flag is set. With write page, data in EEPROM
latches 0 to 3 (Fig.4) are ORed to the individual page bytes
if and only if the corresponding EEPROM flags are set.

In an erase/write cycle, F0 to F3 select which page bytes
are erased and ORed with the corresponding EEPROM
latches.

ORing, in this event, means that the EEPROM latches are
copied to the selected page bytes.

The described page-wise organization of erase and write
cycles allows up to four bytes to be individually erased or
written within 5 ms. This advantage necessitates a
preparation step, called **page setup**, before the actual
erase and/or write cycle can be executed.

Page setup controls EEPROM latches and EEPROM
flags. This will be described in the Sections 7.5.1 to 7.5.5.

7.5.1　PAGE SETUP

Page setup is a preparation step required before write
page, erase page and erase/write page cycles.
As previously described, these page operations include
single-byte write, erase and erase/write as a special event.
EEPROM flags F0 to F3 determine which page bytes will
be affected by the mentioned page operations. EEPROM
Latch 0 to 3 must be preset through DATR to specify the
write cycle data to EEPROM and to set the EEPROM flags
as a side-effect.

Obviously, the actual preset value of the EEPROM latches
is irrelevant for erase page. Preset of one, two, three or all
four EEPROM latches and the corresponding EEPROM
flags can be performed by repeatedly defining ADDR and
writing to DATR (see Table 17).

If more than one EEPROM latch must be preset, the
subcounter consisting of AD0 and AD1 can be induced to
auto-increment after every write to DATR, thus stepping
through all EEPROM latches. For this purpose, increment
mode (Table 12) must be selected. Auto-incrementing
stops at EEPROM Latch 3. It is not mandatory to start at
EEPROM Latch 0 as in shown in Table 18.

Note that AD2 to AD6 are irrelevant during page setup.
They will usually specify the intended EEPROM page,
anticipating the subsequent page cycle.

From now on, it will be assumed that AD2 to AD6 will
contain the intended EEPROM page address after page
setup.

Table 17 Page setup; preset

INSTRUCTION	RESULT
MOV A, #addr	address of EEPROM latch
MOV ADDR, A	send address to ADDR
MOV A, #data	load write, erase/write or erase data
MOV DATR, A	send data to addressed EEPROM latch

Table 18 Page setup; auto-incrementing

INSTRUCTION	RESULT
MOV A, #MC2	increment mode control word
MOV EPCR, A	select increment mode
MOV A, #baddr	EEPROM Latch 0 address (AD0 = AD1 = 0)
MOV ADDR, A	send EEPROM Latch 0 address to ADDR
MOV A, R0	load 1st byte from Register 0
MOV DATR, A	send 1st byte to EEPROM Latch 0
MOV A, R1	load 2nd byte from Register 1
MOV DATR, A	send 2nd byte to EEPROM Latch 1
MOV A, R2	load 3rd byte from Register 2
MOV DATR, A	send 3rd byte to EEPROM Latch 2
MOV A, R3	load 4th byte from Register 3
MOV DATR, A	send 4th byte to EEPROM Latch 3

7.5.2   READ BYTE

Since ADDR auto-increments after a read cycle regardless
of the page boundary, successive bytes can efficiently be
read by repeating the last instruction.

Table 19 Read byte

INSTRUCTION	RESULT
MOV A, #RDADDR	load read address
MOV ADDR, A	send address to ADDR
MOV A, DATR	read EEPROM data

7.5.3   WRITE PAGE

The write cycle performs a logical OR between the data in
the EEPROM latches and that in the addressed EEPROM
page. To actually copy the data from the EEPROM

latches, the corresponding bytes in the page should
previously have been erased.

The EEPROM latches are preset as described in
Section 7.5.1. The actual transfer to the EEPROM is then
performed as shown in Table 20.

The last instruction also starts Timer 2. The data in the
EEPROM latches are ORed with that in the corresponding
page bytes within 5 ms. A single-byte write is simply a
special case of 'write page'.

ADDR auto-increments after the write cycle. If AD0 and
AD1 addressed EEPROM Latch 3 prior to the write cycle,
ADDR will point to the next EEPROM page (by bits AD2
to AD6) and to EEPROM Latch 0 (by bits AD0 and AD1).
This allows efficient coding of multi-page write operations.

Table 20 Write page

INSTRUCTION	RESULT
MOV A, #EWP + MC2	'write page' control word
MOV EPCR, A	start 'write page' cycle

7.5.4   ERASE/WRITE PAGE

The EEPROM latches are preset as described in
Section 7.5.1. The page byte corresponding to the
asserted flags (among F0 to F3) are erased and re-written
with the contents of the respective EEPROM latches.

The last instruction also starts Timer 2. Erasure takes
5 ms upon which Timer Register T2 reloads for another
5 ms cycle for writing. The top cycles together take 10 ms.
A single-byte erase/write is simply a special event of
'erase/write page'.

ADDR auto-increments after the write cycle. If AD0 and
AD1 addressed EEPROM Latch 3 prior to the write cycle,
ADDR will point to the next EEPROM page (by AD2 to
AD6) and to EEPROM Latch 0 (by AD0 and AD1).
This allows efficient coding of multi-page erase/write
operations.

Table 21 Erase/write page

INSTRUCTION	RESULT
MOV A, #EWP + MC3	'erase/write page' control word
MOV EPCR, A	start 'erase/write page' cycle

7.5.5   ERASE PAGE

The EEPROM flags are set as described in Section 7.5.1.
The corresponding page bytes are erased.

The last instruction also starts Timer 2. Erasure takes
5 ms. A single-byte erase is simply a special case of 'erase
page'.

Note that ADDR does not auto-increment after an erase
cycle.

Table 22 Erase page

INSTRUCTION	RESULT
MOV A, #EWP + MC3 + MC2 + MC1	'erase page' control word
MOV EPCR, A	start 'erase page' cycle

7.6   Timer 2

Timer 2 is a 8-bit down-counter decremented at a rate of
$^1/_{480} \times f_{xtal}$. It may be used either for EEPROM timing or as
a general purpose timer. Conflicts between the two
applications should be carefully avoided.

7.6.1   TIMER 2 FOR EEPROM TIMING

When used for EEPROM timing, Timer 2 serves to
generate the 5 ms intervals needed for erasing or writing
the EEPROM. At the decrement rate of $^1/_{480} \times f_{xtal}$, the
reload value for a 5 ms interval is a function of f_{xtal}.
Table 23 summarizes the required reload values for a
number of oscillator frequencies.

Timer 2 is started by setting bit EWP in the EPCR.
The Timer Register T2 is loaded with the reload value from
RELR. T2 decrements to zero.

For an erase/write cycle, underflow of T2 indicates the end
of the erase operation. Therefore, Timer Register T2 is
reloaded from RELR for another 5 ms interval during
which the flagged EEPROM latches are copied to the
corresponding bytes in the page addressed by ADDR.

The second underflow of an erase/write cycle and the first
underflow of write page and erase page conclude the
corresponding EEPROM cycle. Timer 2 is stopped, T2F is
set whereas EWP and MC1 to MC3 are cleared.

Table 23 Reload values as a function of f_{xtal}

f_{xtal} (MHz)	RELOAD VALUE[1] (HEX)
1	0A
2	14
3.58	25
6	3E
10.74	6F
16	A6

Note

1.   The reload value is $(5 \times 10^{-3} \times ^1/_{480} \times f_{xtal}) - 1$;
     f_{xtal} in MHz.

7.6.2   TIMER 2 AS A GENERAL PURPOSE TIMER

When used for purposes other than EEPROM timing,
Timer 2 is started by setting STT2. The Timer 2 Register
T2 (see Table 25) is loaded with the reload value from
RELR. T2 decrements to zero. On underflow, T2 is
reloaded from RELR, T2F is set and T2 continues to
decrement.

Timer 2 can be stopped at any time by clearing STT2.
The value of T2 is then held and can be read out. After
setting STT2 again, Timer 2 decrements from the reload
value. Alternatively, it is possible to read T2 'on the fly' i.e.
while Timer 2 is operating.

8 DERIVATIVE INTERRUPTS

One derivative interrupt event is defined. It is controlled by bits T2F and ET2I in the EPCR (see Tables 10 and 11).

The derivative interrupt event occurs when T2F is set. This request is honoured under the following circumstances:

- No interrupt routine proceeds
- No external interrupt request is pending
- The derivative interrupt is enabled
- ET2I is set.

The derivative interrupt routine must include instructions that will remove the cause of the derivative interrupt by explicitly clearing T2F. If the derivative interrupt is not used, T2F may directly be tested by the program. Obviously, T2F can also be asserted under program control, e.g. to generate a software interrupt.

9 TIMING

Although the PCA3354C; PCD3354A operate over a clock frequency range from 1 MHz to 16 MHz, $f_{xtal} = 3.58$ MHz or 10.74 MHz will usually be chosen to take full advantage of the frequency generator section.

10 RESET

In addition to the conditions given in the *"PCD33xxA Family"* data sheet, all derivative registers are cleared in the reset state.

11 IDLE MODE

In Idle mode, the frequency generator, the EEPROM and the Timer 2 sections remain operative. Therefore, the IDLE instruction may be executed while an erase and/or write access to EEPROM is in progress.

12 STOP MODE

Since the oscillator is switched off, the frequency generator, the EEPROM and the Timer 2 sections receive no clock. It is suggested to clear both the HGF and the LGF registers before entering stop mode. This will cut off the biasing of the internal amplifiers, considerably reducing current requirements.

The Stop mode **must not** be entered while an erase and/or write access to EEPROM is in progress. The STOP instruction may only be executed when EWP in EPCR is zero. The Timer 2 section is frozen during Stop mode. After exit from Stop mode by a HIGH level on CE/$\overline{T0}$, Timer 2 proceeds from the held state.

13 SUMMARY OF I/O PORTS AND MASK OPTIONS

All standard quasi-bidirectional I/O ports are available; see *"PCD33xxA Family"* data sheet.

- Port 0: 8 parallel port lines P0.0 to P0.7
- Port 1: 8 parallel port lines P1.0 to P1.7
- Port 2: 4 parallel port lines P2.0 to P2.3.

In addition to the standard ports, 2 derivative I/O ports are available:

- Derivative Port 0: 8 parallel port lines DP0.0 to DP0.7 (register DP0L)
- Derivative Port 1: 8 parallel port lines DP1.0 to DP1.7 (register DP1L).

The port options and the other ROM mask options are listed in Table 24. See Table 25 for the addresses of DP0L and DP1L.

Table 24 ROM mask options

FUNCTION IMPLEMENTED IN ROM	OPTION		
Program/data	Any mix of instructions and data up to ROM size of 8 kbytes.		
Port Output			
P0.0 to P0.7	standard	open-drain	push-pull
P1.0 to P1.6	standard	open-drain	push-pull
P1.7/MDY; note 1	standard	open-drain	push-pull
P2.0 to P2.3	standard	open-drain	push-pull
DP0.0 to DP0.7	standard	open-drain	push-pull
DP1.0 to DP1.6	standard	open-drain	push-pull
DP1.7/DCO; note 2	standard	open-drain	push-pull
Port State after reset			
P0.0 to P0.7	set	reset	–
P1.0 to P1.6	set	reset	–
P1.7/MDY	set	reset	–
P2.0 to P2.3	set	reset	–
DP0.0 to DP0.7	set	reset	–
DP1.0 to DP1.6	set	reset	–
DP1.7/DCO	set	reset	–
Oscillator			
Transconductance	LOW (g_{mL})	MEDIUM (g_{mM})	HIGH (g_{mH})
Power-on-reset			
Power-on-reset voltage level: V_{POR}	1.2 to 3.6 V in increments of 100 mV; OFF		

Notes

1. If standard (Option 1) or push-pull (Option 3) output is chosen, the P1.7/MDY output becomes a push-pull output. If open-drain (Option 2) is chosen the P1.7/MDY output becomes an open-drain output.

2. If standard (Option 1) or push-pull (Option 3) output is chosen, the DP1.7/DCO output becomes a push-pull output. If open-drain (Option 2) is chosen the DP1.7/DCO output becomes an open-drain output.

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

14 SUMMARY OF DERIVATIVE REGISTERS

Table 25 Register map

ADDR. (HEX)	REGISTER	7	6	5	4	3	2	1	0	R/W
00	not used									
01	EEPROM Address Register (ADDR)	0	AD6	AD5	AD4	AD3	AD2	AD1	AD0	R/W
02	not used									
03	EEPROM Data Register (DATR)	D7	D6	D5	D4	D3	D2	D1	D0	R/W
04	EEPROM Control Register (EPCR)	STT2	ET21	TF2	EWP	MC3	MC2	MC1	0	R/W
05	Timer 2 Reload Register (RELR)	R7	R6	R5	R4	R3	R2	R1	R0	R/W
06	Timer 2 Register (T2)	T2.7	T2.6	T2.5	T2.4	T2.3	T2.2	T2.1	T2.0	R
07	Test Register (TST)	only for test purposes; not to be accessed by the device user								
08 to 10	not used									
11	High Group Frequency Register (HGF)	H7	H6	H5	H4	H3	H2	H1	H0	W
12	Low Group Frequency Register (LGF)	L7	L6	L5	L4	L3	L2	L1	L0	W
13	Clock and Melody Control Register (MDYCON)	0	0	0	0	0	DCO	DIV3	EMO	R/W
14 to 2F	not used									
30	Derivative Port 0 lines (DP0L)	D0.7	D0.6	D0.5	D0.4	D0.3	D0.2	D0.1	D0.0	R
31	Derivative Port 1 lines (DP1L)	D1.7	D1.6	D1.5	D1.4	D1.3	D1.2	D1.1	D1.0	R
32	Derivative Port 0 flip-flop (DP0FF)	F0.7	F0.6	F0.5	F0.4	F0.3	F0.2	F0.1	F0.0	R/W
33	Derivative Port 1 flip-flop (DP1FF)	F1.7	F1.6	F1.5	F1.4	F1.3	F1.2	F1.1	F1.0	R/W
34 to FF	not used									

15 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.8	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I	DC input current	−10	+10	mA
I_O	DC output current	−10	+10	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

16 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Data Handbook IC14, Section: Handling MOS devices"*).

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

17 DC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA3354C) or −25 to +70 °C (PCD3354A); all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	see Fig.5				
	operating	note 1	1.8	–	6	V
	RAM data retention in Stop mode		1.0	–	6	V
I_{DD}	operating supply current	see Figs 6 and 7; note 2				
		V_{DD} = 3 V; value HGF or LGF $\neq$ 0	–	0.8	1.6	mA
		V_{DD} = 3 V; value HGF = LGF = 0	–	0.35	0.7	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF or LGF $\neq$ 0; DIV3 = 1	–	2.7	6.2	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF = LGF = 0	–	1.7	4.2	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); value HGF = LGF = 0	–	3.5	–	mA
$I_{DD(idle)}$	supply current (Idle mode)	see Figs 8 and 9; note 2				
		V_{DD} = 3 V; value HGF or LGF $\neq$ 0	–	0.7	1.4	mA
		V_{DD} = 3 V; value HGF = LGF =0	–	0.25	0.5	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF or LGF $\neq$ 0; DIV3 = 1	–	2.3	5.5	mA
		V_{DD} = 5 V; f_{xtal} = 10.74 MHz (g_{mM}); value HGF = LGF = 0	–	1.3	3.5	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH}); value HGF = LGF = 0	–	2.4	–	mA
$I_{DD(stp)}$	supply current (Stop mode)	See Fig.10; notes 2 and 3				
		V_{DD} = 1.8 V; T_{amb} = 25 °C	–	1.0	5.5	µA
		V_{DD} = 1.8 V; T_{amb} = −25 to +70 °C	–	–	10	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	0.3V_{DD}	V
V_{IH}	HIGH level input voltage		0.7V_{DD}	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	−1	–	+1	µA
Port outputs						
I_{OL}	LOW level output sink current	V_{DD} = 3 V; V_O = 0.4 V; see Fig.11	0.7	3.5	–	mA
I_{OH}	HIGH level pull-up output source current	V_{DD} = 3 V; V_O = 2.7 V; see Fig.12	−10	−30	–	µA
		V_{DD} = 3 V; V_O = 0 V; see Fig.12	–	−140	−300	µA
I_{OH1}	HIGH level push-pull output source current	V_{DD} = 3 V; V_O = 2.6 V; see Fig.13	−0.7	−3.5	–	mA

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
TONE output (see Fig.14; notes 1 and 4)						
$V_{HG(RMS)}$	HGF voltage (RMS values)		158	181	205	mV
$V_{LG(RMS)}$	LGF voltage (RMS values)		125	142	160	mV
$\Delta f / f$	frequency deviation		−0.6	−	0.6	%
V_{DC}	DC voltage level		−	$0.5V_{DD}$	−	V
$|Z_O|$	output impedance		−	100	500	Ω
G_v	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	−	−25	−	dB
EEPROM (notes 1 and 6)						
n_{cyc}	endurance (erase/write cycles)	note 7	10^5	−	−	
t_{ret}	data retention		10	−	−	years
Power-on-reset (see Fig.15)						
ΔV_{POR}	Power-on-reset level variation around chosen V_{POR}	note 8; for PCD3354A	−0.5	0	+0.5	V
V_{POR}	Power-on-reset level	note 9; for PCA3354C	1.7	2.0	2.3	V
Oscillator (see Fig.16)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance	V_{DD} = 5 V	0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance	V_{DD} = 5 V	3	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	$M\Omega$

Notes to the DC characteristics

1. TONE output; EEPROM erase and write require $V_{DD} \geq 2.5$ V:

    a) TONE output requires f_{xtal} < 4 MHz in case DIV3 = 0.

    b) TONE output requires f_{xtal} < 12 MHz in case DIV3 = 1.

2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open:

    a) Maximum values: external clock at XTAL1 and XTAL2 open-circuit.

    b) Typical values: T_{amb} = 25 °C; crystal connected between XTAL1 and XTAL2.

3. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; RESET, T1 and CE/$\overline{T0}$ at V_{SS}; crystal connected between XTAL1 and XTAL2; open-drain outputs connected to V_{SS}; all other outputs open.

4. Values are specified for DTMF frequencies only (CEPT).

5. Related to the Low Group Frequency (LGF) component (CEPT).

6. After final testing the value of each EEPROM bit is typically logic 1.

7. Verified on sampling basis.

8. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.

9. Each device is tested on the condition: $V_{DD(min)} < V_{POR}$; to ensure a correct start-up, even for slow rising supply voltages.

8-bit microcontrollers with DTMF
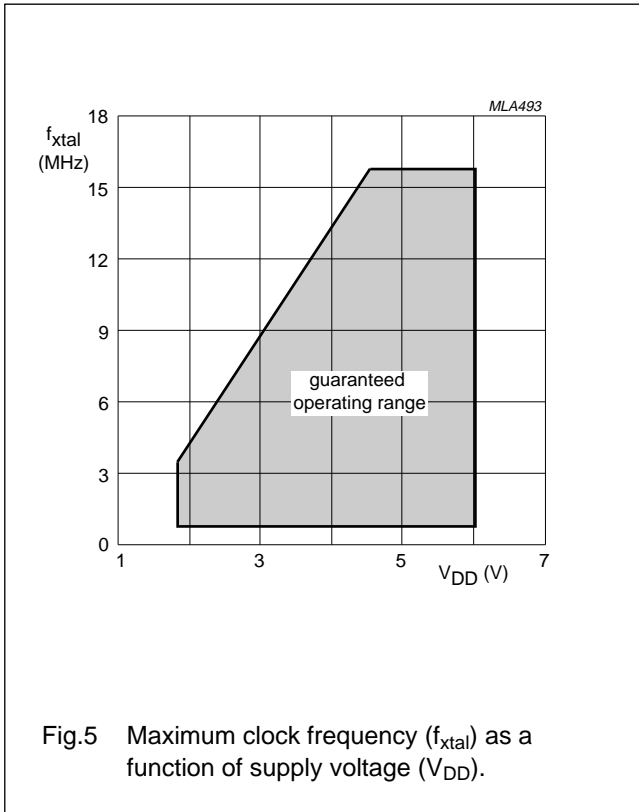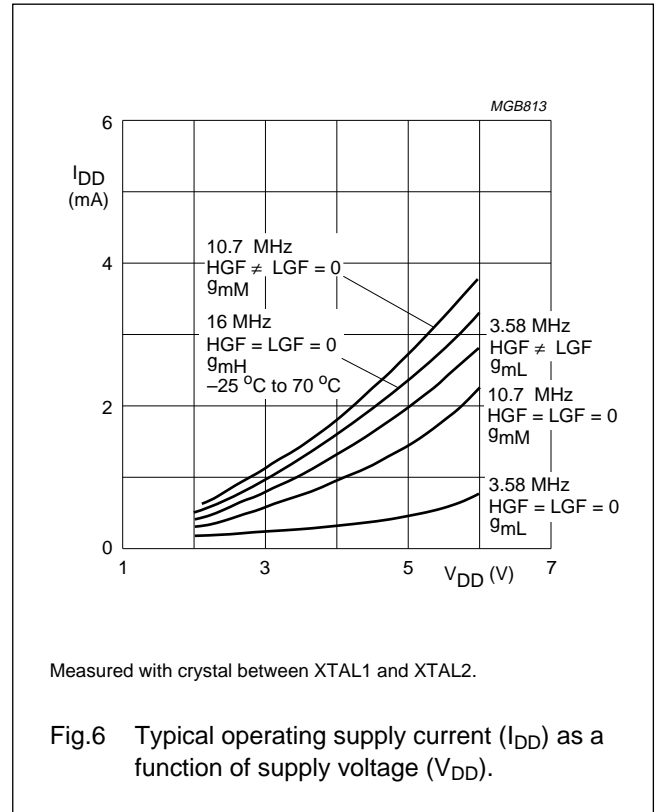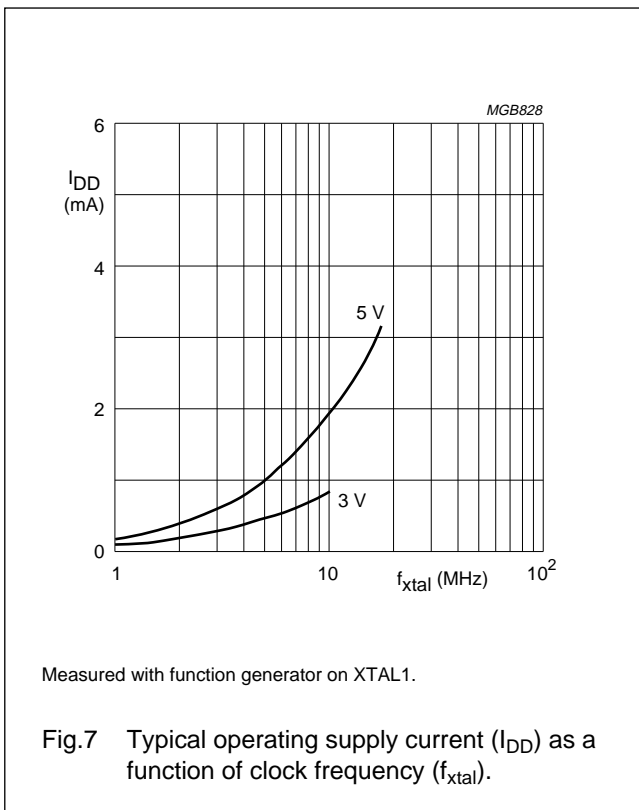generator and 256 bytes EEPROM

PCA3354C; PCD3354A

Fig.5   Maximum clock frequency (f_{xtal}) as a
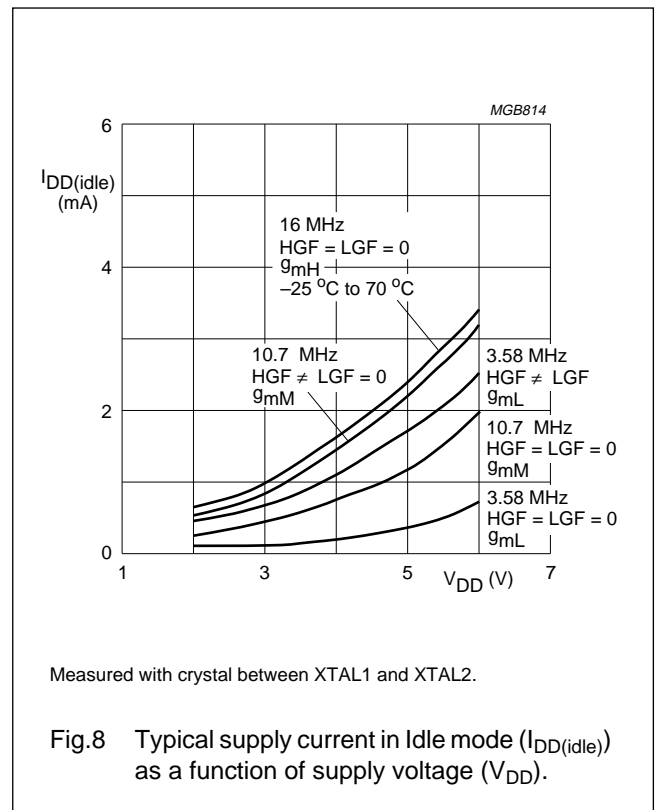function of supply voltage (V_{DD}).

Measured with crystal between XTAL1 and XTAL2.

Fig.6   Typical operating supply current (I_{DD}) as a
function of supply voltage (V_{DD}).

Measured with function generator on XTAL1.

Fig.7   Typical operating supply current (I_{DD}) as a
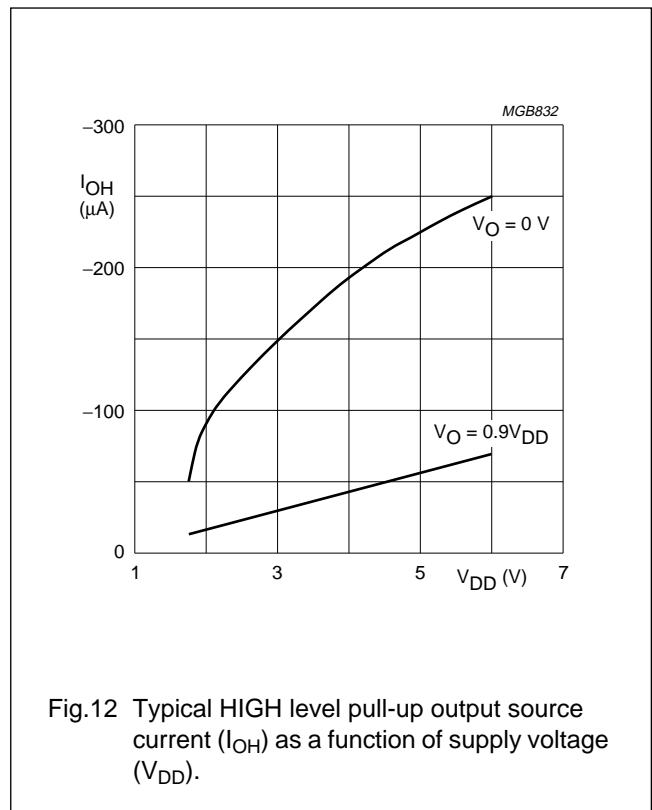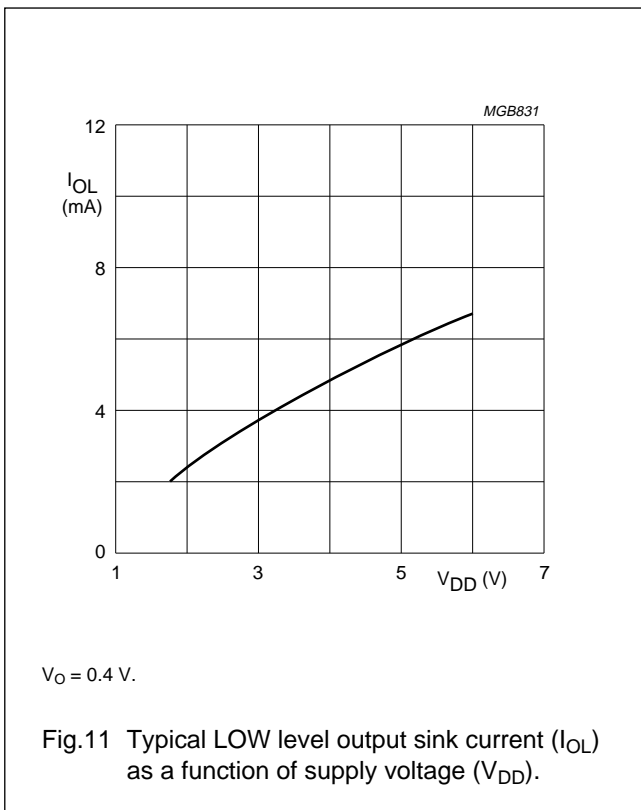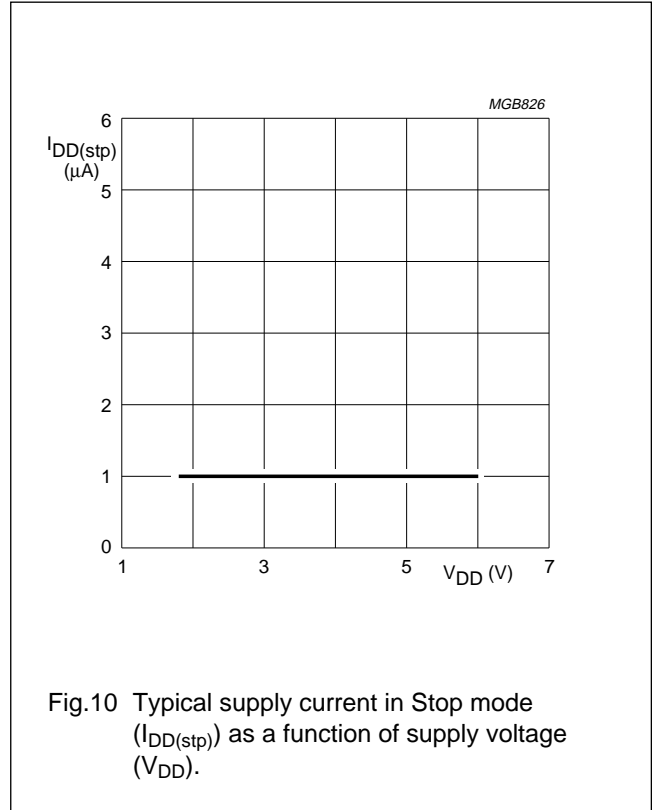function of clock frequency (f_{xtal}).

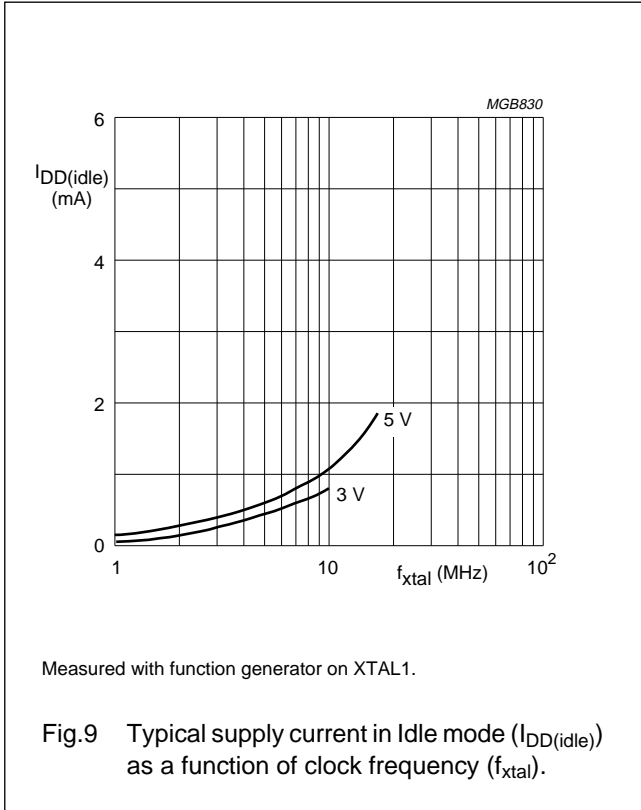
Measured with crystal between XTAL1 and XTAL2.

Fig.8   Typical supply current in Idle mode ($I_{DD(idle)}$)
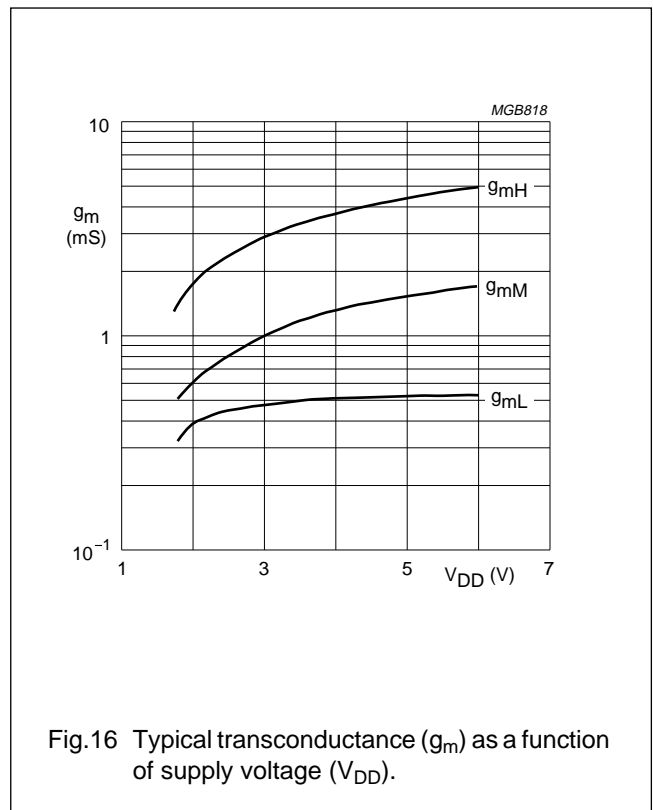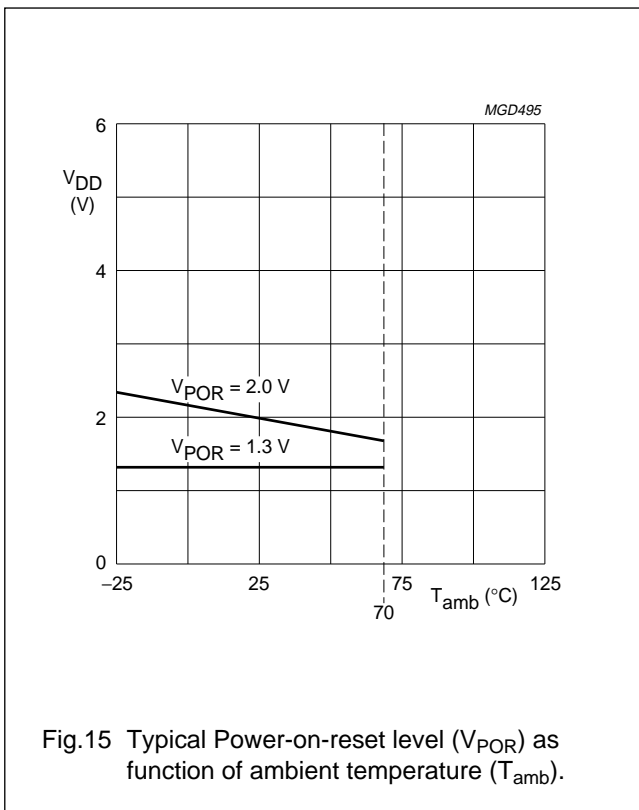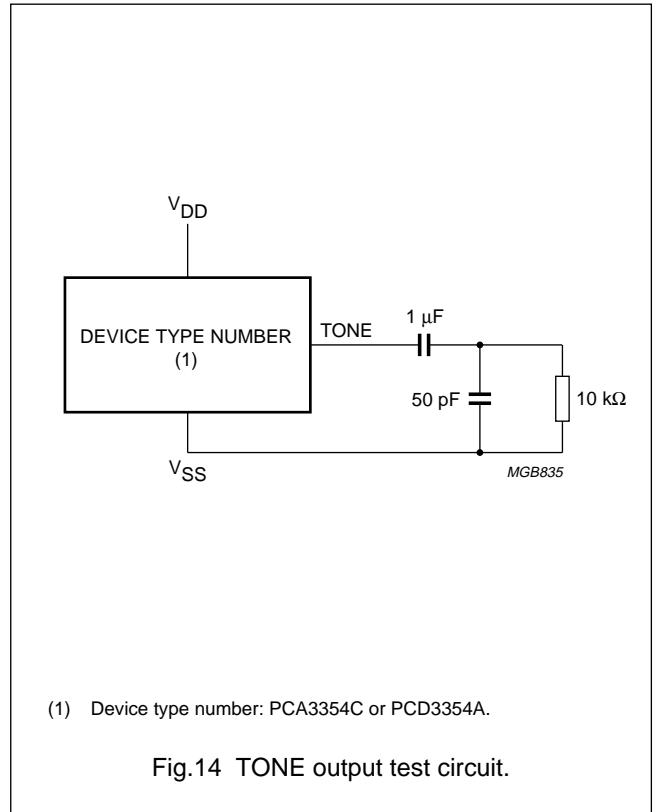as a function of supply voltage (V_{DD}).

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

Fig.9 Typical supply current in Idle mode ($I_{DD(idle)}$) as a function of clock frequency (f_{xtal}).

Measured with function generator on XTAL1.

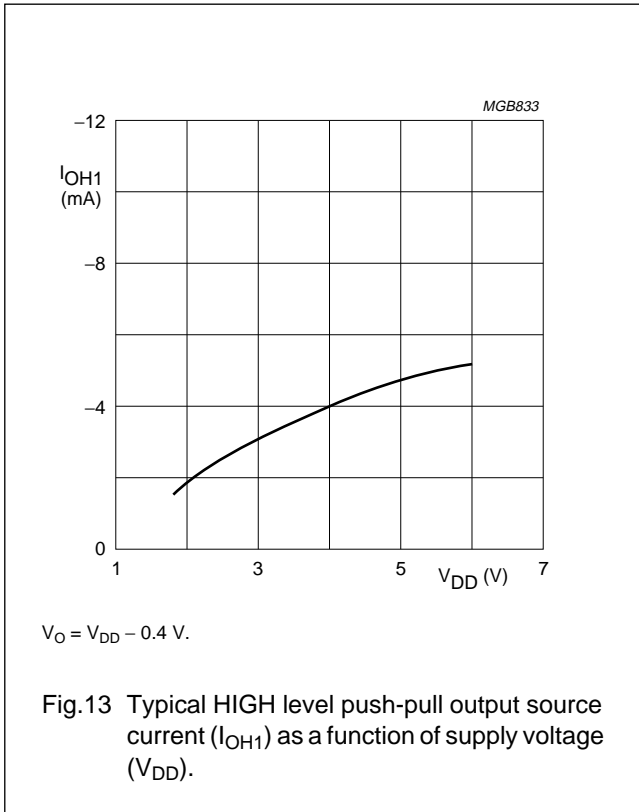Fig.10 Typical supply current in Stop mode ($I_{DD(stp)}$) as a function of supply voltage (V_{DD}).

Fig.11 Typical LOW level output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

V_O = 0.4 V.

Fig.12 Typical HIGH level pull-up output source current (I_{OH}) as a function of supply voltage (V_{DD}).

8-bit microcontrollers with DTMF generator and 256 bytes EEPROM

PCA3354C; PCD3354A

MGB833

$V_O = V_{DD} - 0.4$ V.

Fig.13 Typical HIGH level push-pull output source current (I_{OH1}) as a function of supply voltage (V_{DD}).

MGB835

(1) Device type number: PCA3354C or PCD3354A.

Fig.14 TONE output test circuit.

MGD495

Fig.15 Typical Power-on-reset level (V_{POR}) as function of ambient temperature (T_{amb}).

MGB818

Fig.16 Typical transconductance (g_m) as a function of supply voltage (V_{DD}).

18 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = 0 to +50 °C (PCA3354C) or −25 to +70 °C (PCD3354A); all voltages with respect
to V_{SS}; unless otherwise specified.

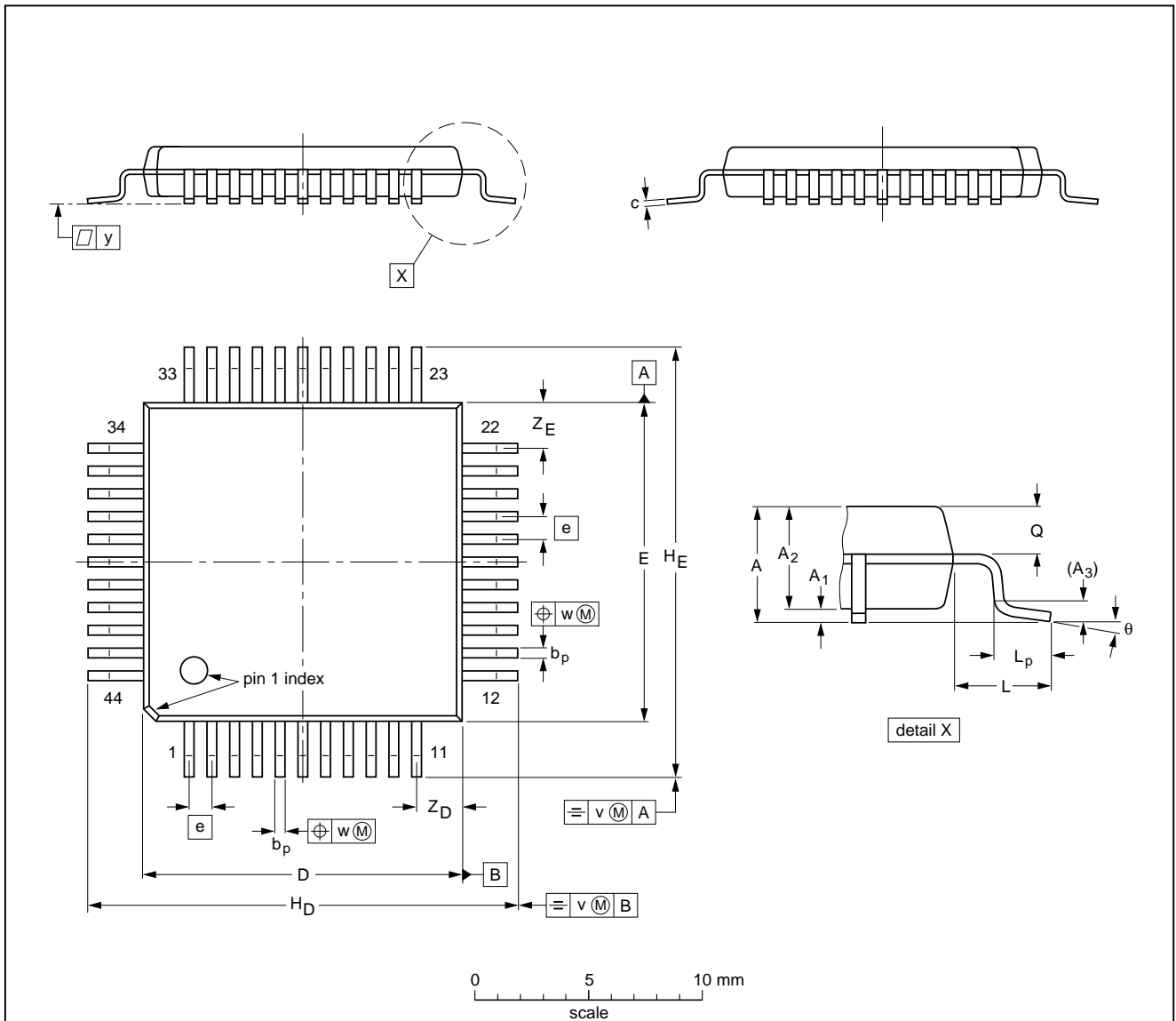| SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.5	1	–	16	MHz

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

19 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 2.35 mm); body 14 x 14 x 2.2 mm   **SOT205-1**

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D[1]	E[1]	e	H_D	H_E	L	L_p	Q	v	w	y	Z_D[1]	Z_E[1]	θ
mm	2.60	0.25 0.05	2.3 2.1	0.25	0.50 0.35	0.25 0.14	14.1 13.9	14.1 13.9	1	19.2 18.2	19.2 18.2	2.35	2.0 1.2	1.2 0.9	0.3	0.15	0.1	2.4 1.8	2.4 1.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT205-1	133E01A					~~92-11-17~~ 95-02-04

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

20 SOLDERING

20.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

20.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

20.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering the following packages: QFP52 (SOT379-1), QFP100 (SOT317-1), QFP100 (SOT317-2), QFP100 (SOT382-1) or QFP160 (SOT322-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

20.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

8-bit microcontrollers with DTMF
generator and 256 bytes EEPROM

PCA3354C; PCD3354A

21 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

22 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 247 9145, Fax. +7 095 247 9144

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: PHILIPS TAIWAN Ltd., 23-30F, 66,
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands   417021/1200/04/pp32   Date of release: 1996 Dec 18   Document order number: 9397 750 01082

Let's make things better.

Philips
Semiconductors

PHILIPS