INTEGRATED CIRCUITS

DATA SHEET

PCB8517
Stand-alone OSD for monitor applications

Objective specification
File under Integrated Circuits, IC02

1997 Mar 03

Philips Semiconductors

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FEATURES

Interface with microcontroller

- 3-wire high speed (maximum 2.5 Mbits/s) serial interface with three types of transmission sequence.

On-Screen Display (OSD)

- On-chip PLL oscillator to generate the OSD dot clock frequency which is 384 × horizontal sync frequency
- Horizontal sync frequency range of 10 to 100 kHz
- 10 rows of 24 characters display buffer
- 128 character fonts
- 12 × 16 character matrix
- Programmable height of displayed character (from 16 to 63 scan-lines); frame basis
- 4 types of character size; single/double character height/width; row basis
- Horizontal starting position: 32 different positions (6 dots for each step)
- Vertical starting position: 64 different positions (4 scan-lines for each step)
- 8 foreground character colours: selection of only 2 out of the 8 (outside the window) and 4 out of the of 8 (in the window) in the same row
- 3 character shadowing modes:
  - No shadow
  - Shadowing
  - Bordering shadow
- 3 fully programmable background windows with overlapping capability and presetting priorities (for multi-level application). The window colour can be selected from 1 out of 8
- Half tone in background window supported
- Single 5 V power supply
- Available in DIP16 package.

GENERAL DESCRIPTION

The PCB8517 is a stand-alone OSD which is used to display the adjustment/status information on the screen of an auto-sync monitor for menu driving application.

The display operation of the device is controlled by a microcontroller which programs the internal 273 bytes of RAM via a 3-wire high-speed serial interface. The on-chip PLL oscillator and programmable character height are used to keep the same character size displayed on the screen in different display modes, VGA, SVGA and XGA for example.

The OSD of the PCB8517 provides display buffers of 10 rows with 24 characters each. These display buffers can select from 128 customized character fonts (with 12 × 16 bit resolution) to be displayed. The characters displayed on the screen can be specified double height, double width, different colour and with/without shadowing. Three positional background windows are provided for multi-level application.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCB8517P	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4

BLOCK DIAGRAM

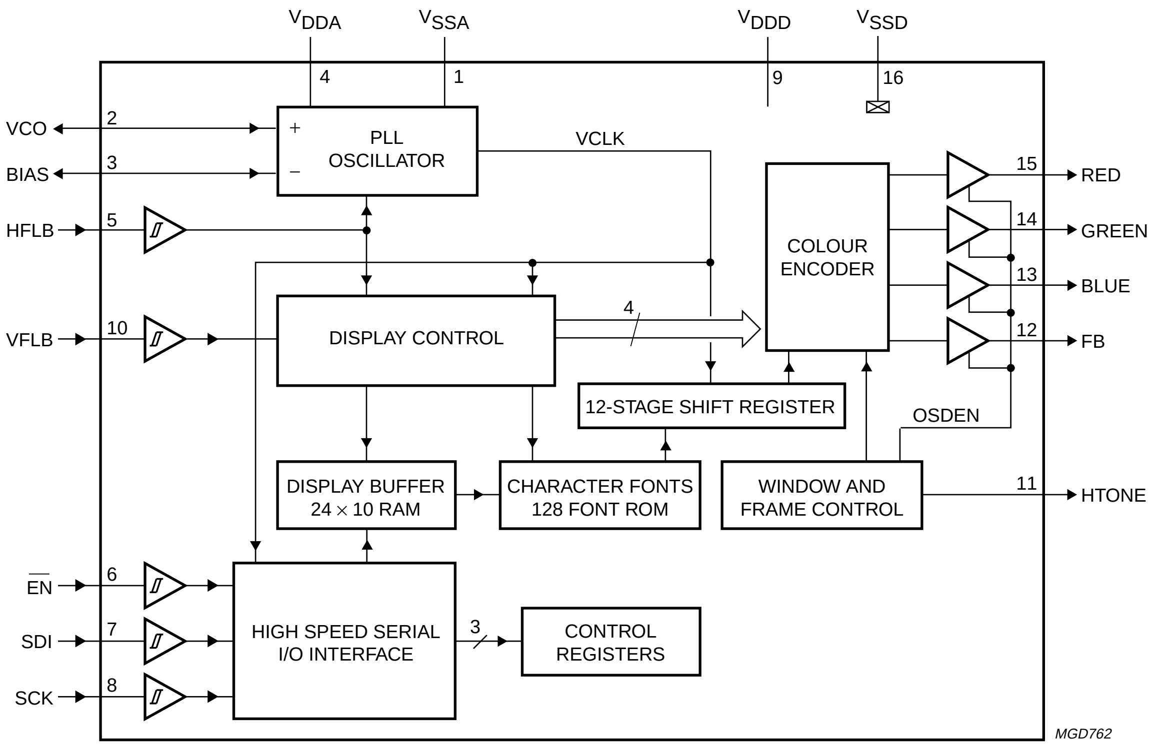


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA}	1	analog ground
VCO	2	DC control voltage input/output to regulate the internal PLL oscillator frequency; a low-pass filter circuit is connected to this pin
BIAS	3	bias input/output to regulate the bias current of internal current control oscillator to resonate at a specific dot frequency
V_{DDA}	4	analog power supply
HFLB	5	horizontal sync input signal from flyback circuit with negative polarity
$\overline{EN}$	6	active LOW input to enable serial interface
SDI	7	data input of serial interface
SCK	8	clock input of serial interface
V_{DDD}	9	digital power supply
VFLB	10	vertical sync input signal from flyback circuit with negative polarity
HTONE	11	half tone control which outputs a logic 1 during windowing except characters are displayed; it is used to lower the external RED, GREEN and BLUE amplifier gain to achieve a transparent windowing effect
FB	12	fast blanking output of OSD; active HIGH and high impedance when OSD is disabled
BLUE	13	blue colour output of OSD; active HIGH and high impedance when OSD is disabled
GREEN	14	green colour output of OSD; active HIGH and high impedance when OSD is disabled
RED	15	red colour output of OSD; active HIGH and high impedance when OSD is disabled
V_{SSD}	16	digital ground

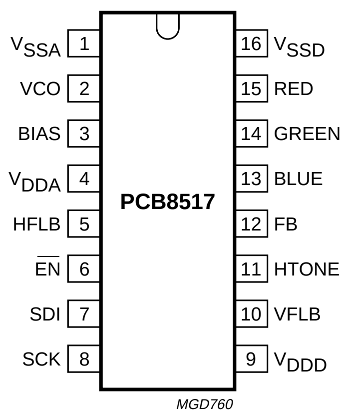


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

3-wire high speed serial interface (HSSI)

The 3-wire ($\overline{EN}$, SDI and SCK) high speed serial interface of the PCB8517 is write only and is used to write data from the microcontroller to the internal 273 bytes of RAM (see Section “Internal RAM organization (see Fig.4)”) to control the OSD. The RAM is organized into 11 rows of 32 columns (see Fig.4) and can be programmed by three types of sequence (see Section “Data sequence and format”).

DATA PROTOCOL

Figure 3 shows the protocol of HSSI. To initiate HSSI transmission, pin $\overline{EN}$ must be LOW to enable the PCB8517 to accept data. The $\overline{EN}$ input must be pulled LOW prior to the occurrence of SCK and remain LOW until after the last SCK clock pulse. The rising edge of SCK facilitates the input data of SDI being shifted into an 8-bit shift register. When the shift register is full this data will be loaded into a row address register, column address register or into one of the internal RAM bytes.

Table 1 shows the switching characteristics when the HFLB pin has a pulse presented, but when there is no horizontal sync pulse present on the HFLB pin, the transmission bit rate will be slowed down to 500 kbit/s.

Table 1 Switching characteristics (under operating conditions)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$t_{su(EN)}$	$\overline{EN}$ to SCK set-up time	200	–	ns
$t_{h(EN)}$	$\overline{EN}$ to SCK hold time	100	–	ns
t_{SCKL}	SCK LOW time	200	–	ns
t_{SCKH}	SCK HIGH time	200	–	ns
$t_{su(SDI)}$	SDI data set-up time	200	–	ns
$t_{h(SDI)}$	SDI data hold time	100	–	ns

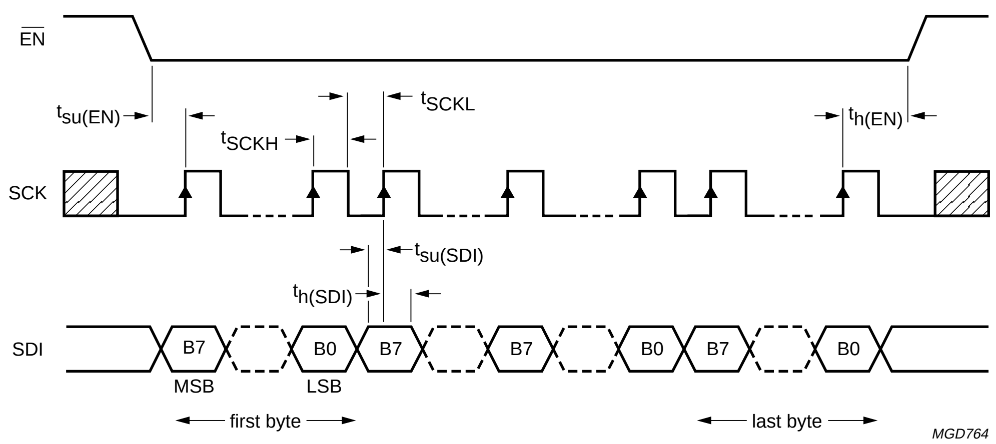


Fig.3 3-wire serial interface protocol.

DATA SEQUENCE AND FORMAT

The PCB8517 provides the following 3 types of transmission sequence:

- Sequence A: R ⇒ CA ⇒ D ⇒ R ⇒ CA ⇒ D etc.
- Sequence B: R ⇒ CA ⇒ D ⇒ CA ⇒ D ⇒ CA ⇒ D etc.
- Sequence C: R ⇒ CB ⇒ D ⇒ D ⇒ D ⇒ D etc.

Where: R = row address,
CA = column address A, CB = column address B,
D = data of RAM.

The column address will be increased by 1 automatically after each bit of data has been stored into the RAM.
In sequence C, if the column address of the last data is 1FH, the row address will also be increased by 1.
The sequence A is particularly suitable for updating small amounts of data between different rows. However, if the current information byte has the same row address as the previous one, sequence B is recommended. For a greater information update, such as a power-up situation, sequence C should be used.

Bit B7 in Table 2 is used to distinguish between row or column address and bit B6 is used to distinguish between column address A or B. When A or B sequence is transmitted, the column address should be formatted as column address A, and the data format of column address B is used for sequence C. There are some limitations on using mixed formats during a single transmission, for example when pin $\overline{EN}$ has been pulled to LOW once.

Allowed:

- From A to B or C
- From B to A.

Not allowed:

- From C to A or B.

Table 2 Data format

ADDRESS	DATA BYTE(1)							
	B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Row address	1	X	X	X	R3	R2	R1	R0
Column address A	0	0	X	C4	C3	C2	C1	C0
Column address B	0	1	X	C4	C3	C2	C1	C0

Note

1. X = don’t care.

Internal RAM organization (see Fig.4)

The internal RAM is addressed with rows 0 to 10 and columns 0 to 31. The OSD character display buffers are located in columns 0 to 23 of rows 0 to 9. Each display buffer contains a character ROM address and the colour control bit corresponding to a display location on the monitor screen.

Each row data is associated with two control registers which are located at columns 30 and 31 of their respective row. Also three window control registers for three windows together with three frame control register occupy the first 13 columns of row 10.

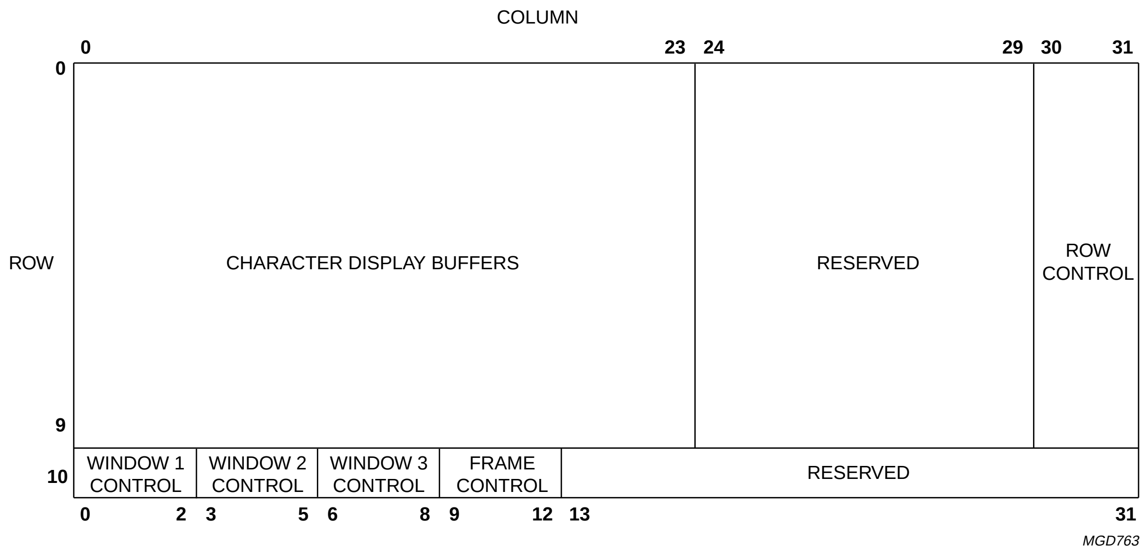


Fig.4 Internal RAM map.

DISPLAY BUFFERS

Table 3 Display buffers; see Table 4

DATA BYTE							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
CCS0	CA6	CA5	CA4	CA3	CA2	CA1	CA0

Table 4 Explanation of Table 3

BIT	NAME	DESCRIPTION
7	CCS0	This bit defines the characters colour. When the character has no window background with it, colour 0 is selected if CCS0 = 0, otherwise colour 1 is selected. When the character is inside a window and the CCS1 bit of the corresponding windows control register is 0, the colour selection is the same as no window background, and if CCS1 = 1, colour 2 is selected when CCS0 = 0, otherwise colour 3 is selected.
6 to 0	CA6 to CA0	These 7 bits define 1 of 128 character symbols to be displayed in this position.

ROW CONTROL REGISTERS

Table 5 Column 30

DATA BYTE							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
R0	G0	B0	R1	G1	B1	CHS	CWS

Table 6 Explanation of Table 5

BIT	NAME	DESCRIPTION
7 to 5	R0, G0, B0	colour definition of colour 0
4 to 2	R1, G1, B1	colour definition of colour 1
1	CHS	This bit defines the height of the display character; when CHS = 1 double height is selected.
0	CWS	This bit defines the width of the display character; when CWS = 1 double width(1) is selected.

Note

1. When the display row is selected to be double width, only even column characters will be displayed on the screen and the odd column characters will not appear.

Table 7 Column 31

DATA BYTE							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
R2	G2	B2	R3	G3	B3	reserved	

Table 8 Explanation of Table 7

BIT	NAME	DESCRIPTION
7 to 5	R2, G2, B2	colour definition of colour 2
4 to 2	R3, G3, B3	colour definition of colour 3

WINDOW CONTROL REGISTERS

There are three control registers for each window. Window 1 occupies columns 0 to 2 of row 10, columns 3 to 5 of row 10 are occupied by window 2 and columns 6 to 8 of row 10 are occupied by window 3. If window overlapping occurs, the highest priority window will cover the lowest. Window 1 has the highest priority and window 3 the lowest.

Table 9 Columns 0, 3 and 6 of row 10

DATA BYTE							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
MSB	row start address		LSB	MSB	row end address		LSB

Table 10 Explanation of Table 9

BIT	NAME	DESCRIPTION
7 to 4	–	These bits specify which row is the start of window.
3 to 0	–	These bits specify which row is the end of window.

Table 11 Columns 1, 4 and 7 of row 10

DATA BYTE							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
MSB	column start address			LSB	WEN	CCS1	reserved

Table 12 Explanation of Table 11

BIT	NAME	DESCRIPTION
7 to 3	–	These bits specify which column is the start of the window.
2	WEN	When this bit is set to logic 1 the corresponding window background is enabled.
1	CCS1	When this bit is set to logic 1, the characters resided within this particular window can have two extra colour selections (i.e. colour 2 and colour 3); see Section “Display buffers”.

Table 13 Columns 2, 5 and 8 of row 10

DATA BYTE							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
MSB	column end address			LSB	WR	WG	WB

Table 14 Explanation of Table 13

BIT	NAME	DESCRIPTION
7 to 3	–	These bits specify which column is the end of the window.
2 to 0	WR, WG, WB	These bits define the colour of the window.

FRAME CONTROL REGISTERS

Table 15 Column 9 of row 10

DATA BYTE							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
reserved		MSB	vertical start position				LSB

Table 16 Explanation of Table 15

BIT	NAME	DESCRIPTION
5 to 0	–	These bits specify the vertical starting position of OSD. The counting starts from the falling edge of the VFLB signal (e.g. enter vertical flyback period) and each increment represents four scan line movement to the bottom. 64 positions are provided. The default value is 4 after power-up. The time from the falling edge of the VFLB signal to starting display is: t_v = (vertical start position) $\times 4 \times t_{h\text{-sync}} + t_{h\text{-sync}}$. Where $t_{h\text{-sync}}$ = one horizontal line display time.

Table 17 Column 10 of row 10

DATA BYTE							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
reserved			MSB	horizontal start position			LSB

Table 18 Explanation of Table 17

BIT	NAME	DESCRIPTION
4 to 0	–	These bits specify the horizontal starting position of OSD. The counting starts from the falling edge of the HFLB signal (e.g. enter horizontal flyback period) and each increment represents six dots movement to the right. 32 positions are provided. The default value is 15 after power-up. The time from the falling edge of the HFLB signal to starting display is: t_h = (horizontal start position) $\times 6 \times t_{dot} + 61 \times t_{dot}$. Where t_{dot} = one pixel display time (e.g. one horizontal line display time/384).

A horizontal display line consists of 384 dots, which include 288 dots (e.g. 12 dots $\times$ 24 characters) for display character, and 96 dots for the blank region.

Table 19 Column 11 of row 10

DATA BYTE							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
reserved		CH5	CH4	CH3	CH2	CH1	CH0

Table 20 Explanation of Table 19

BIT	NAME	DESCRIPTION
5 to 0	CH5 to CH0	These bits specify the height of displayed characters. Table 21 shows the lines to be repeated. The height of character can be specified from 16 to 63 scan lines. For example, when CH5 to CH0 = 00 0010, the height of character will be 18 scan lines, the 4th and 12th line will be double scanned but others will be scanned once.

Table 21 The repeat line of character

CH5 to CH0	LINE NUMBER[1]															
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
CH0 = 1	–	–	–	–	–	–	–	–	V	–	–	–	–	–	–	–
CH1 = 1	–	–	–	–	V	–	–	–	–	–	–	–	V	–	–	–
CH2 = 1	–	–	V	–	–	–	V	–	–	–	V	–	–	–	V	–
CH4 = 1	–	V	–	V	–	V	–	V	–	V	–	V	–	V	–	V
CH5 and CH4 = 0X	all sixteen lines scanned once															
CH5 and CH4 = 10	all sixteen lines scanned twice															
CH5 and CH4 = 11	all sixteen lines scanned three times															

Note

1. V indicates which line of the character will be repeated one more time.

Table 22 Column 12 of row 10

DATA BYTE							
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
OSDEN	BSEN	SHSE	reserved				FBC

Table 23 Explanation of Table 22

BIT	NAME	DESCRIPTION
7	OSDEN	The OSD circuit is active when this bit is set to logic 1. The outputs of R, G, B and FB will be high impedance when OSD is disabled.
6	BSEN	The bordering or shadowing effect is enabled when this bit is set to logic 1.
5	SHSE	The shadowing of characters is selected if this bit is set to logic 1, otherwise bordering of characters is chosen.
0	FBC	This bit defines the output configuration of the FB pin. If this bit is set to logic 0, then the output of FB will be logic HIGH when displaying character or window, otherwise the output of FB is logic HIGH only when displaying characters.

Character ROM

The character ROM contains 128 character fonts. Each font consists of a 12×16 dot matrix.

Bordering and shadowing of characters

The characters displayed on the screen can be specified with or without shadowing or with border shadowing by setting the BSEN and SHSE bits of frame control register “Column 11 of row 10”. If shadowing is specified, there is black shadow on the right and bottom sides of character, and if border shadowing is specified, the black shadowing will surround both internal and external sides of characters (see Fig.5). The characters shadow will not appear if it is outside the display area of character (i.e. 12×16 dots).

Combination of two or more character fonts to formulate a new symbol

User can combine two (or more) character fonts to formulate a new higher resolution symbol in a horizontal direction, but the combination of two fonts in a vertical direction could cause the shadowing or bordering shadow of upper font to be missed if shadowing or bordering is applied.

PLL clock generator

By tracing the signal on the HFLB pin, the on-chip PLL circuit generates the clock (VCLK) which is used for both system clock and dot clock of the OSD. The frequency of VCLK signal is determined by following equation:

$f_{VCLK} = f_{HFLB} \times 384$ (i.e. the frequency range of VCLK signal is from 3.84 to 38.4 MHz).

When there is no horizontal sync pulse present on the HFLB pin, the PLL circuit will generate a 2.5 MHz (approximate) clock for the system clock, and the RED, GREEN, BLUE and FB pins will be high impedance.

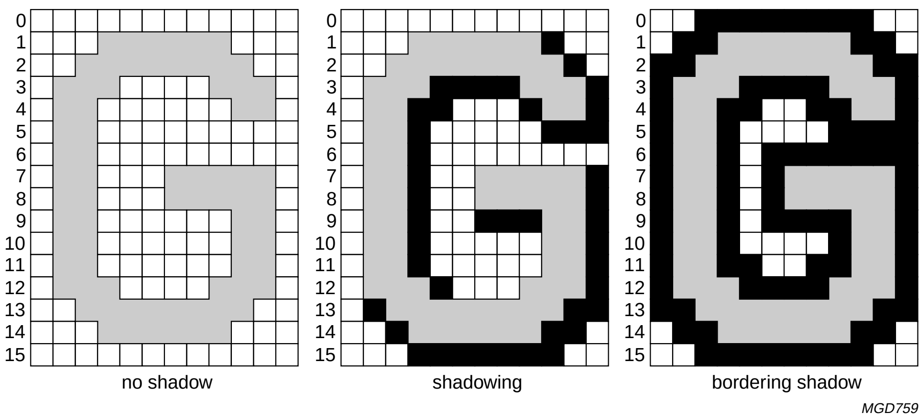


Fig.5 Character shadowing and bordering.

PCB8517P/001 character fonts

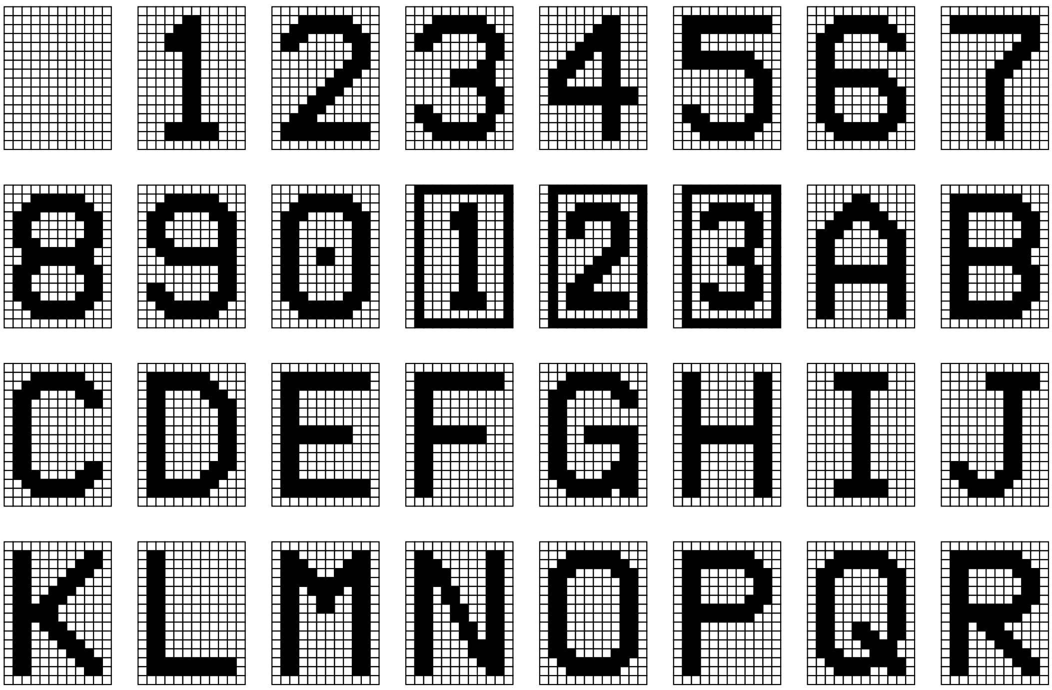
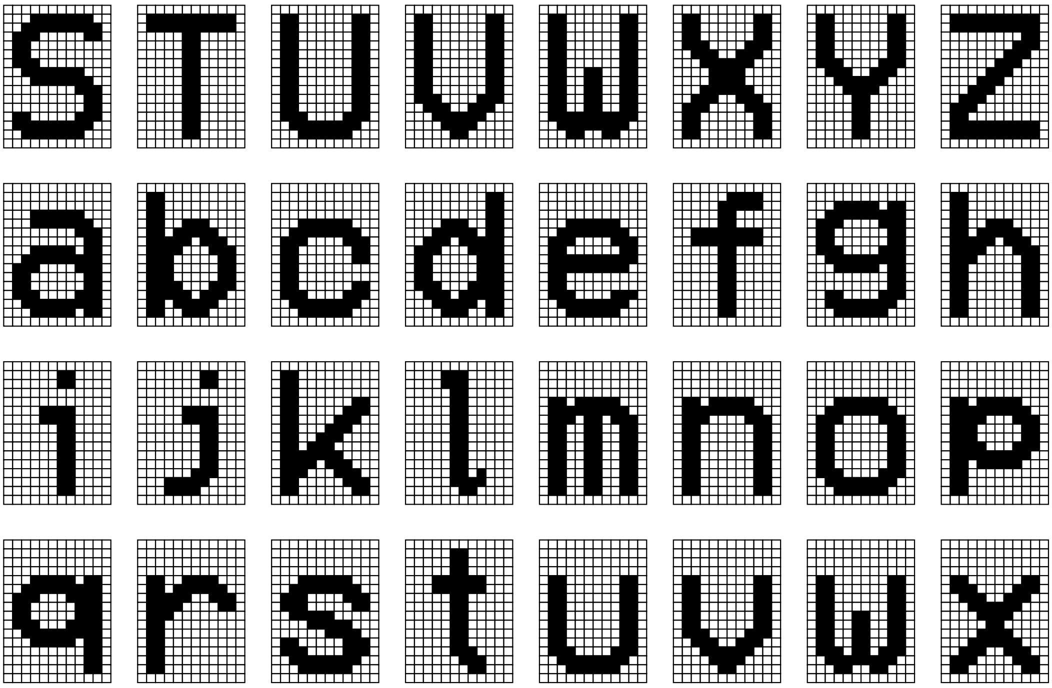


Fig.6 Character fonts 00H to 1FH.



MGD756

Fig.7 Character fonts 20H to 3FH.

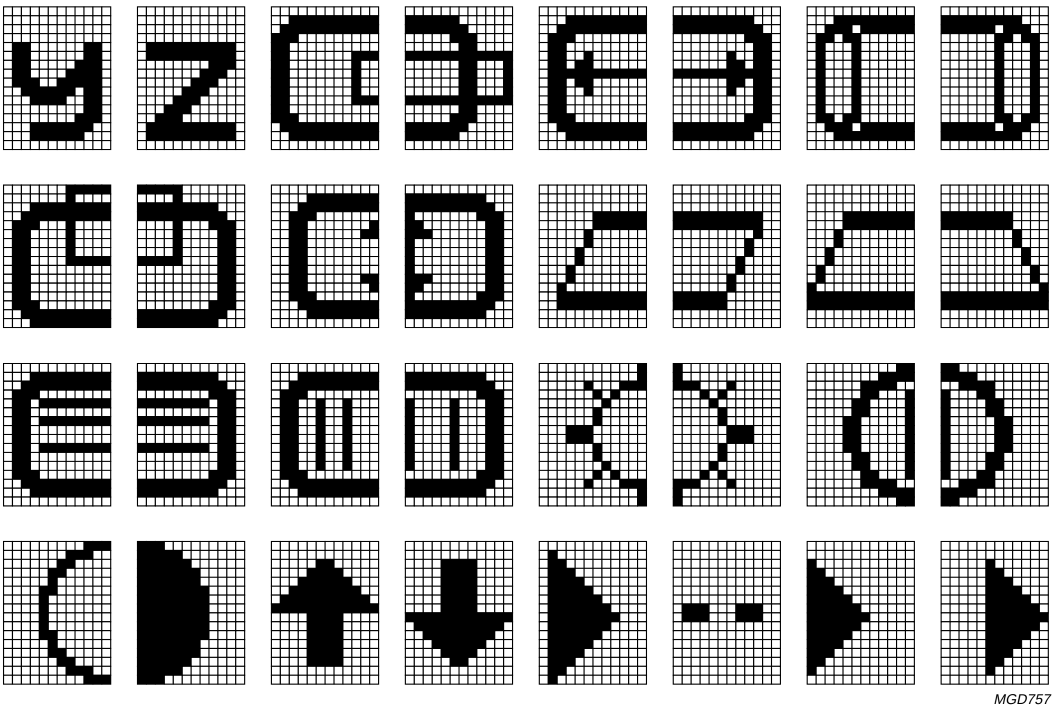


Fig.8 Character fonts 40H to 5FH.

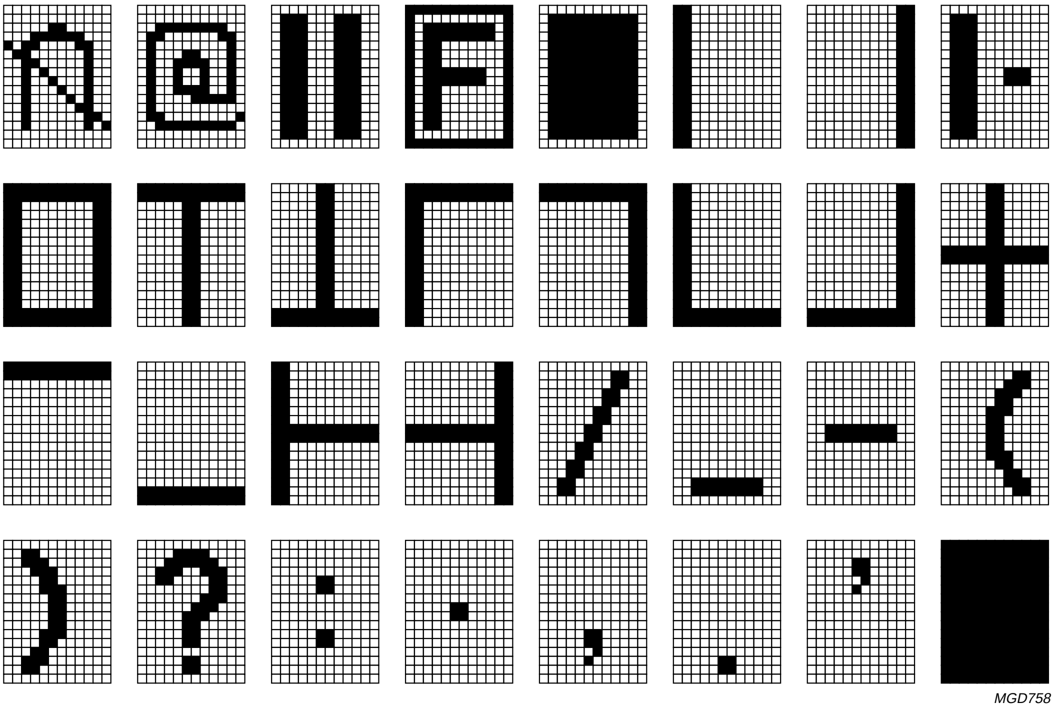


Fig.9 Character fonts 60H to 7FH.

LIMITING VALUES

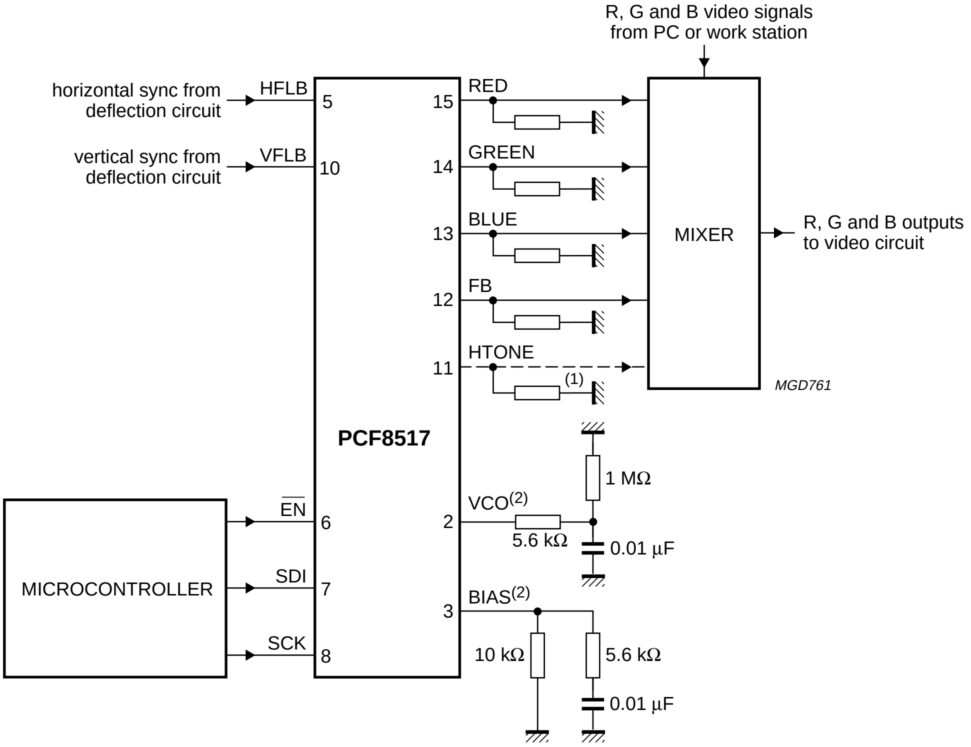
In accordance with the absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DDX}	digital supply voltage	–0.3	+7.0	V
V_i	input voltage (all inputs)	–0.3	V_{DDX} + 0.3	V
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature	0	70	°C

DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DDX}	digital supply voltage		4.75	5.0	5.25	V
I_{DDX}	digital supply current	$V_I = V_{DDX}$; no load on outputs	–	–	25	mA
Inputs						
V_{IH}	HIGH level input voltage		2.0	–	V_{DDX} + 0.3	V
V_{IL}	LOW level input voltage		V_{SSX} – 0.3	–	0.8	V
Outputs						
$I_{OH(source)}$	HIGH level output current (source)	$V_O \geq V_{DDX} - 0.8$	5.0	–	–	mA
$I_{OL(sink)}$	LOW level output current (sink)	$V_O \leq 0.5$	5.0	–	–	mA

APPLICATION INFORMATION



The analog power and ground pins should be separated from other circuits.

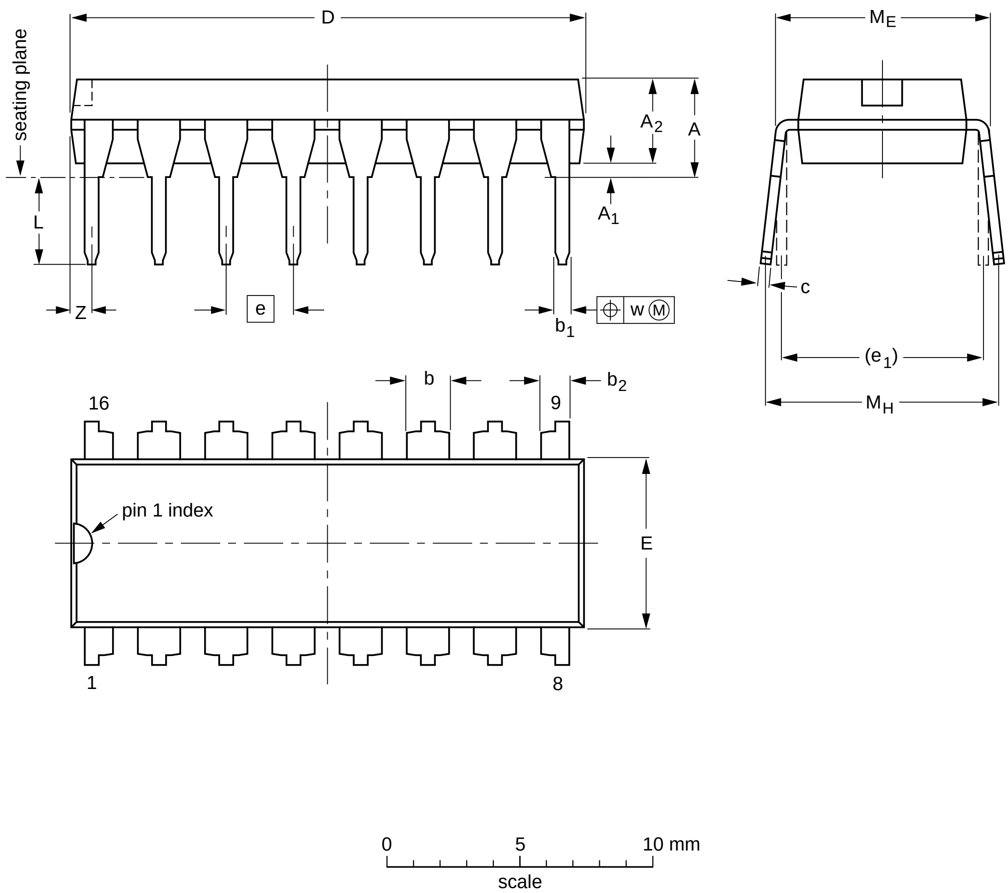
(1) Only connected when half tone is applied.

(2) The recommended circuit or value of components connected to VCO and BIAS could be changed in a different printed-circuit board layout.

Fig.10 Application circuit.

PACKAGE OUTLINE

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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