

# DATA SHEET

## **PCK111**

Low voltage 1:10 differential  
PECL clock driver

Product data

2001 Sep 07

File under Integrated Circuits — ICL03

# Low voltage 1:10 differential PECL clock driver

# PCK111

## FEATURES

- 100 ps part-to-part skew typical
- 35 ps output-to-output skew typical
- Differential design
- $V_{BB}$  output
- Low voltage  $V_{CC}$  range of +2.375 V to +3.8 V for PECL
- 75 k $\Omega$  input pull-down resistors
- ECL/PECL outputs
- Form, fit, and function compatible with MC100EP111

## DESCRIPTION

The PCK111 is a low skew 1-to-10 differential driver, designed with clock distribution in mind. It accepts two clock sources into an input multiplexer. The PECL input signals can be either differential or single-ended if the  $V_{BB}$  output is used. The selected signal is fanned out to 10 identical differential outputs.

The PCK111 is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate-to-gate skew within a device, and empirical modeling is used to determine process control limits that ensure consistent  $t_{PD}$  distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met, it is necessary that both sides of the differential output are terminated into 50  $\Omega$ , even if only one side is being used. In most applications, all ten differential pairs will be used, and therefore terminated. In the case where fewer than ten pairs are used, it is necessary to terminate at least the output pairs on the same package side as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20 ps) of the output(s) being used, which, while not being catastrophic to most designs, will mean a loss of skew margin.

The PCK111 can be used for high performance clock distribution in +3.3 V or +2.5 V systems. Designers can take advantage of the PCK111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies.

The PCK111 may be driven single-endedly utilizing the  $V_{BB}$  bias output with the  $\overline{CLK0}$  input. If a single-ended signal is to be used, the  $V_{BB}$  pin should be connected to the  $\overline{CLK0}$  input and bypassed to ground via a 0.01  $\mu$ F capacitor. The  $V_{BB}$  output can only source/sink 0.2 mA, therefore, it should be used as a switching reference for the PCK111 only. Part-to-part skew specifications are not guaranteed when driving the PCK111 single-endedly.

## PINNING

### Pin configuration

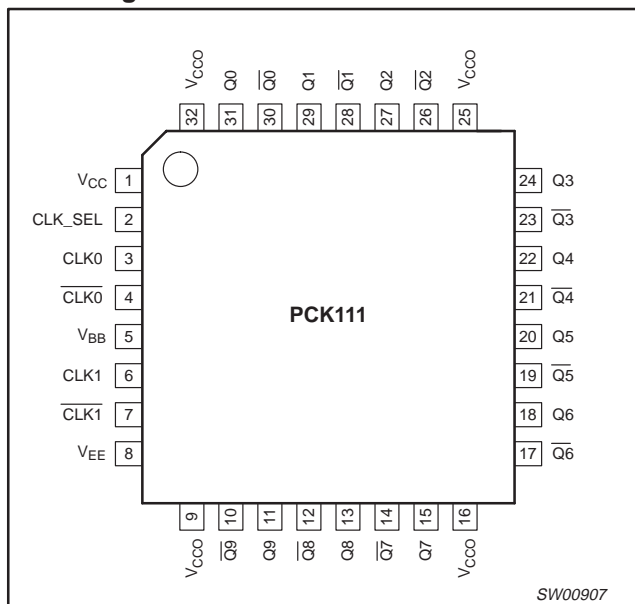


Figure 1. Pin configuration

### Pin description

SYMBOL	PIN	DESCRIPTION
$V_{CC}$	1	Supply voltage
CLK_SEL	2	Active clock select input
CLK0, $\overline{CLK0}$	3, 4	Differential ECL/PECL input pair
$V_{BB}$	5	$V_{BB}$ output
CLK1, $\overline{CLK1}$	6, 7	Differential HSTL input pair
$V_{EE}$	8	Ground
$V_{CCO}$	9, 16, 25, 32	Output drive power supply voltage
Q0–Q9	31, 29, 27, 24, 22, 20, 18, 15, 13, 11	Differential PECL outputs
$\overline{Q0}$ – $\overline{Q9}$	30, 28, 26, 23, 21, 19, 17, 14, 12, 10	Differential PECL outputs

## ORDERING INFORMATION

Type number	Package			Temperature range
	Name	Description	Version	
PCK111BD	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1	–40 to +70 °C

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PECL clock driver

PCK111

LOGIC SYMBOL

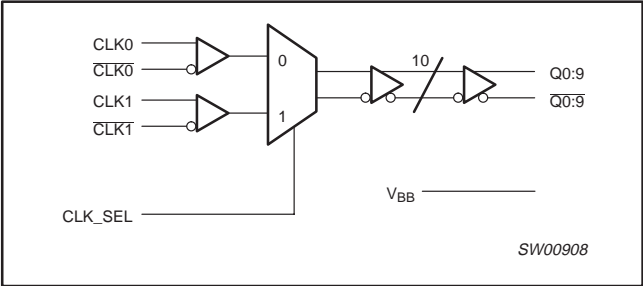


Figure 2. Logic symbol

FUNCTION TABLE

CLK_SEL	Active input
0	CLK0, CLK0
1	CLK1, CLK1

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

SYMBOL	PARAMETER	LIMITS	UNIT
V <sub>CC</sub>	Supply voltage	−0.5 to +4.6	V
ESDHBM	Electrostatic discharge (Human Body Model; 1.5 kΩ, 100 pF)	>2	kV
ESDMM	Electrostatic discharge (Machine Model; 0 kΩ, 200 pF)	>200	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.375	3.8	V
V <sub>IR</sub>	Receiver input voltage	V <sub>EE</sub>	V <sub>CC</sub>	V
T <sub>amb</sub>	Operating ambient temperature range in free air	−40	+85	°C

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## DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.25\text{ to }-3.80\text{ V}$ 

SYMBOL	PARAMETER	CONDITION	-40 °C MIN	-40 °C MAX	25 °C MIN	25 °C MAX	70 °C MIN	70 °C MAX	UNIT
$I_{EE}$	Internal supply current	Absolute value of current	45	85	60	95	65	105	mA
$I_{CC}$	Output and internal supply current	All outputs terminated 50 $\Omega$ to $V_{CC} = -2.0\text{ V}$	270	360	290	380	300	380	mA
$I_{IN}$	Input current	Includes pullup/pulldown resistors	—	150	—	150	—	150	$\mu\text{A}$
$V_{BB}$	Internal bias voltage	$V_{EE} = -3.0\text{ to }-3.80\text{ V}$	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26	V
$V_{BB}$	Internal bias voltage	$V_{EE} = -2.25\text{ to }-2.75\text{ V}$	-1.38	-1.16	-1.38	-1.16	-1.38	-1.16	V
$V_{IH}$	Input HIGH voltage		-1.165	-0.880	-1.165	-0.880	-1.165	-0.880	V
$V_{IL}$	Input LOW voltage		-1.810	-1.475	-1.810	-1.475	-1.810	-1.475	V
$V_{PP}$	Input amplitude	Difference of input = $V_{IH} - V_{IL}$ (Note 1)	0.5	1.3	0.5	1.3	0.5	1.3	V
$V_{CMR}$	Common mode voltage	Cross point of input = average ( $V_{IH}$ , $V_{IL}$ )	$V_{EE} + 1.0$	-0.3	$V_{EE} + 1.0$	-0.3	$V_{EE} + 1.0$	-0.3	V
$V_{OH}$	Output HIGH voltage	$I_{OH} = -30\text{ mA}$	-1.3	-0.95	—	—	-1.2	0.90	V
$V_{OL}$	Output LOW voltage	$I_{OL} = -5\text{ mA}$	-1.85	-1.4	—	—	-1.90	-1.5	V
$V_{OUTpp}$	Differential output swing		350	—	—	—	500	—	MV

### NOTE:

1.  $V_{PP}$  minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum  $V_{PP}$  of 100 mV.

## DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 0\text{ V}$ ,  $V_{EE} = -2.25\text{ to }-3.80\text{ V}$ 

SYMBOL	PARAMETER	CONDITION	-40 °C MIN	-40 °C MAX	25 °C MIN	25 °C MAX	70 °C MIN	70 °C MAX	UNIT
$I_{EE}$	Internal supply current	Absolute value of current	45	85	60	95	65	105	mA
$I_{CC}$	Output and internal supply current	All outputs terminated 50 $\Omega$ to $V_{CC} = -2.0\text{ V}$	270	360	290	380	300	380	mA
$I_{IN}$	Input current	Includes pullup/pulldown resistors	—	150	—	150	—	150	$\mu\text{A}$
$V_{BB}$	Internal bias voltage	$V_{EE} = -3.0\text{ to }-3.80\text{ V}$	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.26$	$V_{CC} - 1.38$	$V_{CC} - 1.26$	V
$V_{BB}$	Internal bias voltage	$V_{EE} = -2.25\text{ to }-2.75\text{ V}$	$V_{CC} - 1.38$	$V_{CC} - 1.16$	$V_{CC} - 1.38$	$V_{CC} - 1.16$	$V_{CC} - 1.38$	$V_{CC} - 1.16$	V
$V_{IH}$	Input HIGH voltage		$V_{CC} - 1.165$	$V_{CC} - 0.880$	$V_{CC} - 1.16$	$V_{CC} - 0.880$	$V_{CC} - 1.16$	$V_{CC} - 0.880$	V
$V_{IL}$	Input LOW voltage		$V_{CC} - 1.810$	$V_{CC} - 1.475$	$V_{CC} - 1.810$	$V_{CC} - 1.475$	$V_{CC} - 1.810$	$V_{CC} - 1.475$	V
$V_{PP}$	Input amplitude	Difference of input = $V_{IH} - V_{IL}$ (Note 1)	0.5	1.3	0.5	1.3	0.5	1.3	V
$V_{CMR}$	Common mode voltage	Cross point of input = average ( $V_{IH}$ , $V_{IL}$ )	1.0	$V_{CC} - 0.3$	1.0	$V_{CC} - 0.3$	1.0	$V_{CC} - 0.3$	V
$V_{dif}$	Differential input voltage	Difference of input = $V_{IH} - V_{IL}$	0.4	1.9	0.4	1.9	0.4	1.9	V
$V_x$	Input crossover voltage	Cross point of input = average ( $V_{IH}$ , $V_{IL}$ )	0.68	0.9	0.68	0.9	0.68	0.9	V
$V_{OH}$	Output HIGH voltage	$I_{OH} = -30\text{ mA}$	$V_{CC} - 1.30$	$V_{CC} - 0.95$	—	—	$V_{CC} - 1.20$	$V_{CC} - 0.90$	V
$V_{OL}$	Output LOW voltage	$I_{OL} = -5\text{ mA}$	$V_{CC} - 1.85$	$V_{CC} - 1.40$	—	—	$V_{CC} - 1.90$	$V_{CC} - 1.50$	V
$V_{OUTpp}$	Differential output swing		350	—	—	—	500	—	MV

### NOTE:

1.  $V_{PP}$  minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum  $V_{PP}$  of 100 mV.

# Low voltage 1:10 differential PECL clock driver

PCK111

## AC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 2.25$  to  $3.80$  V,  $V_{EE} = 0$  V, or  $V_{CC} = 0$  V,  $V_{EE} = -2.25$  to  $-3.80$  V

SYMBOL	PARAMETER	CONDITION	-40 °C MIN	-40 °C MAX	25 °C MIN	25 °C MAX	70 °C MIN	70 °C MAX	UNIT
$t_{PD}$	Differential propagation delay	Nominal (single input condition) $V_{PP} = 0.650$ V, $V_{CMR} = V_{CC} - 0.800$ V (Note 1)	350	500	380	530	450	600	ps
$t_{skew}$	Part-to-part skew	Note 1	—	150	—	150	—	150	ps
$t_{skew}$	Output-to-output same part skew	Note 1	—	70	—	65	—	60	ps
$t_{PD}$	Differential propagation delay	Note 1	280	600	300	620	370	700	ps
$t_{skew}$	Part-to-part skew	Note 1	—	320	—	320	—	320	ps
$t_{skew}$	Output-to-output same part skew	Note 1	—	70	—	65	—	60	ps
$f_{MAX}$	Maximum output frequency	Functional to 1.5 GHz; Timing specifications apply to 1.0 GHz	—	1500	—	1500	—	1500	MHz
$t_r/t_f$	Output rise/fall time at 20% to 80%	All outputs terminated 50 $\Omega$ to $V_{CC} - 2.0$ V	100	300	100	300	100	300	ps

### NOTE:

- For operation with 2.5 V supply, the output termination is 50  $\Omega$  to  $V_{EE}$ .  
For operation with 3.3 V supply, the output termination is 50  $\Omega$  to  $V_{CC} - 2$  V.

## AC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 2.25$  to  $3.80$  V,  $V_{EE} = 0$  V

SYMBOL	PARAMETER	CONDITION	-40 °C MIN	-40 °C MAX	25 °C MIN	25 °C MAX	70 °C MIN	70 °C MAX	UNIT
$t_{PD}$	Differential propagation delay	Nominal (single input condition) $V_{PP} = 0.650$ V, $V_{CMR} = V_{CC} - 0.800$ V (Note 1)	380	530	420	570	500	650	ps
$t_{skew}$	Part-to-part skew	Note 1	—	150	—	150	—	150	ps
$t_{skew}$	Output-to-output same part skew	Note 1	—	70	—	65	—	60	ps
$t_{PD}$	Differential propagation delay	Note 1	300	600	350	650	430	750	ps
$t_{skew}$	Part-to-part skew	Note 1	—	300	—	300	—	320	ps
$t_{skew}$	Output-to-output same part skew	Note 1	—	70	—	65	—	60	ps
$f_{MAX}$	Maximum output frequency	Functional to 1.5 GHz; Timing specifications apply to 1.0 GHz	—	250	—	250	—	250	MHz
$t_r/t_f$	Output rise/fall time at 20% to 80%	All outputs terminated 50 $\Omega$ to $V_{CC} - 2.0$ V	100	300	100	300	100	300	ps

### NOTE:

- For operation with 2.5 V supply, the output termination is 50  $\Omega$  to  $V_{EE}$ .  
For operation with 3.3 V supply, the output termination is 50  $\Omega$  to  $V_{CC} - 2$  V.

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PECL clock driver**

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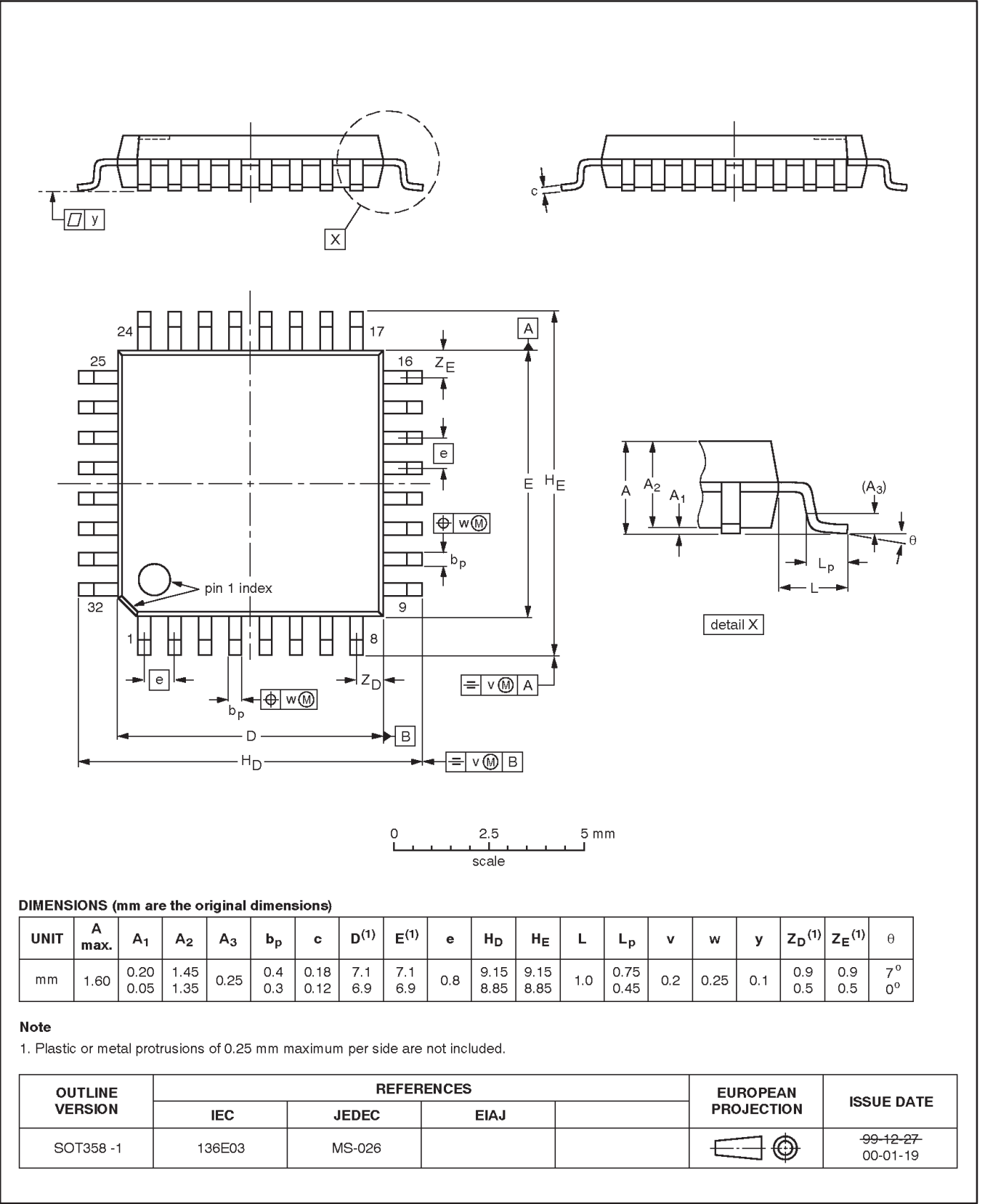
**PCK111****NOTES**

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LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm

SOT358-1



# Low voltage 1:10 differential PECL clock driver

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## Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definitions
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