Burr-Brown Products
from Texas Instruments

PCM1602

www.ti.com

24-Bit, 192kHz Sampling, 6-Channel, Enhanced Multilevel, Delta-Sigma DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 24-BIT RESOLUTION
- ANALOG PERFORMANCE:
  Dynamic Range: 100dB typ (PCM1602Y)
  105dB typ (PCM1602KY)
  SNR: 100dB typ (PCM1602Y)
  105dB typ (PCM1602KY)
  THD+N: 0.003% typ (PCM1602Y)
  0.002% typ (PCM1602KY)
  Full-Scale Output: 3.1Vp-p typ
- 4x/8x OVERSAMPLING INTERPOLATION FILTER:
  Stopband Attenuation: –55dB
  Passband Ripple: ±0.03dB
- SAMPLING FREQUENCY:
  5kHz to 200kHz (Channels 1 and 2)
  5kHz to 100kHz (Channels 3, 4, 5, and 6)
- ACCEPTS 16-, 18-, 20-, AND 24-BIT AUDIO DATA
- DATA FORMATS: Standard, I^2S, and Left-Justified
- SYSTEM CLOCK: 128, 192, 256, 384, 512, or 768f_S
- USER-PROGRAMMABLE FUNCTIONS:
  Digital Attenuation: 0dB to –63dB, 0.5dB/Step
  Soft Mute
  Zero Flags May Be Used As General-Purpose Logic Output
  Digital De-Emphasis
  Digital Filter Roll-Off: Sharp or Slow
- DUAL-SUPPLY OPERATION:
  +5V Analog, +3.3V Digital
- +5V TOLERANT DIGITAL LOGIC INPUTS
- PACKAGE: LQFP-48

APPLICATIONS

- INTEGRATED A/V RECEIVERS
- DVD MOVIE AND AUDIO PLAYERS
- HDTV RECEIVERS
- CAR AUDIO SYSTEMS
- DVD ADD-ON CARDS FOR HIGH-END PCs
- DIGITAL AUDIO WORKSTATIONS
- OTHER MULTICHANNEL AUDIO SYSTEMS

DESCRIPTION

The PCM1602 is a CMOS monolithic integrated circuit that features six 24-bit audio Digital-to-Analog Converters (DACs) and support circuitry in a small LQFP-48 package. The DACs utilize Texas Instrument's enhanced multilevel, delta-sigma architecture that employs fourth-order noise shaping and 8-level amplitude quantization to achieve excellent signal-to-noise performance and a high tolerance to clock jitter.

The PCM1602 accepts industry-standard audio data formats with 16- to 24-bit audio data. Sampling rates up to 200kHz (channels 1 and 2) or 100kHz (channels 3, 4, 5, and 6) are supported. A full set of user-programmable functions are accessible through a 4-wire serial control port that supports register write and read functions.

TEXAS INSTRUMENTS

SBAS163

Printed in U.S.A. December, 2000

SPECIFICATIONS

All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, system clock = 384f_S (f_S = 44.1kHz), and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1602Y PCM1602KY MIN	PCM1602Y PCM1602KY TYP	PCM1602Y PCM1602KY MAX	UNITS
RESOLUTION			24		Bits
DATA FORMAT					
Audio Data Interface Formats			Standard, I²S, Left-Justified		
Audio Data Bit Length			16, 18, 20, 24-Bits Selectable		
Audio Data Format			MSB-First, Binary Two's Complement		
Sampling Frequency (f_S)	V_{OUT} 1, 2	5		200	kHz
	V_{OUT} 3, 4, 5, 6	5		100	kHz
System Clock Frequency			128, 192, 256, 384, 512, 768f_S		
DIGITAL INPUT/OUTPUT					
Logic Family			TTL-Compatible		
Input Logic Level					
V_{IH}		2.0			VDC
V_{IL}				0.8	VDC
Input Logic Current					
I_{IH}(1)	$V_{IN} = V_{DD}$			10	µA
I_{IL}(1)	V_{IN} = 0V			–10	µA
I_{IH}(2)	$V_{IN} = V_{DD}$		65	100	µA
I_{IL}(2)	V_{IN} = 0V			–10	µA
Output Logic Level					
V_{OH}	I_{OH} = –4mA	2.4			VDC
V_{OL}	I_{OL} = +4mA			1.0	VDC
DYNAMIC PERFORMANCE(3) (4)					
PCM1602Y					
THD+N at V_{OUT} = 0dB	f_S = 44.1kHz		0.003	0.009	%
	f_S = 96kHz		0.005		%
	f_S = 192Hz		0.006		%
THD+N at V_{OUT} = –60dB	f_S = 44.1kHz		1.25		%
	f_S = 96kHz		1.40		%
	f_S = 192kHz		1.65		%
Dynamic Range	EIAJ, A-Weighted, f_S = 44.1kHz	94	100		dB
	A-Weighted, f_S = 96kHz		99		dB
	A-Weighted, f_S = 192kHz		98		dB
Signal-to-Noise Ratio	EIAJ, A-Weighted, f_S = 44.1kHz	94	100		dB
	A-Weighted, f_S = 96kHz		99		dB
	A-Weighted, f_S = 192kHz		98		dB
Channel Separation	f_S = 44.1kHz	91	98		dB
	f_S = 96kHz		97		dB
	f_S = 192kHz		96		dB
Level Linearity Error	V_{OUT} = –90dB		±0.5		dB
PCM1602KY					
THD+N at V_{OUT} = 0dB	f_S = 44.1kHz		0.002	0.007	%
	f_S = 96kHz		0.004		%
	f_S = 192kHz		0.005		%
THD+N at V_{OUT} = –60dB	f_S = 44.1kHz		0.7		%
	f_S = 96kHz		0.9		%
	f_S = 192kHz		1.0		%
Dynamic Range	EIAJ, A-Weighted, f_S = 44.1kHz	99	105		dB
	A-Weighted, f_S = 96kHz		103		dB
	A-Weighted, f_S = 192kHz		102		dB
Signal-to-Noise Ratio	EIAJ, A-Weighted, f_S = 44.1kHz	99	105		dB
	A-Weighted, f_S = 96kHz		103		dB
	A-Weighted, f_S = 192kHz		102		dB
Channel Separation	f_S = 44.1kHz	96	103		dB
	f_S = 96kHz		101		dB
	f_S = 192kHz		100		dB
Level Linearity Error	V_{OUT} = –90dB		±0.5		dB
DC ACCURACY					
Gain Error			±1.0	±6	% of FSR
Gain Mismatch, Channel-to-Channel			±1.0	±3	% of FSR
Bipolar Zero Error	$V_{OUT} = 0.5V_{CC}$ at Bipolar Zero		±30	±60	mV
ANALOG OUTPUT					
Output Voltage	Full Scale (–0dB)		62% of V_{CC}		Vp-p
Center Voltage			50% V_{CC}		VDC
Load Impedance	AC Load	5			kΩ

SPECIFICATIONS (Cont.)

All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, system clock = 384f_S (f_S = 44.1kHz), and 24-bit data, unless otherwise noted.

PARAMETER	CONDITIONS	PCM1602Y PCM1602KY MIN	PCM1602Y PCM1602KY TYP	PCM1602Y PCM1602KY MAX	UNITS
DIGITAL FILTER PERFORMANCE					
Filter Characteristics 1, Sharp Roll-Off					
Passband	±0.03dB			0.454f_S	
Passband	–3dB			0.487f_S	
Stopband		0.546f_S			dB
Passband Ripple				±0.03	dB
Stopband Attenuation	Stopband = 0.546f_S	–50			dB
Stopband Attenuation	Stopband = 0.567f_S	–55			
Filter Characteristics 2, Slow Roll-Off					
Passband	±0.5dB			0.198f_S	
Passband	–3dB			0.390f_S	
Stopband		0.884f_S			
Passband Ripple				±0.5	dB
Stopband Attenuation	Stopband = 0.884f_S	–40			dB
Delay Time			20/f_S		sec
De-Emphasis Error			±0.1		dB
ANALOG FILTER PERFORMANCE					
Frequency Response	f = 20kHz		–0.03		dB
	f = 44kHz		–0.20		dB
POWER-SUPPLY REQUIREMENTS(4)					
Voltage Range, V_{DD}		+3.0	+3.3	+3.6	VDC
V_{CC}		+4.5	+5.0	+5.5	VDC
Supply Current, I_{DD}(5)	f_S = 44.1kHz		11	15	mA
	f_S = 96kHz		24		mA
	f_S = 192kHz		19		mA
I_{CC}	f_S = 44.1kHz		27	38	mA
	f_S = 96kHz		28		mA
	f_S = 192kHz		28		mA
Power Dissipation	f_S = 44.1kHz		171	240	mW
	f_S = 96kHz		219		mW
	f_S = 192kHz		203		mW
TEMPERATURE RANGE					
Operation Temperature		–25		+85	°C
Thermal Resistance θ_{JA}	LQFP-48		100		°C/W

NOTES: (1) Pins 38, 40, 41, 45-47 (SCKI, BCK, LRCK, DATA1, DATA2, DATA3). (2) Pins 34-37 (MDI, MC, ML, $\overline{\text{RST}}$). (3) Analog performance specifications are tested with a Shibasoku #725 THD Meter with 400Hz HPF on, 30kHz LPF on, average mode with 20kHz bandwidth limiting. The load connected to the analog output is 5kΩ, or larger, via capacitive loading. (4) Conditions in 192kHz operation are: system clock = 128f_S, DAC3 through DAC6 disabled in Register 8, and oversampling rate = 64f_S in Register 12. (5) CLKO is disabled.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_{DD}	+4.0V
V_{CC}	+6.5V
Ground Voltage Differences	±0.1V
Digital Input Voltage	–0.3V to (6.5V + 0.3V)
Input Current (except power supply)	±10mA
Operating Temperature Under Bias	–40°C to +125°C
Storage Temperature	–55°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 5s)	+260°C
Package Temperature (IR reflow, 10s)	+235°C

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

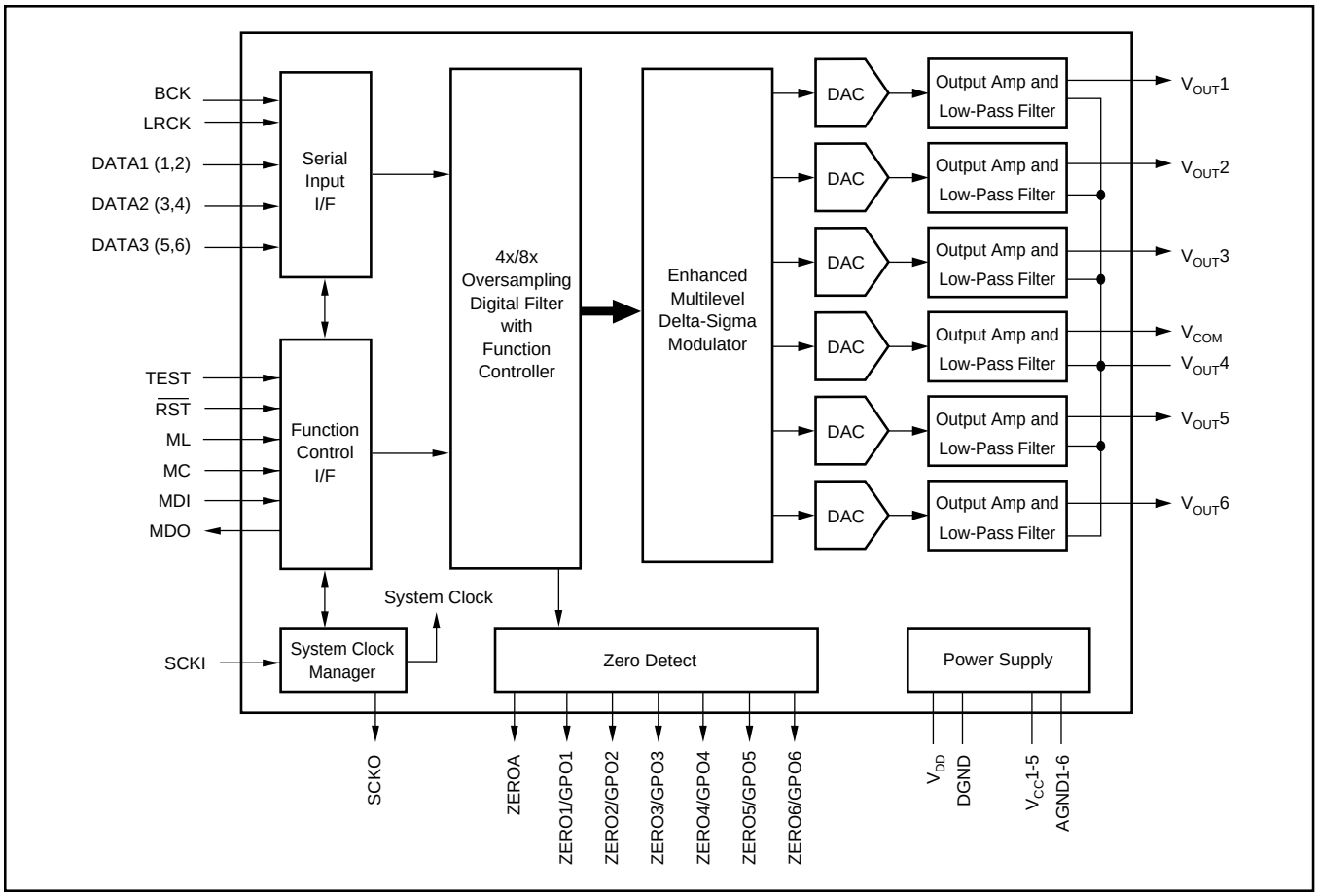
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
PCM1602Y	LQFP-48	340	–25°C to +85°C	PCM1602Y	PCM1602Y	250-Piece Tray
"	"	"	"	"	PCM1602Y/2K	Tape and Reel
PCM1602KY	LQFP-48	340	–25°C to +85°C	PCM1602KY	PCM1602KY	250-Piece Tray
"	"	"	"	"	PCM1602KY/2K	Tape and Reel

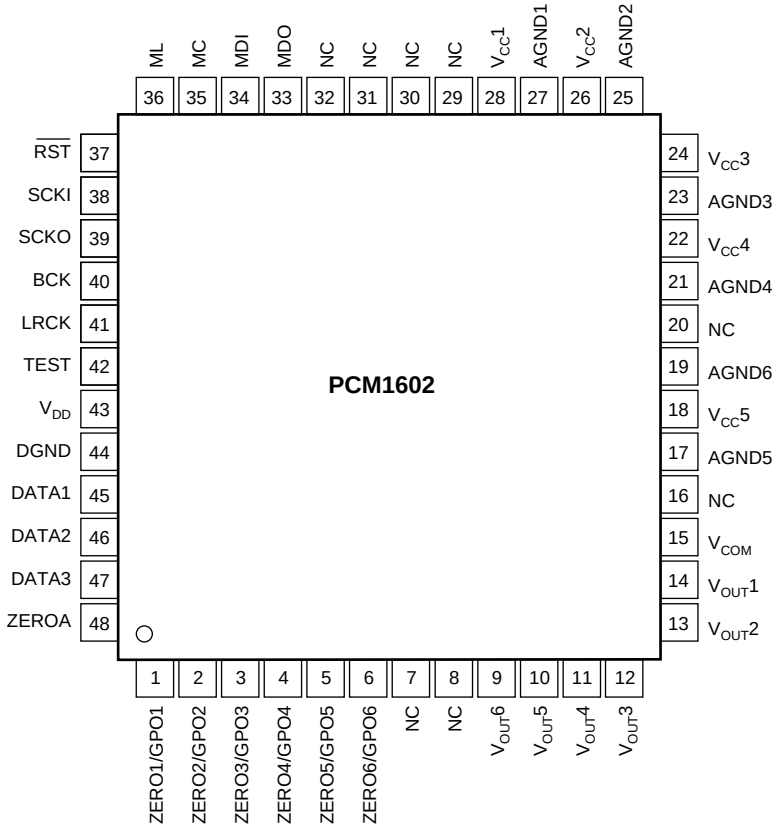
NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "PCM1602Y/2K" will yield a single 2000-piece Tape and Reel.

BLOCK DIAGRAM



PIN CONFIGURATION

Top View **LQFP**



PIN ASSIGNMENTS

PIN	NAME	I/O	DESCRIPTION
1	ZERO1/GPO1	O	Zero Data Flag for $V_{OUT}1$. Can also be used as GPO pin.
2	ZERO2/GPO2	O	Zero Data Flag for $V_{OUT}2$. Can also be used as GPO pin.
3	ZERO3/GPO3	O	Zero Data Flag for $V_{OUT}3$. Can also be used as GPO pin.
4	ZERO4/GPO4	O	Zero Data Flag for $V_{OUT}4$. Can also be used as GPO pin.
5	ZERO5/GPO5	O	Zero Data Flag for $V_{OUT}5$. Can also be used as GPO pin.
6	ZERO6/GPO6	O	Zero Data Flag for $V_{OUT}6$. Can also be used as GPO pin.
7	NC	—	No Connection
8	NC	—	No Connection
9	$V_{OUT}6$	O	Voltage Output of Audio Signal Corresponding to Rch on DATA3. Up to 96kHz.
10	$V_{OUT}5$	O	Voltage Output of Audio Signal Corresponding to Lch on DATA3. Up to 96kHz.
11	$V_{OUT}4$	O	Voltage Output of Audio Signal Corresponding to Rch on DATA2. Up to 96kHz.
12	$V_{OUT}3$	O	Voltage Output of Audio Signal Corresponding to Lch on DATA2. Up to 96kHz.
13	$V_{OUT}2$	O	Voltage Output of Audio Signal Corresponding to Rch on DATA1. Up to 192kHz.
14	$V_{OUT}1$	O	Voltage Output of Audio Signal Corresponding to Lch on DATA1. Up to 192kHz.
15	V_{COM}	O	Common Voltage Output. This pin should be bypassed with a 10µF capacitor to AGND.
16	NC	O	No Connection
17	AGND5	—	Analog Ground
18	$V_{CC}5$	—	Analog Power Supply, +5V
19	AGND6	—	Analog Ground
20	NC	—	No Connection
21	AGND4	—	Analog Ground
22	$V_{CC}4$	—	Analog Power Supply, +5V
23	AGND3	—	Analog Ground
24	$V_{CC}3$	—	Analog Power Supply, +5V
25	AGND2	—	Analog Ground
26	$V_{CC}2$	—	Analog Power Supply, +5V
27	AGND1	—	Analog Ground
28	$V_{CC}1$	—	Analog Power Supply, +5V
29	NC	—	No Connection
30	NC	—	No Connection
31	NC	—	No Connection
32	NC	—	No Connection
33	MDO	O	Serial Data Output for Serial Control Port(3)
34	MDI	I	Serial Data Input for Serial Control Port(1)
35	MC	I	Shift Clock for Serial Control Port(1)
36	ML	I	Latch Enable for Serial Control Port(1)
37	$\overline{RST}$	I	System Reset, Active LOW(1)
38	SCKI	I	System Clock Input. Input frequency is 128, 192, 256, 384, 512, or 768f_S.(2)
39	SCKO	O	Buffered Clock Output. Output frequency is 128, 192, 256, 384, 512, or 768f_S, or one-half of 128, 192, 256, 384, 512, or 768f_S.
40	BCK	I	Shift Clock Input for Serial Audio Data. Clock must be 32, 48, or 64f_S.(2)
41	LRCK	I	Left and Right Clock Input. This clock is equal to the sampling rate, f_S.(2)
42	TEST	—	Test Pin. This pin should be connected to DGND.(1)
43	V_{DD}	—	Digital Power Supply, +3.3V
44	DGND	—	Digital Ground
45	DATA1	I	Serial Audio Data Input for $V_{OUT}1$ and $V_{OUT}2$(2)
46	DATA2	I	Serial Audio Data Input for $V_{OUT}3$ and $V_{OUT}4$(2)
47	DATA3	I	Serial Audio Data Input for $V_{OUT}5$ and $V_{OUT}6$(2)
48	ZEROA	O	Zero Data Flag. Logical “AND” of ZERO1 through ZERO6.

NOTES: (1) Schmitt-Trigger input with internal pull-down, 5V tolerant. (2) Schmitt-Trigger input, 5V tolerant. (3) Tri-state output.

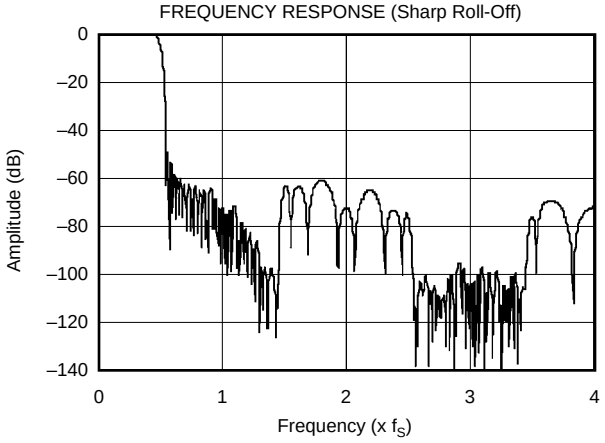
TYPICAL PERFORMANCE CURVES

All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, system clock = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

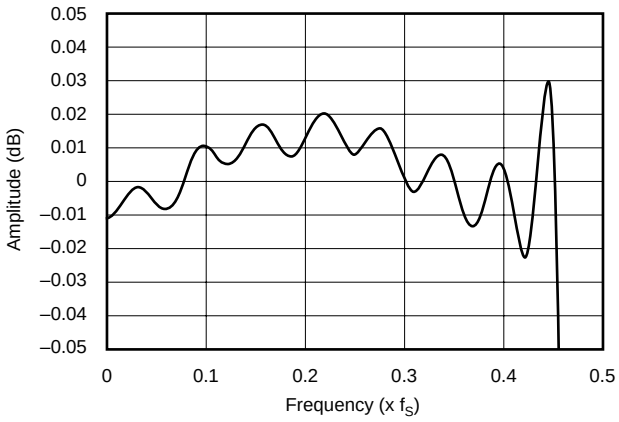
DIGITAL FILTER

Digital Filter (De-Emphasis Off, f_s = 44.1kHz)

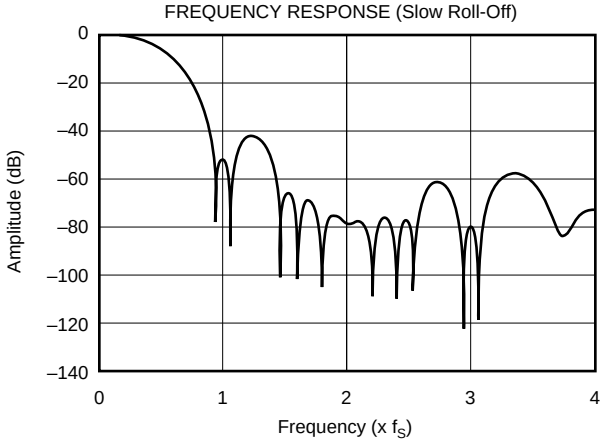
FREQUENCY RESPONSE (Sharp Roll-Off)



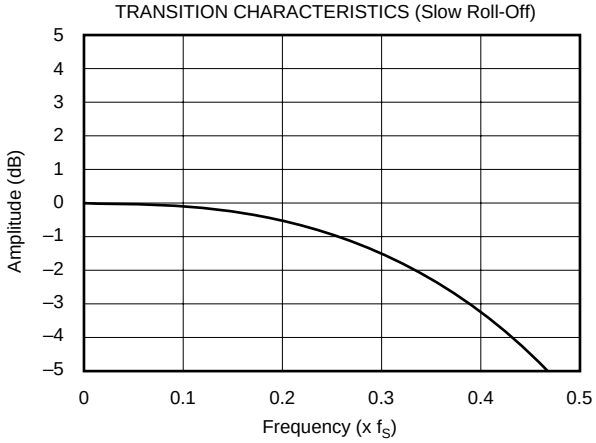
FREQUENCY RESPONSE PASSBAND (Sharp Roll-Off)



FREQUENCY RESPONSE (Slow Roll-Off)

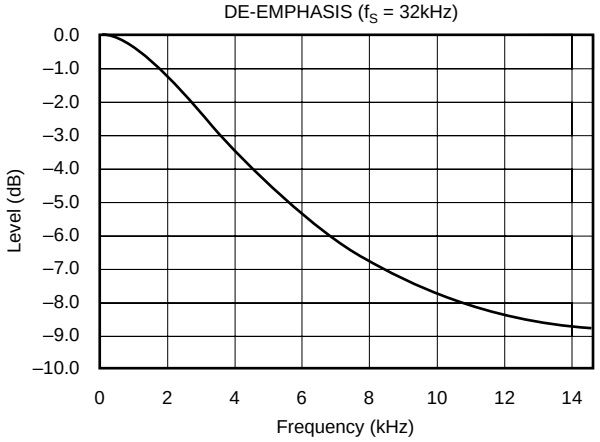


TRANSITION CHARACTERISTICS (Slow Roll-Off)

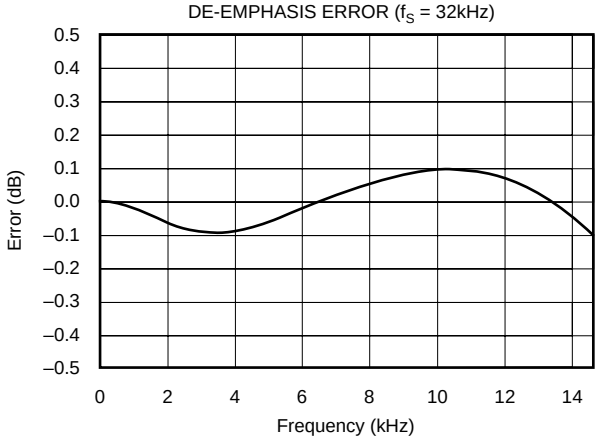


De-Emphasis and De-Emphasis Error

DE-EMPHASIS (f_S = 32kHz)



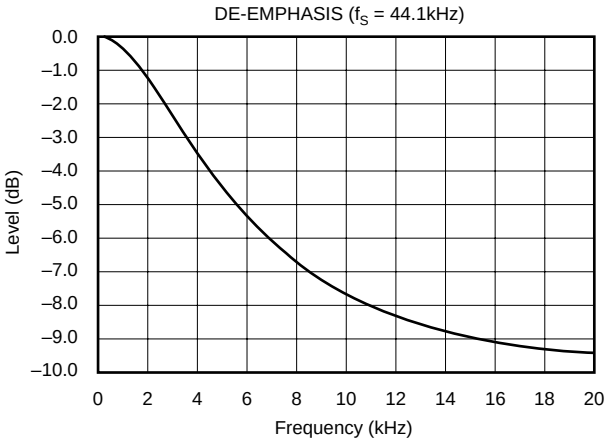
DE-EMPHASIS ERROR (f_S = 32kHz)

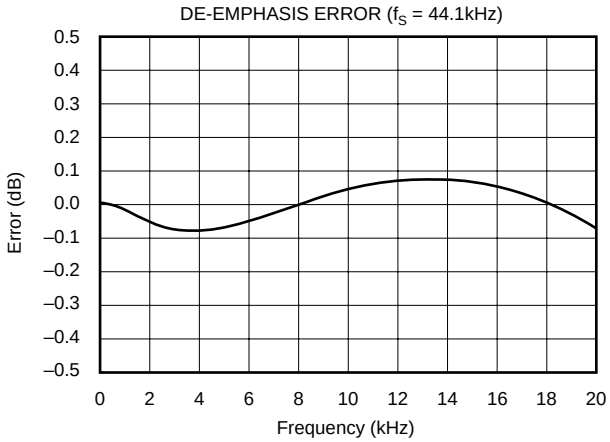


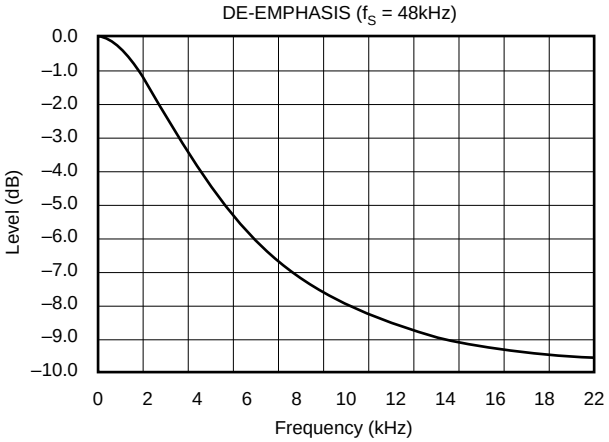
TYPICAL PERFORMANCE CURVES (Cont.)

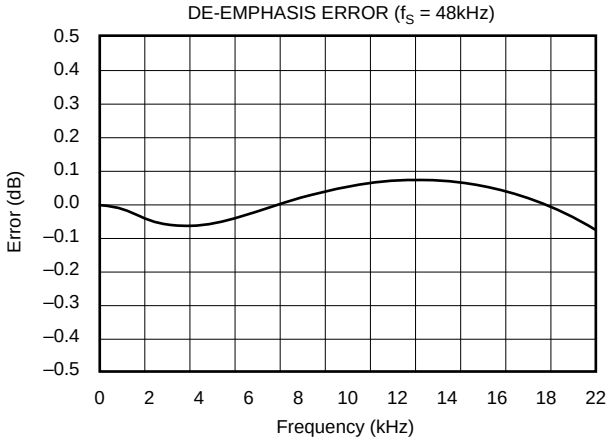
All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, system clock = 384f_S (f_S = 44.1kHz), and 24-bit input data, unless otherwise noted.

De-Emphasis and De-Emphasis Error (Cont.)





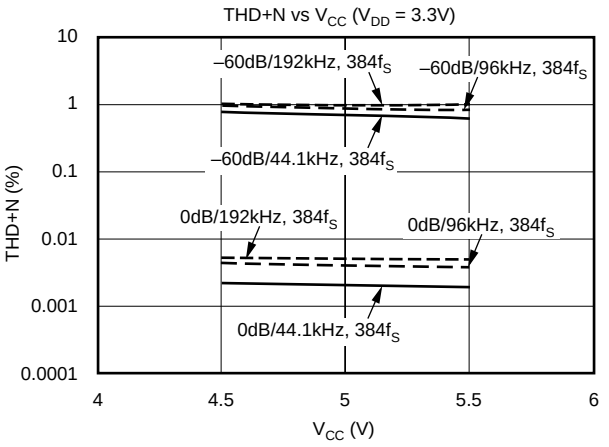


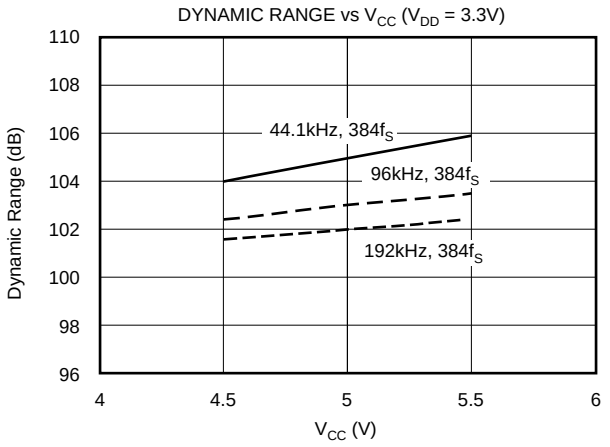


ANALOG DYNAMIC PERFORMANCE

All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, and 24-bit input data, unless otherwise noted. Conditions in 192kHz operation are: system clock = 128f_S, DAC3 through DAC6 = disable of Register 8, and oversampling rate = 64f_S of Register 12.

Supply-Voltage Characteristics

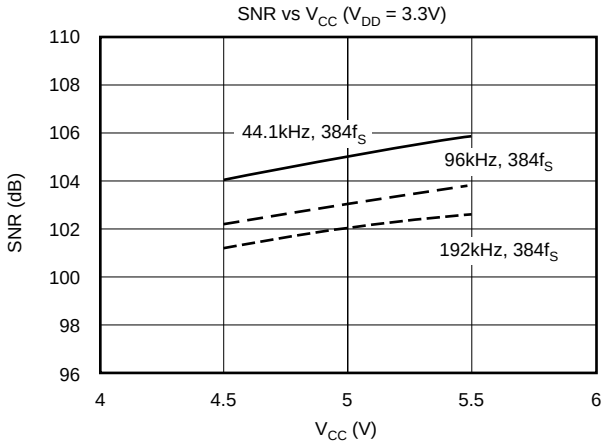


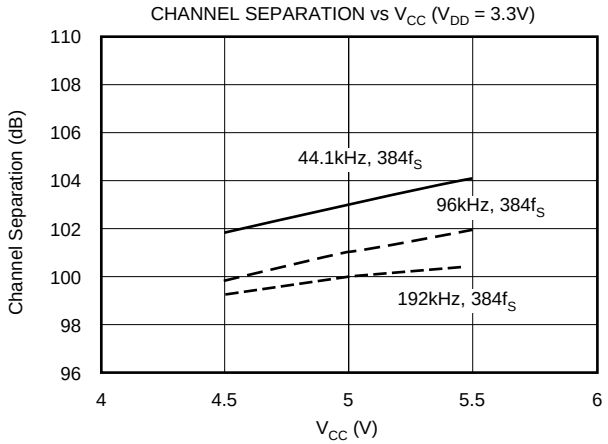


TYPICAL PERFORMANCE CURVES (Cont.)

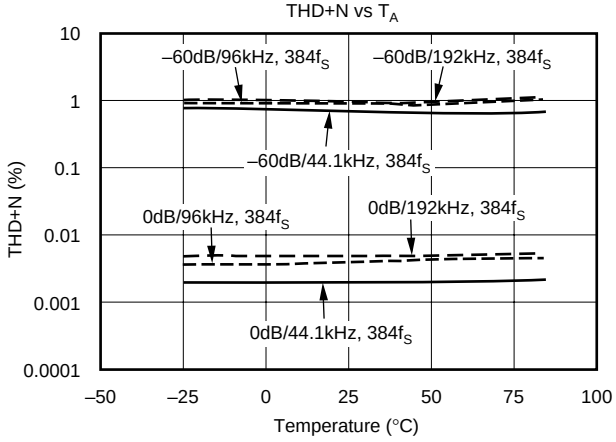
All specifications at T_A = +25°C, V_{CC} = 5.0V, V_{DD} = 3.3V, and 24-bit input data, unless otherwise noted. Conditions in 192kHz operation are: system clock = 128f_S, DAC3 through DAC6 = disable of Register 8, and oversampling rate = 64f_S of Register 12.

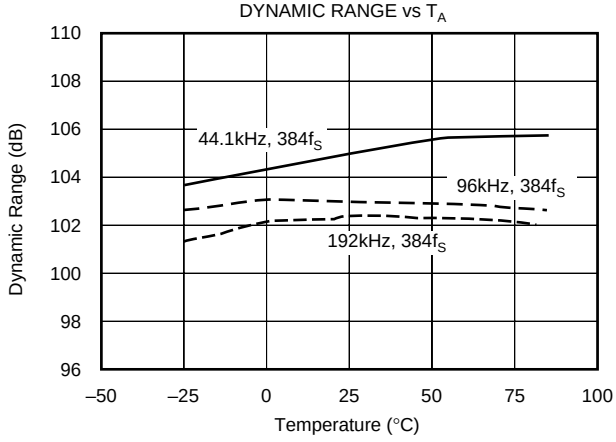
Supply-Voltage Characteristics (Cont.)

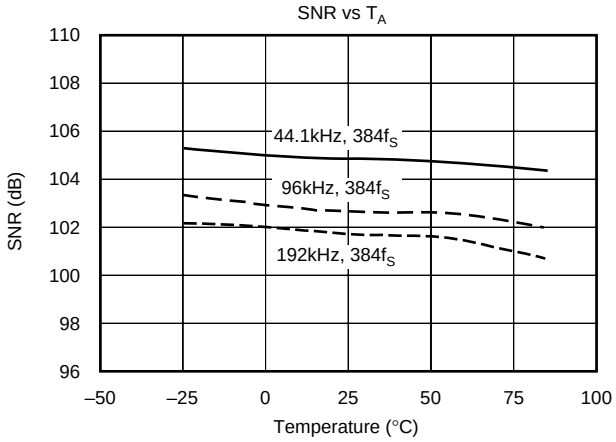


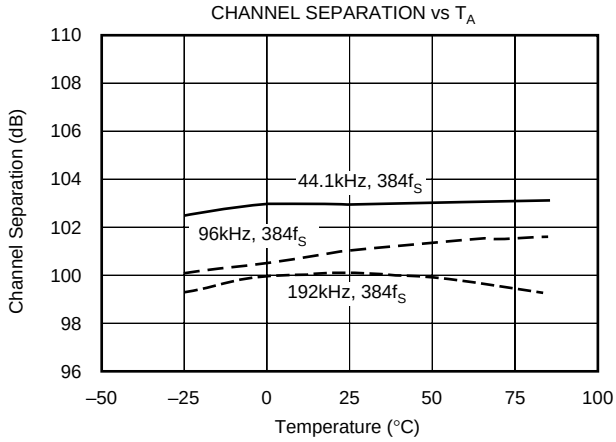


Temperature Characteristics









SYSTEM CLOCK AND RESET FUNCTIONS

SYSTEM CLOCK INPUT

The PCM1602 requires a system clock for operating the digital interpolation filters and multilevel delta-sigma modulators. The system clock is applied at the SCKI input (pin 38). Table I shows examples of system clock frequencies for common audio sampling rates.

Figure 1 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. The PLL1700 multiclock generator from Texas Instruments is an excellent choice for providing the PCM1602 system clock.

The 192kHz sampling frequency operation is available on DATA1 for $V_{OUT}1$ and $V_{OUT}2$. It is recommended that $V_{OUT}3$, $V_{OUT}4$, $V_{OUT}5$, and $V_{OUT}6$ be forced to the bipolar zero level using the DAC3, DAC4, DAC5, and DAC6 bits of Register 9 when operating at 192kHz.

SYSTEM CLOCK OUTPUT

A buffered version of the system clock input is available at the SCKO output (pin 39). SCKO can operate at either full (f_{SCKI}) or half ($f_{SCKI}/2$) rate. The SCKO output frequency may be programmed using the CLKD bit of Register 9. The SCKO output pin can also be enabled or disabled using the CLKE bit of Register 9. If the SCKO output is not required, it is recommended to disable it using the CLKE bit. The default is SCKO enabled.

POWER-ON AND EXTERNAL RESET FUNCTIONS

The PCM1602 includes a power-on reset function, as shown in Figure 2. With the system clock active, and V_{DD} > 2.0V (typical, 1.6V to 2.4V), the power-on reset function will be enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2.0V. After the initialization period, the PCM1602 will be set to its reset default state, as described in the Mode Control Register section of this data sheet.

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)					
	128f_S	**192f_S**	**256f_S**	**384f_S**	**512f_S**	**768f_S**
8kHz	—	—	2.0480	3.0720	4.0960	6.1440
16kHz	—	—	4.0960	6.1440	8.1920	12.2880
32kHz	—	—	8.1920	12.2880	16.3840	24.5760
44.1kHz	—	—	11.2896	16.9344	22.5792	33.8688
48kHz	—	—	12.2880	18.4320	24.5760	36.8640
96kHz	—	—	24.5760	36.8640	49.1520	(1)
192kHz	24.5760	36.8640	(2)	(2)	(2)	(2)

NOTES: (1) The 768f_S system clock rate is not supported for f_S > 64kHz. (2) This system clock is not supported for the given sampling frequency.

TABLE I. System Clock Rates for Common Audio Sampling Frequencies.

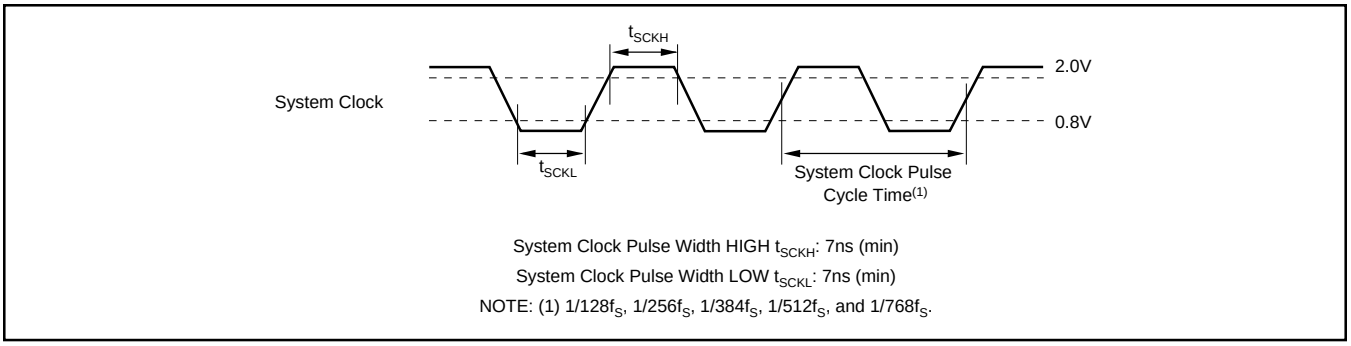


FIGURE 1. System Clock Timing.

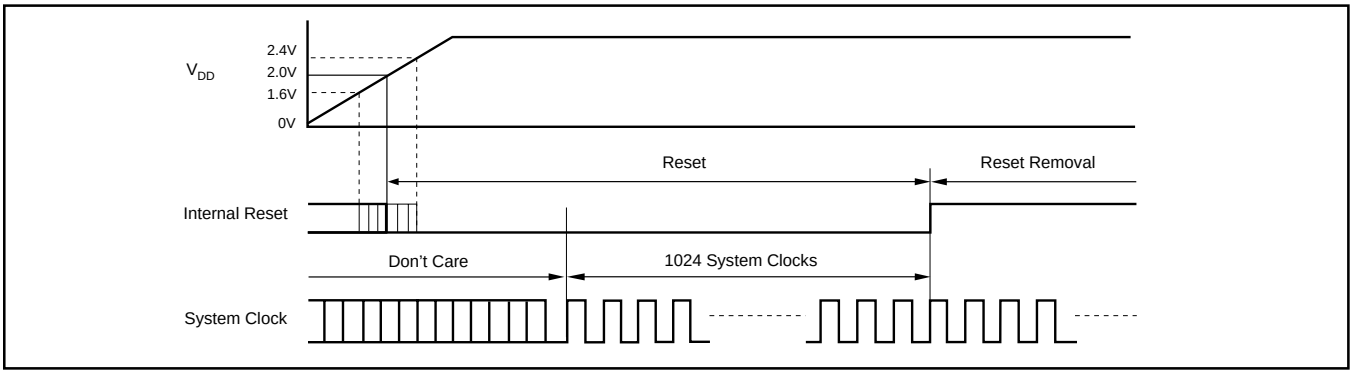


FIGURE 2. Power-On Reset Timing.

The PCM1602 also includes an external reset capability using the $\overline{RST}$ input (pin 37). This allows an external controller or master reset circuit to force the PCM1602 to initialize to its reset default state. For normal operation, $\overline{RST}$ should be set to a logic "1".

The external reset operation and timing is shown in Figure 3. The $\overline{RST}$ pin is set to logic "0" for a minimum of 20ns. After the initialization sequence is completed, the PCM1602 will be set to its reset default state, as described in the Mode Control Registers section of this data sheet.

During the reset period (1024 system clocks), the analog outputs are forced to the bipolar zero level (or $V_{CC}/2$). After the reset period, the internal registers are initialized in the next $1/f_S$ period and, if SCKI, BCK, and LRCK are provided continuously, the PCM1602 provides proper analog output with unit-group delay, as specified in this data sheet.

The external reset is especially useful in applications where there is a delay between PCM1602 power-up and system clock activation. In this case, the $\overline{RST}$ pin should be held at a logic "0" level until the system clock has been activated.

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1602 is comprised of a 5-wire synchronous serial port. It includes LRCK (pin 41), BCK (pin 40), DATA1 (pin 45), DATA2 (pin 46), and DATA3 (pin 47). BCK is the serial audio bit clock, and is used to clock the serial data present on DATA1, DATA2, and DATA3 into the audio interface's serial shift register. Serial data is clocked into the PCM1602 on the rising edge of BCK. LRCK is the serial audio left/right clock. It is used to latch serial data into the serial audio interface's internal registers.

Both LRCK and BCK must be synchronous to the system clock. Ideally, it is recommended that LRCK and BCK be derived from the system clock input, SCKI. LRCK is operated at the sampling frequency (f_S). BCK may be operated at 32, 48, or 64 times the sampling frequency (I^2S format does not support BCK = $32f_S$).

Internal operation of the PCM1602 is synchronized with LRCK. Accordingly, it is held when the sampling rate clock of LRCK is changed, or SCKI and/or BCK is broken at least for one clock cycle. If SCKI, BCK, and LRCK are provided continuously after this hold condition, the internal operation will be resynchronized automatically, less than $3/f_S$ period. In this resynchronize period, and following $3/f_S$, the analog outputs are forced to the bipolar zone level (or $V_{CC}/2$). External resettling is not required.

AUDIO DATA FORMATS AND TIMING

The PCM1602 supports industry-standard audio data formats, including Standard, I^2S, and Left-Justified (see Figure 4). Data formats are selected using the format bits, FMT[2:0], in Register 9. The default data format is 24-bit Standard. All formats require Binary Two's Complement, MSB-first audio data. See Figure 5 for a detailed timing diagram of the serial audio interface.

DATA1, DATA2, and DATA3 each carry two audio channels, designated as the Left and Right channels. The Left channel data always precedes the Right channel data in the serial data stream for all data formats. Table II shows the mapping of the digital input data to the analog output pins.

DATA INPUT	CHANNEL	ANALOG OUTPUT
DATA1	Left	$V_{OUT}1^{(1)}$
DATA1	Right	$V_{OUT}2^{(1)}$
DATA2	Left	$V_{OUT}3^{(2)}$
DATA2	Right	$V_{OUT}4^{(2)}$
DATA3	Left	$V_{OUT}5^{(2)}$
DATA3	Right	$V_{OUT}6^{(2)}$
NOTES: (1) Up to 192kHz. (2) Up to 96kHz.		

TABLE II. Audio Input Data to Analog Output Mapping.

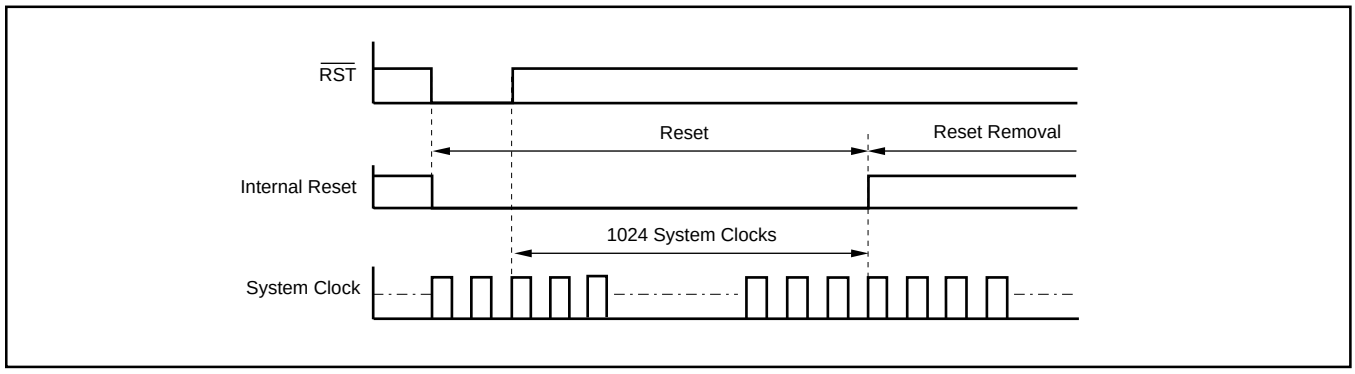


FIGURE 3. External Reset Timing.

SERIAL CONTROL INTERFACE

The serial control interface is a 4-wire synchronous serial port that operates asynchronously to the serial audio interface. The serial control interface is utilized to program and read the on-chip mode registers. The control interface includes MDO (pin 33), MDI (pin 34), MC (pin 35), and ML (pin 36). MDO is the serial data output, used to read back the values of the mode registers; MDI is the serial data input, used to program the mode registers; MC is the serial bit clock, used to shift data in and out of the control port; and ML is the control port latch clock.

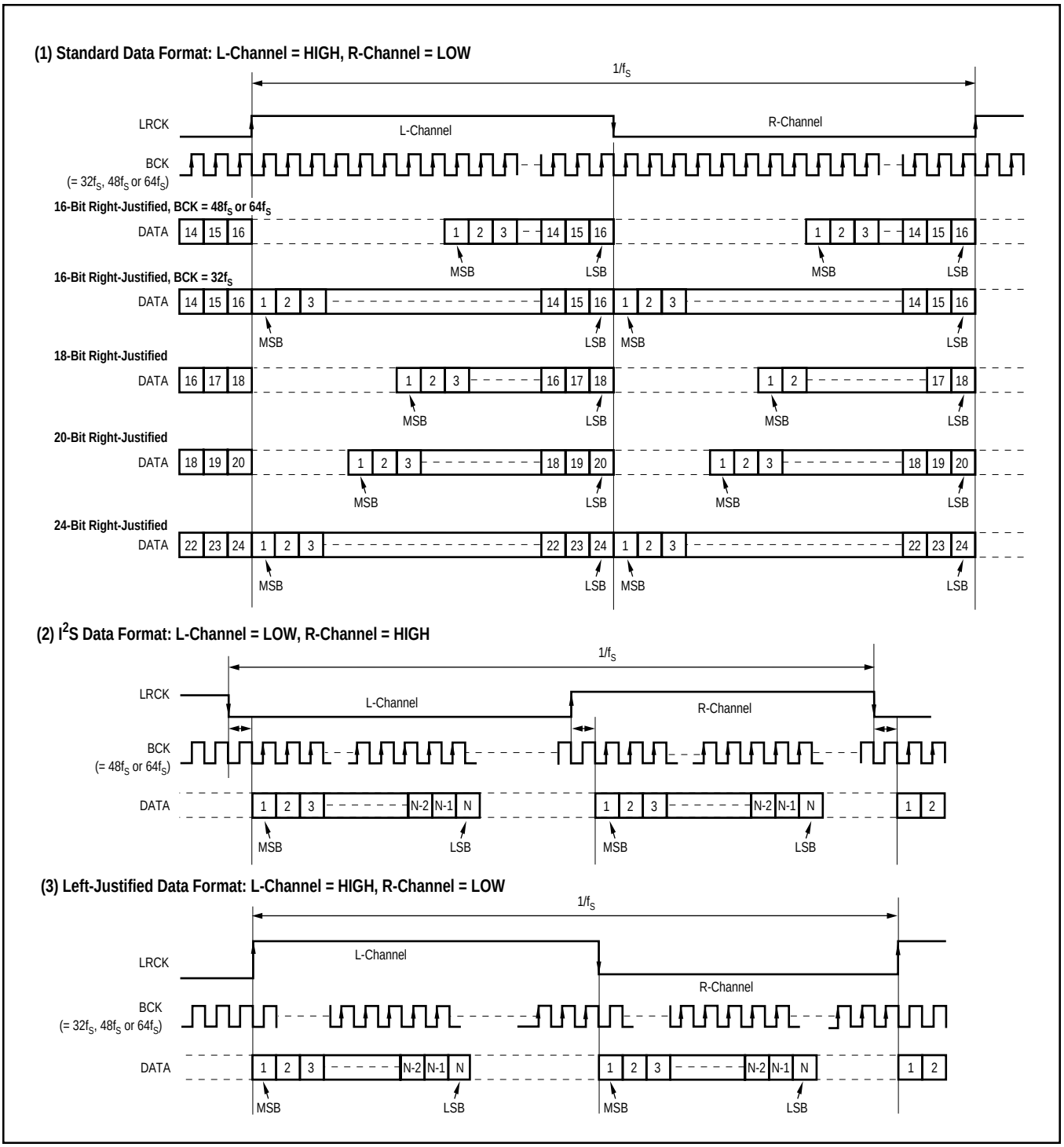
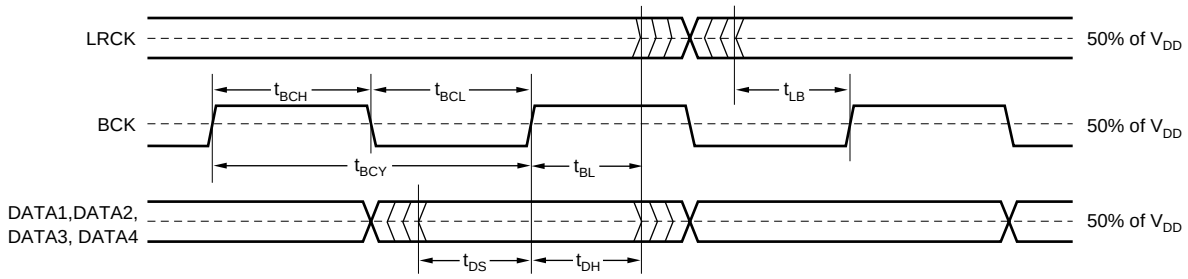


FIGURE 4. Audio Data Input Formats.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{BCY}	BCK Pulse Cycle Time		32, 48, or 64f_S(1)	
t_{BCH}	BCK High Level Time	35		ns
t_{BCL}	BCK Low Level Time	35		ns
t_{BL}	BCK Rising Edge to LRCK Edge	10		ns
t_{LB}	LRCK Falling Edge to BCK Rising Edge	10		ns
t_{DS}	DATA Set Up Time	10		ns
t_{DH}	DATA Hold Time	10		ns

NOTE: (1) f_S is the sampling frequency (e.g., 44.1kHz, 48kHz, 96kHz, etc.)

FIGURE 5. Audio Interface Timing.

REGISTER WRITE OPERATION

All Write operations for the serial control port use 16-bit data words. Figure 6 shows the control data word format. The most significant bit is the Read/Write (R/W) bit. When set to "0", this bit indicates a Write operation. There are seven bits, labeled IDX[6:0], that set the register index (or address) for the Write operation. The least significant eight bits, D[7:0], contain the data to be written to the register specified by IDX[6:0].

Figure 7 shows the functional timing diagram for writing the serial control port. ML is held at a logic "1" state until a register needs to be written. To start the register write cycle, ML is set to logic "0". Sixteen clocks are then provided on MC, corresponding to the 16-bits of the control data word on MDI. After the sixteenth clock cycle has completed, ML is set to logic "1" to latch the data into the indexed mode control register.

SINGLE REGISTER READ OPERATION

Read operations utilize the 16-bit control word format shown in Figure 6. For Read operations, the R/W bit is set to "1". Read operations ignore the index bits, IDX[6:0], of the control data word. Instead, the REG[6:0] bits in Control Register 11 are used to set the index of the register that is to be read during the Read operation. Bits IDX[6:0] should be set to 00_H for Read operations.

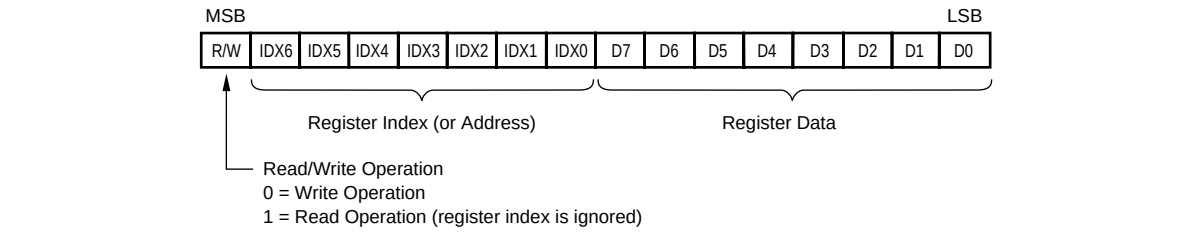


FIGURE 6. Control Data Word Format for MDI.

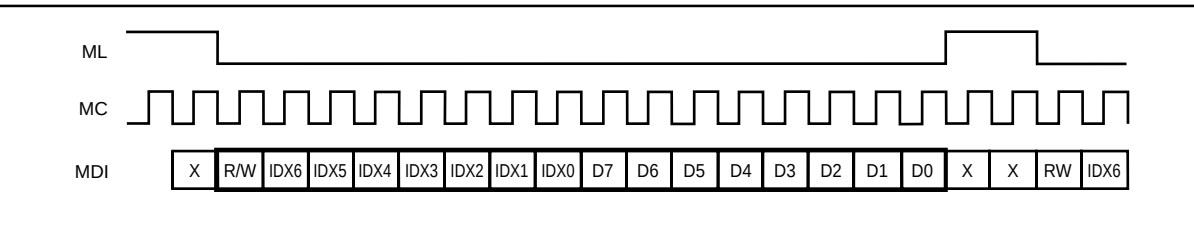


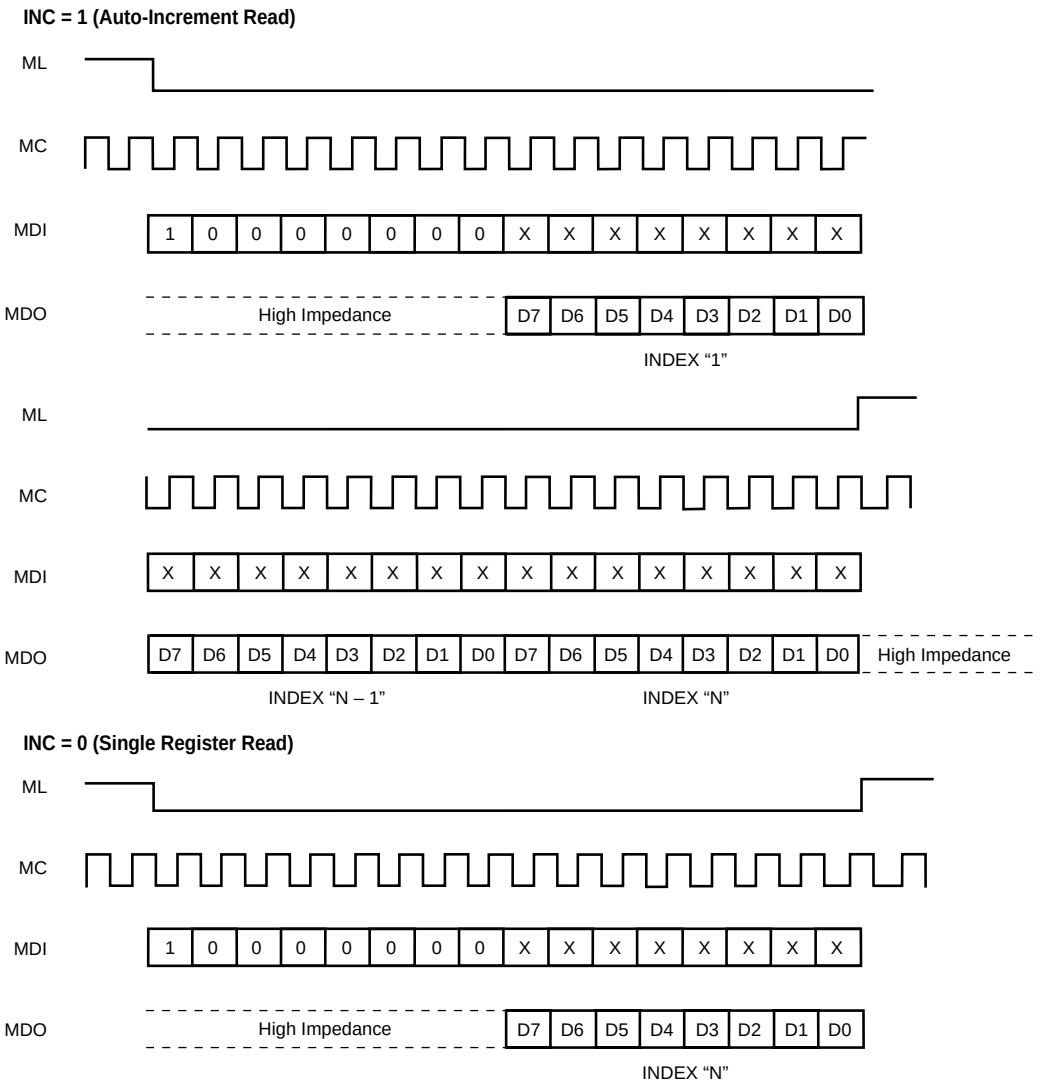
FIGURE 7. Write Operation Timing.

The details of the Read operation are shown in Figure 8. First, Control Register 11 must be written with the index of the register to be read back. Additionally, the INC bit must be set to logic “0” in order to disable the Auto-Increment Read function. The Read cycle is then initiated by setting ML to logic “0” and setting the R/W bit of the control data word to logic “1”, indicating a Read operation. MDO remains at a high-impedance state until the last eight bits of the 16-bit read cycle, which corresponds to the eight data bits of the register indexed by the REG[6:0] bits of Control Register 11. The Read cycle is completed when ML is set to “1”, immediately after the MC clock cycle for the least significant bit of indexed control register has completed.

AUTO-INCREMENT READ OPERATION

The Auto-Increment Read function allows for multiple registers to be read sequentially. The Auto-Increment Read function is enabled by setting the INC bit of Control Register 11 to “1”. The sequence always starts with Register 1, and ends with the register indexed by the REG[6:0] bits in Control Register 11.

Figure 8 shows the timing of the Auto-Increment Read operation. The operation begins by writing Control Register 11, setting INC to “1”, and setting REG[6:0] to the last register to be read in the sequence. The actual Read operation starts on the next HIGH to LOW transition of the ML pin.



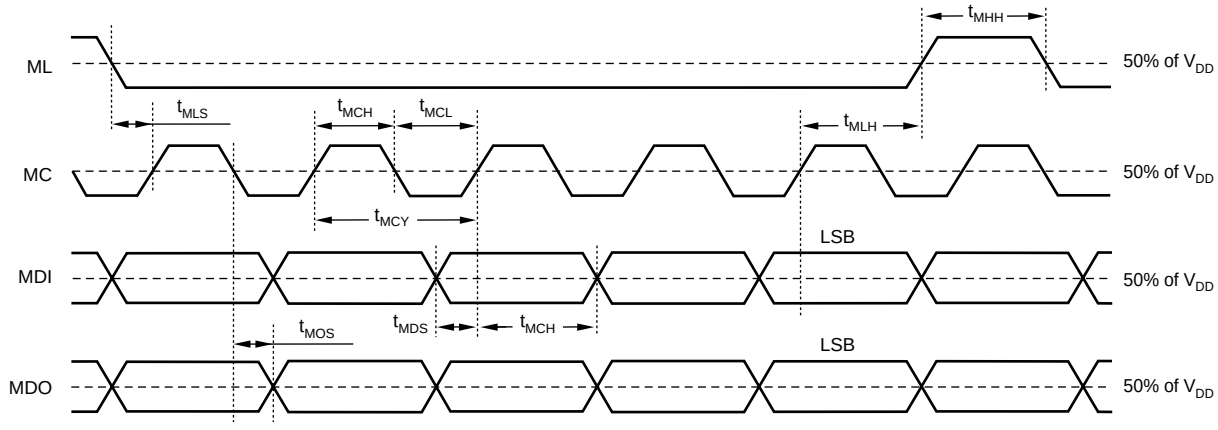
NOTES: (1) X = Don’t care. (2) Index which it begins to read in the read mode can set by REG[6:0] in Register 11, data from Register 1 to Register 12 can be read by setting it as “INC = 1” in Register 11. For example, set REG[6:0] = “0001001” to read from Register 9. (INC = “0” or “1”.)

FIGURE 8. Read Operation Timing.

The Read cycle starts by setting the R/W bit of the control word to “1”, and setting all of the IDX[6:0] bits to “0”. All subsequent bits input on the MDI are ignored while ML is set to “0”. For the first eight clocks of the Read cycle, MDO is set to a high-impedance state. This is followed by a sequence of 8-bit words, each corresponding the data contained in Control Registers 1 through N, where N is defined by the REG[6:0] bits in Control Register 11. The Read cycle is completed when ML is set to “1”, immediately after the MC clock cycle for the least significant bit of Control Register N has completed.

CONTROL INTERFACE TIMING REQUIREMENTS

Figure 9 shows a detailed timing diagram for the Serial Control interface. Pay special attention to the setup and hold times, as well as t_{MLS} and t_{MLH}, which define minimum delays between edges of the ML and MC clocks. These timing parameters are critical for proper control port operation.



SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{MCY}	MC Pulse Cycle Time	100		ns
t_{MCL}	MC Low Level Time	50		ns
t_{MCH}	MC High Level Time	50		ns
t_{MHH}	ML High Level Time	300		ns
t_{MLS}	ML Falling Edge to MC Rising Edge	20		ns
t_{MLH}	ML Hold Time(1)	20		ns
t_{MDH}	MDI Hold Time	15		ns
t_{MDS}	MDL Set Up Time	20		ns
t_{MOS}	MC Falling Edge to MDSO Stable		30	ns

NOTE: (1) MC rising edge for LSB to ML rising edge.

FIGURE 9. Control Interface Timing.

MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM1602 includes a number of user-programmable functions that are accessed via control registers. The registers are programmed using the Serial Control Interface that was previously discussed in this data sheet. Table III lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

The mode control register map is shown in Table IV. Each register includes a R/W bit that determines whether a register read (R/W = 1) or write (R/W = 0) operation is performed. Each register also includes an index (or address) indicated by the IDX[6:0] bits.

Reserved Registers

Registers 0 and 12 are reserved for factory use. To ensure proper operation, the user should not write or read these registers.

FUNCTION	RESET DEFAULT	CONTROL REGISTER	INDEX, IDX[6:0]
Digital Attenuation Control, 0dB to –63dB in 0.5dB Steps	0dB, No Attenuation	1 through 6	AT1[7:0], AT2[7:0] AT3[7:0], AT4[7:0] AT5[7:0], AT6[7:0]
Soft Mute Control	Mute Disabled	7	MUT[6:1]
DAC 1-6 Operation Control	DAC 1-6 Enabled	8	DAC[6:1]
Audio Data Format Control	24-Bit Standard Format	9	FMT[2:0]
Digital Filter Roll-Off Control	Sharp Roll-Off	9	FLT
SCKO Frequency Selection	Full Rate (= f_{SCKI})	9	CLKD
SCKO Output Enable	SCKO Enabled	9	CLKE
De-Emphasis All Channel Function Control	De-Emphasis All Channel Disabled	10	DMC
De-Emphasis All Channel Sample Rate Selection	44.1kHz	10	DMF[1:0]
Output Phase Select	Normal Phase	10	DREV
Zero Flag Polarity Select	High	10	ZREV
Read Register Index Control	REG[6:0] = 01_H	11	REG[6:0]
Read Auto-Increment Control	Auto-Increment Disabled	11	INC
General-Purpose Output Enable	Zero Flag Enabled	12	GPOE
General-Purpose Output Bits (GPO1-GPO6)	Disabled	12	GPO[6:1]
Oversampling Rate Control	64x	12	OVER

TABLE III. User-Programmable Mode Controls.

IDX (B8-B14)	REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
00_H	Register0	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	N/A(1)	N/A(1)	N/A(1)	N/A(1)	N/A(1)	N/A(1)	N/A(1)	N/A(1)
01_H	Register1	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
02_H	Register2	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
03_H	Register3	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
04_H	Register4	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
05_H	Register5	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
06_H	Register6	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60
07_H	Register7	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(2)	RSV(2)	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1
08_H	Register8	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(2)	RSV(2)	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1
09_H	Register9	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(2)	RSV(2)	FLT	CLKD	CLKE	FMT2	FMT1	FMT0
$0A_H$	Register10	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV(2)	ZREV	DREV	DMF1	DMF0	DMC	DMC	DMC
$0B_H$	Register11	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	INC	REG6	REG5	REG4	REG3	REG2	REG1	REG0
$0C_H$	Register12	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	GPOE	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1

NOTES: (1) N/A = not assigned. No operation even if setting any data. (2) RSV = reserved for test operation. It should be set “0” during regular operation.

TABLE IV. Mode Control Register Map.

REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 1	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT17	AT16	AT15	AT14	AT13	AT12	AT11	AT10
Register 2	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT27	AT26	AT25	AT24	AT23	AT22	AT21	AT20
Register 3	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT37	AT36	AT35	AT34	AT33	AT32	AT31	AT30
Register 4	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT47	AT46	AT45	AT44	AT43	AT42	AT41	AT40
Register 5	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT57	AT56	AT55	AT54	AT53	AT52	AT51	AT50
Register 6	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	AT67	AT66	AT65	AT64	AT63	AT62	AT61	AT60

R/W **Read/Write Mode Select**

When R/W = 0, a write operation is performed.

When R/W = 1, a read operation is performed.

Default Value: 0

ATx[7:0] **Digital Attenuation Level Setting**

where x = 1 through 6, corresponding to the DAC output $V_{OUT}x$.

These bits are Read/Write.

Default Value: $1111\ 1111_B$

Each DAC output, $V_{OUT}1$ through $V_{OUT}6$, has a digital attenuator associated with it. The attenuator may be set from 0dB to –63dB, in 0.5dB steps. Changes in attenuator levels are made by incrementing or decrementing, by one step (0.5dB), for every $8/f_S$ time interval until the programmed attenuator setting is reached. Alternatively, the attenuator may be set to infinite attenuation (or mute).

The attenuation level may be set using the formula below.

Attenuation Level (dB) = 0.5 $(ATx[7:0]_{DEC} - 255)$

where: $ATx[7:0]_{DEC}$ = 0 through 255

for: $ATx[7:0]_{DEC}$ = 0 through 128, the attenuator is set to infinite attenuation.

The following table shows attenuator levels for various settings.

ATx[7:0]	Decimal Value	Attenuator Level Setting
$1111\ 1111_B$	255	0dB, No Attenuation (default)
$1111\ 1110_B$	254	–0.5dB
$1111\ 1101_B$	253	–1.0dB
•	•	•
•	•	•
•	•	•
$1000\ 0010_B$	130	–62.5dB
$1000\ 0001_B$	129	–63.0dB
$1000\ 0000_B$	128	Mute
•	•	•
•	•	•
•	•	•
$0000\ 0000_B$	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 7	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	MUT6	MUT5	MUT4	MUT3	MUT2	MUT1

R/W **Read/Write Mode Select**

When R/W = 0, a write operation is performed.
When R/W = 1, a read operation is performed.
Default Value: 0

MUTx **Soft Mute Control**

Where x = 1 through 6, corresponding to the DAC output $V_{OUT}x$.
These bits are Read/Write.
Default Value: 0

MUTx = 0	Mute Disabled (default)
MUTx = 1	Mute Enabled

The mute bits, MUT1 through MUT6, are used to enable or disable the Soft Mute function for the corresponding DAC outputs, $V_{OUT}1$ through $V_{OUT}6$. The Soft Mute function is incorporated into the digital attenuators. When Mute is disabled (MUTx = 0), the attenuator and DAC operate normally. When Mute is enabled by setting MUTx = 1, the digital attenuator for the corresponding output will be decreased from the current setting to the infinite attenuation setting one attenuator step (0.5dB) at a time. This provides a quiet, pop-free muting of the DAC output. Upon returning from Soft Mute, by setting MUTx = 0, the attenuator will be increased one step at a time to the previously programmed attenuator level.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 8	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1

R/W **Read/Write Mode Select**

When R/W = 0, a write operation is performed.
When R/W = 1, a read operation is performed.
Default Value: 0

DACx **DAC Operation Control**

where x = 1 through 6, corresponding to the DAC output $V_{OUT}x$.
These bits are Read/Write.
Default Value: 0

DACx = 0	DAC Operation Enabled (default)
DACx = 1	DAC Operation Disabled

The DAC operation controls are used to enable and disable the DAC outputs, $V_{OUT}1$ through $V_{OUT}6$. When DACx = 0, the output amplifier input is connected to the DAC output. When DACx = 1, the output amplifier input is switched to the DC common-mode voltage (V_{COM}), equal to $V_{CC}/2$.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 9	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	RSV	FLT	CLKD	CLKE	FMT2	FMT1	FMT0

R/W **Read/Write Mode Select**

When R/W = 0, a write operation is performed.
When R/W = 1, a read operation is performed.
Default Value: 0

FLT **Digital Filter Roll-Off Control**

These bits are Read/Write.
Default Value: 0

FLT = 0	Sharp Roll-Off (default)
FLT = 1	Slow Roll-Off

The FLT bit allows the user to select the digital filter roll-off that is best suited to their application. Two filter roll-off sections are available: Sharp or Slow. The filter responses for these selections are shown in the Typical Performance Curves section of this data sheet.

CLKD **SCKO Frequency Selection**

This bit is Read/Write.
Default Value: 0

CLKD = 0	Full Rate, $f_{SCKO} = f_{SCKI}$ (default)
CLKD = 1	Half Rate, $f_{SCKO} = f_{SCKL}/2$

The CLKD bit is used to determine the clock frequency at the system clock output pin, SCKO.

CLKE **SCKO Output Enable**

This bit is Read/Write.
Default Value: 0

CLKE = 0	SCKO Enabled (default)
CLKE = 1	SCKO Disabled

The CLKE bit is used to enable or disable the system clock output pin, SCKO. When SCKO is enabled, it will output either a full or half rate clock, based upon the setting of the CLKD bit. When SCKO is disabled, it is set to a LOW level.

FMT[2:0] **Audio Interface Data Format**

These bits are Read/Write.
Default Value: 000_B

FMT[2:0]	Audio Data Format Selection
000	24-Bit Standard Format, Right-Justified Data (default)
001	20-Bit Standard Format, Right-Justified Data
010	18-Bit Standard Format, Right-Justified Data
011	16-Bit Standard Format, Right-Justified Data
100	I^2S Format, 16- to 24-bits
101	Left-Justified Format, 16- to 24-Bits
110	Reserved
111	Reserved

The FMT[2:0] bits are used to select the data format for the serial audio interface.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 10	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	RSV	ZREV	DREV	DMF1	DMF0	DMC	DMC	DMC

R/W **Read/Write Mode Select**

When R/W = 0, a write operation is performed.

When R/W = 1, a read operation is performed.

Default Value: 0

DMF[1:0] **Sampling Frequency Selection for the De-Emphasis Function**

These bits are Read/Write.

Default Value: 00_B

DMF[1:0]	De-Emphasis Same Rate Selection
00	44.1kHz (default)
01	48kHz
10	32kHz
11	Reserved

The DMF[1:0] bits are used to select the sampling frequency used for the Digital De-Emphasis function when it is enabled. The de-emphasis curves are shown in the Typical Performance Curves section of this data sheet. The table below shows the available sampling frequencies.

DMC **Digital De-Emphasis, All Channels Function Control**

This bit is Read/Write.

Default Value: 0

DMC = 0	De-Emphasis Disabled for All Channels (default)
DMC = 1	De-Emphasis Enabled for All Channels

The DMC bit is used to enable or disable the De-Emphasis function for all channels. To select more than one of three DMC bits, enable or disable the De-Emphasis function.

DREV **Output Phase Select**

Default Value: 0

DREV = 0	Normal Output (default)
DREV = 1	Inverted Output

The DREV bit is the output analog signal phase control.

ZREV **Zero Flag Polarity Select**

Default Value: 0

ZREV = 0	Zero Flag Pins HIGH at a Zero Detect (default)
ZREV = 1	Zero Flag Pins LOW at a Zero Detect

The ZREV bit allows the user to select the polarity of the Zero Flag pins.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 11	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	INC	REG6	REG5	REG4	REG3	REG2	REG1	REG0

R/W **Read/Write Mode Select**

When R/W = 0, a write operation is performed.

When R/W = 1, a read operation is performed.

Default Value: 0

INC **Auto-Increment Read Control**

This bit is Read/Write.

Default Value: 0

INC = 0	Auto-Increment Read Disabled (default)
INC = 1	Auto-Increment Read Enabled

The INC bit is used to enable or disable the Auto-Increment Read feature of the Serial Control Interface. Refer to the Serial Control Interface section of this data sheet for details regarding Auto-Increment Read operation.

REG[6:0] **Read Register Index**

These bits are Read/Write.

Default Value: 01_H

The REG[6:0] bits are used to set the index of the register to be read when performing the Single Register Read operation. In the case of an Auto-Increment Read operation, the REG[6:0] bits indicate the index of the last register to be read in the Auto-Increment Read sequence. For example, if Registers 1 through 6 are to be read during an Auto-Increment Read operation, the REG[6:0] bits would be set to 06_H. Refer to the Serial Control Interface section of this data sheet for details regarding the Single Register and Auto-Increment Read operations.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 12	R/W	IDX6	IDX5	IDX4	IDX3	IDX2	IDX1	IDX0	OVER	GPOE	GPO6	GPO5	GPO4	GPO3	GPO2	GPO1

GPOx **General-Purpose Logic Output**

Where: x = 1 through 6, corresponding pins GPO1 through GPO6.

These bits are Read/Write.

Default Value: 0

GPOx = 0	Set GPOx to “0”
GPOx = 1	Set GPOx to “1”

The general-purpose output pins, GPO1 through GPO6, are enabled by setting GPOE = 1. These pins are used as general-purpose outputs for controlling user-defined logic functions. When general-purpose outputs are disabled (GPOE = 0), they default to the zero-flag function, ZERO1 through ZERO6.

GPOE **General-Purpose Output Enable**

This bit is Read/Write.

Default Value: 0

GPOE = 0	General-Purpose Outputs Disabled Pins default to zero-flag function (ZERO1 through ZERO6).
GPOE = 1	General-Purpose Outputs Enabled Data written to GPO1 through GPO6 will appear at the corresponding pins.

OVER **Oversampling Rate Control**

This bit is Read/Write.

Default Value: 0

System Clock Rate = 256, 384, 512, or 768f_S:

OVER = 0	64x Oversampling (default)
OVER = 1	128x Oversampling

System Clock Rate = 128 or 192f_S:

OVER = 0	32x Oversampling (default)
OVER = 1	64x Oversampling

The OVER bit is used to control the oversampling rate of the delta-sigma DACs. The OVER = 1 setting is recommended when the oversampling rate is 192kHz (system clock rate is 128 or 192f_S).

ANALOG OUTPUTS

The PCM1602 includes six independent output channels, $V_{OUT}1$ through $V_{OUT}6$. These are unbalanced outputs, each capable of driving 3.1Vp-p typical into a 5kΩ AC load with V_{CC} = +5V. The internal output amplifiers for $V_{OUT}1$ through $V_{OUT}6$ are DC biased to the common-mode (or bipolar zero) voltage, equal to $V_{CC}/2$.

The output amplifiers include an RC continuous-time filter, which helps to reduce the out-of-band noise energy present at the DAC outputs due to the noise-shaping characteristics of the PCM1602's delta-sigma DACs. The frequency response of this filter is shown in Figure 10. By itself, this filter is not enough to attenuate the out-of-band noise to an acceptable level for most applications. An external low-pass filter is required to provide sufficient out-of-band noise rejection. Further discussion of DAC post-filter circuits is provided in the Applications Information section of this data sheet.

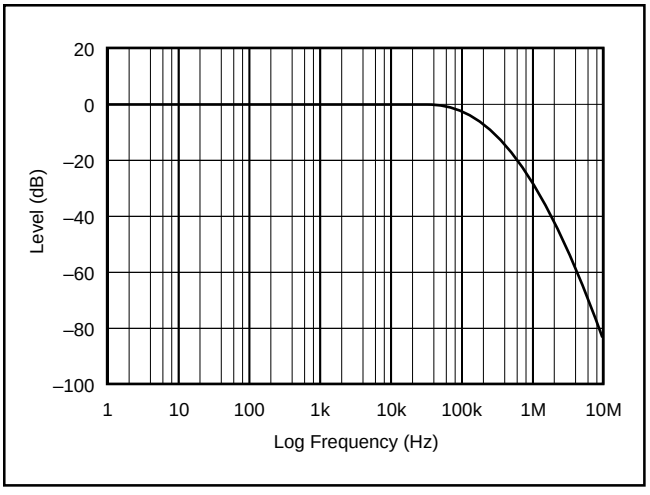


FIGURE 10. Output Filter Frequency Response.

V_{COM} OUTPUT

One unbuffered, common-mode voltage output pin, V_{COM} (pin 15), is brought out for decoupling purposes. This pin is nominally biased to a DC voltage level equal to $V_{CC}/2$. If this pin is to be used to bias external circuitry, a voltage follower is required for buffering purposes. Figure 11 shows an example of using the V_{COM} pin for external biasing applications.

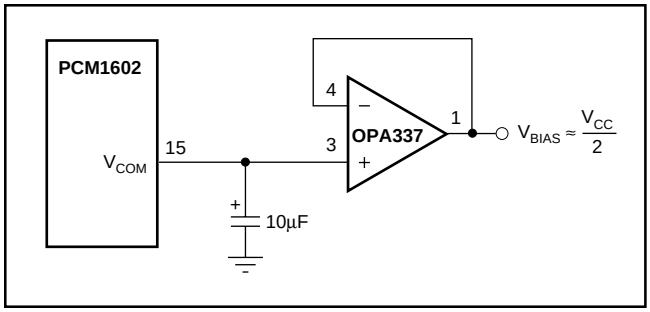


FIGURE 11. Biasing External Circuits Using the V_{COM} Pin.

ZERO FLAG

Zero Detect Condition

Zero Detection for each output channel is independent from the others. If the data for a given channel remains at a “0” level for 1024 sample periods (or LRCK clock periods), a Zero Detect condition exists for that channel.

Zero Output Flags

Given that a Zero Detect condition exists for one or more channels, the Zero Flag pins for those channels will be set to a logic “1” state. There are Zero Flag pins for each channel, ZERO1 through ZERO6 (pins 1 through 6). In addition, all six Zero Flags are logically “AND”ed together, and the result provided at the ZEROA pin (pin 48), which is set to a logic “1” state when all channels indicate a Zero Detect condition. The Zero Flag pins can be used to operate external mute circuits, or used as status indicators for a microcontroller, audio signal processor, or other digitally controlled functions.

The active polarity of zero flag output can be inverted by setting the ZREV bit of Control Register 10 to “1”. The reset default is active high output, or ZREV = 0.

APPLICATIONS INFORMATION

CONNECTION DIAGRAMS

A basic connection diagram with the necessary power-supply bypassing and decoupling components is shown in Figure 12. Texas Instruments recommends using the component values shown in Figure 12 for all designs.

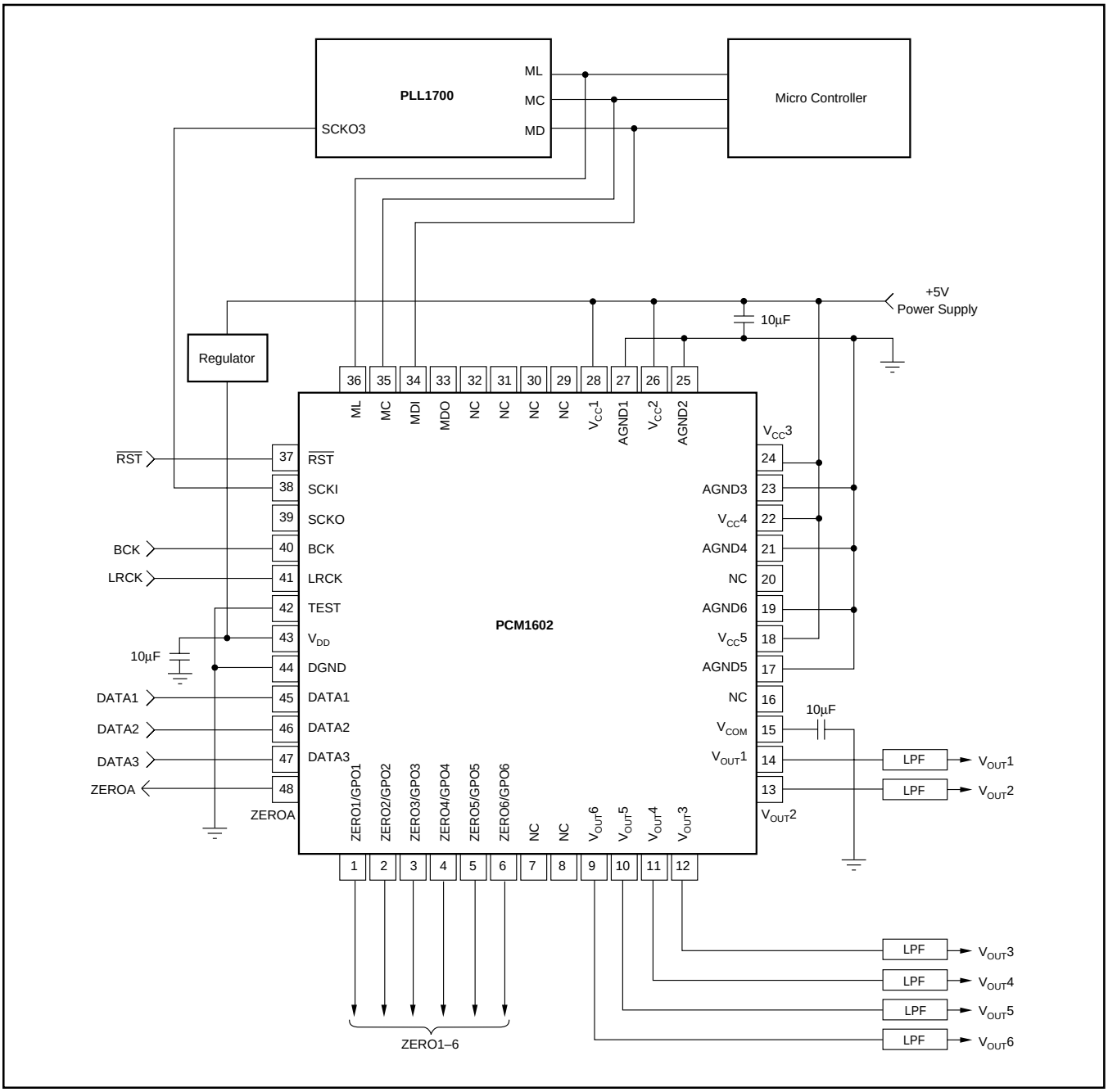


FIGURE 12. Basic Connection Diagram.

A typical application diagram is shown in Figure 13. The REG1117-3.3 from Texas Instruments is used to generate +3.3V for V_{DD} from the +5V analog power supply. The PLL1700E from Texas Instruments is used to generate the system clock input at SCKI, as well as generating the clock for the audio signal processor.

Series resistors (22Ω to 100Ω) are recommended for SCKI, LRCK, BCK, DATA1, DATA2, and DATA3. The series resistor combines with the stray PCB and device input capacitance to form a low-pass filter which removes high-frequency noise from the digital signal, thus reducing high-frequency emission.

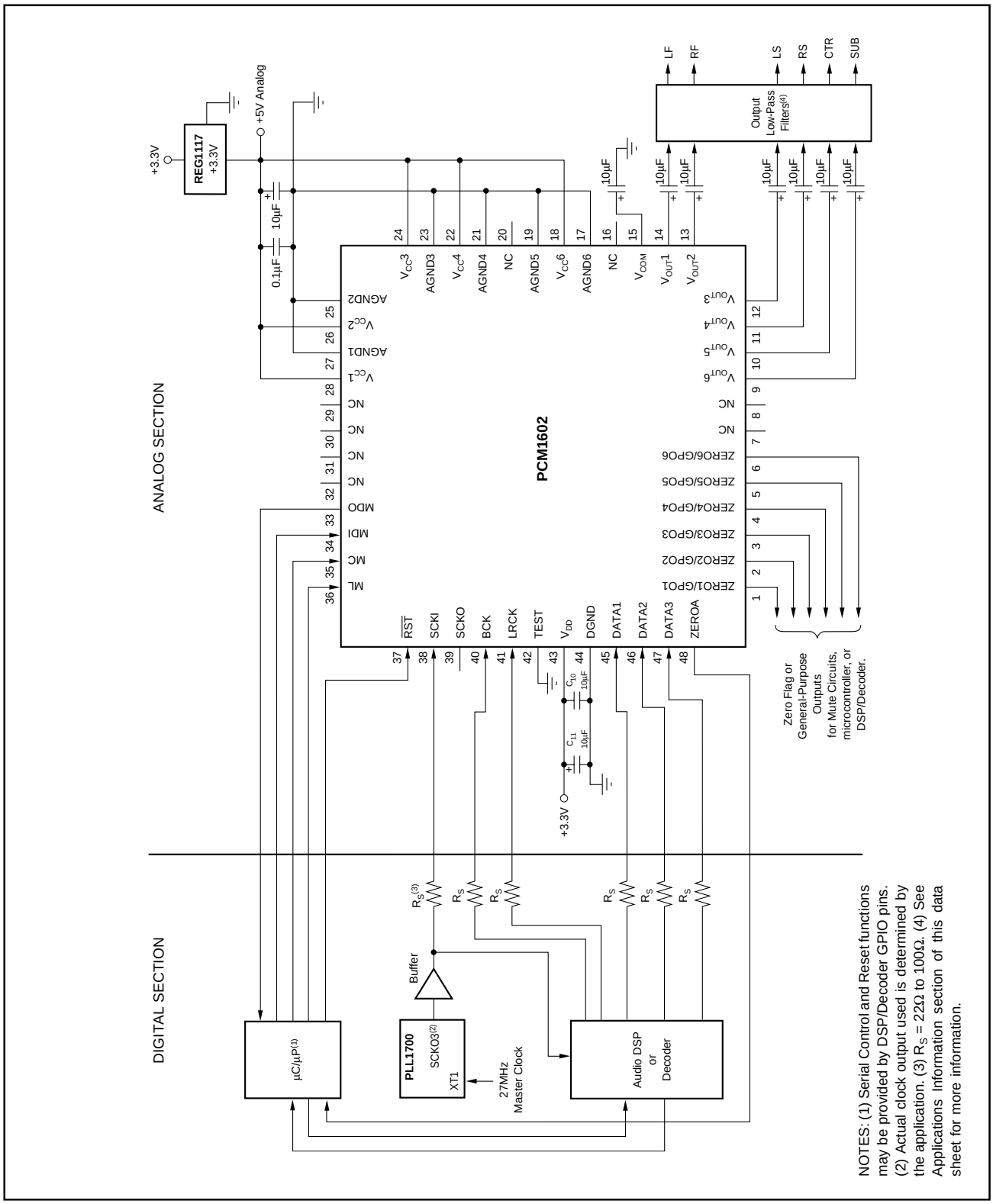


FIGURE 13. Typical Application Diagram.

POWER SUPPLIES AND GROUNDING

The PCM1602 requires a +5V analog supply and a +3.3V digital supply. The +5V supply is used to power the DAC analog and output filter circuitry, while the +3.3V supply is used to power the digital filter and serial interface circuitry. For best performance, the +3.3V supply should be derived from the +5V supply using a linear regulator (see Figure 13).

Two capacitors are required for supply bypassing (see Figure 12). These capacitors should be located as close as possible to the PCM1602 package. The 10µF capacitors should be tantalum or aluminum electrolytic, while the 0.1µF capacitors are ceramic (X7R type is recommended for surface-mount applications).

DAC OUTPUT FILTER CIRCUITS

Delta-sigma DACs utilize noise-shaping techniques to improve in-band Signal-to-Noise Ratio (SNR) performance at the expense of generating increased out-of-band noise above the Nyquist Frequency, or $f_S/2$. The out-of-band noise must be low-pass filtered in order to provide the optimal converter performance. This is accomplished by a combination of on-chip and external low-pass filtering.

Figures 14 and 15 show the recommended external low-pass active filter circuits for dual- and single-supply applications. These circuits are second-order Butterworth filters using the Multiple FeedBack (MFB) circuit arrangement, that reduces sensitivity to passive component variations over frequency and temperature. For more information regarding MFB active filter design, please refer to the Texas Instruments Applications Bulletin AB-034, available from our web site (www.ti.com), or your local Texas Instruments sales office.

Since the overall system performance is defined by the quality of the DACs and their associated analog output circuitry, high-quality audio op amps are recommended for the active filters. The OPA2134 and OPA2353 dual op amps from Texas Instruments are shown in Figures 14 and 15, and are recommended for use with the PCM1602.

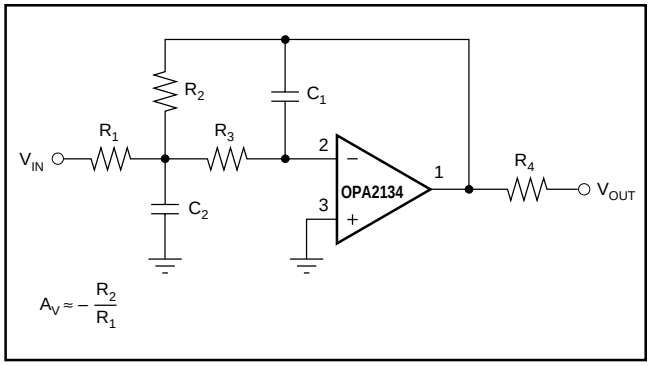


FIGURE 14. Dual Supply Filter Circuit.

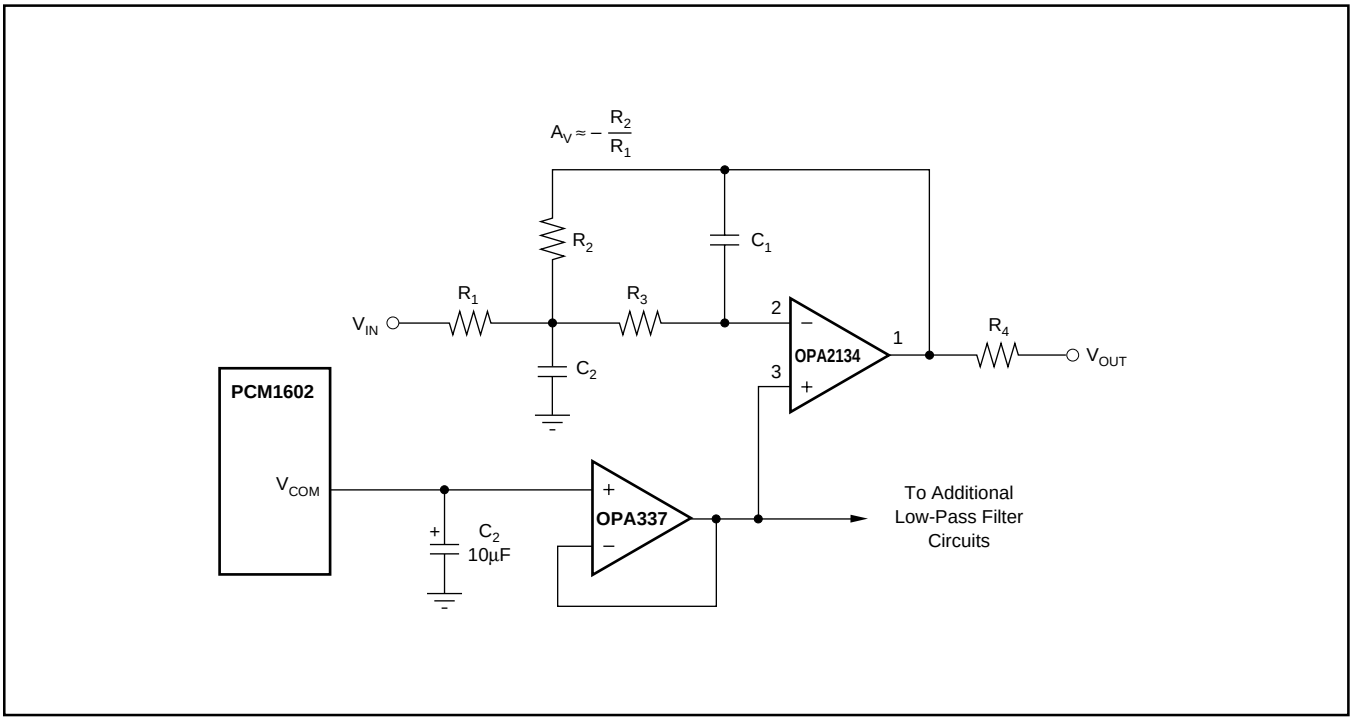


FIGURE 15. Single-Supply Filter Circuit.

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1602 is shown in Figure 16. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1602 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the DACs. In cases where a common +5V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital +5V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 17 shows the recommended approach for single-supply applications.

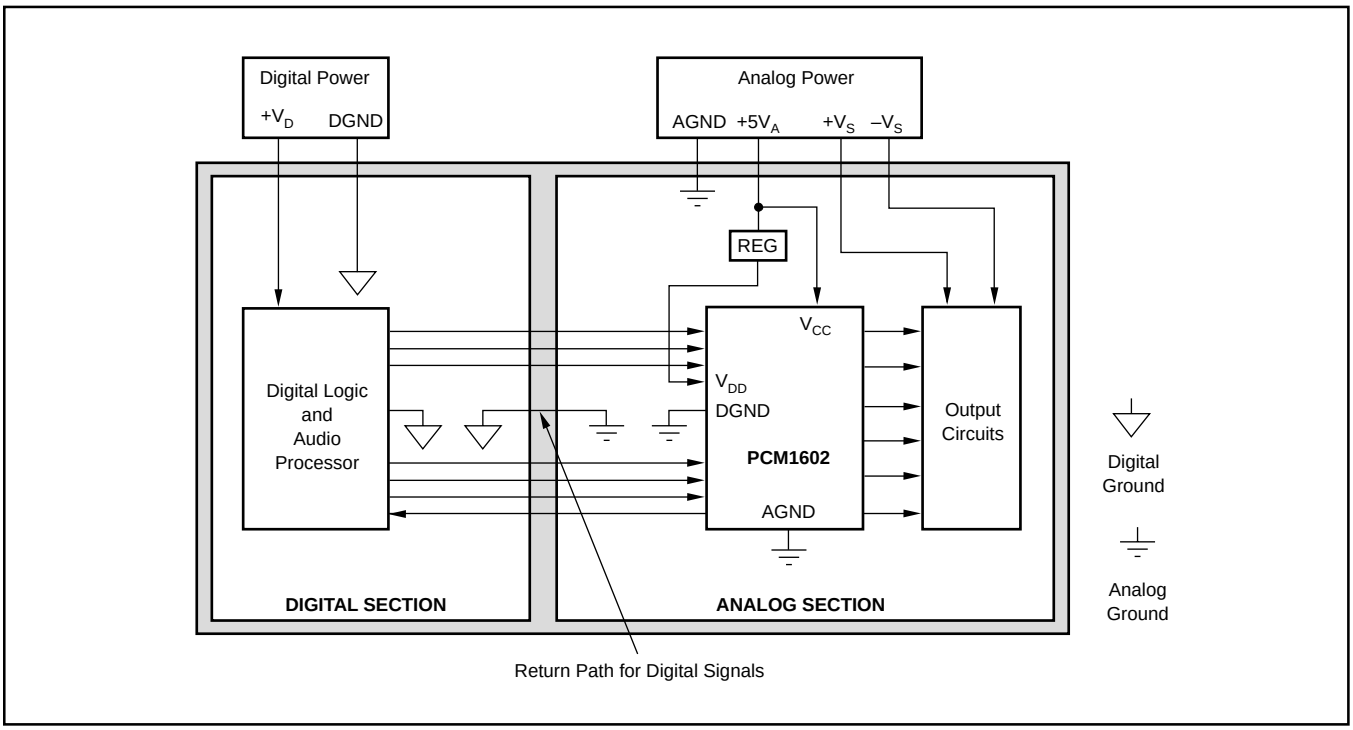


FIGURE 16. Recommended PCB Layout.

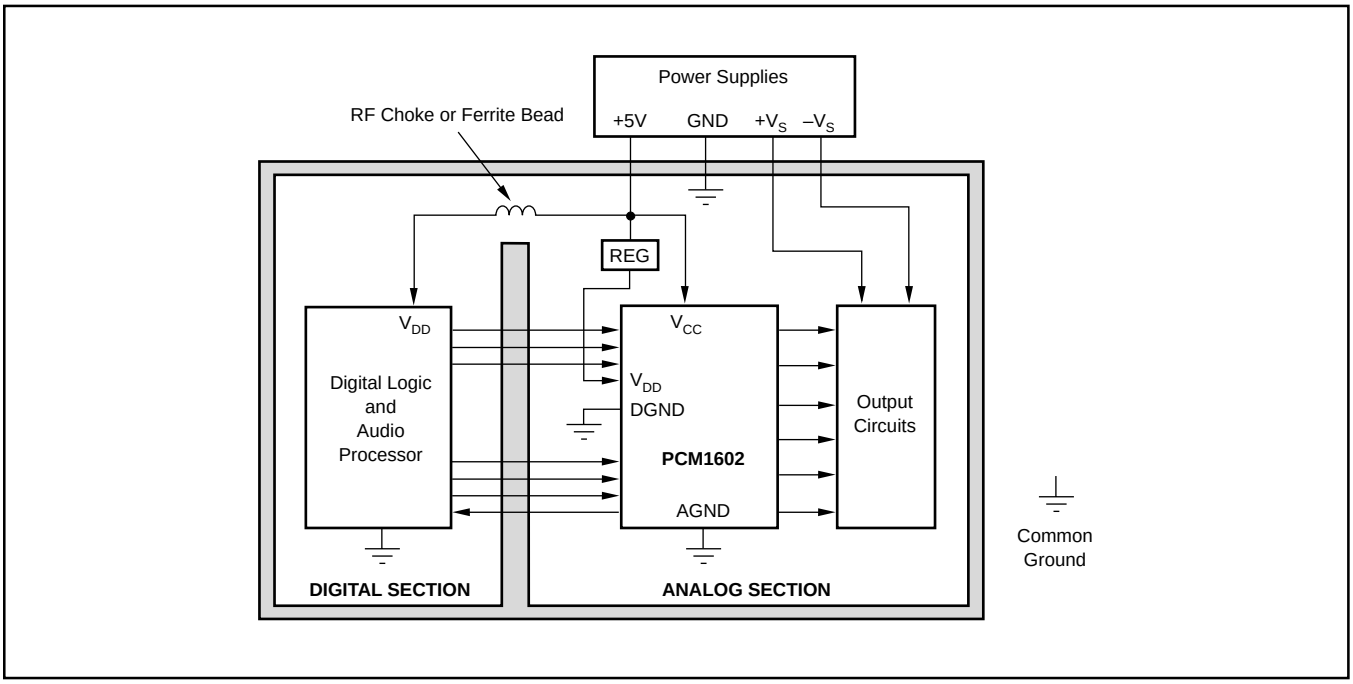


FIGURE 17. Single-Supply PCB Layout.

THEORY OF OPERATION

The DAC section of the PCM1602 is based on a multi-bit delta-sigma architecture. This architecture utilizes a fourth-order noise shaper and an 8-level amplitude quantizer, followed by an analog low-pass filter. A block diagram of the delta-sigma modulator is shown in Figure 19. This architecture has the advantage of stability and improved jitter tolerance, when compared to traditional 1-bit (2-level) delta-sigma designs.

The combined oversampling rate of the digital interpolation filter and the delta-sigma modulator is 32, 64, or $128f_S$. The total oversampling rate is determined by the desired sampling frequency. If $f_S \leq 96kHz$, then the OVER bit in Register 12 may be set to an oversampling rate of 64 or $128f_S$. If $f_S > 96kHz$, then the OVER bit may be used to set the oversampling rate to 32 or $64f_S$. Figure 20 shows the out-of-band quantization noise plots for both the 64x and 128x oversampling scenarios. Notice that the 128x oversampling plot shows significantly improved out-of-band noise performance, allowing for a simplified low-pass filter to be used at the output of the DAC.

Figure 18 illustrates the simulated jitter sensitivity of the PCM1602. To achieve best performance, the system clock jitter should be less than 300 picoseconds. This is easily achieved using a quality clock generation IC, like the PLL1700 from Texas Instruments.

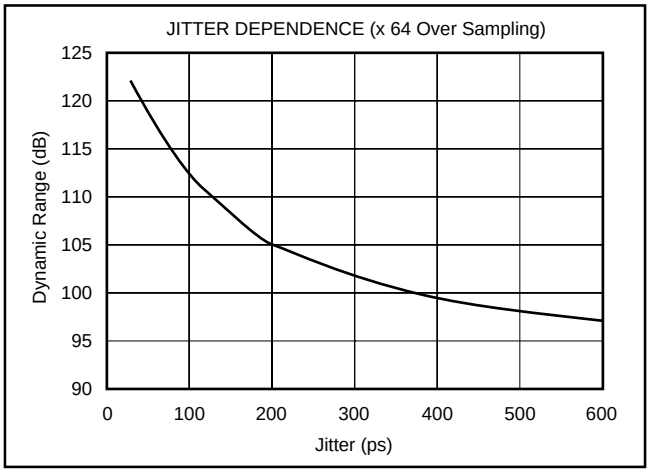


FIGURE 18. Jitter Sensitivity.

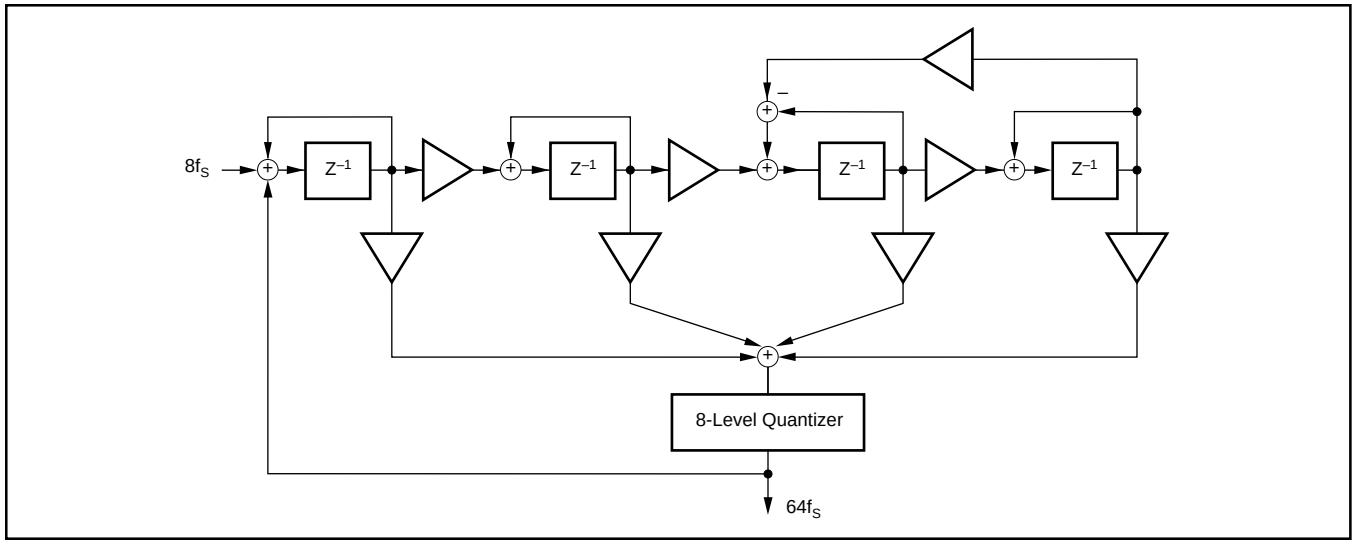


FIGURE 19. Eight-Level Delta-Sigma Modulator.

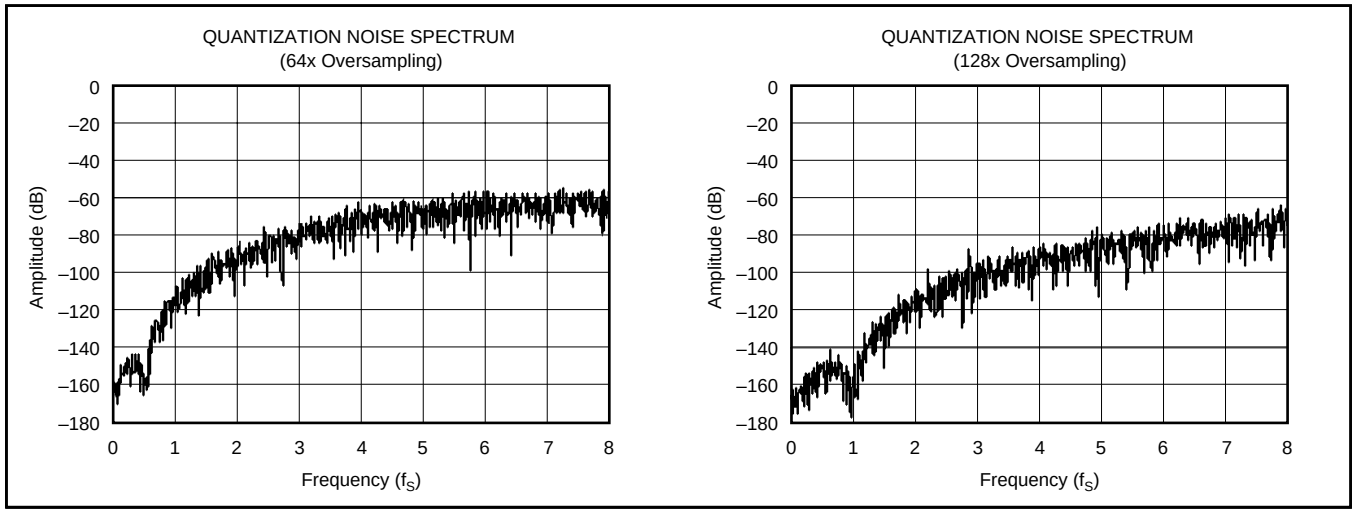


FIGURE 20. Quantization Noise Spectrum.

KEY PERFORMANCE PARAMETERS AND MEASUREMENT

This section provides information on how to measure key dynamic performance parameters for the PCM1602. In all cases, an Audio Precision System Two Cascade or equivalent audio measurement system is utilized to perform the testing.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion + Noise (THD+N) is a significant figure of merit for audio DACs, since it takes into account both harmonic distortion and all noise sources within a specified measurement bandwidth. The true rms value of the distortion and noise is referred to as THD+N. The test setup for THD+N measurements is shown in Figure 21.

For the PCM1602 DACs, THD+N is measured with a full-scale, 1kHz digital sine wave as the test stimulus at the input of the DAC. The digital generator is set to a 24-bit audio word length and a sampling frequency of 44.1kHz, or 96kHz. The digital generator output is taken from the unbalanced S/PDIF connector of the measurement system. The S/PDIF data is transmitted via coaxial cable to the digital audio receiver on the DEM-DAI1602 demo board. The receiver is then configured to output 24-bit data in either I^2S or left-justified data format. The DAC audio interface format is programmed to match the receiver output format. The analog output is then taken from the DAC post filter and connected to the analog analyzer input of the measurement system. The analog input is band-limited, using filters resident in the analyzer. The resulting THD+N is measured by the analyzer and displayed by the measurement system.

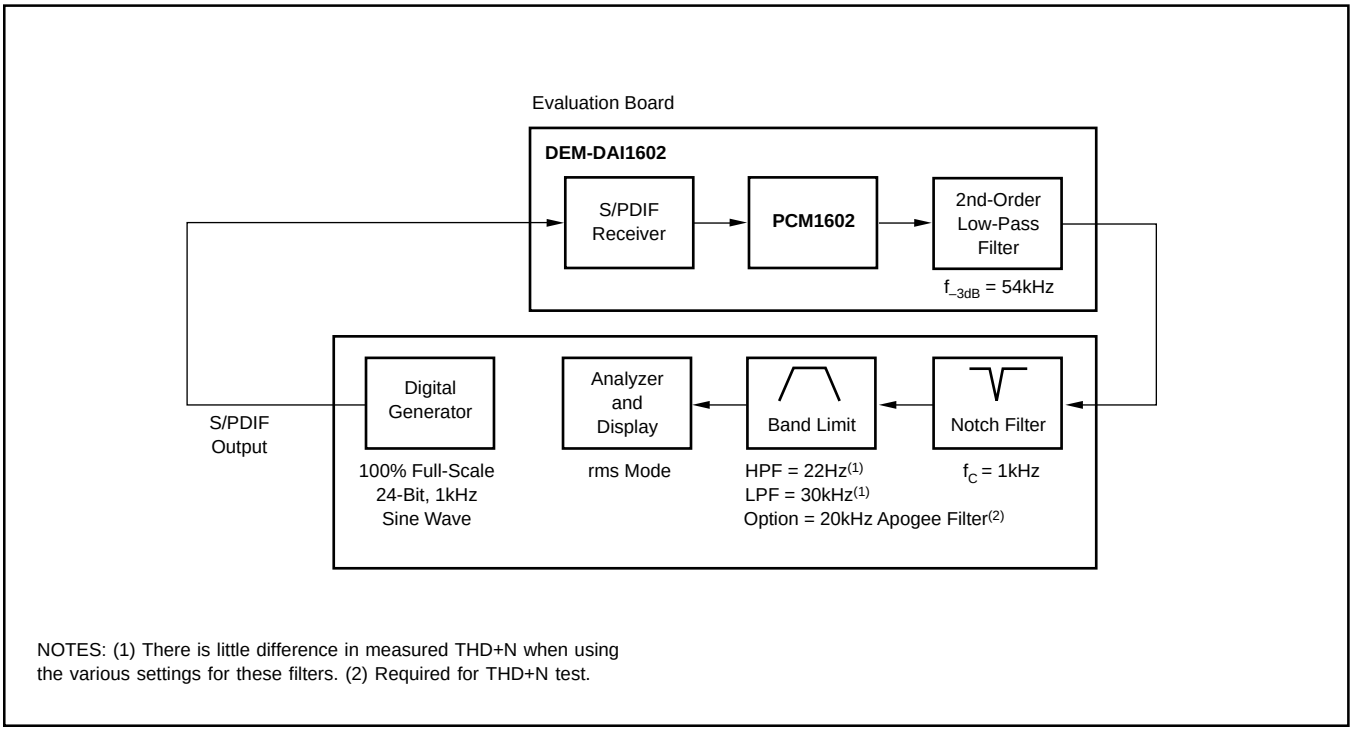


FIGURE 21. Test Setup for THD+N Measurements.

DYNAMIC RANGE

Dynamic range is specified as A-Weighted, THD+N measured with a –60dBFS, 1kHz digital sine wave stimulus at the input of the DAC. This measurement is designed to give a good indication of how the DAC will perform, given a low-level input signal.

The measurement setup for the dynamic range measurement is shown in Figure 22, and is similar to the THD+N test setup discussed previously. The differences include the band-limit filter selection, the additional A-Weighting filter, and the –60dBFS input level.

IDLE CHANNEL SIGNAL-TO-NOISE RATIO

The SNR test provides a measure of the noise of the DAC. The input to the DAC is in all "0"s data, and the DAC's Infinite Zero Detect Mute function must be disabled (default condition at power-up for the PCM1602). This ensures that the delta-sigma modulator output is connected to the output amplifier circuit so that idle tones (if present) may be observed at the output. The dither function of the digital signal generator must also be disabled to ensure an all "0"s data stream at the input of the DAC.

The measurement setup for SNR is identical to that used for dynamic range, with the exception of the input signal level. (see the notes provided in Figure 22.)

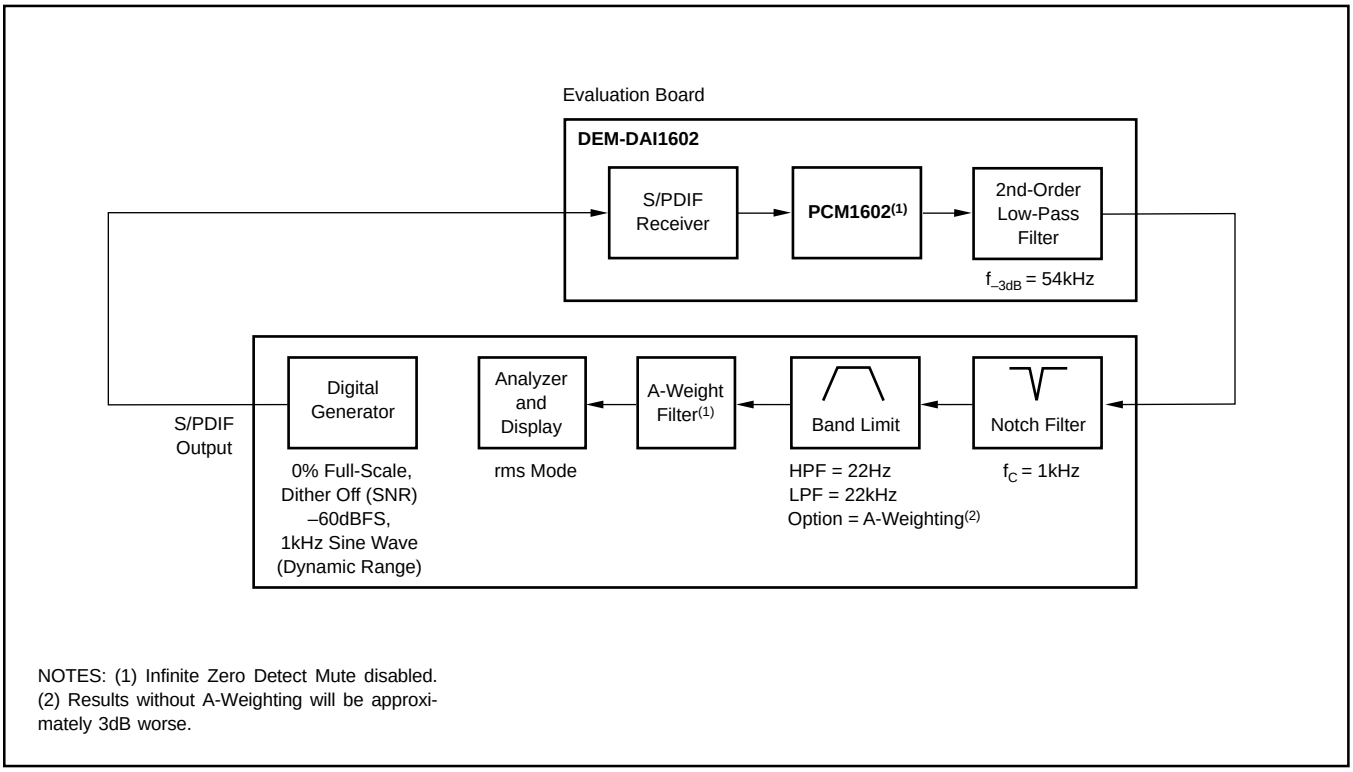


FIGURE 22. Test Set-Up for Dynamic Range and SNR Meeasurements.

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
PCM1602KY	ACTIVE	LQFP	PT	48	250
PCM1602KY/2K	ACTIVE	LQFP	PT	48	2000
PCM1602Y	ACTIVE	LQFP	PT	48	250
PCM1602Y/2K	ACTIVE	LQFP	PT	48	2000

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265