SLES042A − JUNE 2002 − REVISED JUNE 2004

STEREO AUDIO CODEC WITH USB INTERFACE, SINGLE-ENDED ANALOG INPUT/OUTPUT AND S/PDIF

FEATURES

- **PCM2904: Without S/PDIF**
- **PCM2906: With S/PDIF**
- **On-Chip USB Interface:**
  - **With Full-Speed Transceivers**
  - **Fully Compliant With USB 1.1 Specification**
  - **Certified by USB-IF**
  - **Partially Programmable Descriptors(1)**
  - **USB Adaptive Mode for Playback**
  - **USB Asynchronous Mode for Record**
  - **Bus Powered**
- **16-Bit Delta-Sigma ADC and DAC**
- **Sampling Rate:**
  - **DAC: 32, 44.1, 48 kHz**
  - **ADC: 8, 11.025, 16, 22.05, 32, 44.1, 48 kHz**
- **On-Chip Clock Generator With Single 12-MHz Clock Source**
- **Single Power Supply: 5 V Typical (V_{BUS})**
- **Stereo ADC:**
  - **Analog Performance at V_{BUS} = 5 V**
    - **THD+N = 0.01%**
    - **SNR = 89 dB**
    - **Dynamic Range = 89 dB**
  - **Decimation Digital Filter**
    - **Pass-Band Ripple = ±0.05 dB**
    - **Stop-Band Attenuation = –65 dB**
  - **Single-Ended Voltage Input**
  - **Antialiasing Filter Included**
  - **Digital LCF Included**
- **Stereo DAC:**
  - **Analog Performance at V_{BUS} = 5 V**
    - **THD+N = 0.005%**
    - **SNR = 96 dB**
    - **Dynamic Range = 93 dB**
  - **Oversampling Digital Filter**
    - **Pass-Band Ripple = ±0.1 dB**
    - **Stop-Band Attenuation = –43 dB**
  - **Single-Ended Voltage Output**
  - **Analog LPF Included**
- **Multifunctions:**
  - **Human Interface Device (HID) Volume ± Control and Mute Control**
  - **Suspend Flag**
- **Package: 28-Pin SSOP, Lead-Free Product**

APPLICATIONS

- **USB Audio Speaker**
- **USB Headset**
- **USB Monitor**
- **USB Audio Interface Box**

DESCRIPTION

The PCM2904/2906 is Texas Instruments single-chip USB stereo audio codec with USB-compliant full-speed protocol controller and S/PDIF (PCM2906 only). The USB protocol controller works with no software code, but the USB descriptors can be modified in some areas (for example, vendor ID/product ID). The PCM2904/2906 employs SpAct™ architecture, TI's unique system that recovers the audio clock from USB packet data. On-chip analog PLLs with SpAct enable playback and record with low clock jitter and with independent playback and record sampling rates.

(1)The descriptor can be modified by changing a mask.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING ORDERING INFORMATION

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
PCM2904DB	28-lead SSOP	28DB	−25°C to 85°C	PCM2904	PCM2904DB	Rails
					PCM2904DBR	Tape and reel
PCM2906DB	28-lead SSOP	28DB	−25°C to 85°C	PCM2906	PCM2906DB	Rails
					PCM2906DBR	Tape and reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		PCM2904/PCM2906	UNIT
Supply voltage, V_{BUS}		-0.3 to 6.5	V
Ground voltage differences, AGNDC, AGNDP, AGNDX, DGND, DGNDU		±0.1	V
Digital input voltage	SEL0, SEL1, TEST0 (DIN)(2)	−0.3 to 6.5	V
	D+, D–, HID0, HID1, HID2, XTI, XTO, TEST1 (DOUT)(2), $\overline{SSPND}$	−0.3 to (V_{DDI} + 0.3) < 4	
Analog input voltage	$V_{IN}L$, $V_{IN}R$, V_{COM}, $V_{OUT}R$, $V_{OUT}L$	−0.3 to V_{CCCI}+ 0.3) < 4	V
	V_{CCCI}, V_{CCP1I}, V_{CCP2I}, V_{CCXI}, V_{DDI}	−0.3 to 4	
Input current (any pins except supplies)		±10	mA
Ambient temperature under bias		−40 to 125	°C
Storage temperature, T_{stg}		−55 to 150	°C
Junction temperature T_J		150	°C
Lead temperature (soldering)		260	°C, 5 s
Package temperature (IR reflow, peak)		250	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) ( ): PCM2906

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, V_{BUS}, = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM2904DB, PCM2906DB			UNIT
			MIN	TYP	MAX	
Digital Input/Output						
	Host interface	Apply USB Revision 1.1, full speed				
	Audio data format	USB isochronous data format				
Input Logic						
V_{IH}(1)	Input logic level		2		3.3	Vdc
V_{IL}(1)					0.8	
V_{IH}(2) (3)			2.52		3.3	
V_{IL}(2) (3)					0.9	
V_{IH}(4)			2		5.25	
V_{IL}(4)					0.8	
V_{IH}(5)			2.52		5.25	
V_{IL}(5)					0.9	
I_{IH}(1)(2)(4)	Input logic current	V_{IN} = 3.3 V			±10	μA
I_{IL}(1)(2)(4)		V_{IN} = 0 V			±10	
I_{IH}(3)		V_{IN} = 3.3 V		50	80	
I_{IL}(3)		V_{IN} = 0 V			±10	
I_{IH}(5)		V_{IN} = 3.3 V		65	100	
I_{IL}(5)		V_{IN} = 0 V			±10	
Output Logic						
V_{OH}(1)	Output logic level		2.8			Vdc
V_{OL}(1)					0.3	
V_{OH}(6)		I_{OH} = –4 mA	2.8			
V_{OL}(6)		I_{OL} = 4 mA			0.5	
V_{OH}(7)		I_{OH} = −2 mA	2.8			
V_{OL}(7)		I_{OL} = 2 mA			0.5	
Clock Frequency						
	Input clock frequency, XTI		11.994	12.000	12.006	MHz
ADC Characteristics						
	Resolution			8, 16		bits
	Audio data channel			1, 2		channel
Clock Frequency						
f_S	Sampling frequency		8, 11.025, 16, 22.05, 32, 44.1, 48			kHz
DC Accuracy						
	Gain mismatch, channel-to-channel			±1	±5	% of FSR
	Gain error			±2	±10	% of FSR
	Bipolar zero error			±0		% of FSR

(1) Pins 1, 2: D+, D–
(2) Pin 21: XTI
(3) Pins 5, 6, 7: HID0, HID1, HID2
(4) Pins 8, 9: SEL0, SEL1
(5) Pin 24: DIN
(6) Pin 25: DOUT
(7) Pin 28: $\overline{\text{SSPND}}$

ELECTRICAL CHARACTERISTICS(continued)

all specifications at T_A = 25°C, V_{BUS}, = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM2904DB, PCM2906DB			UNIT
			MIN	TYP	MAX	
Dynamic Performance(1)						
THD+N	Total harmonic distortion plus noise	V_{IN} = –0.5 dB(2), V_{CCCI} = 3.67 V		0.01%	0.02%	
		V_{IN} = –0.5 dB(3)		0.1%		
		V_{IN} = –60 dB		5%		
	Dynamic range	A-weighted	81	89		dB
	S/N ratio	A-weighted	81	89		dB
	Channel separation		80	85		dB
Analog Input						
	Input voltage			0.6 V_{CCCI}		Vp−p
	Center voltage			0.5 V_{CCCI}		V
	Input impedance			30		kΩ
	Antialiasing filter frequency response	–3 dB		150		kHz
		f_{IN} = 20 kHz		–0.08		dB
Digital Filter Performance						
	Pass band				0.454 f_S	Hz
	Stop band		0.583 f_S			Hz
	Pass-band ripple				±0.05	dB
	Stop-band attenuation		–65			dB
t_d	Delay time			17.4/f_S		s
	LCF frequency response	–3 dB		0.078 f_S		MHz
DAC Characteristics						
	Resolution			8, 16		bits
	Audio data channel			1, 2		channel
Clock Frequency						
f_S	Sampling frequency			32, 44.1, 48		kHz
DC Accuracy						
	Gain mismatch, channel-to-channel			±1	±5	% of FSR
	Gain error			±2	±10	% of FSR
	Bipolar zero error			±2		% of FSR
Dynamic Performance(4)						
THD+N	Total harmonic distortion plus noise	V_{OUT} = 0 dB		0.005%	0.016%	
		V_{OUT} = –60 dB		3%		
	Dynamic range	EIAJ, A-weighted	87	93		dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted	90	96		dB
	Channel separation		86	92		dB

(1) f_{IN} = 1 kHz, using the System Two™ audio measurement system by Audio Precision™ in RMS mode with 20 kHz LPF, 400 Hz HPF in calculation.
(2) Using external voltage regulator for V_{CCCI} (as shown in Figure 36 and Figure 37, using REG103xA−A)
(3) Using internal voltage regulator for V_{CCCI} (as shown in Figure 38 and Figure 39)
(4) f_{OUT} = 1 kHz, using the System Two audio measurement system by Audio Precision in RMS mode with 20 kHz LPF, 400 Hz HPF.

ELECTRICAL CHARACTERISTICS(continued)

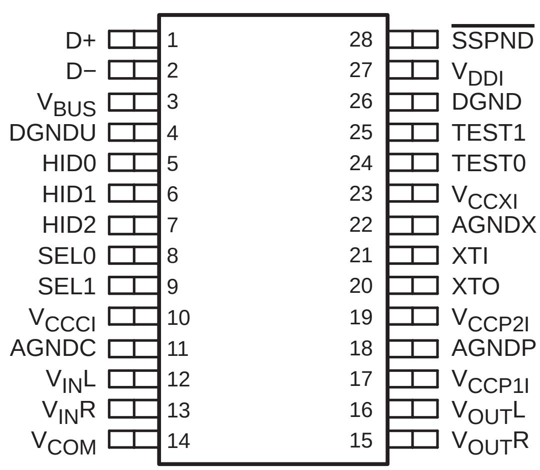
all specifications at T_A = 25°C, V_{BUS}, = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted

PARAMETER		TEST CONDITIONS	PCM2904DB, PCM2906DB			UNIT
			MIN	TYP	MAX	
Analog Output						
V_O	Output voltage			0.6 V_{CCCI}		Vp−p
	Center voltage			0.5 V_{CCCI}		V
	Load impedance	AC coupling	10			kΩ
	LPF frequency response	–3 dB		250		kHz
		f = 20 kHz		–0.03		dB
	Digital filter performance					
	Pass band				0.445 f_S	Hz
	Stop band		0.555 f_S			Hz
	Pass-band ripple				±0.1	dB
	Stop-band attenuation		–43			dB
t_d	Delay time			14.3 f_S		s
Power Supply Requirements						
V_{BUS}	Voltage range		4.35	5	5.25	VDC
	Supply current	ADC, DAC operation		56	67	mA
		Suspend mode (1)		210		μA
P_D	Power dissipation	ADC, DAC operation		280	352	mW
		Suspend mode (1)		1.05		
	Internal power supply voltage(2)		3.25	3.35	3.5	VDC
Temperature Range						
	Operating temperature		−25		85	°C
θ_{JA}	Thermal resistance	28-pin SSOP		100		°C/W

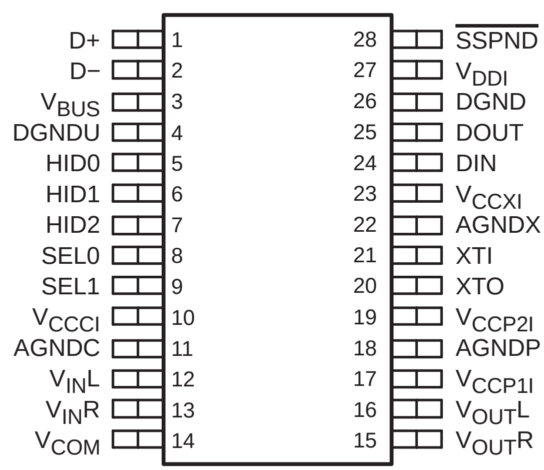
(1) In USB suspend state
(2) Pins 10, 17, 19, 23, 27: V_{CCCI}, V_{CCP1I}, V_{CCP2I}, V_{CCXI}, V_{DDI}

PIN ASSIGNMENTS

PCM2904
(TOP VIEW)



PCM2906
(TOP VIEW)



PCM2904 Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
AGNDC	11	−	Analog ground for codec
AGNDP	18	−	Analog ground for PLL
AGNDX	22	−	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	−	Digital ground
DGNDU	4	−	Digital ground for USB transceiver
HID0	5	I	HID key state input (mute), active high(3)
HID1	6	I	HID key state input (volume up), active high(3)
HID2	7	I	HID key state input (volume down), active high(3)
SEL0	8	I	Must be set to high(5)
SEL1	9	I	Must be set to high(5)
$\overline{SSPND}$	28	O	Suspend flag, active low (Low: suspend, High: operational)
TEST0	24	I	Test pin, must be connected to GND
TEST1	25	O	Test pin, must be left open
V_{BUS}	3	−	Connect to USB power (V_{BUS})
V_{CCCI}	10	−	Internal analog power supply for codec(4)
V_{CCP1I}	17	−	Internal analog power supply for PLL(4)
V_{CCP2I}	19	−	Internal analog power supply for PLL(4)
V_{CCXI}	23	−	Internal analog power supply for oscillator(4)
V_{COM}	14	−	Common for ADC/DAC (V_{CCCI}/2) (4)
V_{DDI}	27	−	Internal digital power supply(4)
$V_{IN}L$	12	I	ADC analog input for L-channel
$V_{IN}R$	13	I	ADC analog input for R-channel
$V_{OUT}L$	16	O	DAC analog output for L-channel
$V_{OUT}R$	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input(2)
XTO	20	O	Crystal oscillator output

(1) LV-TTL level

(2) 3.3-V CMOS-level input

(3) 3.3-V CMOS-level input with internal pulldown. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which have no direct connection with the internal DAC or ADC. See the *Interface #3* and *End-Points* sections.

(4) Connect a decoupling capacitor to GND.

(5) TTL Schmitt trigger, 5-V tolerant

PCM2906 Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTIONS
AGNDC	11	–	Analog ground for codec
AGNDP	18	–	Analog ground for PLL
AGNDX	22	–	Analog ground for oscillator
D–	2	I/O	USB differential input/output minus(1)
D+	1	I/O	USB differential input/output plus(1)
DGND	26	–	Digital ground
DGNDU	4	–	Digital ground for USB transceiver
DIN	24	I	S/PDIF input(5)
DOUT	25	O	S/PDIF output
HID0	5	I	HID key state input (mute), active high(3)
HID1	6	I	HID key state input (volume up), active high(3)
HID2	7	I	HID key state input (volume down), active high(3)
SEL0	8	I	Must be set to high(6)
SEL1	9	I	Must be set to high(6)
$\overline{\text{SSPND}}$	28	O	Suspend flag, active low (Low: suspend, High: operational)
V_{BUS}	3	–	Connected to USB power (V_{BUS})
V_{CCCI}	10	–	Internal analog power supply for codec(4)
V_{CCP1I}	17	–	Internal analog power supply for PLL(4)
V_{CCP2I}	19	–	Internal analog power supply for PLL(4)
V_{CCXI}	23	–	Internal analog power supply for oscillator(4)
V_{COM}	14	–	Common for ADC/DAC (V_{CCCI}/2) (4)
V_{DDI}	27	–	Internal digital power supply(4)
$V_{IN}L$	12	I	ADC analog input for L-channel
$V_{IN}R$	13	I	ADC analog input for R-channel
$V_{OUT}L$	16	O	DAC analog output for L-channel
$V_{OUT}R$	15	O	DAC analog output for R-channel
XTI	21	I	Crystal oscillator input(2)
XTO	20	O	Crystal oscillator output

(1) LV-TTL level

(2) 3.3-V CMOS-level input

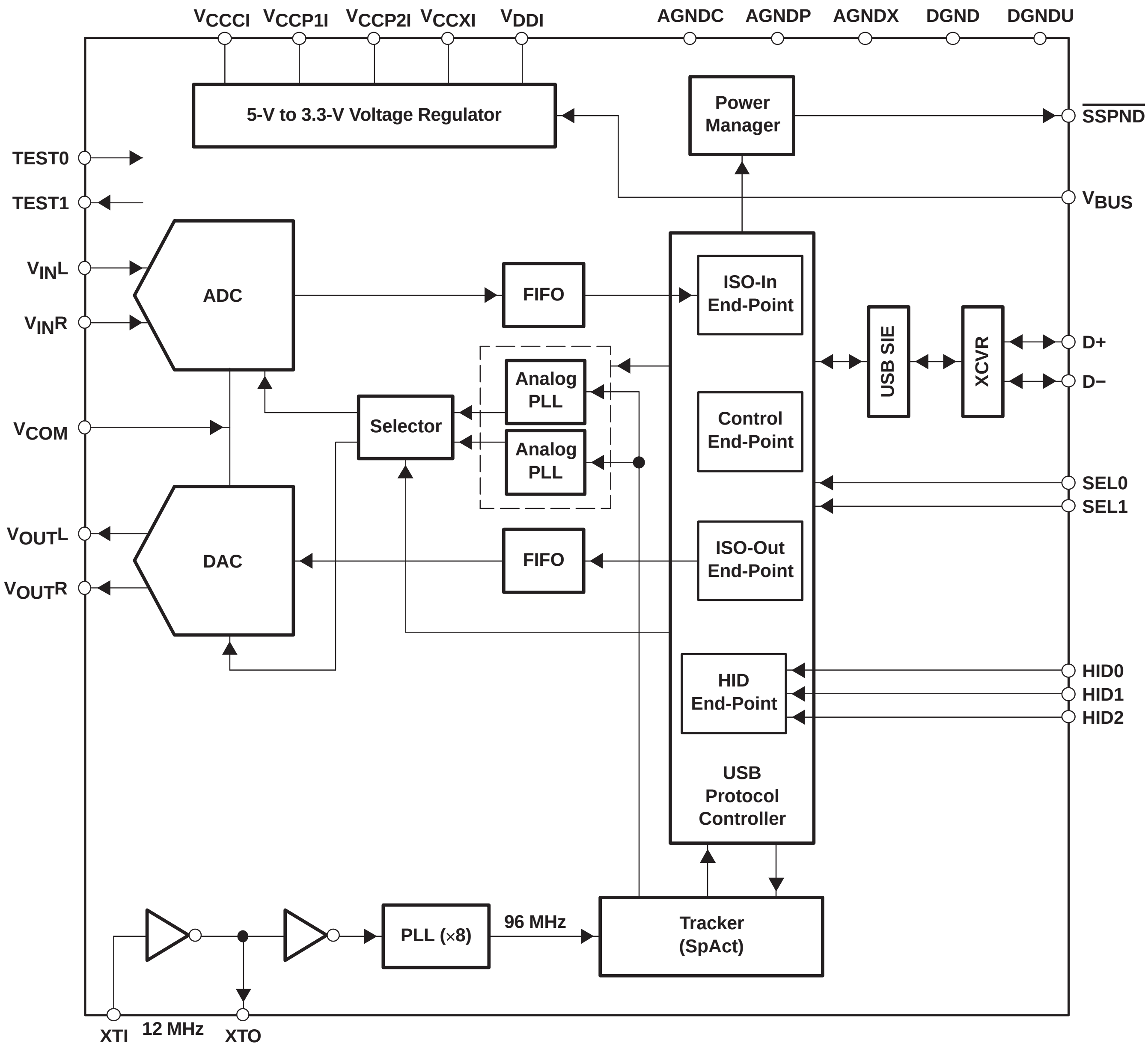
(3) 3.3-V CMOS-level input with internal pulldown. This pin informs the PC of serviceable control signals such as mute, volume up, or volume down, which have no direct connection with the internal DAC or ADC. See the *Interface #3* and *End-Points* sections.

(4) Connect a decoupling capacitor to GND.

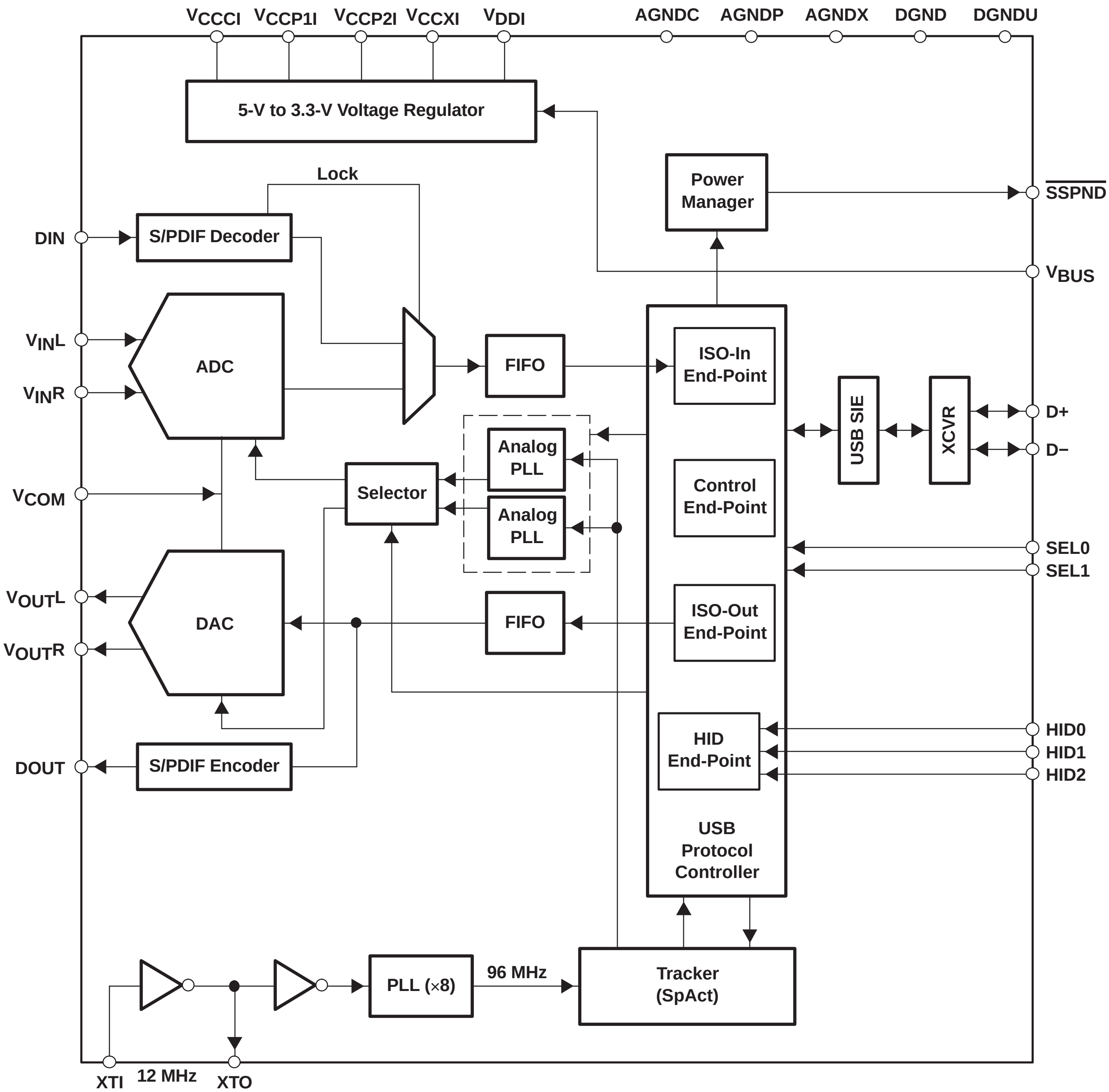
(5) 3.3-V CMOS level input with internal pulldown, 5 V tolerant

(6) TTL Schmitt trigger, 5-V tolerant

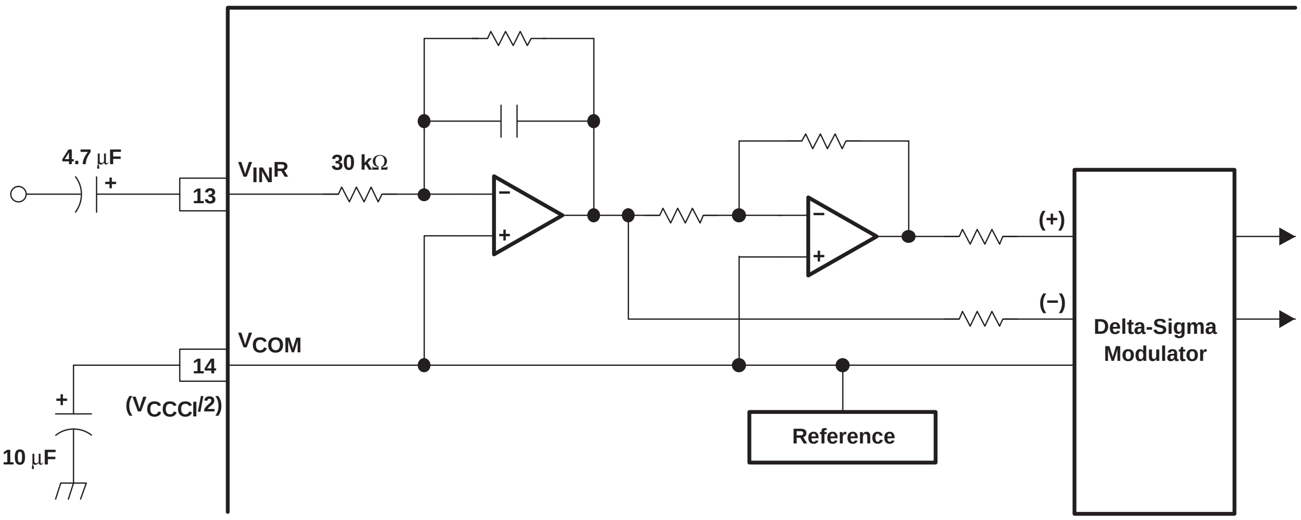
PCM2904 FUNCTIONAL BLOCK DIAGRAM



PCM2906 FUNCTIONAL BLOCK DIAGRAM



BLOCK DIAGRAM OF ANALOG FRONT-END (RIGHT CHANNEL)



TYPICAL CHARACTERISTICS

ADC

TOTAL HARMONIC DISTORTION + NOISE
vs
FREE-AIR TEMPERATURE

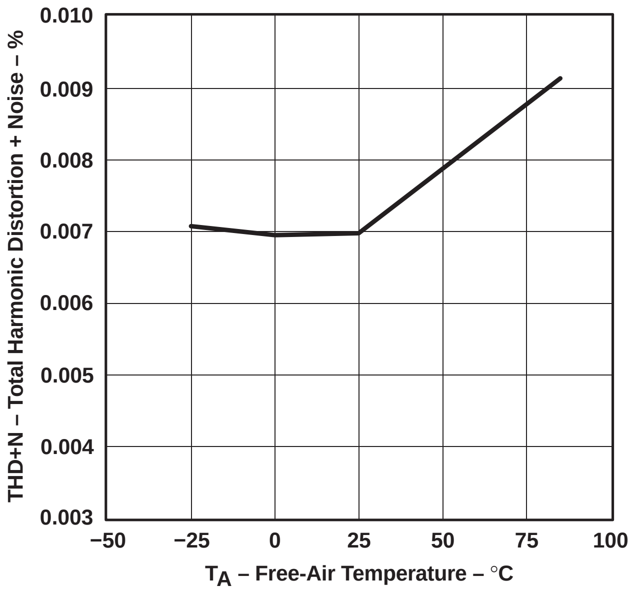


Figure 1. THD + N at –0.5 dB vs Temperature

DYNAMIC RANGE and SNR
vs
FREE-AIR TEMPERATURE

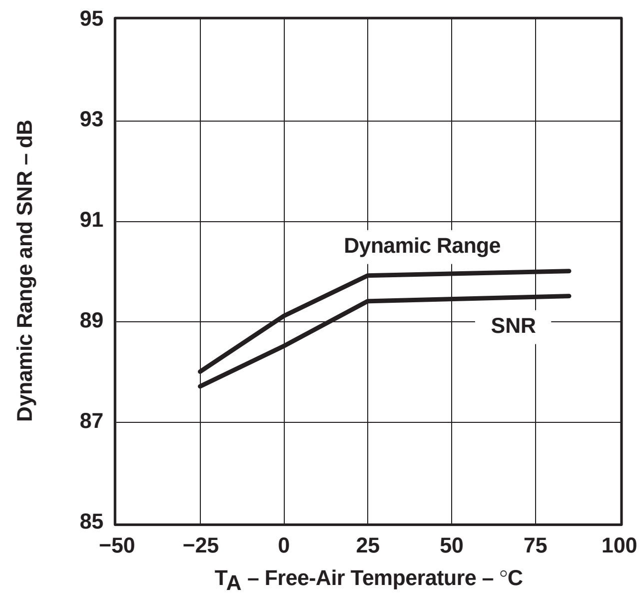


Figure 2

TOTAL HARMONIC DISTORTION + NOISE
vs
SUPPLY VOLTAGE

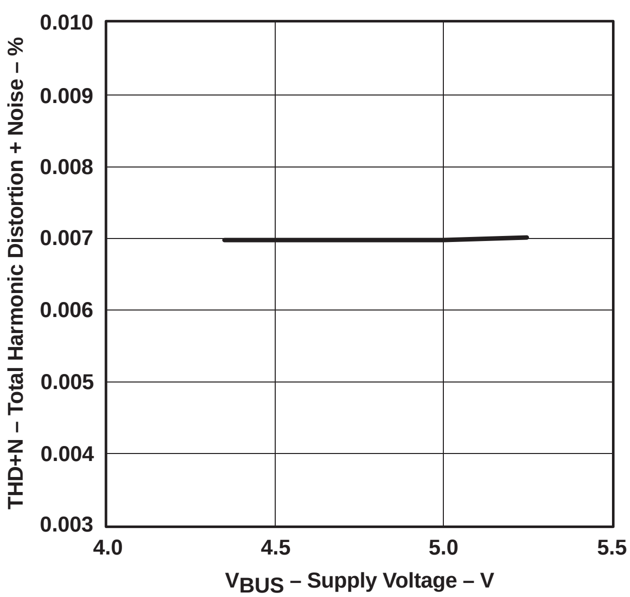


Figure 3. THD + N at –0.5 dB vs Supply Voltage

DYNAMIC RANGE and SNR
vs
SUPPLY VOLTAGE

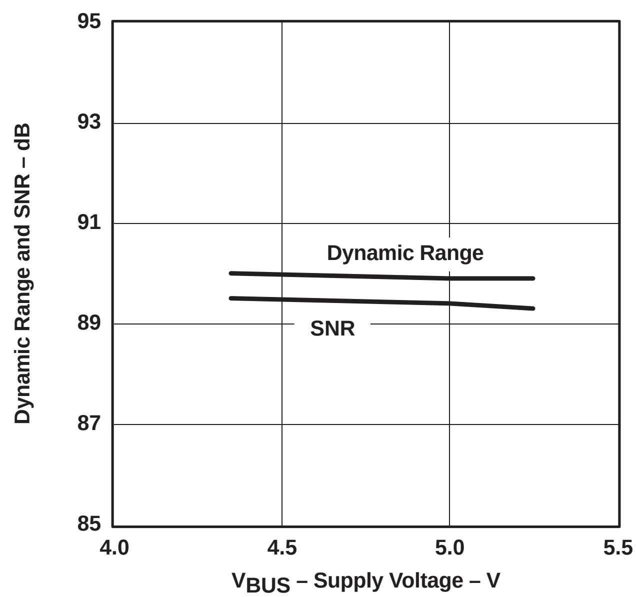


Figure 4

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, using REG103xA−A, unless otherwise noted.

ADC

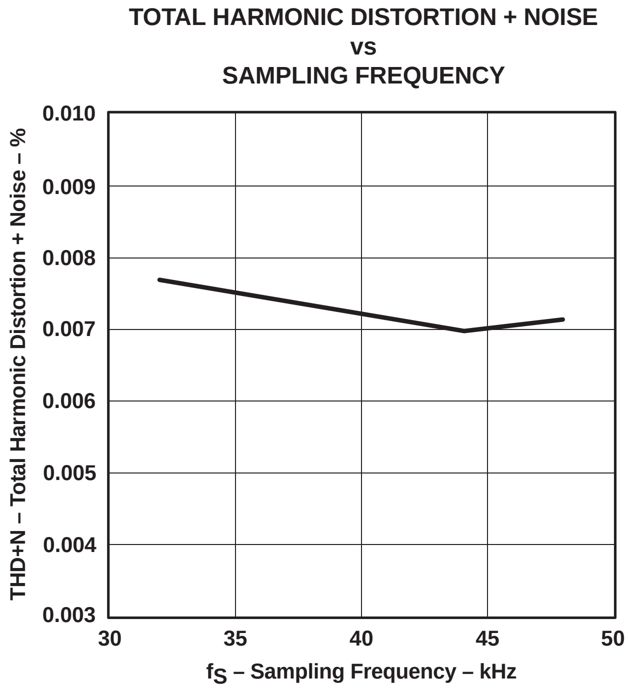


Figure 5. THD + N at –0.5 dB vs Sampling Frequency

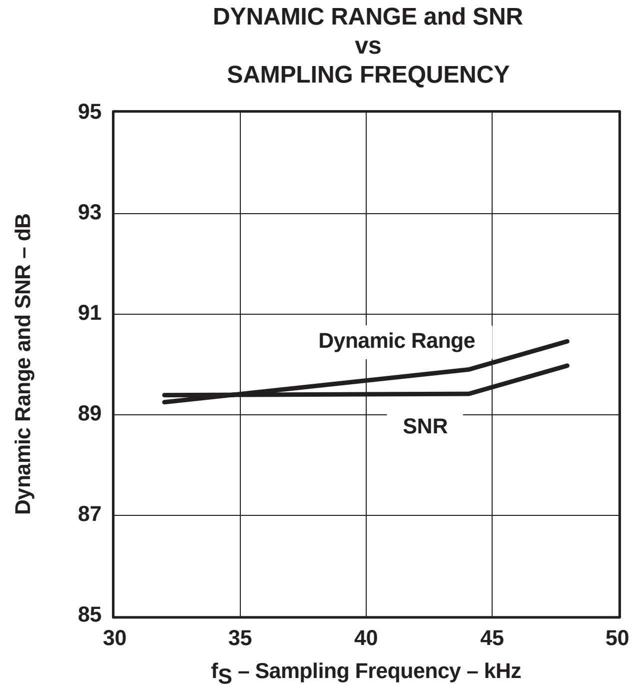


Figure 6

DAC

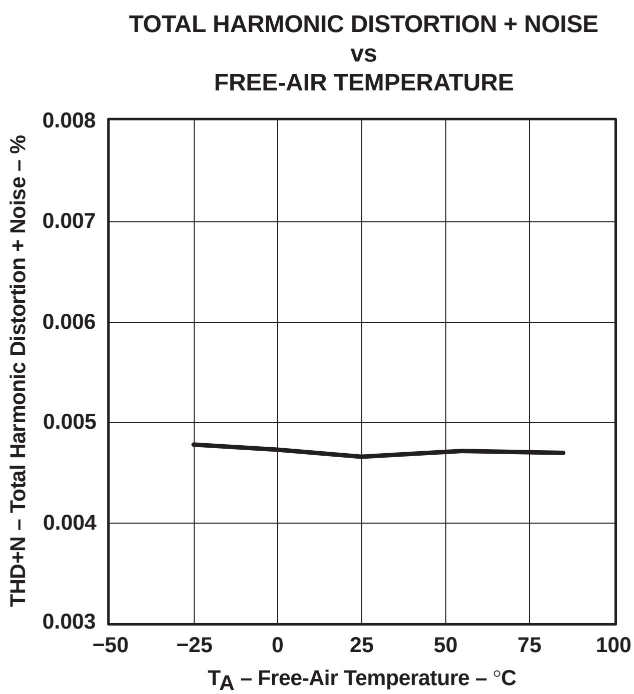


Figure 7. THD + N at 0 dB vs Temperature

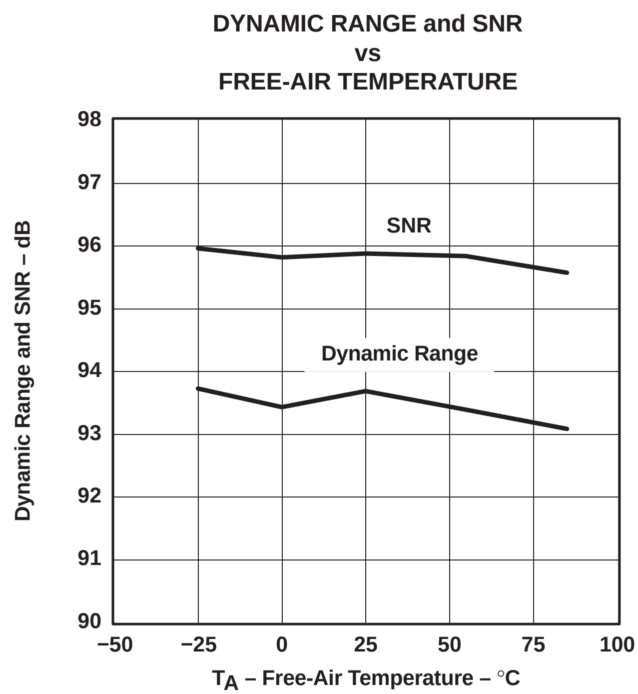


Figure 8

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, using REG103xA-A, unless otherwise noted.

DAC

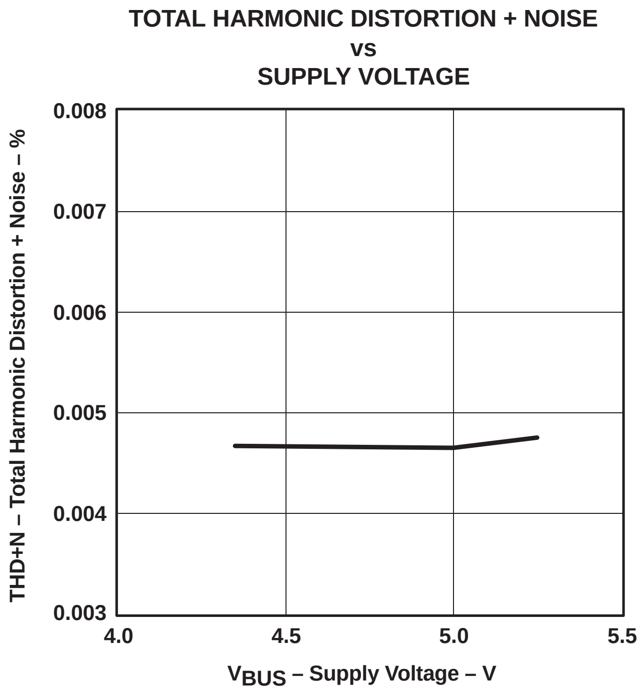


Figure 9. THD + N at 0 dB vs Supply Voltage

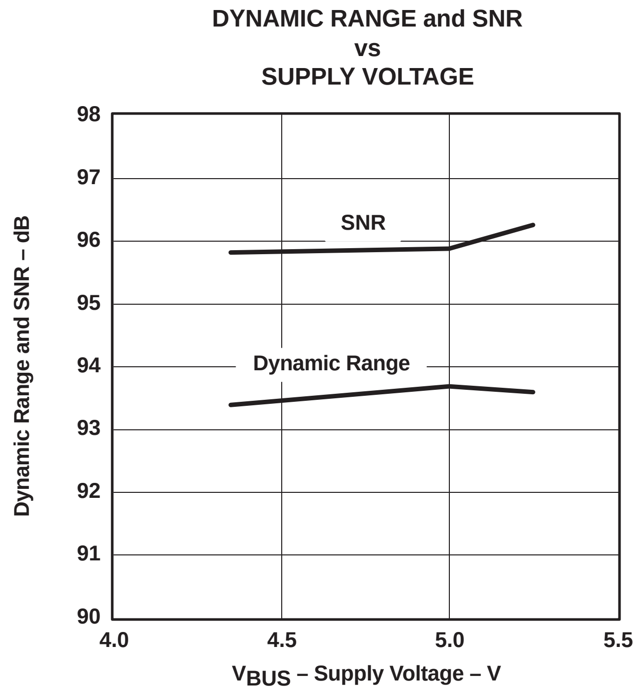


Figure 10

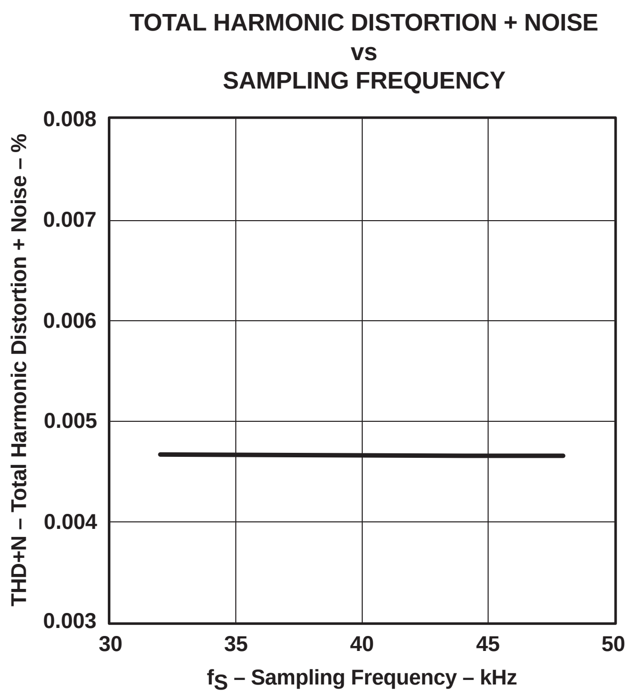


Figure 11. THD + N at 0 dB vs Sampling Frequency

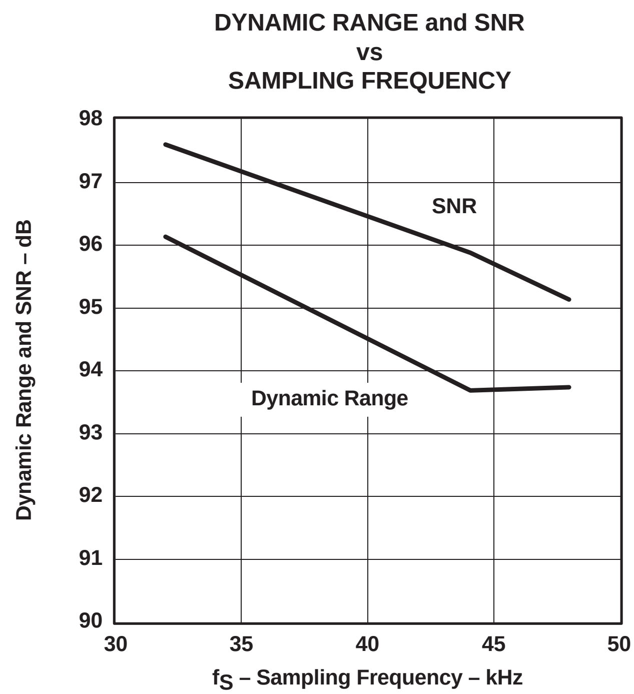


Figure 12

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, using REG103xA-A, unless otherwise noted.

SUPPLY CURRENT

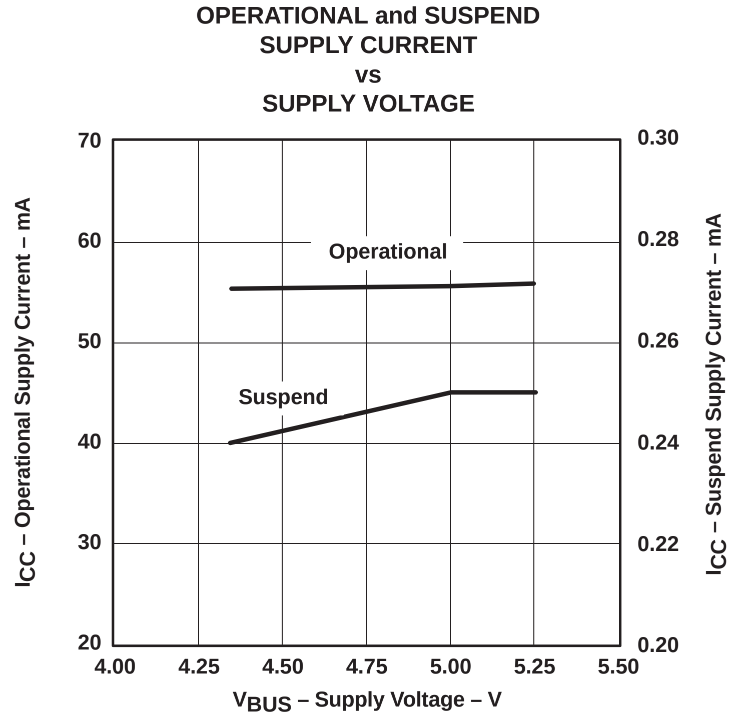


Figure 13

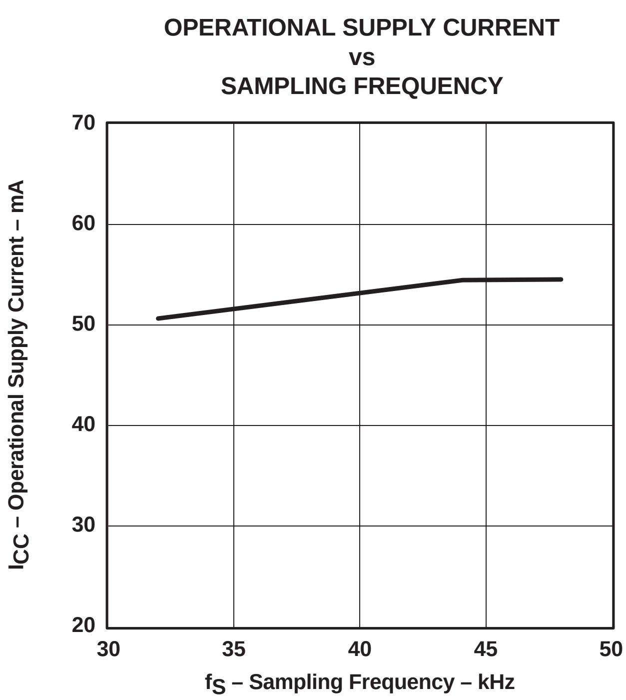


Figure 14. Supply Current vs Sampling Frequency, ADC and DAC at Same f_S

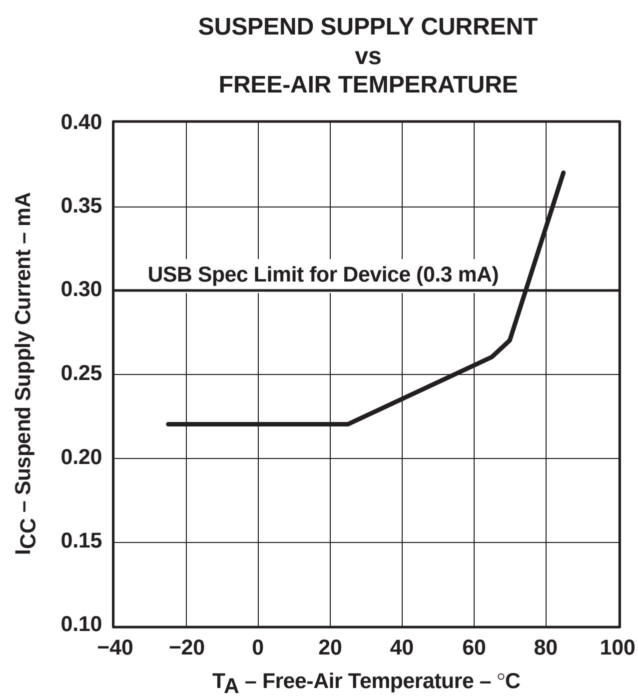


Figure 15. Supply Current vs Temperature in Suspend Mode

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, using REG103xA-A, unless otherwise noted.

ADC DIGITAL DECIMATION FILTER FREQUENCY RESPONSE

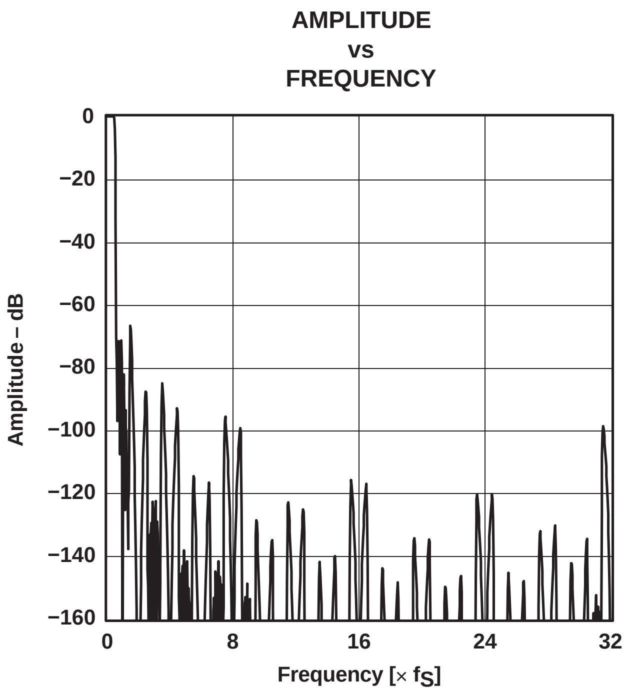


Figure 16. Overall Characteristic

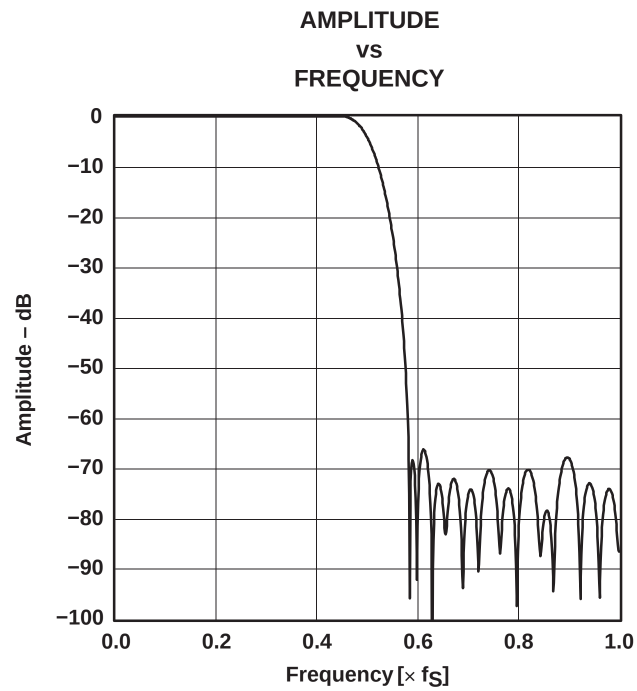


Figure 17. Stop-Band Attenuation

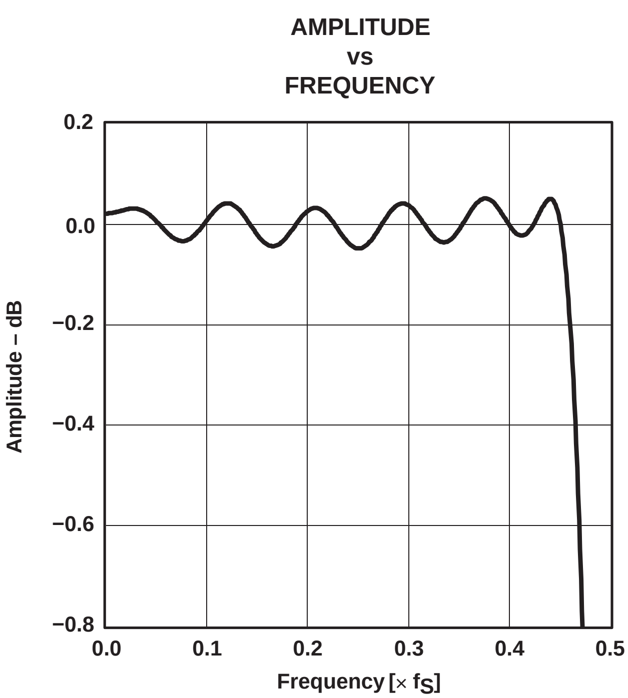


Figure 18. Pass-Band Ripple

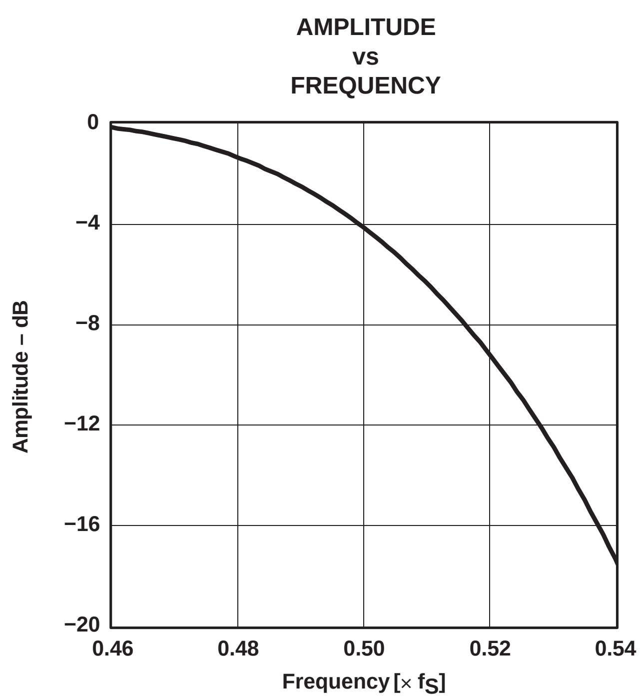


Figure 19. Transition-Band Response

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

ADC DIGITAL HIGH-PASS FILTER FREQUENCY RESPONSE

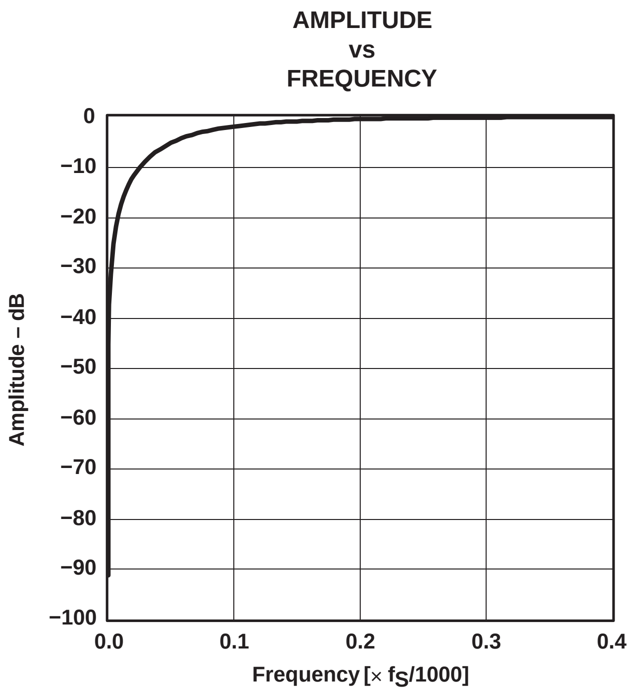


Figure 20. Stop-Band Characteristic

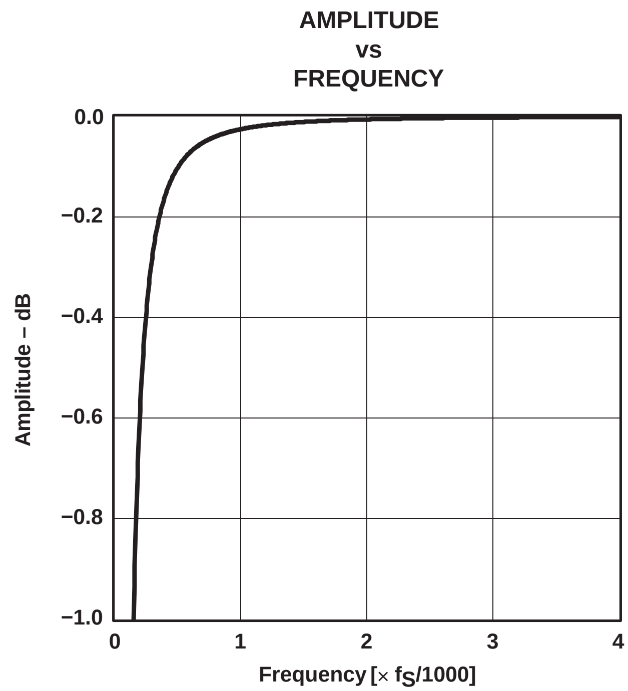


Figure 21. Pass-Band Characteristic

ADC ANALOG ANTIALIASING FILTER FREQUENCY RESPONSE

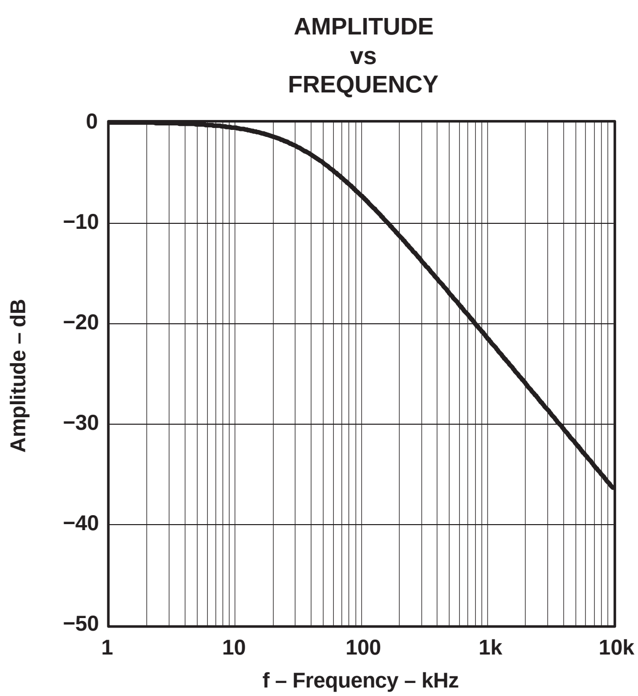


Figure 22. Stop-Band Characteristic

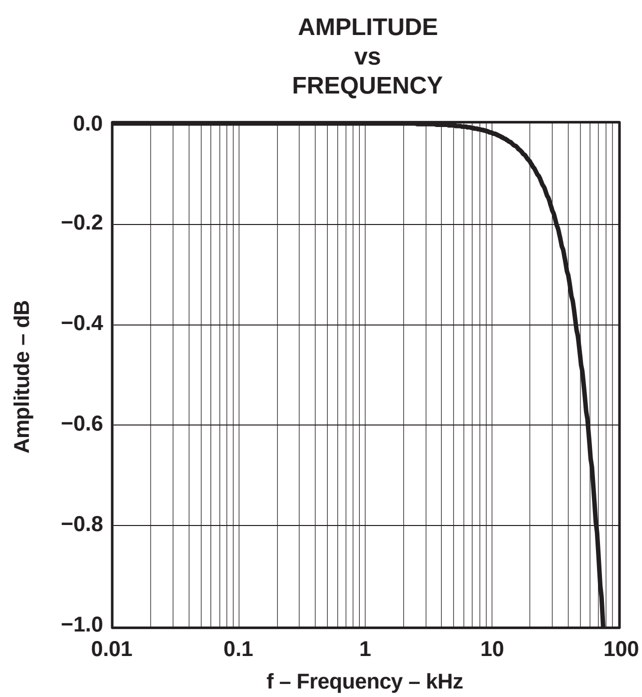


Figure 23. Pass-Band Characteristic

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

DAC DIGITAL INTERPOLATION AND DE-EMPHASIS FILTER FREQUENCY RESPONSE

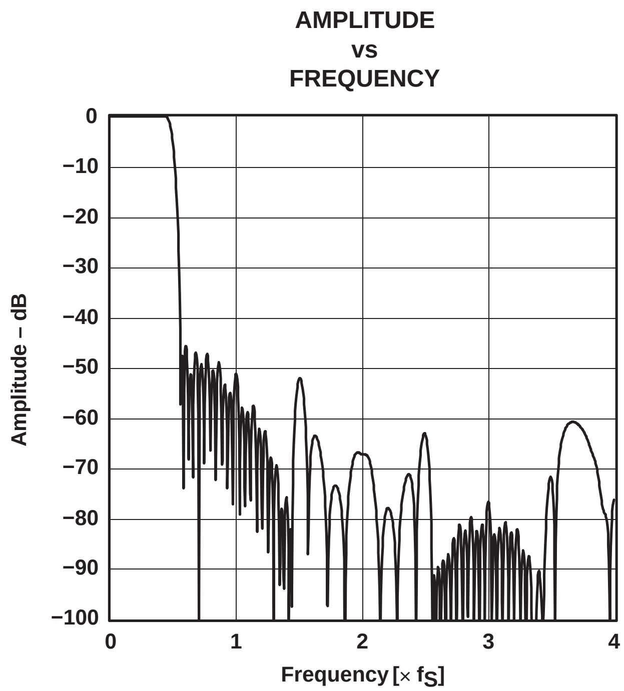


Figure 24. Stop-Band Attenuation

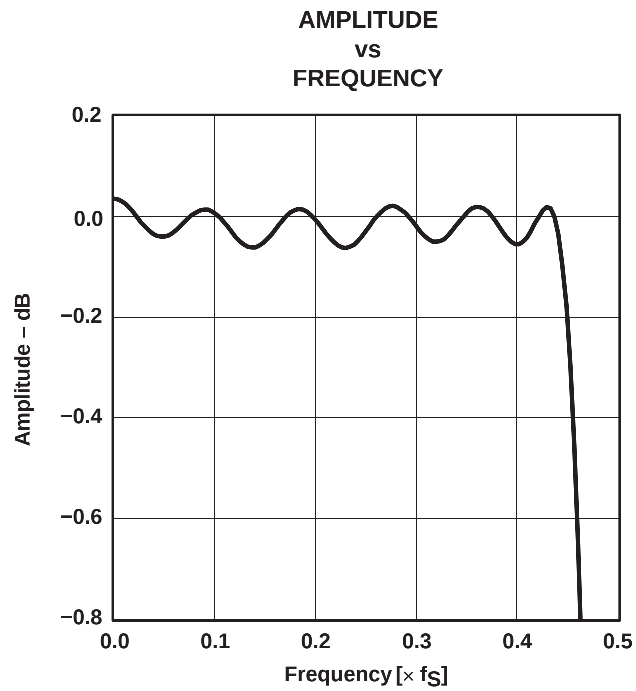


Figure 25. Pass-Band Ripple

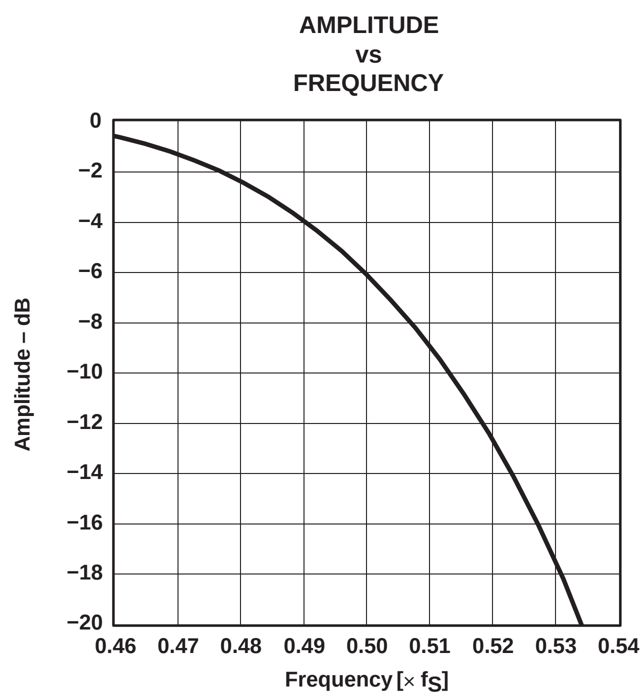


Figure 26. Transition-Band Response

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

DAC ANALOG FIR FILTER FREQUENCY RESPONSE

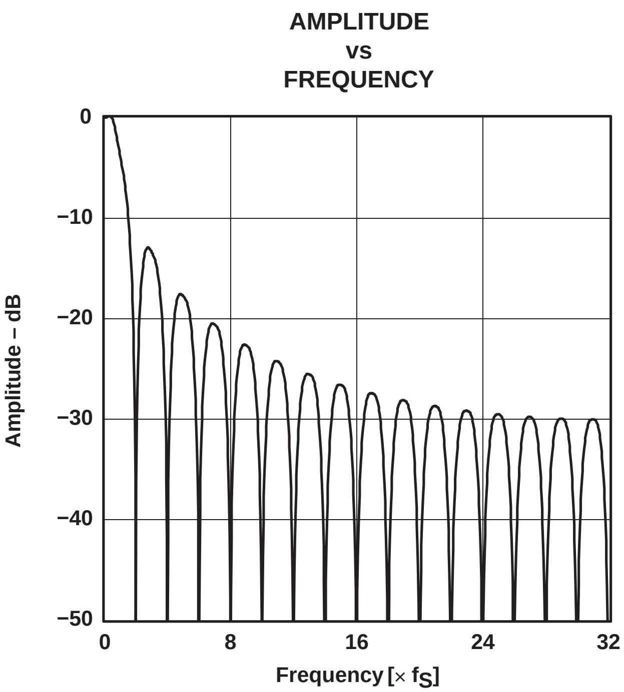


Figure 27. Stop-Band Characteristic

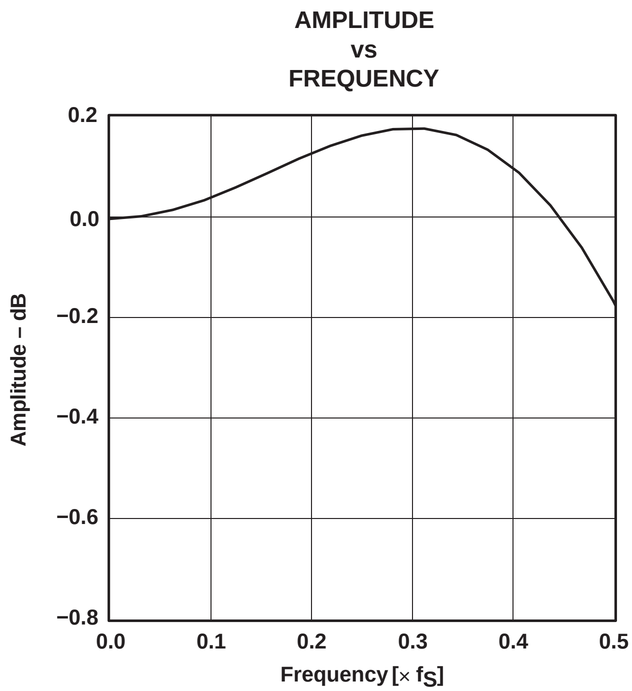


Figure 28. Pass-Band Characteristic

DAC ANALOG LOW-PASS FILTER FREQUENCY RESPONSE

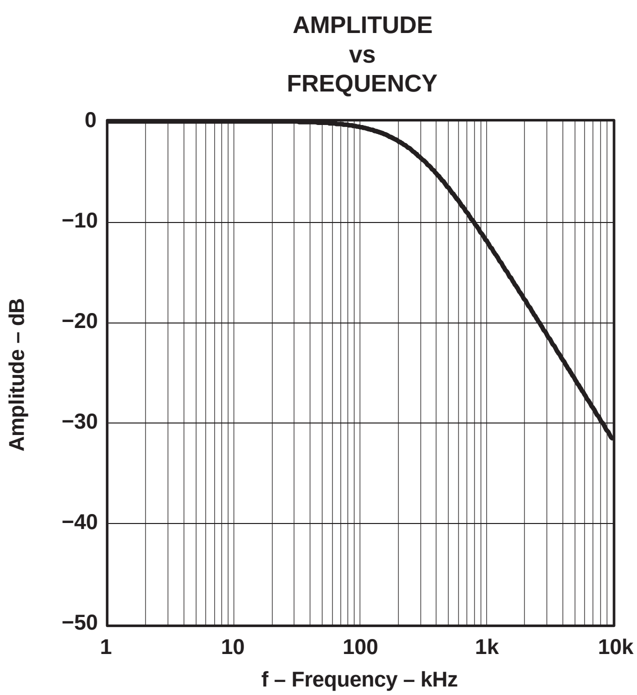


Figure 29. Stop-Band Characteristic

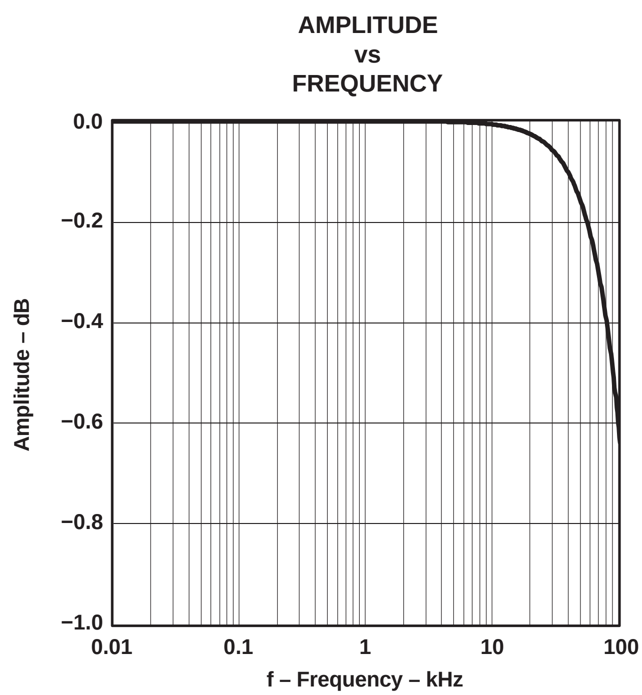


Figure 30. Pass-Band Characteristic

All specifications at T_A = 25°C, V_{BUS} = 5 V, f_S = 44.1 kHz, f_{IN} = 1 kHz, 16-bit data, unless otherwise noted.

USB INTERFACE

Control data and audio data are transferred to the PCM2904/2906 via D+ (pin 1) and D– (pin 2). All data to/from the PCM2904/2906 is transferred at full speed. The device descriprtor contains the information described in Table 1. The device descriptor can be modified on request; contact a Texas Instruments representative about the details.

Table 1. Device Descriptor

USB revision	1.1 compliant
Device class	0x00 (device defined interface level)
Device sub class	0x00 (not specified)
Device protocol	0x00 (not specified)
Max packet size for end-point 0	8 byte
Vendor ID	0x08BB (default value, can be modified)
Product ID	0x2904/0x2906 (default value, can be modified)
Device release number	1.0 (0x0100)
Number of configurations	1
Vendor string	String #1 (see Table 3)
Product string	String #2 (see Table 3)
Serial number	Not supported

The configuration descriptor contains the information described in Table 2. The configuration descriptor can be modified on request; contact a Texas Instruments representative about the details.

Table 2. Configuration Descriptor

Interface	Four interfaces
Power attribute	0x80 (Bus powered, no remote wakeup)
Max power	0xFA (500 mA. Default value, can be modified)

The string descriptor contains the information described in Table 3. The string descriptor can be modified on request; contact a Texas Instruments representative about the details.

Table 3. String Descriptor

#0	0x0409
#1	Burr-Brown from TI (default value, can be modified)
#2	USB audio codec (default value, can be modified)

DEVICE CONFIGURATION

Figure 31 illustrates the USB audio function topology. The PCM2904/2906 has four interfaces. Each interface is constructed by alternative settings.

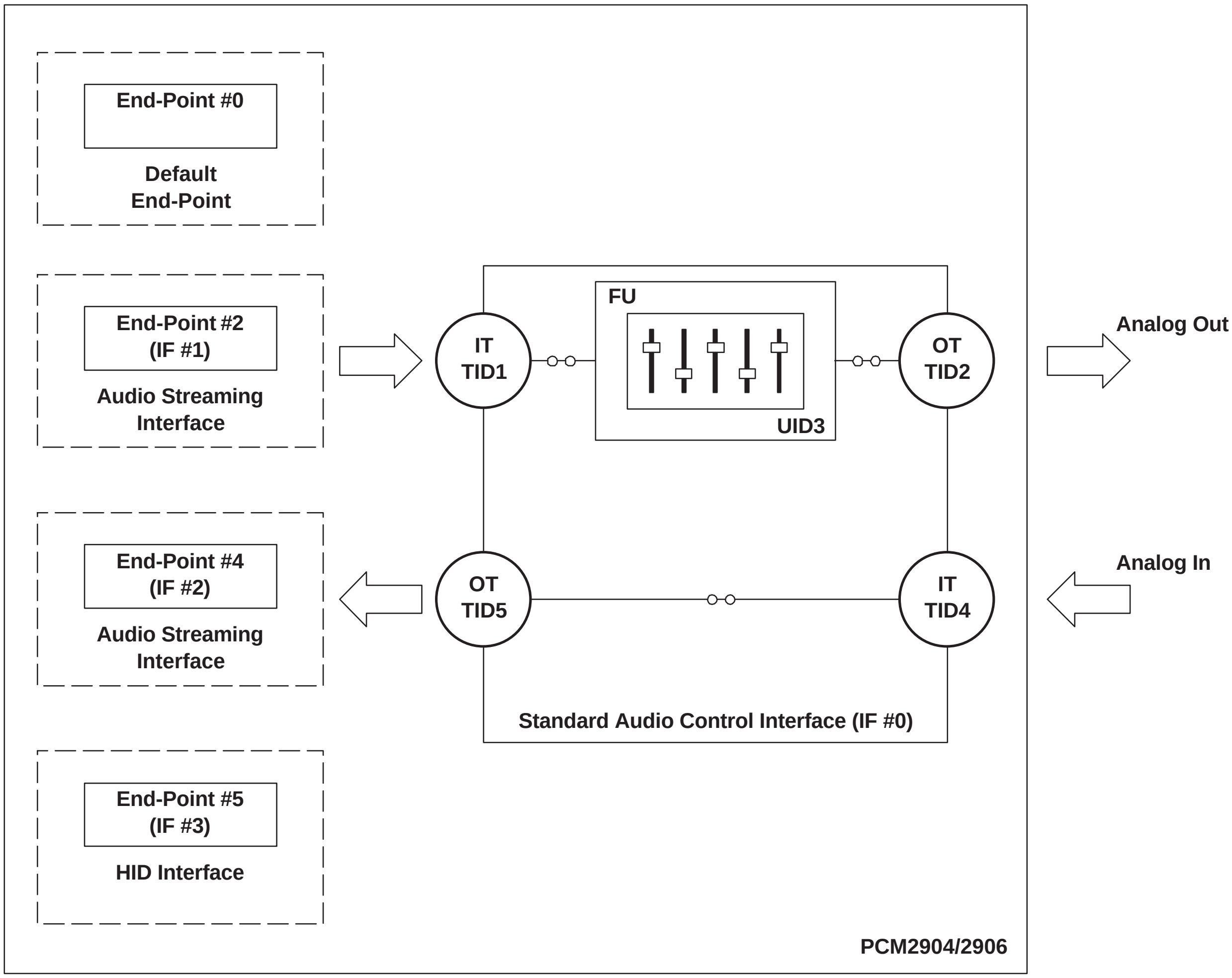


Figure 31. USB Audio Function Topology

Interface #0

Interface #0 is the control interface. Alternative setting #0 is the only possible setting for interface #0. Alternative setting #0 describes the standard audio control interface. The audio control interface is constructed by a terminal. The PCM2904/2906 has the following five terminals.

- Input terminal (IT #1) for isochronous-out stream
- Output terminal (OT #2) for audio analog output
- Feature unit (FU #3) for DAC digital attenuator
- Input terminal (IT #4) for audio analog input
- Output terminal (OT #5) for isochronous-in stream

Input terminal #1 is defined as a *USB stream* (terminal type 0x0101). Input terminal #1 can accept 2-channel audio streams consisting of left and right channels. Output terminal #2 is defined as a *speaker* (terminal type 0x0301). Input terminal #4 is defined as a *microphone* (terminal type 0x0201). Output terminal #5 is defined as a *USB stream* (terminal type 0x0101). Output terminal #5 can generate 2-channel audio streams consisting of left and right channels. Feature unit #3 supports the following sound control features.

- Volume control
- Mute control

The built-in digital volume controller can be manipulated by an audio-class-specific request from 0.0 dB to –64 dB in steps of 1 dB. Each channel can be set for different values. The master volume control is not supported. A request to the master volume is stalled and ignored. The built-in digital mute controller can be manipulated by audio-class-specific request. A master mute control request is acceptable. A request to an individual channel is stalled and ignored.

Interface #1

Interface #1 is the audio streaming data-out interface. Interface #1 has the following seven alternative settings. Alternative setting #0 is the zero-bandwidth setting. All other alternative settings are operational settings.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero bandwidth				
01	16 bit	Stereo	2s complement (PCM)	Adaptive	32, 44.1, 48
02	16 bit	Mono	2s complement (PCM)	Adaptive	32, 44.1, 48
03	8 bit	Stereo	2s complement (PCM)	Adaptive	32, 44.1, 48
04	8 bit	Mono	2s complement (PCM)	Adaptive	32, 44.1, 48
05	8 bit	Stereo	Offset binary (PCM8)	Adaptive	32, 44.1, 48
06	8 bit	Mono	Offset binary (PCM8)	Adaptive	32, 44.1, 48

Interface #2

Interface #2 is the audio streaming data-in interface. Interface #2 has the following 19 alternative settings. Alternative setting #0 is the zero-bandwidth setting. All other alternative settings are operational settings.

ALTERNATIVE SETTING	DATA FORMAT			TRANSFER MODE	SAMPLING RATE (kHz)
00	Zero bandwidth				
01	16 bit	Stereo	2s complement (PCM)	Asynchronous	48
02	16 bit	Mono	2s complement (PCM)	Asynchronous	48
03	16 bit	Stereo	2s complement (PCM)	Asynchronous	44.1
04	16 bit	Mono	2s complement (PCM)	Asynchronous	44.1
05	16 bit	Stereo	2s complement (PCM)	Asynchronous	32
06	16 bit	Mono	2s complement (PCM)	Asynchronous	32
07	16 bit	Stereo	2s complement (PCM)	Asynchronous	22.05
08	16 bit	Mono	2s complement (PCM)	Asynchronous	22.05
09	16 bit	Stereo	2s complement (PCM)	Asynchronous	16
0A	16 bit	Mono	2s complement (PCM)	Asynchronous	16
0B	8 bit	Stereo	2s complement (PCM)	Asynchronous	16
0C	8 bit	Mono	2s complement (PCM)	Asynchronous	16
0D	8 bit	Stereo	2s complement (PCM)	Asynchronous	8
0E	8 bit	Mono	2s complement (PCM)	Asynchronous	8
0F	16 bit	Stereo	2s complement (PCM)	Synchronous	11.025
10	16 bit	Mono	2s complement (PCM)	Synchronous	11.025
11	8 bit	Stereo	2s complement (PCM)	Synchronous	11.025
12	8 bit	Mono	2s complement (PCM)	Synchronous	11.025

Interface #3

Interface #3 is the interrupt data-in interface. Alternative setting #0 is the only possible setting for interface #3. Interface #3 constructs the HID consumer control device. Interface #3 reports the following three key statuses.

- Mute (0xE209)
- Volume up (0xE909)
- Volume down (0xEA09)

End-Points

The PCM2904/2906 has the following four end-points.

- Control end-point (EP #0)
- Isochronous-out audio data stream end-point (EP #2)
- Isochronous-in audio data stream end-point (EP #4)
- HID end-point (EP #5)

The control end-point is a default end-point. The control end-point is used to control all functions of the PCM2904/2906 by the standard USB request and USB audio class specific request from the host. The isochronous-out audio data stream end-point is an audio sink end-point, which receives the PCM audio data. The isochronous-out audio data stream end-point accepts the adaptive transfer mode. The isochronous-in audio data stream end-point is an audio source end-point that transmits the PCM audio data. The isochronous-in audio data stream end-point uses the asynchronous transfer mode. The HID end-point is an interrupt-in end-point. The HID end-point reports HID0, HID1, and HID2 pin status in every 32 ms.

The human interface device (HID) pins are defined as consumer control devices. The HID function is designed as an independent end-point from both isochronous-in and -out end-points. This means that the result obtained from the HID operation depends on the host software. Typically, the HID function is used as a primary audio-out device.

Clock and Reset

The PCM2904/2906 requires a 12-MHz (±500 ppm) clock for the USB and audio functions. The clock can be generated by a built-in oscillator with a 12-MHz crystal resonator. The 12-MHz crystal resonator must be connected to XTI (pin 21) and XTO (pin 20) with one high-value (1-MΩ) resistor and two small capacitors, the capacitance of which depends on the load capacitance of the crystal resonator. An external clock can be supplied to XTI (pin 21). If an external clock is used, XTO (pin 20) must be left open. Because there is no clock disabling signal, use of the external clock supply is not recommended. $\overline{\text{SSPND}}$ (pin 28) is unable to use clock disabling.

The PCM2904/2906 has an internal power-on reset circuit, which is triggered automatically when V_{BUS} (pin 3) exceeds 2.5 V typical (2.7 V to 2.2 V). About 700 µs is required until internal reset release.

Digital Audio Interface (PCM2906)

The PCM2906 employs S/PDIF for both input and output. Isochronous-out data from the host is encoded to the S/PDIF output and the DAC analog output. Input data is selected from either the S/PDIF or ADC analog input. When the device detects S/PDIF input and successfully locks the received data, the isochronous-in transfer data source automatically selected is S/PDIF; otherwise, the data source selected is the ADC analog input.

Supported Input Data (PCM2906)

The following data formats are accepted by S/PDIF for input and output. All other data formats are unusable as S/PDIF.

- 48-kHz 16-bit stereo
- 44.1-kHz 16-bit stereo
- 32-kHz 16-bit stereo

Mismatch between the input data format and the host command may cause unexpected results, with the following exceptions:

- Recording in monaural format from stereo data input at the same data rate
- Recording in 8-bit format from 16-bit data input at the same data rate

A combination of the two foregoing conditions is not accepted.

For playback, all possible data-rate sources are converted to the 16-bit stereo format at the same source data rate.

Channel Status Information (PCM2906)

The channel status information is fixed as consumer application, PCM mode, copyright, and digital/digital converter. All other bits are fixed as 0s except for the sample frequency, which is set automatically according to the data received through the USB.

Copyright Management (PCM2906)

Isochronous-in data is affected by the serial copy management system (SCMS). When the control bit indicates that the received digital audio data is original, the input digital audio data is transferred to the host. If the data is indicated as first generation or higher, the transferred data is routed to the analog input.

Digital audio data output is always encoded as original with SCMS control.

The implementation of this feature is optional. It is the designer's responsibility to determine whether to implement this feature in a product or not.

INTERFACE SEQUENCE

Power-On, Attach, and Playback Sequence

The PCM2904/2906 is ready for setup when the reset sequence has finished and the USB device is attached. After a connection has been established by setup, the PCM2904/PCM2906 is ready to accept USB audio data. While waiting for the audio data (idle state), the analog output is set to bipolar zero (BPZ).

When receiving the audio data, the PCM2904/2906 stores the first audio packet, which contained 1-ms audio data, into the internal storage buffer. The PCM2904/2906 starts playing the audio data when detecting the following start-of-frame (SOF) packet.

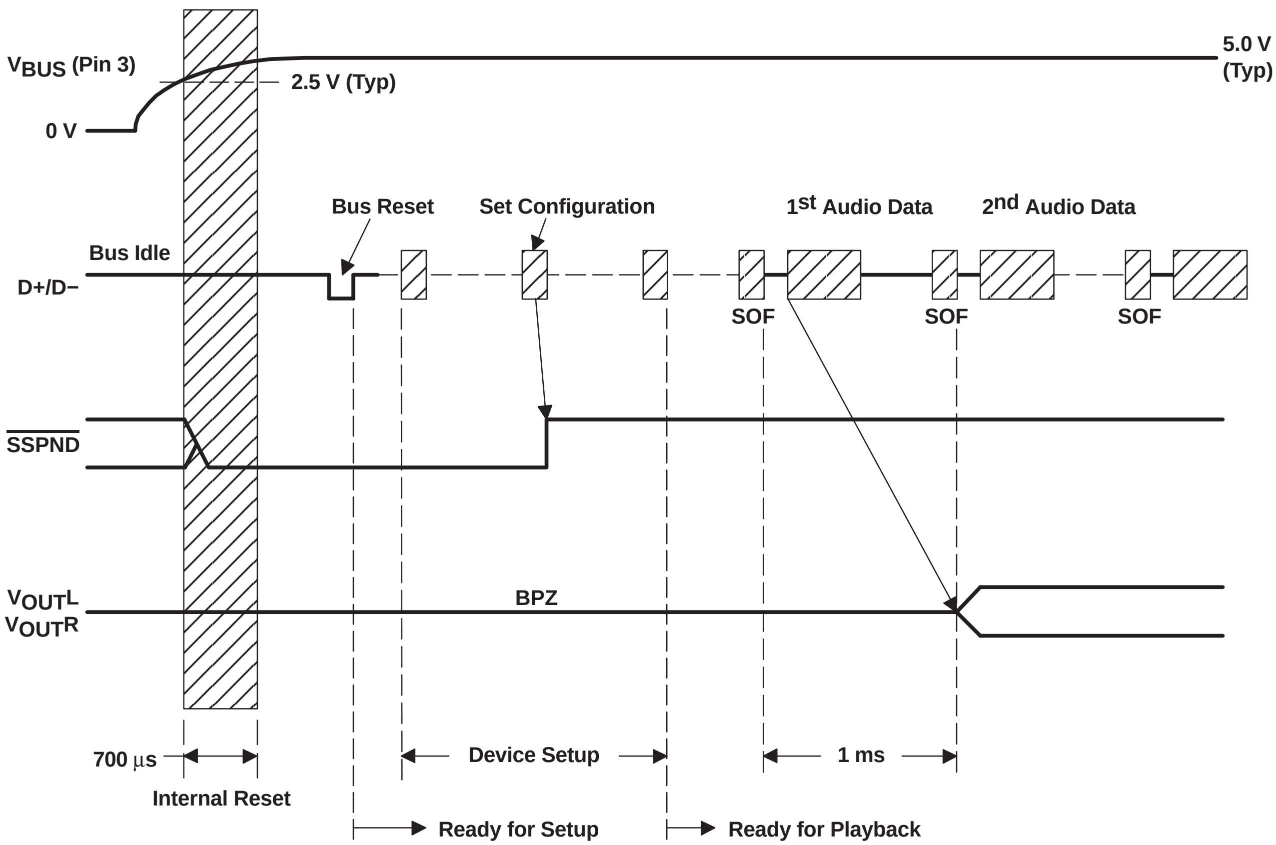


Figure 32. Initial Sequence

Play, Stop, and Detach Sequence

When the host finishes or aborts the playback, the PCM2904/2906 stops playing after the last audio data has played.

Record Sequence

The PCM2904/2906 starts audio capture into the internal memory after receiving the SET_INTERFACE command.

Suspend and Resume Sequence

The PCM2904/2906 enters the suspend state after a constant idle state on the USB bus, approximately 5 ms. While the PCM2904/2906 enters the suspend state, the $\overline{\text{SSPND}}$ flag (pin 28) is asserted. The PCM2904/2906 wakes up immediately on detecting a non-idle state on the USB.

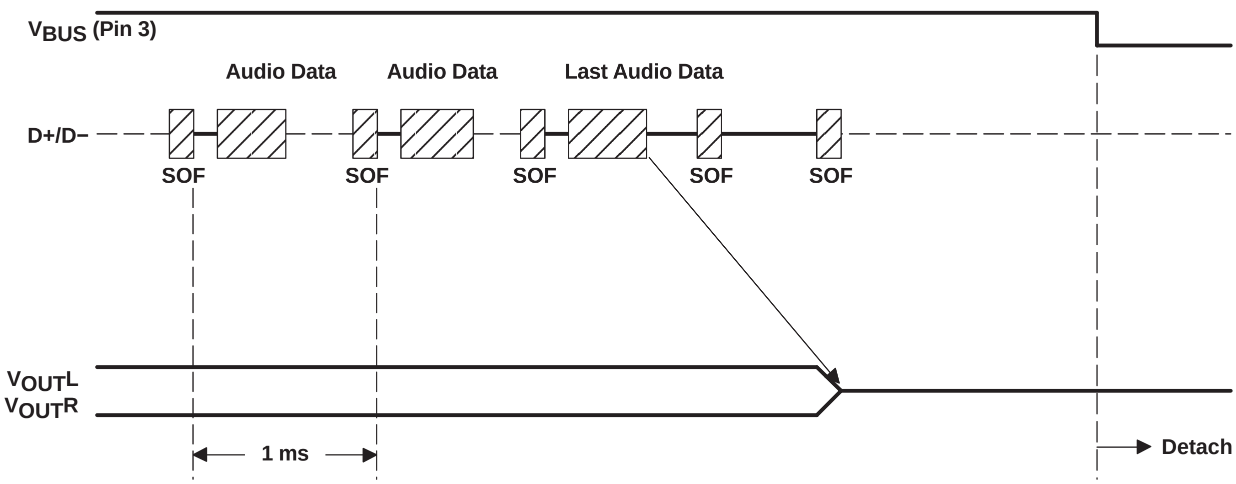


Figure 33. Play, Stop, and Detach

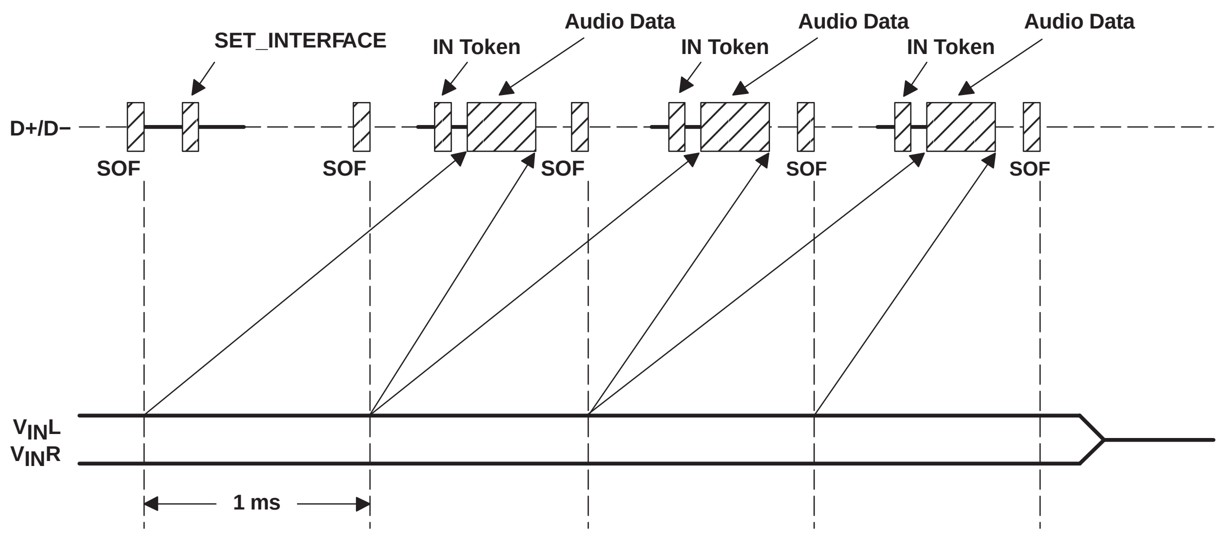


Figure 34. Record Sequence

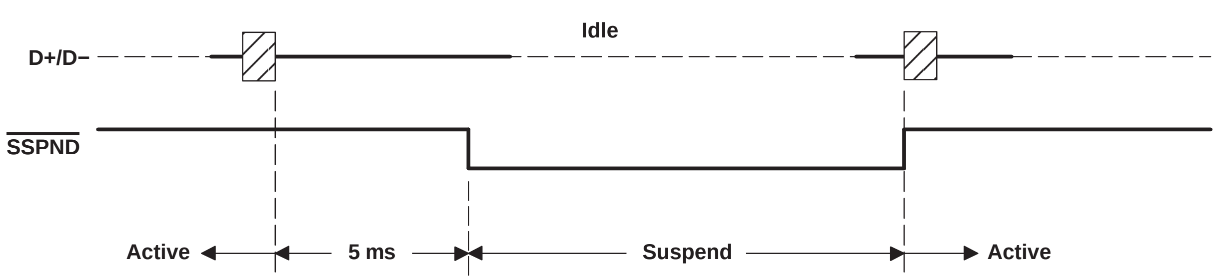
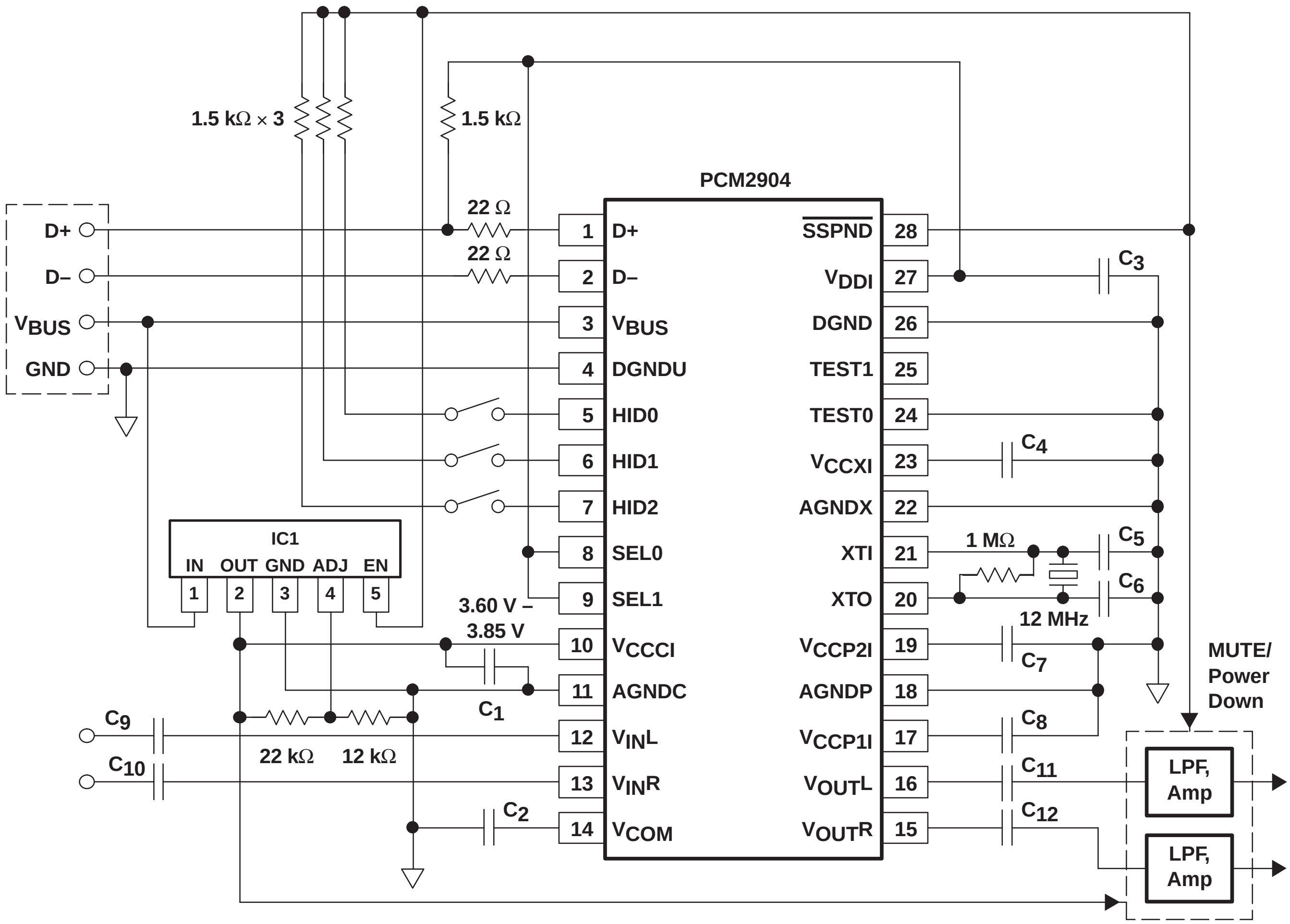


Figure 35. Suspend and Resume

PCM2904 TYPICAL CIRCUIT CONNECTION 1

Figure 36 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.



NOTES:

C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF.)

C_1, C_2: 10 µF

C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)

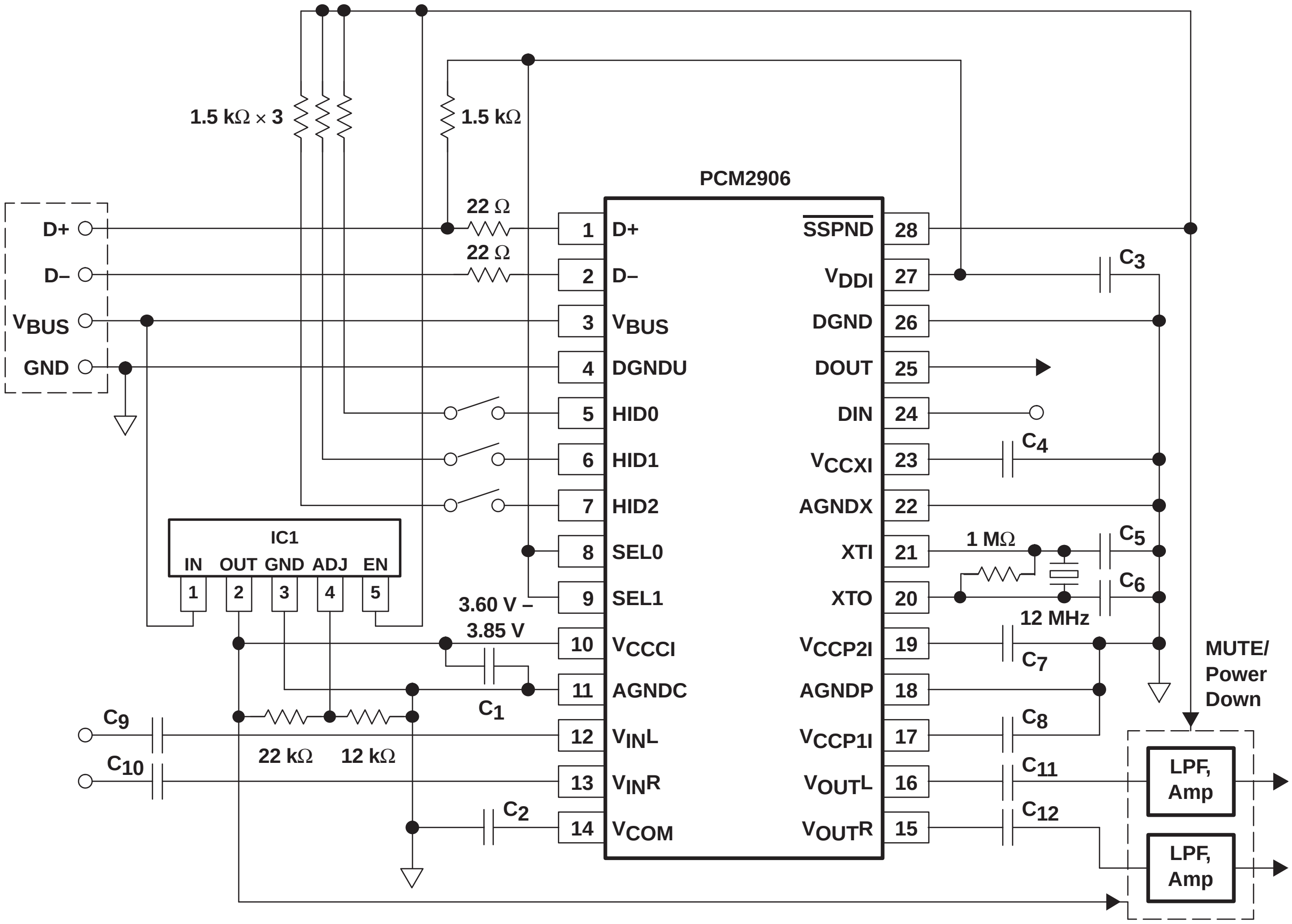
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.

IC1 : REG103xA-A (TI) or equivalent. Analog performance may vary depending on IC1.

Figure 36. Bus-Powered Configuration for High-Performance PCM2904 Application

PCM2906 TYPICAL CIRCUIT CONNECTION 1

Figure 37 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.

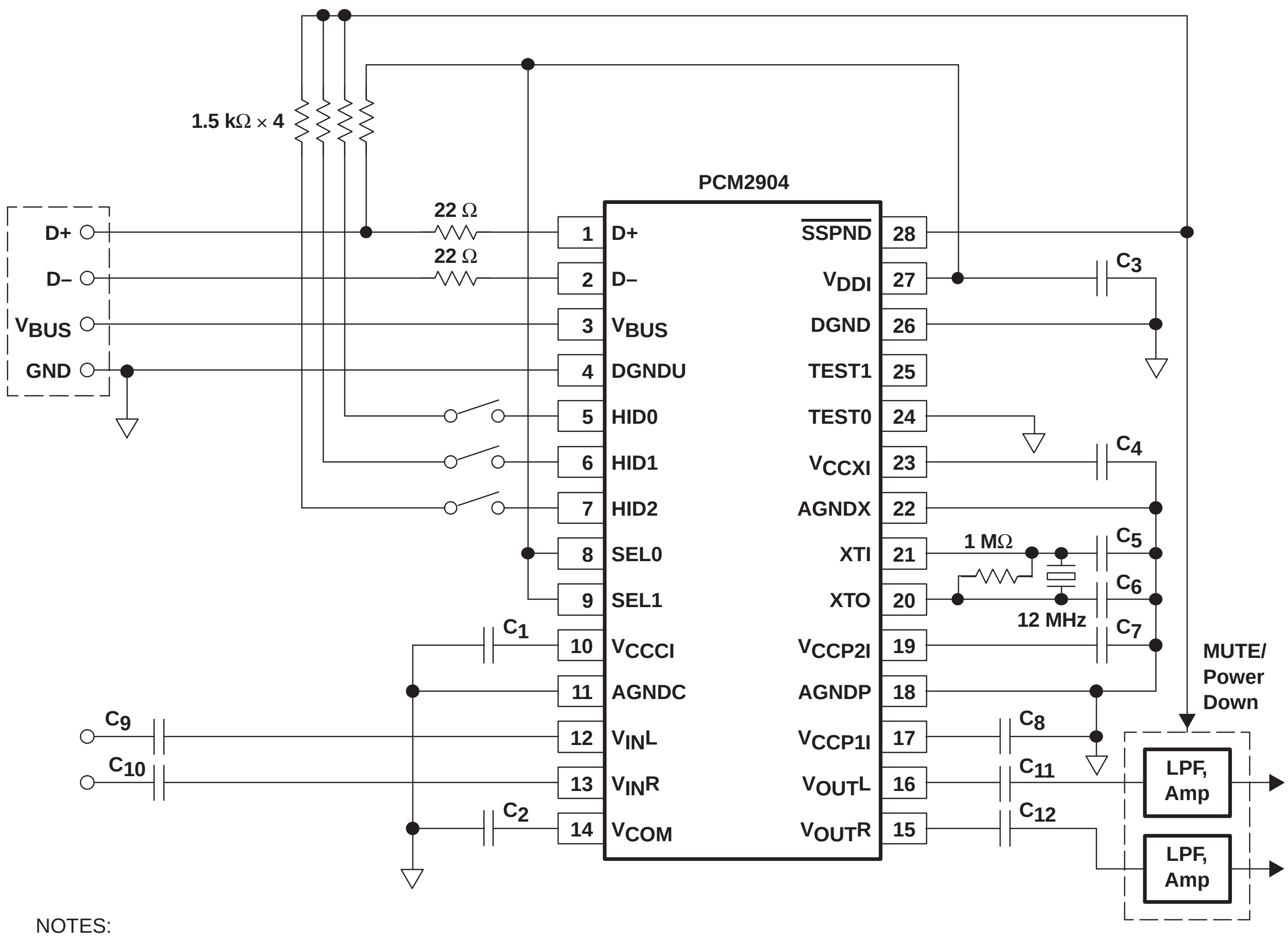


NOTES:
C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF.)
C_1, C_2: 10 µF
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
IC1 : REG103xA-A (TI) or equivalent. Analog performance may vary depending on IC1.

Figure 37. Bus-Powered Configuration for High-Performance PCM2906 Application

PCM2904 TYPICAL CIRCUIT CONNECTION 2

Figure 38 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.

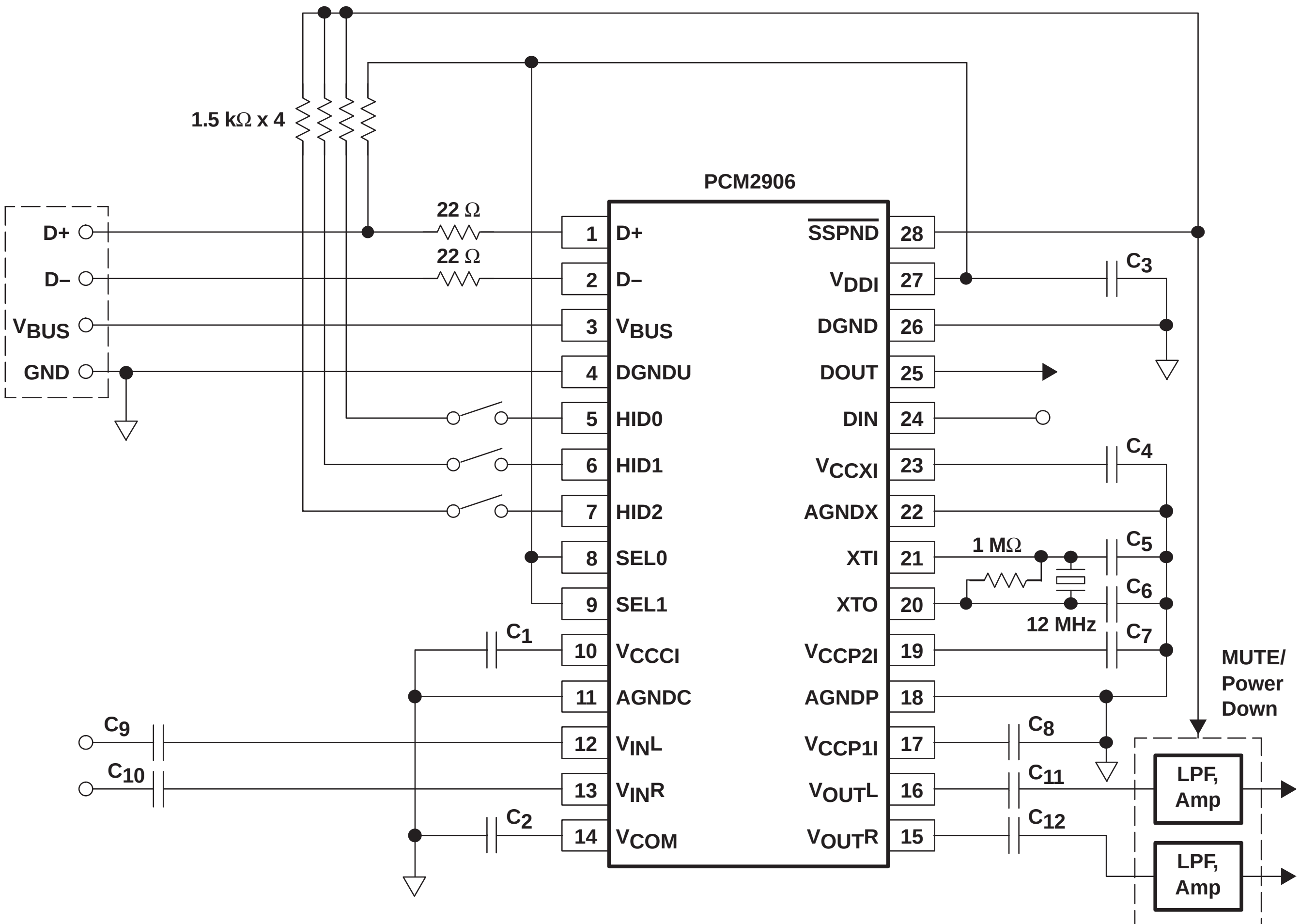


NOTES:
C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF.)
C_1, C_2: 10 µF
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
In this case, the analog performance of the A/D converter may be degraded.

Figure 38. PCM2904 Bus-Powered Configuration

PCM2906 TYPICAL CIRCUIT CONNECTION 2

Figure 39 illustrates a typical circuit connection for a simple application. The circuit illustrated is for information only. The whole board design should be considered to meet the USB specification as a USB compliant product.



NOTES:
C_3, C_4, C_7, C_8: 1 µF (These capacitors must be less than 2 µF.)
C_1, C_2: 10 µF
C_5, C_6: 10 pF to 33 pF (depending on crystal resonator)
C_9, C_{10}, C_{11}, C_{12}: The capacitance may vary depending on design.
In this case, the analog performance of the A/D converter may be degraded.

Figure 39. PCM2906 Bus-Powered Configuration

APPLICATION INFORMATION

OPERATING ENVIRONMENT

To get the appropriate operation, one of the following operating systems must be working on the host PC that has the USB port assured by the manufacturer. If the condition is fulfilled, the operation of the PCM2904/2906 does not depend on the operating speed of the CPU.

Texas Instruments has confirmed following operating environments.

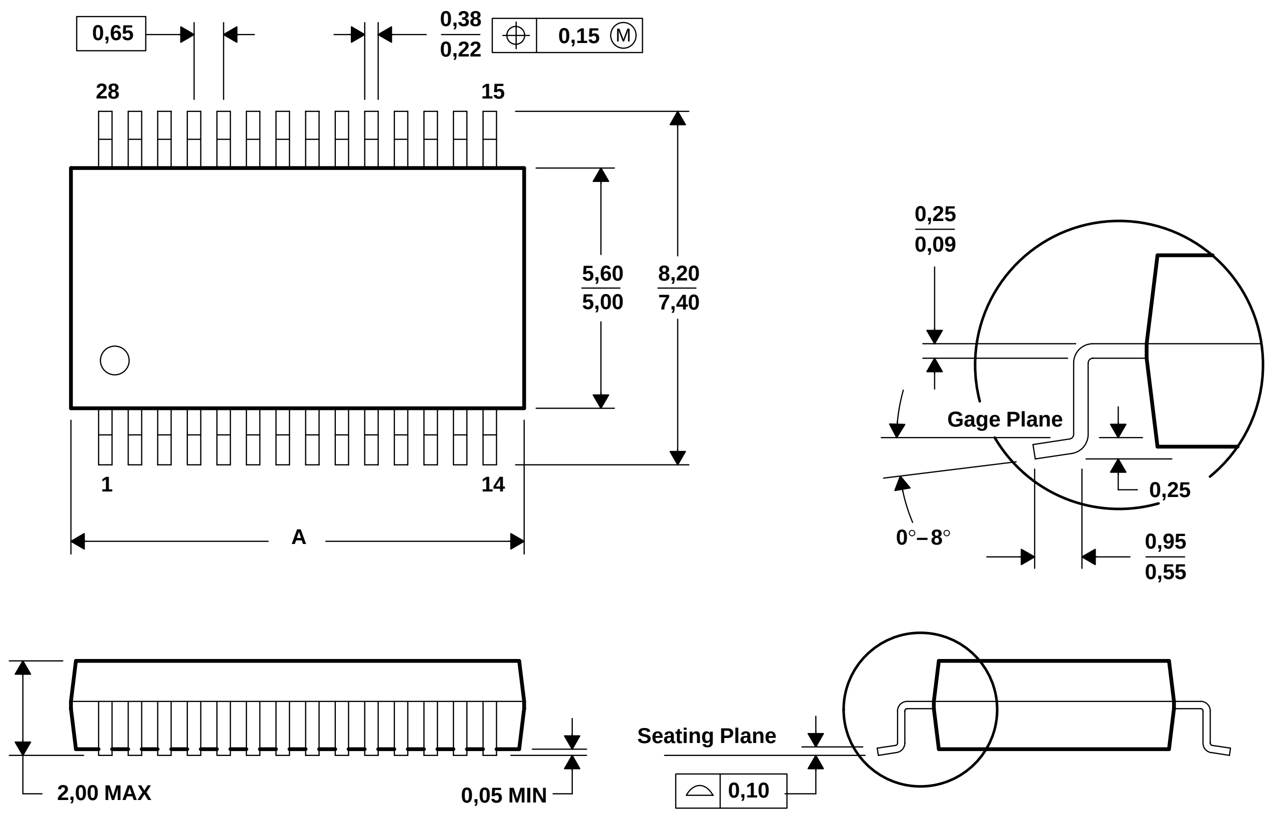
- Operating System
  - Microsoft™ Windows™ 98/98SE/Me™ Japanese/English Edition
  - Microsoft Windows 2000 Professional Japanese/English Edition
  - Microsoft Windows XP™ Home/Professional Japanese/English Edition (For Windows™ XP, use the latest version of the USB audio driver that is available on Windows update site)
  - Apple™ Computer Mac™ OS 9.1 or later Japanese/English Edition
  - Apple Computer Mac OS™ X 10.0 or later English Edition
  - Apple Computer Mac OS X 10.1 or later Japanese Edition (For Mac OS X 10.0 Japanese Edition, plug and play does not work for USB audio device appropriately)
- PC: Following PC-AT compatible computers for above OS (OS requirement must be met)
  - Motherboard using Intel™ 440BX or ZX chipset (using USB controller in the chipset)
  - Motherboard using Intel i810 chipset (using USB controller in the chipset)
  - Motherboard using Intel i815 chipset (using USB controller in the chipset)
  - Motherboard using Intel i820 chipset (using USB controller in the chipset)
  - Motherboard using Intel i845 chipset (using USB controller in the chipset)
  - Motherboard using Intel i850 chipset (using USB controller in the chipset)
  - Motherboard using Apollo KT133 chipset (using USB controller in the chipset)
  - Motherboard using Apollo Pro plus chipset (using USB controller in the chipset)
  - Motherboard using MVP4 or MVP3 chipset (using USB controller in the chipset)
  - Motherboard using Aladdin V chipset (using USB controller in the chipset)
  - Motherboard using SiS530 or SiS559 chipset (using USB controller in the chipset)
  - Motherboard using SiS735 chipset (using USB controller in the chipset)

NOTE: The OSs and PCs for which the operation of the PCM2904/2906 was confirmed are listed above. The PCM2904/2906 may also work with other OSs and PCs that have not been tested. Furthermore, there is no assurance that the PCM2904/2906 will work with every PC having a compatible chipset, because other design factors of the motherboard may also cause incompatibility.

The PCM2904/2906 has been acknowledged in the USB compliance test. However, the acknowledgement is just for the PCM2904/2906 from Texas Instruments. Be careful that the acknowledgement is not for the customer’s USB system using the PCM2904/2906.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265