PARADIGM

PDM41256

256K Static RAM
32K x 8-Bit

Features

- ☐ High-speed access times
  Com'l: 7, 8, 10, 12, and 15 ns
  Ind'l: 8, 10, 12, and 15 ns
- ☐ Low power operation (typical)
  - PDM41256SA
    Active: 400 mW
    Standby: 150 mW
  - PDM41256LA
    Active: 350 mW
    Standby: 25 mW
- ☐ Single +5V (±10%) power supply
- ☐ TTL-compatible inputs and outputs
- ☐ Packages
  Plastic SOJ (300 mil) - TSO
  Plastic TSOP - T

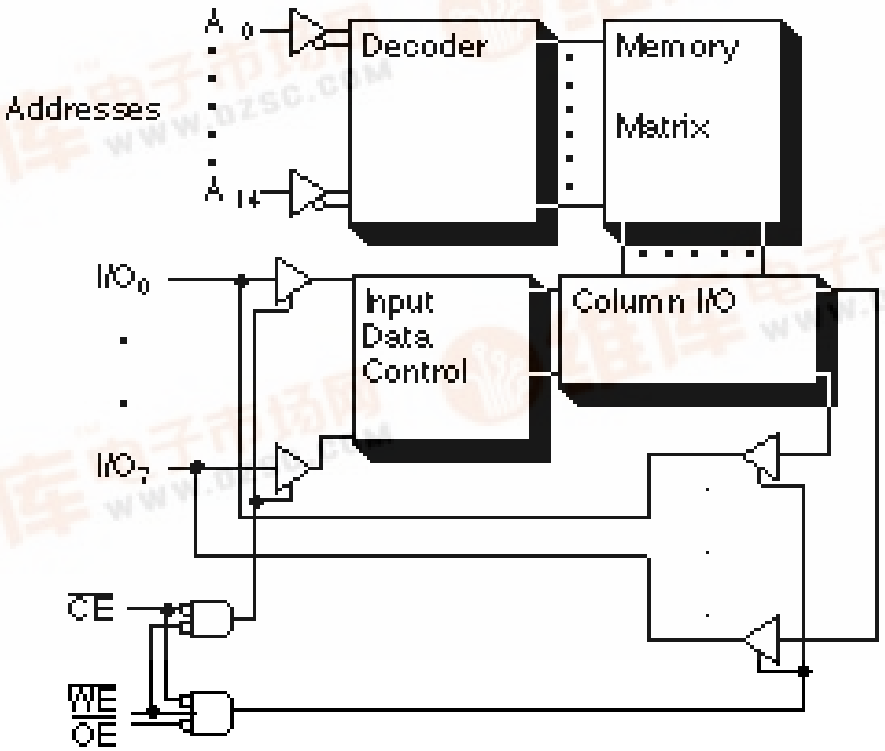
Description

The PDM41256 is a high-performance CMOS static RAM organized as 32,768 x 8 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to this device is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ are both LOW.

The PDM41256 operates from a single +5V power supply and all the inputs and outputs are fully TTL-compatible. The PDM41256 comes in two versions, the standard power version PDM41256SA and a low power version the PDM41256LA. The two versions are functionally the same and only differ in their power consumption.

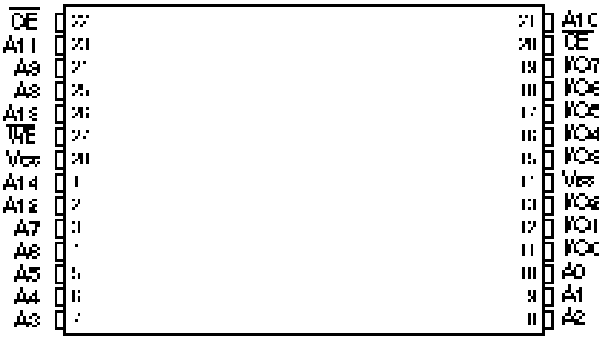
The PDM41256 is available in a 28-pin plastic TSOP and a 28-pin 300-mil plastic SOJ.

Functional Block Diagram



Pin Configurations

TSOP



SOJ

Pin Description

Name	Description
A14-A0	Address Inputs
I/O7-I/O0	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{CE}$	Chip Enable Input
V_{CC}	Power (+5V)
V_{SS}	Ground

Truth Table

$\overline{OE}$	$\overline{WE}$	$\overline{CE}$	I/O	MODE
X	X	H	Hi-Z	Standby
L	H	L	D_{OUT}	Read
X	L	L	D_{IN}	Write
H	H	L	Hi-Z	Output Disable

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to Vss	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C
Industrial	Ambient Temperature	–40	25	85	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		PSM41256SA		PSM41256LA		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = Vss to V_{CC}	Com'l/ Ind.	–5	5	–5	5	µA
I_{LO}	Output Leakage Current	V_{CC}= MAX., $\overline{CE}$ = V_{IH}, V_{OUT} = Vss to V_{CC}	Com'l/ Ind.	–5	5	–5	5	µA
V_{IL}	Input Low Voltage			–0.5(1)	0.8	–0.5(1)	0.8	V
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{OL}	Output Low Voltage	I_{OL}=8 mA, V_{CC} = Min. I_{OL} = 10 mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{CC} = Min.		2.4	—	2.4	—	V

NOTE: 1. V_{IL}(min) = –3.0V for pulse width less than 20 ns.

Power Supply Characteristics

Symbol	Parameter	Power	-7	-8		-10		-12		-15		Units
			Com'l.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	
I_{CC}	Operating Current $\overline{CE}$ = V_{IL}	SA	210	200	210	190	200	180	190	170	180	mA
	f = f_{MAX} = 1/t_{RC} V_{CC} = Max I_{OUT} = 0 mA	LA	190	180	190	170	180	160	170	150	160	mA
I_{SB}	Standby Current $\overline{CE}$ = V_{IH}	SA	90	80	80	70	70	60	60	50	50	mA
	f = f_{MAX} = 1/t_{RC} V_{CC} = Max	LA	90	80	80	70	70	60	60	50	50	mA
I_{SB1}	Full Standby Current $\overline{CE}$ ≥ V_{CC} – 0.2V	SA	20	20	20	20	20	20	20	20	20	mA
	f = 0 V_{CC} = Max V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V	LA	5	5	10	5	10	5	10	5	10	mA

SHADED AREA = PRELIMINARY DATA
NOTE:All values are maximum guaranteed values.

Capacitance(1) (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE: 1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

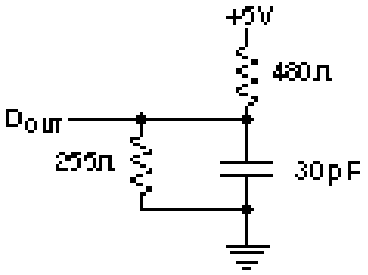


Figure 1. Output Load Equivalent

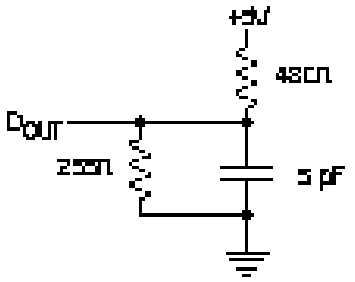


Figure 2. Output Load Equivalent (for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE}, t_{LZOE}, t_{HZOE})

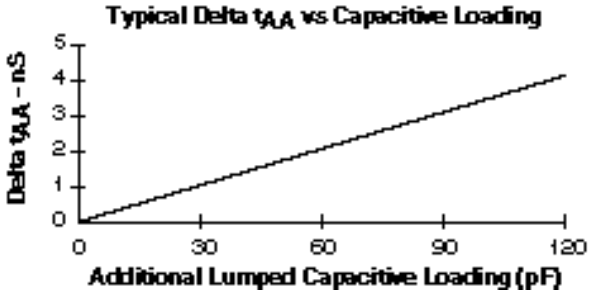
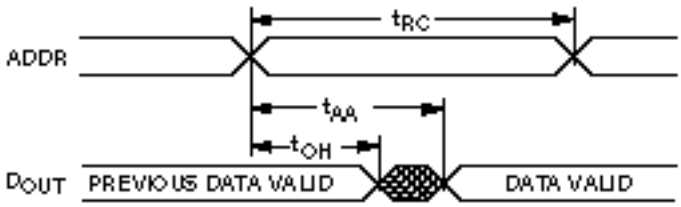
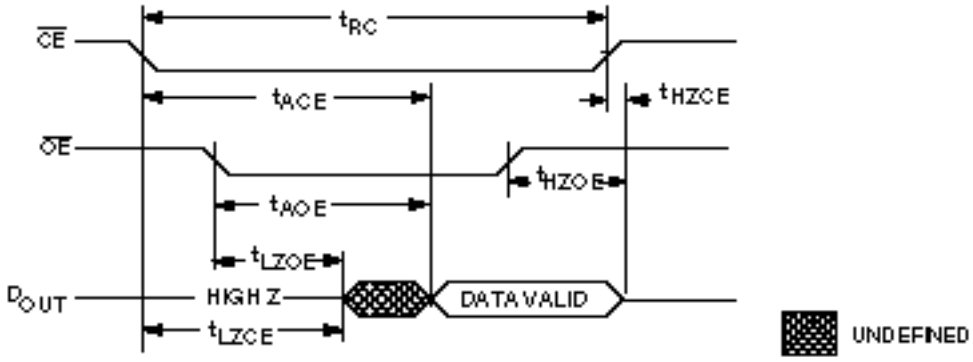


Figure 3.

Read Cycle No. 1(1)



Read Cycle No. 2(2)

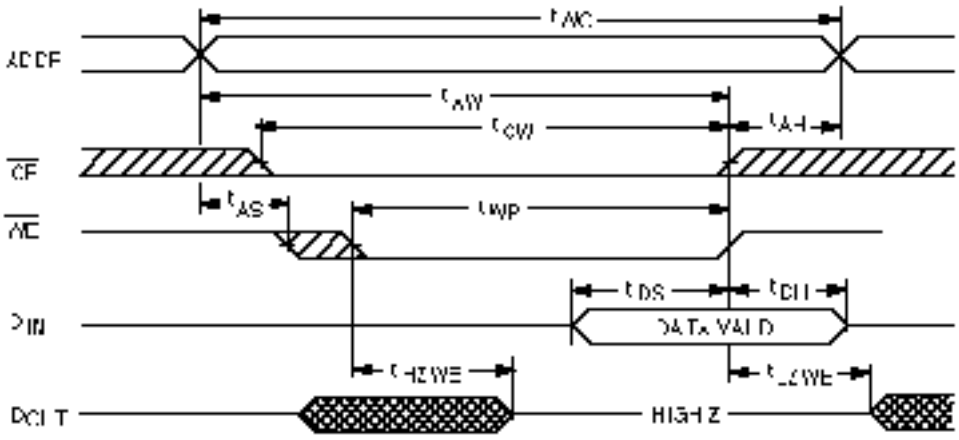


AC Electrical Characteristics

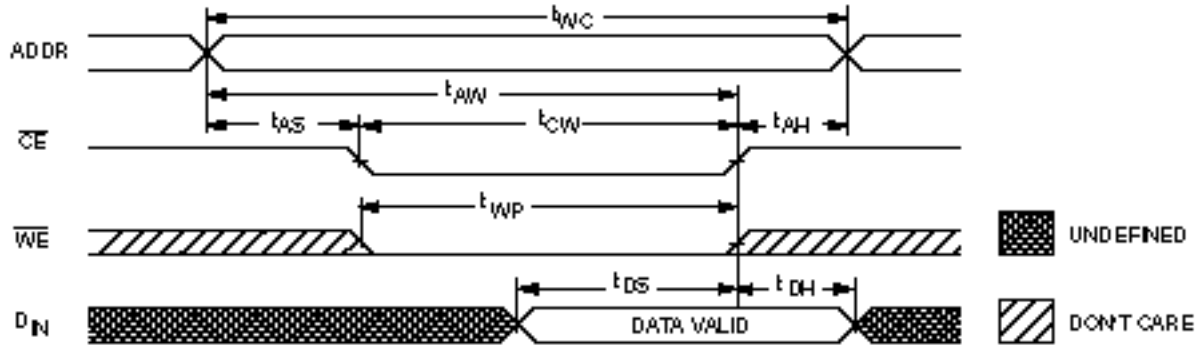
Description		--7(6)		--8(6)		-10(6)		-12		-15		
READ Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
READ cycle time	t_{RC}	7		8		10		12		15		ns
Address access time	t_{AA}		7		8		10		12		15	ns
Chip enable access time	t_{ACE}		7		8		10		12		15	ns
Output hold from address change	t_{OH}	3		3		3		3		3		ns
Chip enable to output in low Z(3, 4, 5)	t_{LZCE}	5		5		5		5		5		ns
Chip disable to output in high Z(3, 4, 5)	t_{HZCE}		5		6		6		6		6	ns
Chip enable to power up time(4)	t_{PU}	0		0		0		0		0		ns
Chip disable to power down time(4)	t_{PD}		7		8		10		12		15	ns
Output enable access time	t_{AOE}		5		5		5		6		8	ns
Output enable to output in low Z(4, 5)	t_{LZOE}	0		0		0		0		0		ns
Output disable to output in high Z(4, 5)	t_{HZOE}		5		6		6		6		6	ns

SHADED AREA = PRELIMINARY DATA.
Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)

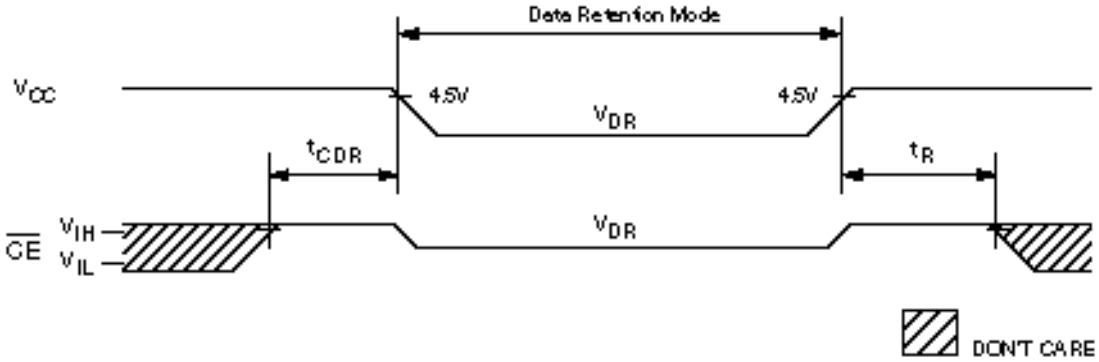


AC Electrical Characteristics

Description		-7[6]		-8[6]		-10[6]		-12		-15		
WRITE Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE cycle time	t_{WC}	7		8		10		12		15		ns
Chip enable to end of write	t_{CW}	7		8		10		10		12		ns
Address valid to end of write	t_{AW}	7		8		10		10		12		ns
Address setup time	t_{AS}	0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		ns
Write pulse width	t_{WP}	7		8		10		10		11		ns
Data setup time	t_{DS}	6		7		7		7		7		ns
Data hold time	t_{DH}	0		0		0		0		0		ns
Write disable to output in low Z[4, 5]	t_{LZWE}	0		0		0		0		0		ns
Write enable to output in high Z[4, 5]	t_{HZWE}		3		3		3		3		3	ns

SHADED AREA = PRELIMINARY DATA.

Low V_{CC} Data Retention Waveform



Data Retention Electrical Characteristics (LA Version Only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	V_{CC} = 2V	—	95	500	µA
			V_{CC} = 3V	—	350	750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[4]	Operation Recovery Time			t_{RC}	—	—	ns

NOTES: (For three previous Electrical Characteristics tables)

1. The device is continuously selected. Chip Enable is held in its active state.
2. The address is valid prior to or coincident with the latest occuring Chip Enable.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
4. This parameter is sampled.
5. The parameter is tested with CL = 5 pF as shown in Figure 2. Transition is measured ±200 mV from steady state voltage
6. Vcc = 5V ± 5%.

Ordering Information