ICs for Communications

Multichannel Network Interface Controller for HDLC + Extensions MUNICH128X

PEB 20324 Version 2.2

Hardware Reference Manual 04.99

DS 1

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Chapter 6	Chapter 5	Updated.
Tables 1...8	Tables 2-1 ...2-8	Pin Description Tables updated.

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Preface

The MUNICH128X is a 128-channel WAN Protocol Controller which provides four independent 24/32-channel HDLC controllers, each with a dedicated 64-channel DMA Controller and a Serial PCM Interface Controller. The device is offered in a 160-pin MQFP package, making it ideal for high-port-density applications.

Organization of this Document

This Hardware Reference Manual is divided into 7 chapters. It is organized as follows:

- Chapter 1, Introduction
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- Chapter 2, Pin Description
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- Chapter 3, Functional IC Description
  Gives a general functional overview of the MUNICH128X.

- Chapter 4, Electrical Characteristics
  Gives a detailed description of all electrical DC and AC characteristics and provides timing diagrams and values for all interfaces.

- Chapter 5, Test Modes
  Gives a detailed description of the JTAG boundary scan interface.

- Chapter 6, Package Outline

Related Documentation

MUNICH128X Version 2.2

Prpgrammer’s Reference Manual 03.99 DS1

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1 Introduction

The MUNICH128X is a 128-channel WAN Protocol Controller which provides four independent 24/32-channel HDLC controllers, each with a dedicated 64-channel DMA Controller and a Serial PCM Interface Controller. The device is offered in a 160-pin MQFP package, making it ideal for high-port-density applications.

The MUNICH128X provides capability for up to 128 full duplex serial PCM channels. The chip performs layer 2 HDLC formatting/deformatting or V.110 or X.30 protocols up to a data rate of 38.4 kbit/s (V.110) or 64 kbit/s (HDLC). The MUNICH128X also performs transparent transmission for DMI modes 0, 1, and 2. Processed data is transferred to host memory via the PCI interface or de-multiplexed bus interface.

The MUNICH128X is compatible with the LAPD ISDN (Integrated Services Digital Network) protocol specified by CCITT, as well as with HDLC, SDLC, LAPB and DMI protocols. It provides rate adaptation for time slot transmission from 64 kbit/s down to 8 kbit/s and the concatenation of time slots, supporting the ISDN H0, H11, H12 superchannels.

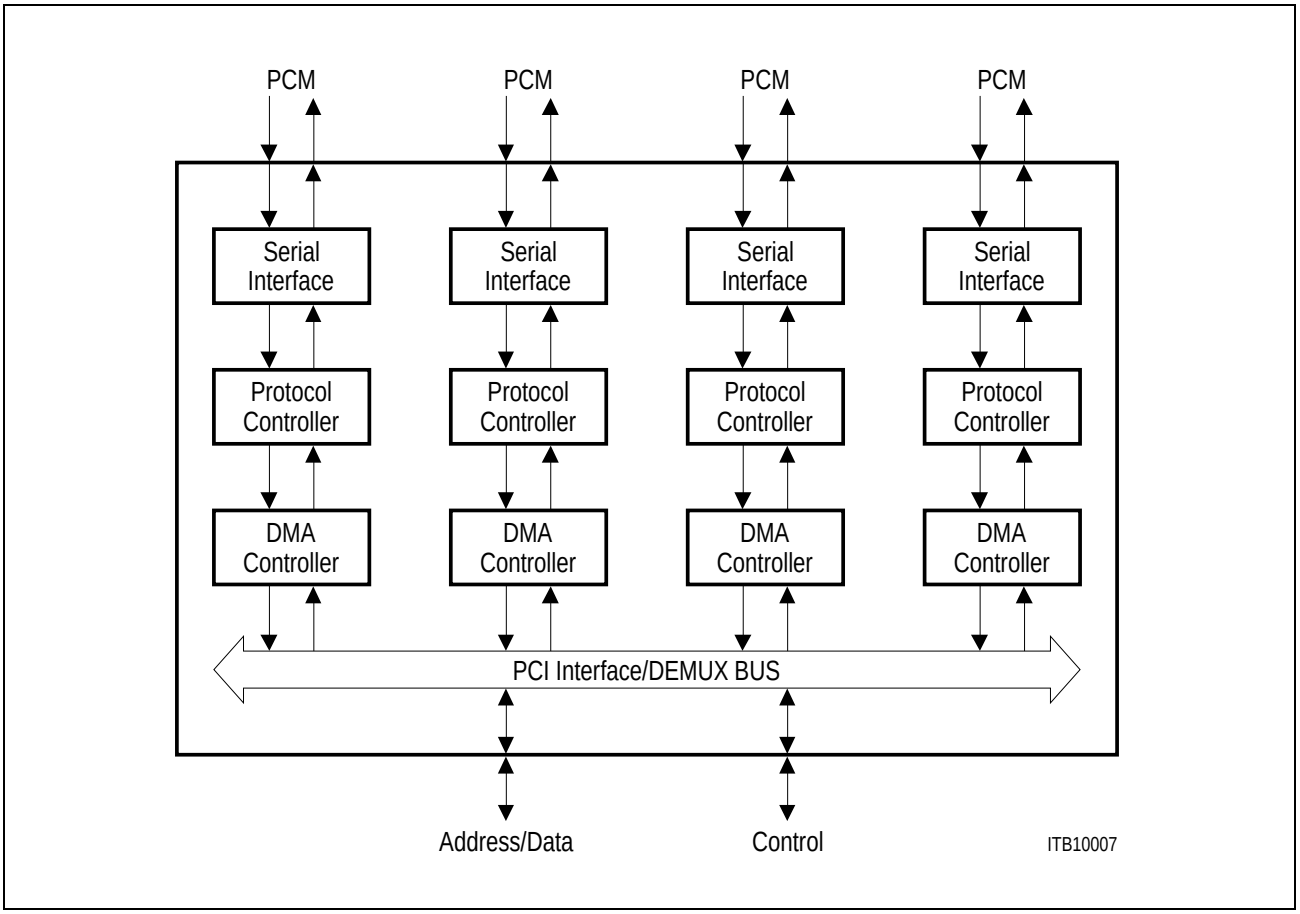


Figure 1-1 Simplified Block Diagram

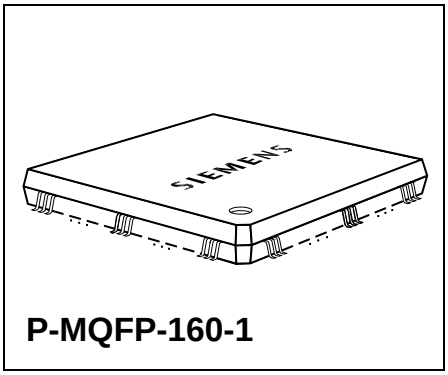
Multichannel Network Interface Controller for HDLC + Extensions
MUNICH128X

PEB 20324

Version 2.2

CMOS

1.1 Features



P-MQFP-160-1

Four independent 24/32-channel HDLC PCM Controllers with common PCI interface.

Each of them provides:

- Dedicated 1024 byte Tx Buffer
- Dedicated 1024 byte Rx Buffer
- Dedicated Serial PCM Interface Controller
  - T1 rates: 1.536, 1.544, 3.088, 6.176 Mbit/s
  - E1 rates: 2.048, 4.096, 8.192 Mbit/s

- Dedicated 64-channel DMA Controller
  - Supports linked-list buffer processing
  - 16-DWord Tx DMA FIFO
  - 16-DWord Rx DMA FIFO
  - 4-DWord burst of Rx descriptors
  - 3-DWord burst of Tx descriptors

  - n-DWord burst of configuration blocks
    (n is unlimited according the MUNICH128X, but internal port arbitration may lead to a lower typical burst size of 4 or 8 DWords)
- **Dynamic Programmable Channel Allocation**
  - Compatible with T1/DS1 24-channel and CEPT 32-channel PCM byte format
  - Concatenation of any, not necessarily consecutive, time slots to superchannels independently for receive and transmit direction
  - Support of H0, H11, H12 ISDN-channels
  - Subchanneling on each time slot possible

Type	Package
PEB 20324	P-MQFP-160-1
PEF 20324	P-MQFP-160-1

- **Bit Processor Functions** (adjustable for each channel)
  - HDLC Protocol
    - Automatic flag detection
    - Shared opening and closing flag
    - Detection of interframe-time-fill change, generation of interframe-time-fill ‘1’s or flags
    - Zero bit insertion
    - Flag stuffing and flag adjustment for rate adaption
    - CRC generation and checking (16 or 32 bits)
    - Transparent CRC option per channel and/or per message
    - Error detection (abort, long frame, CRC error, 2 categories of short frames, non-octet frame content)
    - ABORT/IDLE flag generation
  - V.110/X.30 Protocol
    - Automatic synchronization in receive direction, automatic generation of the synchronization pattern in transmit direction
    - E/S/X bits freely programmable in transmit direction, may be changed during transmission; changes monitored and reported in receive direction
    - Generation/detection of loss of synchronism
    - Bit framing with network data rates from 600 bit/s up to 38.4 Kbit/s
  - Transparent Mode A
    - Slot synchronous transparent transmission/reception without frame structure
    - Flag generation, flag stuffing, flag extraction, flag generation in the abort case with programmable flag
    - Synchronized data transfer for fractional T1/PRI channels
  - Transparent Mode B
    - Transparent transmission/reception in frames delimited by 00_H flags
    - Shared opening and closing flag
    - Flag stuffing, flag detection, flag generation in the abort case
    - Error detection (non octet frame content, short frame, long frame)
  - Transparent Mode R
    - Transparent transmission/reception with GSM 08.60 frame structure
    - Automatic 0000_H flag generation/detection
    - Support of 40, $39^1/_2$, $40^1/_2$ octet frames
    - Error detection (non octet frame contents, short frame, long frame)
  - Protocol Independent
    - Channel inversion (data, flags, IDLE code)
    - Format conventions as in CCITT Q.921 § 2.8
    - Data over- and underflow detected

- **32 Bit / 33 MHz PCI 2.1 Interface**
- **32 Bit / 33 MHz De-multiplexed Bus Interface Option**
- **0.5 µm, 3.3 V-Optimized Technology**
- **3.3 V I/O Capability with 5.0 V Input Tolerance**
- **160-pin MQFP Package**

1.2 Logic Symbol

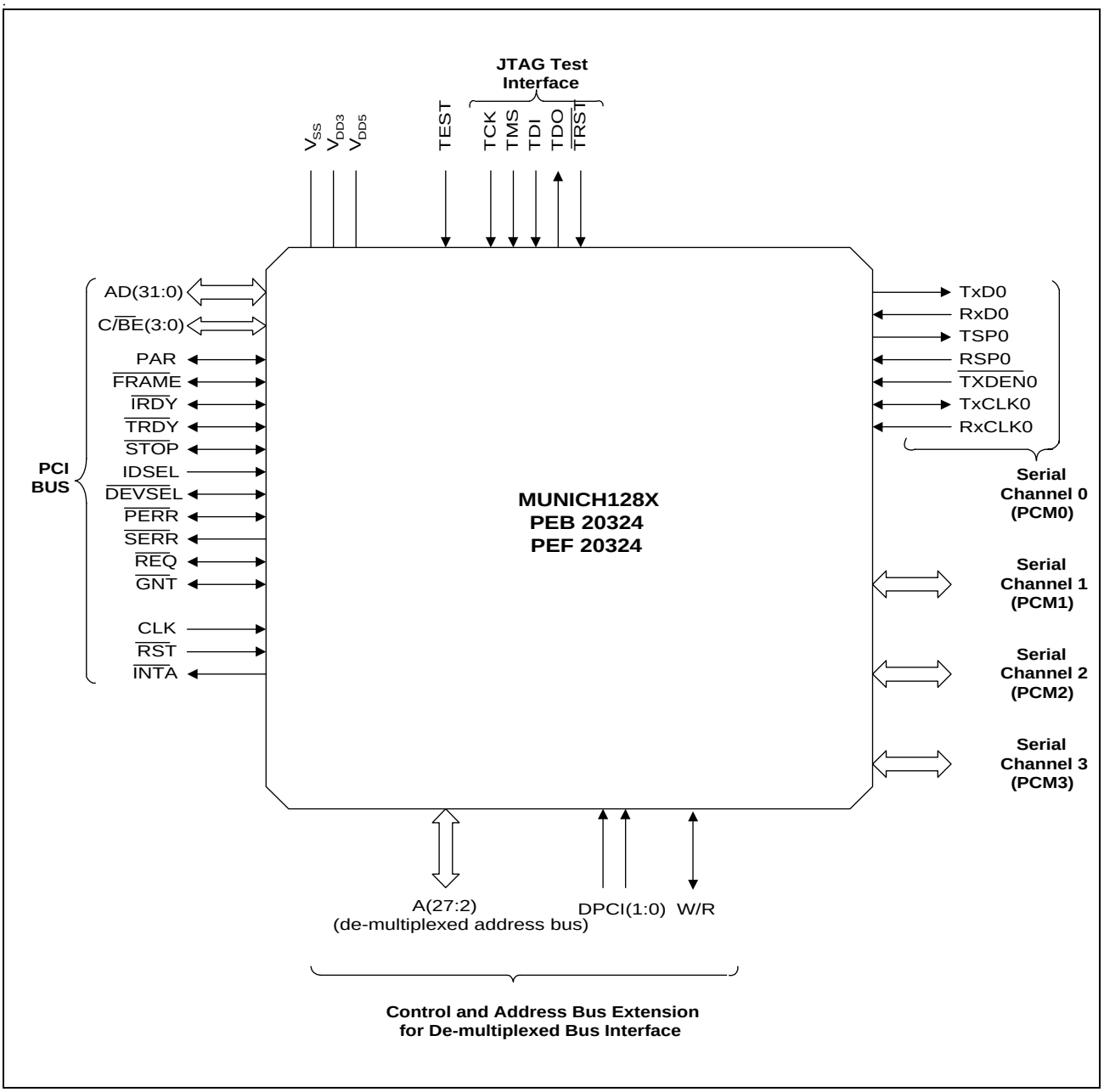


Figure 1-2 Logic Symbol

1.3 Typical Applications

The MUNICH128X provides protocol processing and host memory buffer management for four independent T1/E1 PRI ports. As such, the MUNICH128X fits into a system between the framer or LIU/framer devices (e.g., the Siemens FALC®54/FALC®54-LH transceiver) and the host bus (e.g. PCI Bus), as illustrated in Figure 1-3.

The MUNICH128X provides four independent Serial PCM ports which connect directly into the framer devices. In PCI based systems a dedicated microcontroller or PCI bridge chip is necessary to configure the framer or LIU/framer devices.

Additionally, the MUNICH128X provides a PCI 2.1 interface which connects directly to the system PCI bus. Optionally, this bus can be configured in De-multiplexed Mode.

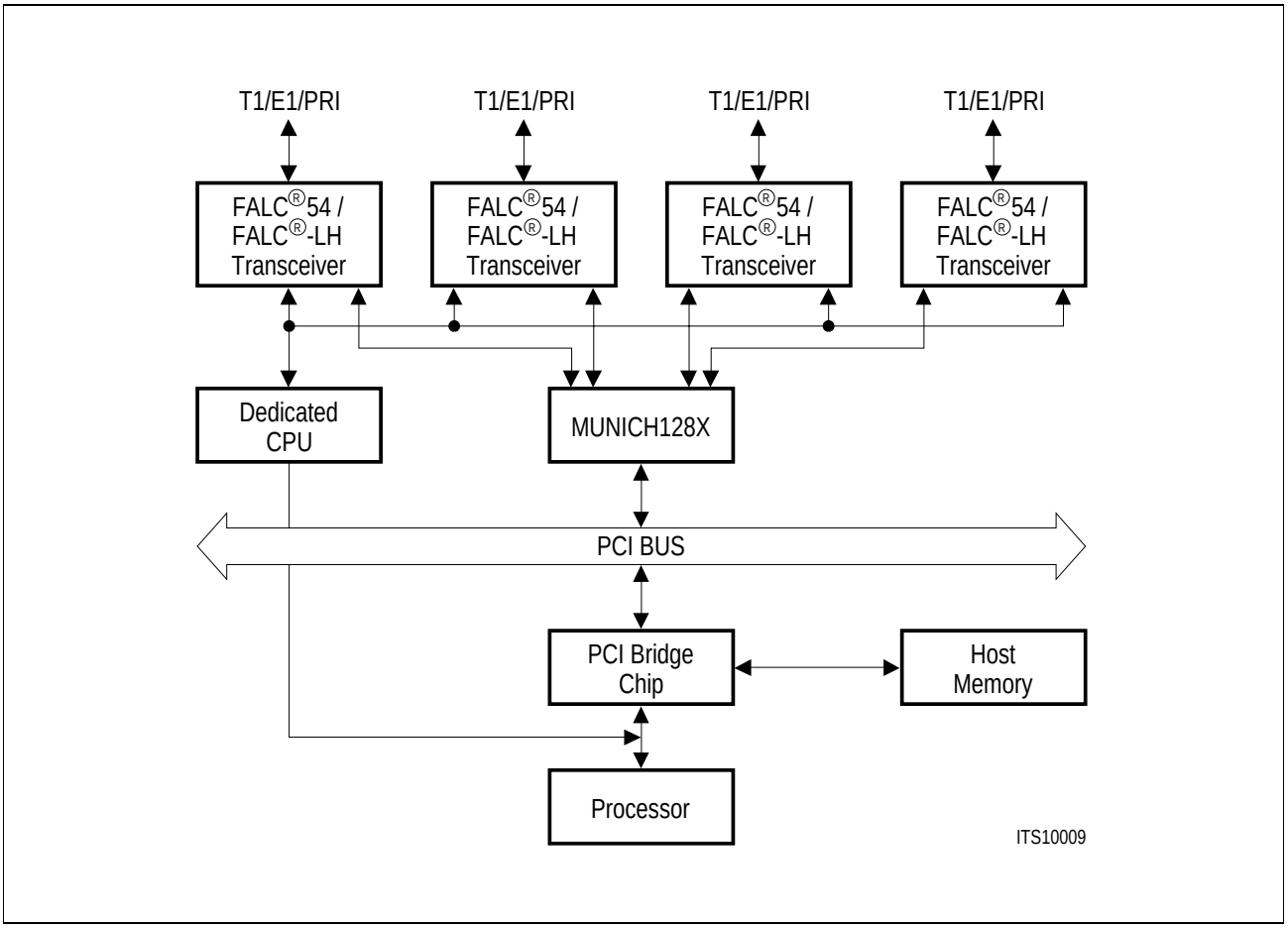


Figure 1-3 System Integration of the MUNICH128X in PCI-Based System

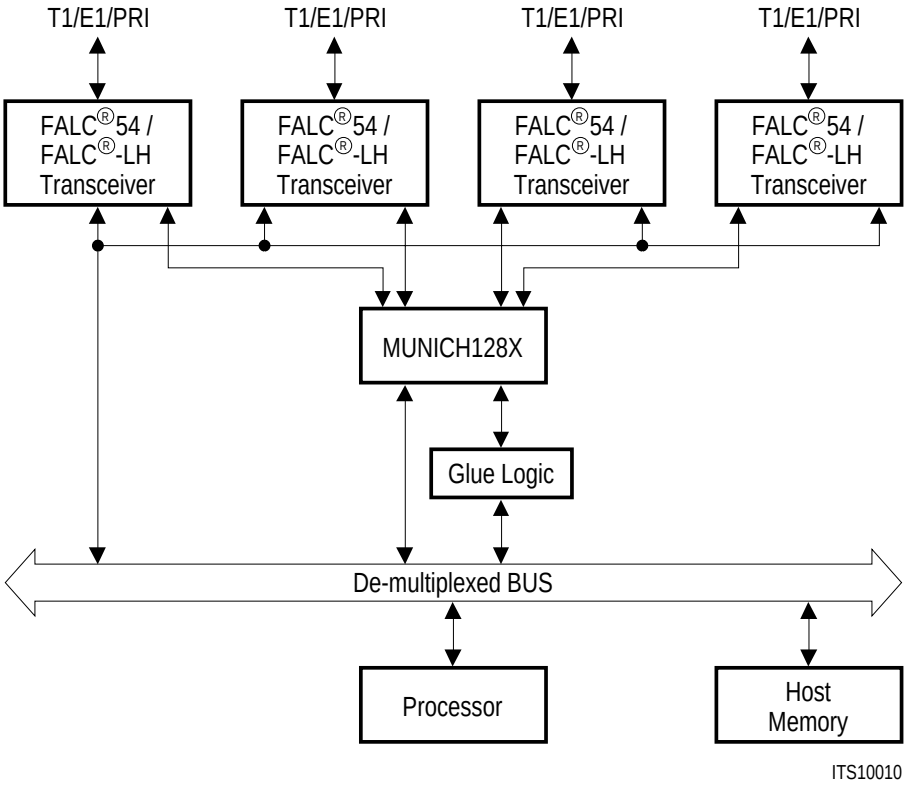


Figure 1-4 System Integration of the MUNICH128X in De-multiplexed System

1.4 Differences to the MUNICH32

- 128-channel capability
- Symmetrical Rx and Tx Buffer Descriptor formats for faster switching
- Improved Tx idle channel polling process for significantly reducing bus occupancy of idle Tx channels
- Dedicated 1024 byte Tx Buffer
- Dedicated 1024 byte Rx Buffer
- Burst capability also on transmit and receive data sections (8 DWORDs)
- Additional PCM modes supported: 3.088 MBit/s, 6.176 MBit/s, 8.192 MBit/s
- 32 Bit / 33 MHz PCI 2.1 master/slave interface;
  this interface can be configured in De-mux mode
- Separate Rx and Tx Status Queues in host memory
  (the MUNICH128X provides one set for each of the four HDLC Controllers)
- Slave access to on-chip registers
- Time Slot-shift capability:
  - Programmable from -4 clock edges to +3 clock edges
    relative to the synchronization pulse
  - Programmable to sample Tx and/or Rx data at either falling or rising edge of clock
- Software initiated action request (via the Command Register)
- Tx End-of-Packet transmitted-on-wire interrupt capability for each channel
- Tx packet size increased to 64 Kbytes (HDLC mode)
- Rx packet size 8 Kbyte limit interrupt disable
- Tx data TRISTATE^{TM} control line
- Synchronized data transfer in TMA mode
  for complete transparency when using fractional T1/PRI
- Little/Big Endian data formats

2 Pin Descriptions

2.1 Pin Diagram

(top view)

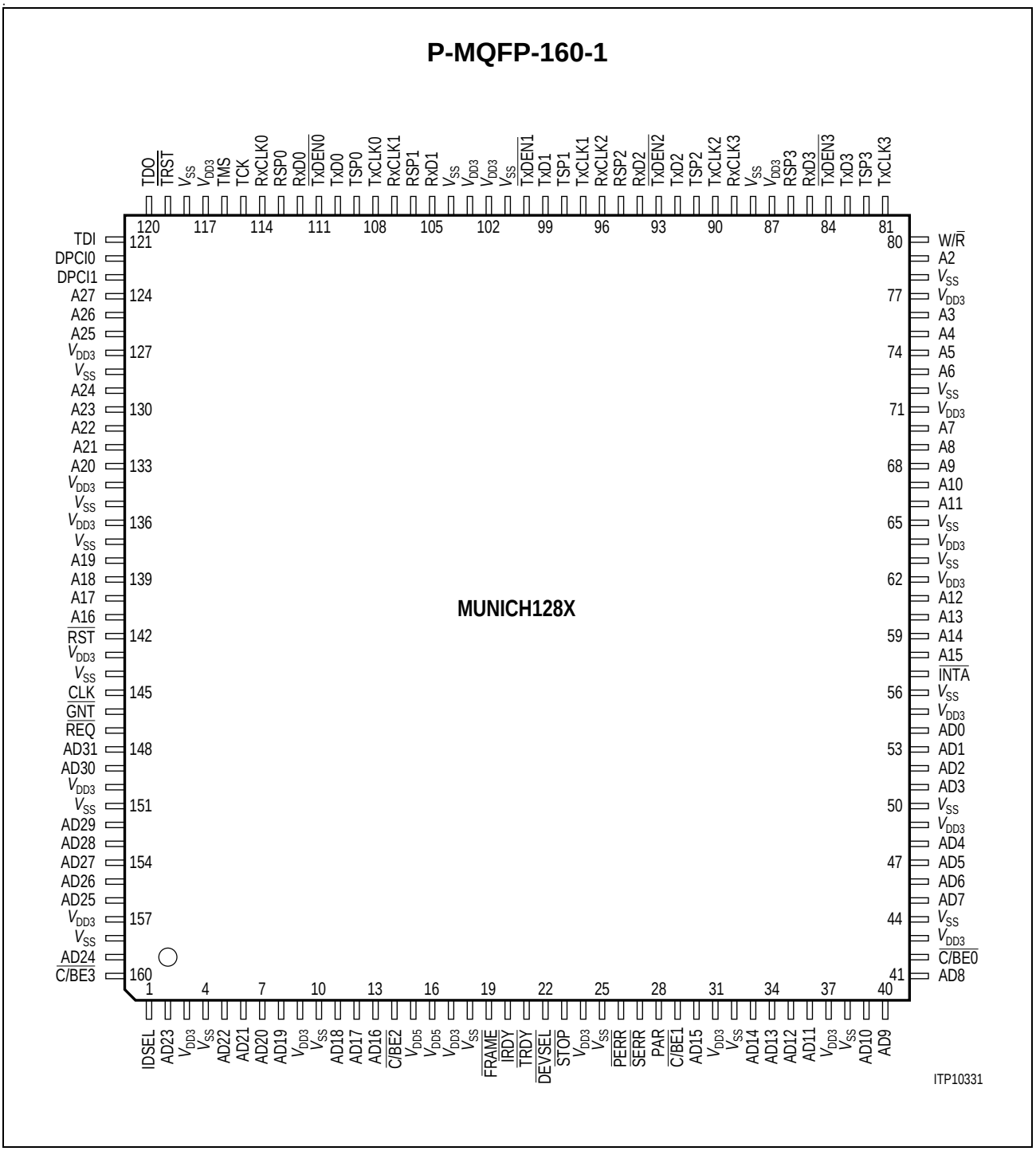


Figure 2-1 Pin Configuration

Pin descriptions in **Tables 2-1** to **2-8** are grouped by functional block, as shown by the heading for that group. Pin types are indicated by abbreviations:

Signal Type Definitions:

The following signal type definitions are partly taken from the PCI Specification Revision 2.1:

I	*Input* is a standard input-only signal.
O	*Totem Pole Output* is a standard active driver.
t/s, I/O	*Tri-State* or *I/O* is a bi-directional, tri-state input/output pin.
s/t/s	*Sustained Tri-State* is an active low tri-state signal owned and driven by one and only one agent at a time. (For further information refer to the PCI Specification Revision 2.1)
o/d	*Open Drain* allows multiple devices to share as a wire-OR. A pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.

Signal Name Conventions:

NC	*Not Connected Pin* Such pins are not bonded with the silicon. Although any potential at these pins will not impact the device it is recommended to leave them unconnected. NC pins might be used for additional functionality in later versions of the device. Leaving them unconnected will guarentee hardware compatibility to later device versions.
Reserved	*Reserved* pins are for vendor specific use only and should be connected as recommended to guarantee normal operation.

Note: The signal type definition specifies the functional usage of a pin. This does not reflect necessarily the implementation of a pin, e.g. a pin defined of signal type 'Input' may be implemented with a bidirectional pad.

Note: All unused input or I/O pins without internal Pull-Up/Down resistor must be connected to a defined level either connected to V_{DD3} /V_{SS} or to a Pull-Up/Down resistor (<= 10k).

Table 2-1 Pin Descriptions by Functional Block: Port 0 Serial Interface

Pin No.	Symbol	Type	Description
114	RxCLK0	I	**Receive Clock 0** The clock input pin used for sampling the data on RxD0. The MUNICH128X supports the following PCM clock rates; programmed via the MODE1 register: T1: 1.536 MHz, 1.544 MHz, 3.088 MHz, 6.176 MHz; E1: 2.048 MHz, 4.096 MHz, 8.192 MHz.
112	RxD0	I	**Receive Data 0** The data input pin which is sampled using RxCLK0.
113	RSP0	I	**Receive Synchronization Pulse 0** The input pin used for Rx PCM frame synchronization; the synchronization pulse marks the *first* bit in the PCM frame.
108	TxCLK0	I	**Transmit Clock 0** The clock input used for clocking out the data on TxD0. In most applications, the signal that drives this pin is externally connected to RxCLK0.
110	TxD0	O	**Transmit Data 0** Provides the data which is clocked out of the MUNICH128X by TxCLK0; data is push-pull for active bits in the PCM frame and TRISTATE™ for inactive bits.
109	TSP0	I	**Transmit Synchronization Pulse 0** The input pin used for Tx PCM frame synchronization; the synchronization pulse marks the *last* bit in the PCM frame.
111	$\overline{\text{TxDEN0}}$	O	**Transmit Data Enable 0** An active low output signal which specifies data on the TxD0 output pin is valid.

Table 2-2 Pin Descriptions by Functional Block: Port 1 Serial Interface

Pin No.	Symbol	Type	Description
107	RxCLK1	I	**Receive Clock 1** The clock input pin used for sampling the data on RxD1 The MUNICH128X supports the following PCM clock rates, programmed via the MODE1 register: T1: 1.536 MHz, 1.544 MHz, 3.088 MHz, 6.176 MHz; E1: 2.048 MHz, 4.096 MHz, 8.192 MHz.
105	RxD1	I	**Receive Data 1** The data input pin which is sampled using RxCLK1.
106	RSP1	I	**Receive Synchronization Pulse 1** The input pin used for Rx PCM frame synchronization; the synchronization pulse marks the *first* bit in the PCM frame.
97	TxCLK1	I	**Transmit Clock 1** The clock input used for clocking out the data on TxD1. In most applications, the signal that drives this pin is externally connected to RxCLK1.
99	TxD1	O	**Transmit Data 1** Provides the data which is clocked out of the MUNICH128X by TxCLK1; data is push-pull for active bits in the PCM frame and TRISTATE™ for inactive bits.
98	TSP1	I	**Transmit Synchronization Pulse 1** The input pin used for Tx PCM frame synchronization; the synchronization pulse marks the *last* bit in the PCM frame.
100	$\overline{\text{TxDEN1}}$	O	**Transmit Data Enable 1** An active low output signal which specifies data on the TxD1 output pin is valid.

Table 2-3 Pin Descriptions by Functional Block: Port 2 Serial Interface

Pin No.	Symbol	Type	Description
96	RxCLK2	I	**Receive Clock 2** The clock input pin used for sampling the data on RxD2. The MUNICH128X supports the following PCM clock rates, programmed via the MODE1 register: T1: 1.536 MHz, 1.544 MHz, 3.088 MHz, 6.176 MHz; E1: 2.048 MHz, 4.096 MHz, 8.192 MHz.
94	RxD2	I	**Receive Data 2** The data input pin which is sampled using RxCLK2.
95	RSP2	I	**Receive Synchronization Pulse 2** The input pin used for Rx PCM frame synchronization; the synchronization pulse marks the *first* bit in the PCM frame.
90	TxCLK2	I	**Transmit Clock 2** The clock input used for clocking out the data on TxD2. In most applications, the signal that drives this pin is externally connected to RxCLK2.
92	TxD2	O	**Transmit Data 2** Provides the data which is clocked out of the MUNICH128X by TxCLK2; data is push-pull for active bits in the PCM frame and TRISTATE™ for inactive bits.
91	TSP2	I	**Transmit Synchronization Pulse 2** The input pin used for Tx PCM frame synchronization; the synchronization pulse marks the *last* bit in the PCM frame.
93	$\overline{\text{TxDEN2}}$	O	**Transmit Data Enable 2** An active low output signal which specifies data on the TxD2 output pin is valid.

Table 2-4 Pin Descriptions by Functional Block: Port 3 Serial Interface

Pin No.	Symbol	Type	Description
89	RxCLK3	I	**Receive Clock 3** The clock input pin used for sampling the data on RxD3. The MUNICH128X supports the following PCM clock rates, programmed via the MODE1 register: T1: 1.536 MHz, 1.544 MHz, 3.088 MHz, 6.176 MHz; E1: 2.048 MHz, 4.096 MHz, 8.192 MHz.
85	RxD3	I	**Receive Data 3** The data input pin which is sampled using RxCLK3.
86	RSP3	I	**Receive Synchronization Pulse 3** The input pin used for Rx PCM frame synchronization; the synchronization pulse marks the *first* bit in the PCM frame.
81	TxCLK3	I	**Transmit Clock 3** The clock input used for clocking out the data on TxD3. In most applications, the signal that drives this pin is externally connected to RxCLK3.
83	TxD3	O	**Transmit Data 3** Provides the data which is clocked out of the MUNICH128X by TxCLK3; data is push-pull for active bits in the PCM frame and TRISTATE™ for inactive bits.
82	TSP3	I	**Transmit Synchronization Pulse 3** The input pin used for Tx PCM frame synchronization; the synch. pulse marks the *last* bit in the PCM frame.
84	$\overline{\text{TxDEN3}}$	O	**Transmit Data Enable 3** An active low output signal which specifies data on the TxD3 output pin is valid.

Table 2-5 Pin Descriptions by Functional Block: PCI Interface

Pin No.	Symbol	Type	Description
2, 5…8, 11…13, 30, 33…36, 39…41, 45…48, 51…54, 148, 149, 152…156, 159	AD(31:0)	t/s	**Address/Data Bus** A bus transaction consists of an address phase followed by one or more data phases. When MUNICH128X is Master, AD(31:0) are outputs in the address phase of a transaction. During the data phases, AD(31:0) remain outputs for write transactions, and become inputs for read transactions. When MUNICH128X is Slave, AD(31:0) are inputs in the address phase of a transaction. During the data phases, AD(31:0) remain inputs for write transactions, and become outputs for read transactions. AD(31:0) is sampled on the rising edge of CLK.
14, 29, 42, 160	$\overline{\text{C/BE}}$(3:0)	t/s	**Command/Byte Enable** During the address phase of a transaction, $\overline{\text{C/BE}}$(3:0) define the bus command. During the data phase, $\overline{\text{C/BE}}$(3:0) are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. $\overline{\text{C/BE0}}$ applies to byte 0 (lsb) and $\overline{\text{C/BE3}}$ applies to byte 3 (msb). When MUNICH128X is Master, $\overline{\text{C/BE}}$(3:0) are outputs. When MUNICH128X is Slave, $\overline{\text{C/BE}}$(3:0) are inputs. $\overline{\text{C/BE}}$(3:0) is sampled on the rising edge of CLK.
28	PAR	t/s	**Parity** PAR is even parity across AD(31:0) and $\overline{\text{C/BE}}$(3:0). PAR is stable and valid one clock after the address phase. PAR has the same timing as AD(31:0) but delayed by one clock. When MUNICH128X is Master, PAR is output during address phase and write data phases. When MUNICH128X is Slave, PAR is output during read data phases. Parity errors detected by the MUNICH128X are indicated on $\overline{\text{PERR}}$ output. PAR is sampled on the rising edge of CLK.

Table 2-5 Pin Descriptions by Functional Block: PCI Interface (cont'd)

Pin No.	Symbol	Type	Description
19	FRAME	s/t/s	**Frame** FRAME indicates the beginning and end of an access. FRAME is asserted to indicate a bus transaction is beginning. While FRAME is asserted, data transfers continue. When FRAME is deasserted, the transaction is in the final phase. When MUNICH128X is Master, FRAME is an output. When MUNICH128X is Slave, FRAME is an input. FRAME is sampled on the rising edge of CLK.
20	IRDY	s/t/s	**Initiator Ready** IRDY indicates the bus master's ability to complete the current data phase of the transaction. It is used in conjunction with TRDY. A data phase is completed on any clock where both IRDY and TRDY are sampled asserted. During a write, IRDY indicates that valid data is present on AD(31:0). During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are asserted together. When MUNICH128X is Master, IRDY is an output. When MUNICH128X is Slave, IRDY is an input. IRDY is sampled on the rising edge of CLK.
21	TRDY	s/t/s	**Target Ready** TRDY indicates a slave's ability to complete the current data phase of the transaction. During a read, TRDY indicates that valid data is present on AD(31:0). During a write, it indicates the target is prepared to accept data. When MUNICH128X is Master, TRDY is an input. When MUNICH128X is Slave, TRDY is an output. TRDY is sampled on the rising edge of CLK.
23	STOP	s/t/s	**STOP** STOP is used by a slave to request the current master to stop the current bus transaction. When MUNICH128X is Master, STOP is an input. When MUNICH128X is Slave, STOP is an output. STOP is sampled on the rising edge of CLK.

Table 2-5 Pin Descriptions by Functional Block: PCI Interface (cont'd)

Pin No.	Symbol	Type	Description
1	IDSEL	I	**Initialization Device Select** When MUNICH128X is slave in a transaction, if IDSEL is active in the address phase and C/BE(3:0) indicates a Config read or write, the MUNICH128X assumes a read or write to a configuration register. In response, the MUNICH128X asserts DEVSEL during the subsequent CLK cycle. IDSEL is sampled on the rising edge of CLK.
22	DEVSEL	s/t/s	**Device Select** When activated by a slave, it indicates to the current bus master that the slave has decoded its address as the target of the current transaction. If no bus slave activates DEVSEL within six bus CLK cycles, the master should abort the transaction. When MUNICH128X is Master, DEVSEL is input. If DEVSEL is not activated within six clock cycles after an address is output on AD(31:0), the MUNICH128X aborts the transaction and generates an INTA. When MUNICH128X is Slave, DEVSEL is output.
26	PERR	s/t/s	**Parity Error** When activated, indicates a parity error over the AD(31:0) and C/BE(3:0) signals (compared to the PAR input). It has a delay of one CLK cycle with respect to AD and C/BE(3:0) (i.e., it is valid for the cycle immediately following the corresponding PAR cycle). PERR is asserted relative to the rising edge of CLK.
27	SERR	o/d	**System Error** The MUNICH128X asserts this signal to indicate a fatal system error. SERR is sampled on the rising edge of CLK.
147	REQ	t/s	**Request** Used by the MUNICH128X to request control of the PCI. REQ is sampled on the rising edge of CLK.

Table 2-5 Pin Descriptions by Functional Block: PCI Interface (cont'd)

Pin No.	Symbol	Type	Description
146	$\overline{\text{GNT}}$	t/s	**Grant** This signal is asserted by the arbiter to grant control of the PCI to the MUNICH128X in response to a bus request via $\overline{\text{REQ}}$. After $\overline{\text{GNT}}$ is asserted, the MUNICH128X will begin a bus transaction only after the current bus Master has deasserted the $\overline{\text{FRAME}}$ signal. $\overline{\text{GNT}}$ is sampled on the rising edge of CLK.
145	CLK	I	**Clock** Provides timing for all PCI transactions. Most PCI signals are sampled or output relative to the rising edge of CLK. The maximum CLK frequency is 33 MHz.
142	$\overline{\text{RST}}$	I	**Reset** An active $\overline{\text{RST}}$ signal brings all PCI registers, sequencers and signals into a consistent state. All PCI output signals are driven to their initial state.
57	$\overline{\text{INTA}}$	O (o/d)	**Interrupt Request** When an interrupt status is active and unmasked, the MUNICH128X activates this open-drain output. Examples of interrupt sources are transmission/reception error, completion of transmit or receive packets etc. The MUNICH128X deactivates $\overline{\text{INTA}}$ when the global interrupt status register STAT is read. $\overline{\text{INTA}}$ is activated/deactivated asynchronous to the CLK.

Table 2-6 Pin Descriptions by Functional Block: DEMUX Interface (additional signals to PCI Interface)

Pin No.	Symbol	Type	Description
122, 123	DPCI(1:0)	I	**PCI/De-multiplexed Mode select** DPCI(1:0) = 00_2 : PCI Mode DPCI(1:0) = 01_2 : reserved DPCI(1:0) = 10_2 : PCI/De-multiplexed Mode DPCI(1:0) = 11_2 : reserved **Pins DPCI(1:0) should be connected to V_{DD3}/V_{SS} to achieve the appropriate mode selection.**
58…61, 66…70, 73…76, 79, **124**…126, 129…133, 138…141	A(27:2)	I/O	**DEMUX Address Bus** These pins provide the address bus for the De-multiplexed Interface, when DPCI(1:0) = 10_2. **Note:** Pin 124 ’A27’ provides a buffered PCI clock output signal if configured in PCI operation mode (DPCI(1:0) = ’00’).
80	W/$\overline{R}$	I/O	**Write/Read** This signal distinguishes write and read operations in the De-multiplexed mode. It is tristate when the MUNICH128X is in PCI mode. **A Pull-Up resistor to V_{DD3} is recommended if De-multiplexed mode is not used.**

Table 2-7 Pin Descriptions by Functional Block: Power Supply

Pin No.	Symbol	Type	Description
4, 10, 18, 25, 32, 38, 44, 50, 56, 63, 65, 72, 78, 88, 101, 104, 118, 128, 135, 137, 144, 151, 158	V_{SS}	-	**Ground (0 V)** All pins must have the same reference level.
3, 9, 17, 24, 31, 37, 43, 49, 55, 62, 64, 71, 77, 87, 102, 103, 117, 127, 134, 136, 143, 150, 157	V_{DD3}	-	**Supply Voltage (3.3 V ± 0.3 V)** All pins must have the same reference level.
15, 16	V_{DD5}	-	**Supply Voltage** **These pins MUST be connected to 5 V supply.** The MUNICH128X uses 3.3 V I/O pads that always require additional 5 V supply. The 5 V power supply allows the MUNICH128X I/O pads to provide 5 V input tolerance.

Table 2-8 Pin Descriptions by Functional Block: Test Interface

Pin No.	Symbol	Type	Description
115	TCK	I	JTAG Test Clock **A Pull-Up resistor to V_{DD3} is recommended if boundary scan unit is not used.**
116	TMS	I	JTAG Test Mode Select **A Pull-Up resistor to V_{DD3} is recommended if boundary scan unit is not used.**
121	TDI	I	JTAG Test Data Input **A Pull-Up resistor to V_{DD3} is recommended if boundary scan unit is not used.**
120	TDO	O	JTAG Test Data Output
119	$\overline{\text{TRST}}$	I	JTAG Reset **$\overline{\text{TRST}}$ should be connected to VSS if boundary scan unit is not used.**

3 Functional Description

3.1 Functional Overview

The MUNICH128X provides four independent “cores” as well as global functional blocks (see **Figure 3-1**).

3.2 Block Diagram

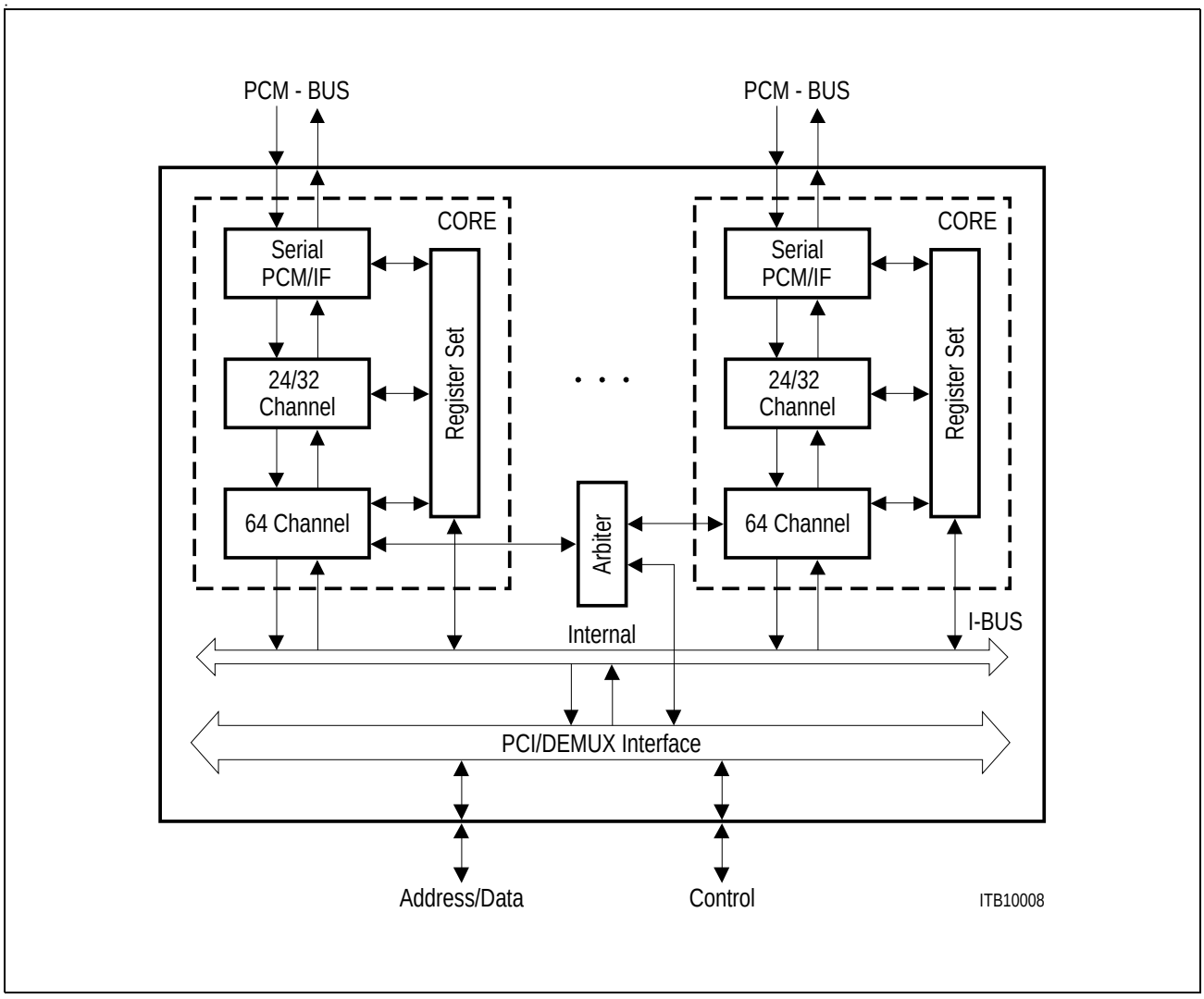


Figure 3-1 Block Diagram

3.3 Functional Blocks

Each core consists of dedicated circuitry: Serial PCM Interface Controller, Configuration and State RAM (CSR), 24/32-channel HDLC Controller with internal Transmit and Receive Buffers, 64-Channel DMA Controller, and Register Set.

3.3.1 Serial PCM Interface Controller

This block controls both Parallel–to-Serial (Tx) and Serial-to-Parallel (Rx) conversion and PCM timing. Additionally, this block controls the multiplexing of channels through the HDLC controller, as well as switching for the test loops.

3.3.2 Configuration and State RAM (CSR)

This block contains internal RAM which maintains the state of each channel. The Multiplex Control Block of the Serial PCM Interface Controller handles the switching of the CSR information into and out of the 24/32-channel HDLC Controller.

3.3.3 24/32-channel HDLC Controller

The HDLC Controller performs protocol processing for each channel independently, based on the CSR information for each channel.

3.3.3.1 Tx Block

Transmit Buffer (TB)

The Tx Block of the HDLC Controller contains a 1024 byte buffer (TB) which may be allocated to all 32 channels of one cove equally (i.e., 2-DWords per channel) or may be allocated based on superchannel considerations (e.g., 8–DWords per channel for 8 channels).

HDLC Protocol

Bit stuffing, flag generation, flag stuffing and adjustment, and CRC generation (either 16-bit or 32-bit) are performed.

V.110 and V.30 Protocol

Bit framing from 600 bit/s to 38.4 Kbit/s, automatic generation of the synchronization pattern, generation of loss of synchronization, programmable E/SX bits (including during run-time) are performed.

Transparent Mode A

This mode supports slot synchronous, transparent transmission without frame structure. It provides flag generation, flag stuffing, flag generation in the abort case with programmable flag, and synchronized data transfer for fractional T1/E1 PRI applications.

Transparent Mode B

This mode supports transparent transmission in frames delimited by 00_H flags, shared closing and opening flag, flag stuffing and flag generation in the abort case.

Transparent Mode R

This mode supports transparent transmission with GSM 08.60 frame structure with automatic 0000_H flag generation and support of 40, 39.5, and 40.5 octet frames.

Protocol Independence

Channel inversion (data, flags, idle code) follows the format conventions as in CCITT Q.921.

3.3.3.2 Rx Block

Receive Buffer (RB)

The Rx Block of the HDLC Controller contains a 1024 byte buffer (RB) which is allocated to channels via requests from the protocol controller, as determined by the received data for each channel.

HDLC Protocol

Flag detection (supports multiple flags between packets or a single flag shared as a closing flag and an opening flag between packets), abort character detection, idle code detection, zero-bit detection and deletion, packet length count, and CRC checking (either 16-bit or 32-bit) are performed.

V.110 and V.30 Protocol

Bit framing from 600 bit/s to 38.4 Kbit/s, automatic synchronization of the synchronization pattern, detection of loss of synchronization, programmable E/SX bits (including during run–time) are performed.

Transparent Mode A

Mode A supports slot synchronous transparent reception without frame structure. It provides flag detection, flag extraction and synchronized data transfer for fractional T1/ E1 PRI applications.

Transparent Mode B

This mode supports transparent reception in frames delimited by 00_H flags. Sharing closing flag and opening flag, and flag detection.

Transparent Mode R

This mode supports transparent reception with GSM 08.60 frame structure with automatic 0000_H flag detection. Support of 40, 39.5, and 40.5 octet frames, and error detection (non–octet frame contents, short frame, long frame).

Protocol Independence

Channel inversion (data, flags, idle code) follows the format conventions as in CCITT Q.921, data overflow and underflow detection.

3.3.3.3 64-channel DMA Controller Block

This block controls memory address calculation, buffer management (including linked-lists) and interrupt processing. The 24/32-channel HDLC Controller has a dedicated DMA channel for each channel and direction. During run-time, the DMA Controller performs operations with host memory primarily as a bus master. This block provides 32 input and 32 output channels.

3.3.3.4 Register Set

This block provides configuration and control of the Serial PCM Interface Controller, the HDLC Controller and the DMA Controller. Also, a shared status register STAT provides status and interrupt information associated with each of the four cores.

3.4 Global Functional Blocks

The MUNICH128X provides global functional blocks for the Internal Bus, Arbiter, and 32 Bit / 33 MHz PCI 2.1 Interface as well as De-multiplexed Bus Interface Controller.

3.4.1 Internal Bus

This block of the MUNICH128X interfaces the Bus Interface Controller to the four DMA Controllers. This is a 33 MHz, 32 Bit demultiplexed bus that operates in a synchronous, non–burst manner for data transfers and operates in a synchronous burst manner for descriptor transfers.

3.4.2 Arbiter

The Arbiter provides access control of the Internal Bus. A “round-robin” Arbiter is used which provides “fairness” for the four master DMA controllers.

3.4.3 32 Bit / 33 MHz Bus Interface Controller

The MUNICH128X may be configured either for 32 Bit / 33 MHz PCI bus operation or for a 32 Bit / 33 MHz De-multiplexed bus interface. The MUNICH128X input pins DPCI(1:0) are used to select the desired configuration.

The De-multiplexed bus interface is a synchronous interface very similar to the PCI interface with the following exceptions:

1. The W/$\overline{R}$ input/output signal replaces the function of the PCI command nibble of the C/BE(3:0) bit field.
2. Note, that in DEMUX mode as in PCI mode the MUNICH128X provides only the first address of a Master burst read or write transaction. If burst transactions are not supported by the local bus environment, burst capability can be disabled by bit DBE in the global configuration register (CONF).

3.5 System Integration

The MUNICH128X provides protocol processing and host memory buffer management for four independent T1/E1 PRI ports. As such, the MUNICH128X fits into a system between the framer or LIU/framer devices (e.g., the Siemens FALC®54/FALC®54-LH transceiver) and the host bus (e.g. PCI Bus), as illustrated in **Figure 3-1**.

The MUNICH128X provides four independent Serial PCM ports which connect directly into the framer devices. In PCI based systems a dedicated microcontroller or PCI bridge chip is necessary to configure the framer or LIU/framer devices.

Additionally, the MUNICH128X provides a PCI 2.1 interface which connects directly to the system PCI bus. Optionally, this bus can be configured in De-multiplexed Mode.

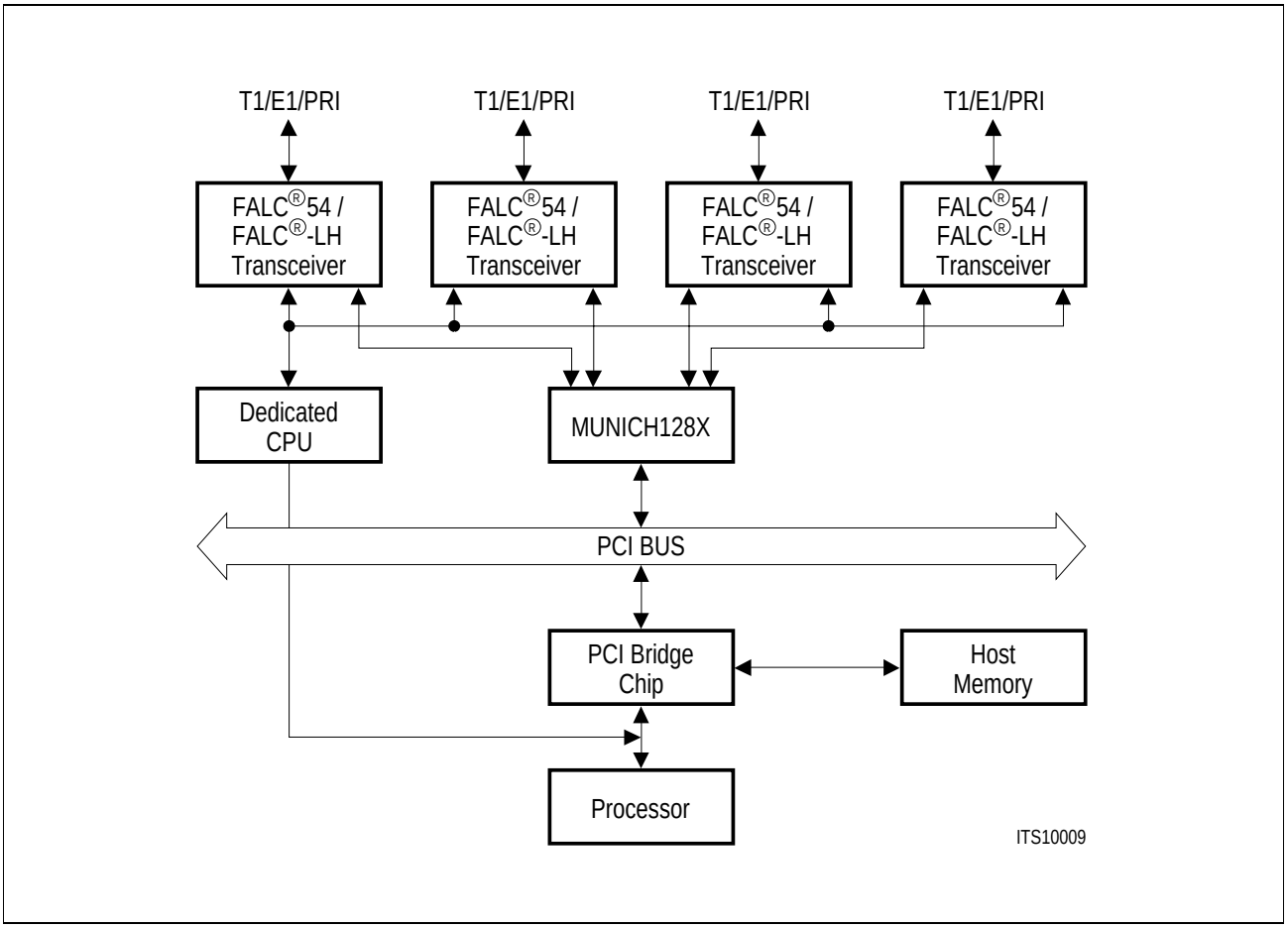


Figure 3-1 System Integration of the MUNICH128X in PCI-Based System

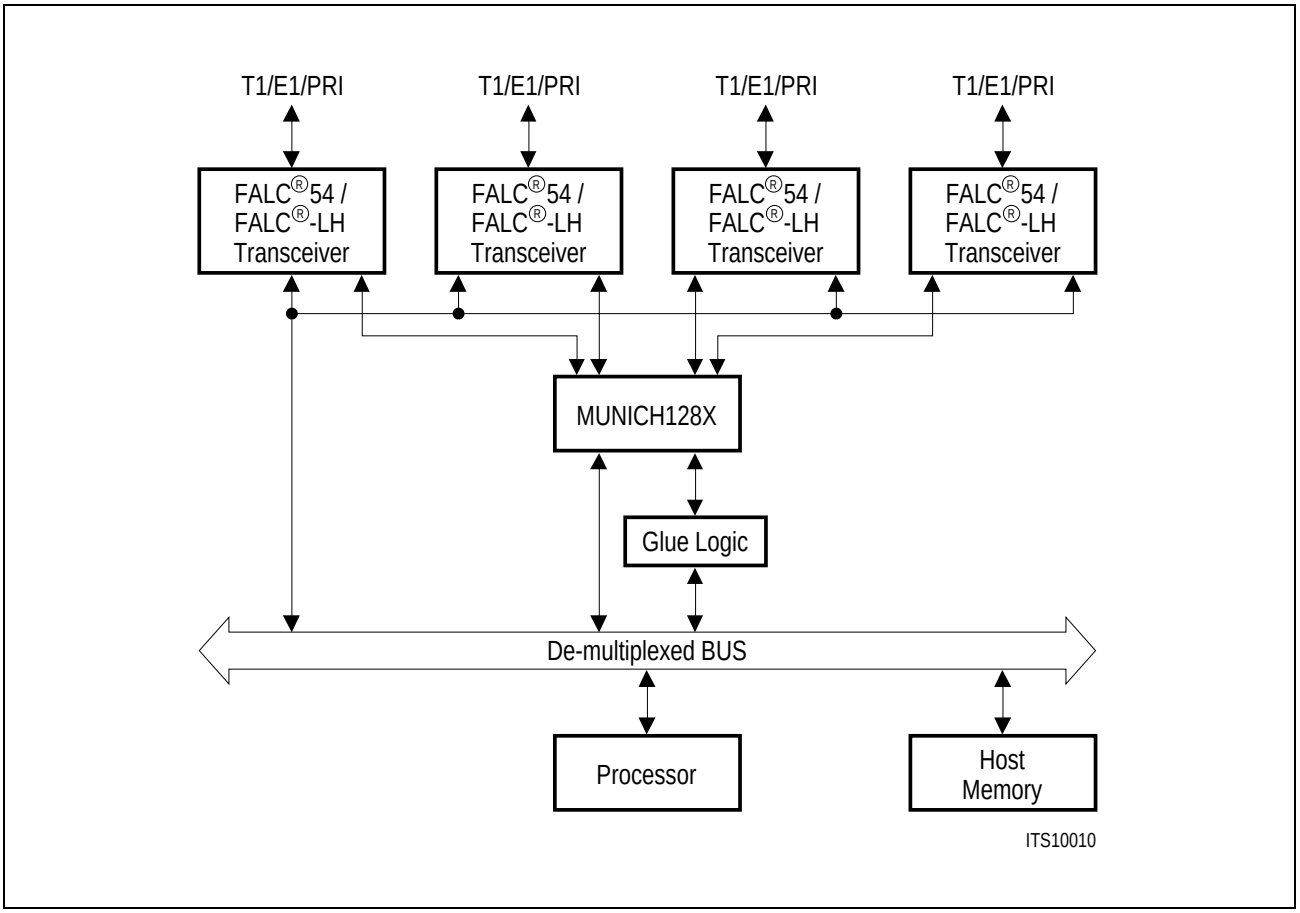


Figure 3-2 System Integration of the MUNICH128X in De-multiplexed System

4 Operational Description

4.1 Operational Overview

The MUNICH128X is a “channelized” WAN protocol controller that performs protocol processing on up to 128 full duplex serial PCM channels. It performs HDLC-based layer 2 protocol formatting and deformatting, as well as rate adaptation, for each of the 128 channels independently.

The MUNICH128X provides dedicated registers for each of the four HDLC controllers, with each set similar to the “core” registers of the MUNICH32X. Software developed for the “core” of the MUNICH32X requires minimal modification to run optimally on the MUNICH128X. The architecture of the register sets allows any number of HDLC controllers within an MUNICH128X device to operate with host software images that differ only in their offset from the PCI base address and their pointers into host memory.

Host software sets the operating mode, rate adaptation method and time slot assignment of each channel by configuring “blocks” (CCBs) within host memory.

During “run-time” the MUNICH128X performs all data and descriptor transfers as a bus master. Additionally, host software may access any register of a particular HDLC Controller within the MUNICH128X, with the device acting as a bus slave.

The MUNICH128X provides a single Status Register, which maintains information of all interrupt events for the controller.

5 Electrical Characteristics

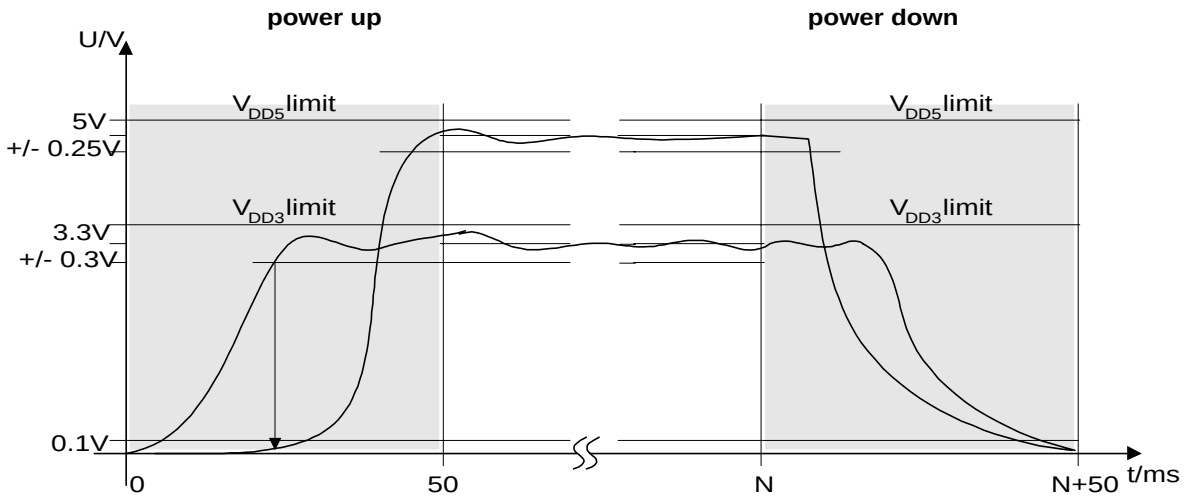
5.1 Important Electrical Requirements

V_{DD3} = 3.3 V ± 0.3 V **$V_{DD3\ max}$ = 3.6 V**

V_{DD5} = 5.0 V ± 0.25 V **$V_{DD5\ max}$ = 5.25 V**

During all MUNICH128X power-up and power-down situations the difference $|V_{DD5} - V_{DD3}|$ may not exceed 3.6V. The absolute maximums of V_{DD5} and V_{DD3} should never be exceeded.

Figure 5-1 shows that both V_{DD3} and V_{DD5} can take on any time sequence not exceeding a voltage difference of 3.6V, for up to 50 milliseconds at power-up and power-down.Within 50 milliseconds of power-up the voltages must be within their respective absolute voltage limits. At power-down, within 50 milliseconds of either voltage going outside its operational range, the voltage difference should not exceed 3.6V and both voltages must be returned below 0.1V:



Within the grey boxes any shape of V_{DD3} and V_{DD5} signal is allowed with the requirements that the absolute limits of each signal are not exceeded, the slew rate recommendation for V_{DD3} is met to guarantee proper boundary scan reset and the voltage difference does not exceed 3.6V.

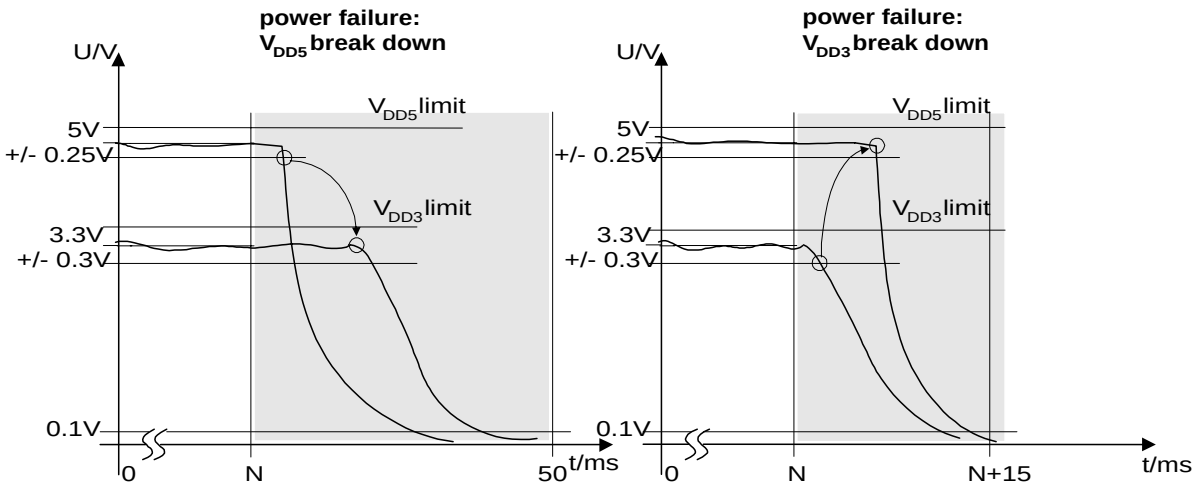
Outside the grey boxes the voltages provided to V_{DD3} and V_{DD5} should be inside the normal operation range.

In this power-up example V_{DD5} is enabled after V_{DD3} reached its minimum operation value which is a typical implementation.

For power-down V_{DD5} is switched off before V_{DD3}.

Figure 5-1 Power-up and Power-down scenarios

Similar criteria also apply to power down in case of power failure situations:



Within the grey boxes any shape of V_{DD3} and V_{DD5} signal is allowed with the requirements that the absolute limits of each signal are not exceeded and the specified voltage differences are not exceeded.

a. In case of V_{DD5} break-down the 3.6V difference is not exceeded anyway. The voltages must return below 0.1V within 50 milliseconds.
b. In case of V_{DD3} break-down the maximum voltage difference must not exceed 4.5 V for a maximum of 15 milliseconds.The voltages must return below 0.1V within 50 milliseconds.
This scenario is allowed for 2000 power failure cycles.

Figure 5-2 Power-Failure scenarios

5.2 Absolute Maximum Ratings

Table 5-1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Ambient temperature under bias *PEB* *PEF*	T_A	 0 -40	 70 85	°C
Junction temperature under bias	T_J		125	°C
Storage temperature	T_{stg}	– 65	125	°C
Voltage at any pin with respect to ground	V_S	– 0.4	V_{DD5} + 0.4	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$		1000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.
The RF Pins 20, 21, 26, 29, 32, 33, 34 and 35 are not protected against voltage stress > 300 V (versus V_S or GND). The high frequency performance prohibits the use of adequate protective structures.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.3 Thermal Package Characteristics

Table 5-2 Thermal Package Characteristics

Parameter		Symbol	Value	Unit
Thermal Package Resistance Junction to Ambient				
Airflow:	Ambient Temperature:			
without airflow	T_A=+25°C	$\theta_{JA(0,25)}$	29	°C/W

5.4 Operating Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature *PEB* *PEF*	T_A	 0 -40	 70 85	°C	
Supply voltage VDD3	V_{DD3}	3.0	3.6	V	
Supply voltage VDD5	V_{DD5}	4.75	5.25	V	
Ground	V_{SS}	0	0	V	

Note: In the operating range, the functions given in the circuit description are fulfilled.

5.5 DC Characteristics

a) Non-PCI Interface Pins

Table 5-3 Non-PCI Interface Pins
T_A = 0 to + 70°C; V_{DD5} = 5 V ± 5%, V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0 V

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
L-input voltage		V_{IL}	– 0.4	0.8	V	
H-input voltage		V_{IH}	2.0	V_{DD5} + 0.4	V	
L-output voltage		V_{QL}		0.45	V	I_{QL} = 7 mA (pin TXD) I_{QL} = 2 mA (all others / non-PCI)
H-output voltage		V_{QH}	2.4		V	I_{QH} = – 400 µA
Power supply current	operational	I_{CC3}		< 300	mA	V_{DD3} = 3.3 V, V_{DD5} = 5.0 V, inputs at 0 V/V_{DD3}, no output loads
	power down (no clocks)	I_{CC3}		< 5	mA	
	operational	I_{CC5}		< 1	mA	V_{DD3} = 3.3 V, V_{DD5} = 5.0 V, inputs at 0 V/V_{DD3}, no output loads
	power down (no clocks)	I_{CC5}		< 1	mA	
Peak Power supply current during RAM initialization process		$I_{CC3Peak}$		< 700	mA	V_{DD3} = 3.3 V, V_{DD5} = 5.0 V, inputs at 0 V/V_{DD3}, no output loads, 300 PCI clocks after power-up
		$I_{CC5Peak}$		< 10	mA	
Input leakage current Output leakage current		I_{LI} I_{LQ}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

*Note: The electrical characteristics described in **section 5.2** also apply here!*

b) PCI Pins

According to the PCI specification V2.1 from June 1, 1995
(Chapter 4: Electrical Specification for 5 V signalling)

Note: According the electrical characteristics all DEMUX Interface pins (DPCI(1:0), A(27:2), W/$\overline{R}$) are treated as PCI Interface pins.

5.6 Capacitances

a) Non-PCI Interface Pins

Table 5-4 Non-PCI Interface Pins
T_A = 25°C; V_{DD5} = 5 V ± 5%, V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input capacitance	C_{IN}	1	5	pF	
Output capacitance	C_{OUT}	5	10	pF	
I/O-capacitance	C_{IO}	6	15	pF	

b) PCI Pins

According to the PCI specification V2.1 from June 1, 1995
(Chapter 4: Electrical Specification for 5 V signalling)

Note: According the electrical characteristics all DEMUX Interface pins DPCI(1:0), A(27:2), W/$\overline{R}$) are treated as PCI Interface pins.

5.7 AC Characteristics

a) Non-PCI Interface Pins

T_A = 0 to + 70°C; V_{DD5} = 5 V ± 5%; V_{DD3} = 3.3 V ± 0.3 V

Inputs are driven to 2.4 V for a logical “1” and to 0.4 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and at 0.8 V for a logical “0”.

The AC testing input/output waveforms are shown below.

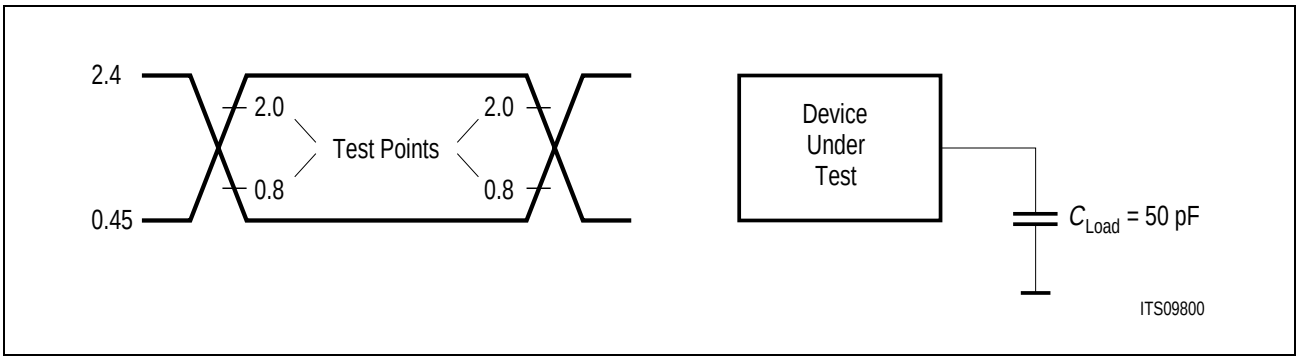


Figure 5-1 Input/Output Waveform for AC Tests

b) PCI Pins

According to the PCI specification V2.1 from June 1, 1995
(Chapter 4: Electrical Specification for 5 V signalling)

Note: According the electrical characteristics all DEMUX Interface pins DPCI(1:0), A(27:2), W/$\overline{R}$) are treated as PCI Interface pins.

5.7.1 PCI Bus Interface Timing

The AC testing input/output waveforms are shown in **figures 5-2** and **5-3** below.

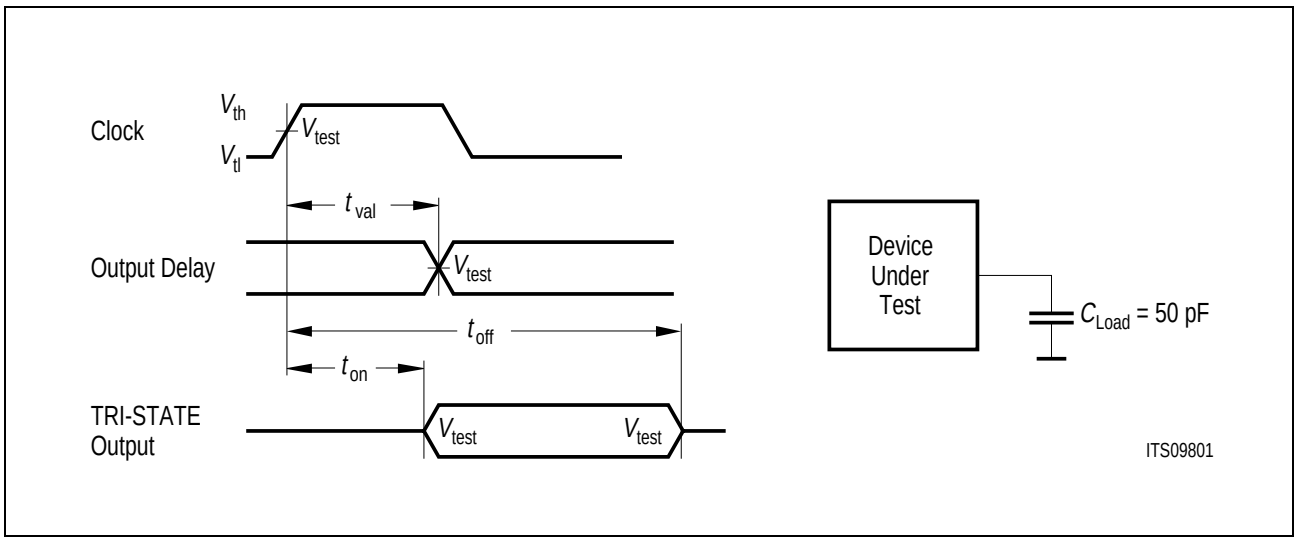


Figure 5-2 PCI Output Timing Measurement Waveforms

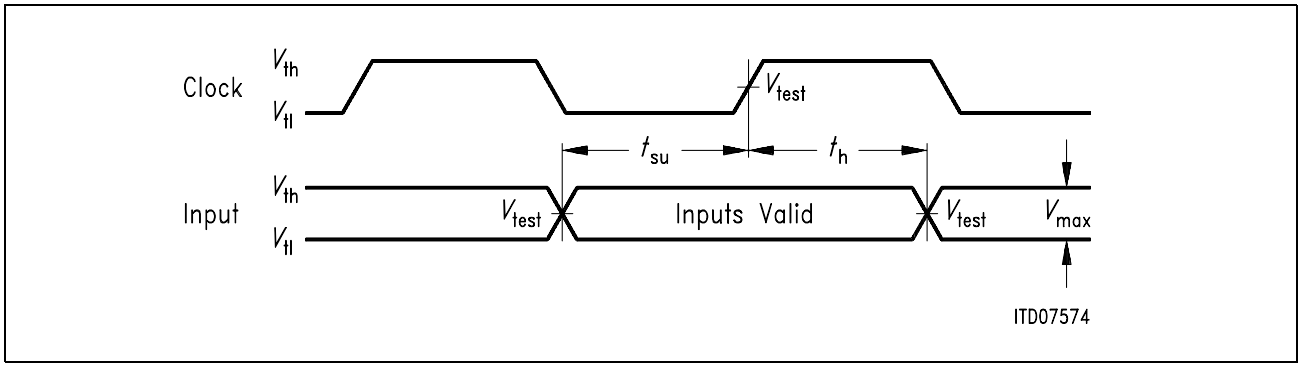


Figure 5-3 PCI Input Timing Measurement Waveforms

Table 5-5 PCI Input and Output Measurement Conditions

Symbol	Value	Unit
V_{th}	2.4	V
V_{tl}	0.4	V
V_{test}	1.5	V
V_{max}	2.0	V

The timings below show the basic read and write transaction between an initiator (Master) and a target (Slave) device. The MUNICH128X is able to work both as master and slave.

As a master the MUNICH128X reads/writes data from/to host memory using DMA and burst. The slave mode is used by an CPU to access the MUNICH128X PCI Configuration Space and the on-chip registers.

5.7.1.1 PCI Read Transaction

The transaction starts with an address phase which occurs during the first cycle when FRAME is activated (clock 2 in **figure 5-4**). During this phase the bus master (initiator) outputs a valid address on AD(31:0) and a valid bus command on C/BE(3:0). The first clock of the first data phase is clock 3. During the data phase C/BE indicate which byte lanes on AD(31:0) are involved in the current data phase.

The first data phase on a read transaction requires a turn-around cycle. In **figure 5-4** the address is valid on clock 2 and then the master stops driving AD. The target drives the AD lines following the turnaround when DEVSEL is asserted. (TRDY cannot be driven until DEVSEL is asserted.) The earliest the target can provide valid data is clock 4. Once enabled, the AD output buffers of the target stay enabled through the end of the transaction.

A data phase may consist of a data transfer and wait cycles. A data phase completes when data is transferred, which occurs when both IRDY and TRDY are asserted. When either is deasserted a wait cycle is inserted. In the example below, data is successfully transferred on clocks 4, 6 and 8, and wait cycles are inserted on clocks 3, 5 and 7. The first data phase completes in the minimum time for a read transaction. The second data phase is extended on clock 5 because TRDY is deasserted. The last data phase is extended because IRDY is deasserted on clock 7.

The Master knows at clock 7 that the next data phase is the last. However, the master is not ready to complete the last transfer, so IRDY is deasserted on clock 7, and FRAME stays asserted. Only when IRDY is asserted can FRAME be deasserted, which occurs on clock 8.

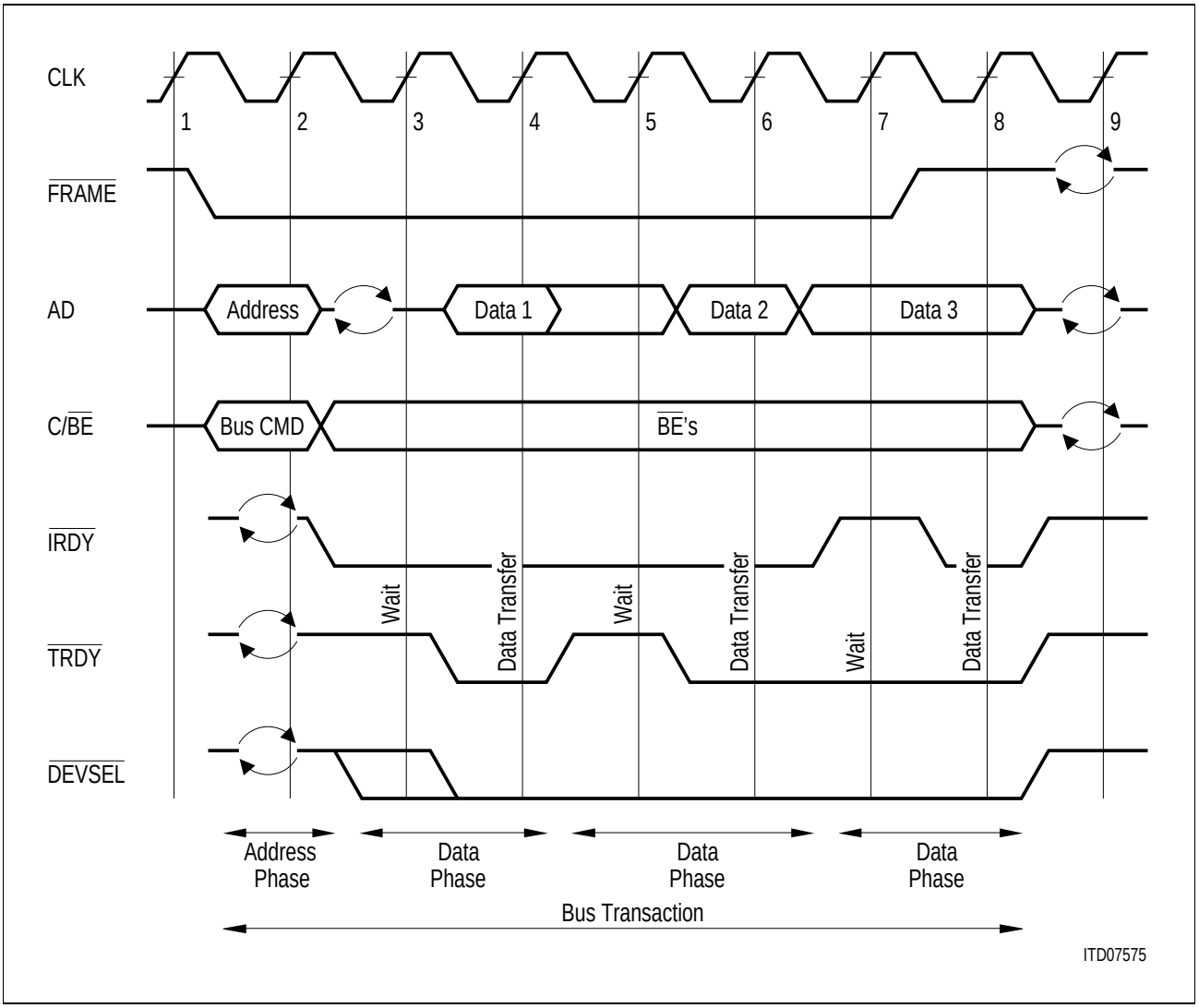


Figure 5-4 PCI Read Transaction

5.7.1.2 PCI Write Transaction

The transaction starts when FRAME is activated (clock 2 in **figure 5-5**). A write transaction is similar to a read transaction except no turnaround cycle is required following the address phase. In the example, the first and second data phases complete with zero wait cycles. The third data phase has three wait cycles inserted by the target. Both initiator and target insert a wait cycle on clock 5. In the case where the initiator inserts a wait cycle (clock 5), the data is held on the bus, but the byte enables are withdrawn. The last data phase is characterized by IRDY being asserted while the FRAME signal is deasserted. This data phase is completed when TRDY goes active (clock 8).

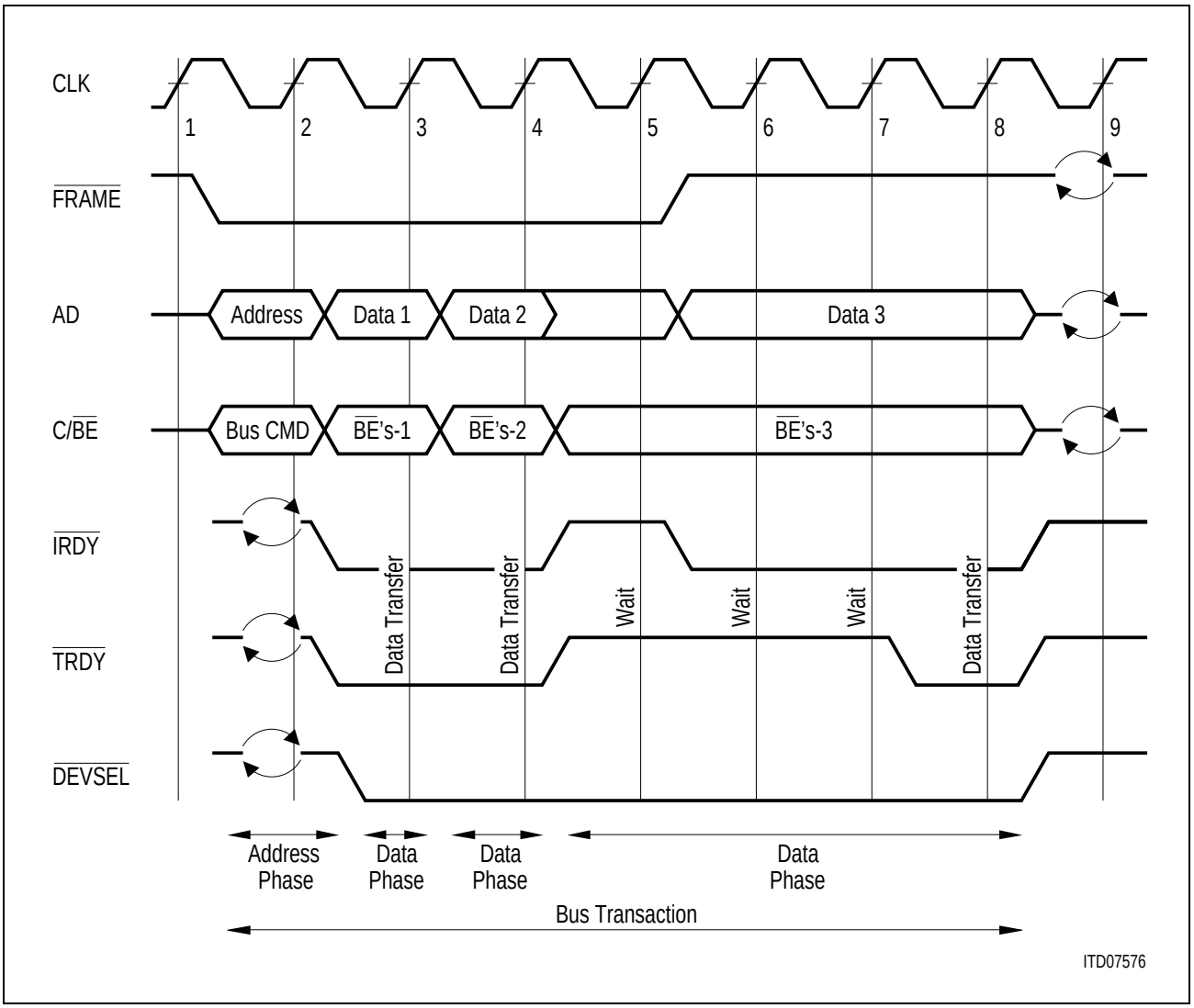


Figure 5-5 PCI Write Transaction

5.7.1.3 PCI Timing Characteristics

When the MUNICH128X operates as a PCI Master (initiator) and it either reads or writes a burst – as controlled by the on-chip DMA controller – it does not deactivate IRDY between consecutive data. In other words, no wait states are inserted by the MUNICH128X as a transaction initiator. The numbers of wait states, inserted by the MUNICH128X as initiator are listed in **table 5-6**.

Table 5-6 Number of Wait States Inserted by the MUNICH128X as Initiator

Transaction	Number of Wait States	
	1st Data Cycle	2nd and Subsequent Data Cycles
Memory read burst	0	0
Memory write burst	0	0
Fast Back-to-back burst; 1st transaction	0	0
Fast Back-to-back burst; 2nd and subsequent transactions	1	0

When the MUNICH128X operates as a PCI Slave (target), it inserts wait cycles by deactivating TRDY. The numbers of wait states, typically inserted by the MUNICH128X are listed in **table 5-6:**

Table 5-7 Number of Wait States Inserted by the MUNICH128X as Slave

Transaction	Number of Wait States
Configuration read	2
Configuration write	0
Register read	3
Register write	0
LBI read	3
LBI write	0

The number of wait states inserted by the MUNICH128X as target is not critical because accesses to the MUNICH128X are usually kept to a minimum in a system.

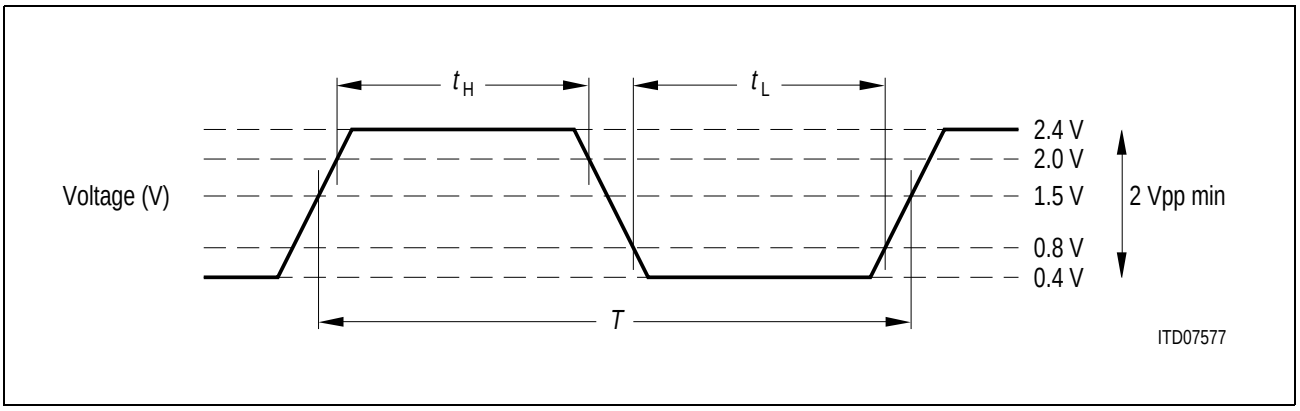


Figure 5-6 PCI Clock Specification

Table 5-8 PCI Clock Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
CLK cycle time	T	30			ns
CLK high time	t_H	11			ns
CLK low time	t_L	11			ns
CLK slew rate (see note)		1		4	V/ns

*Note: Rise and fall times are specified in terms of the edge rate measured in V/ns. This slew rate must be met across the minimum peak-to-peak portion of the clock waveform as shown in **figure 5-6**.*

Table 5-9 PCI Interface Signal Characteristics

Parameter	Limit Values			Unit	Remarks
	min.	typ.	max.		
CLK to signal valid delay bussed signals	(2)		11	ns	Notes 1, 2
CLK to signal valid delay point-to-point	(2)		12	ns	Notes 1, 2
Float to active delay	2		(3)	ns	
Active to float delay			20	ns	
Input setup time to CLK bussed signals	7			ns	Note 2
Input setup time to CLK point-to-point	10			ns	Note 2
Input hold time from CLK	0			ns	

Note 1Minimum times are measured with 0 pF equivalent load; maximum times are measured with 50 pF equivalent load.

Note 2$\overline{REQ}$ and $\overline{GNT}$ are point-to-point signals. All other signals are bussed $\overline{GNT}$ setup (min) time: 10ns

5.7.2 De-multiplexed Bus Interface

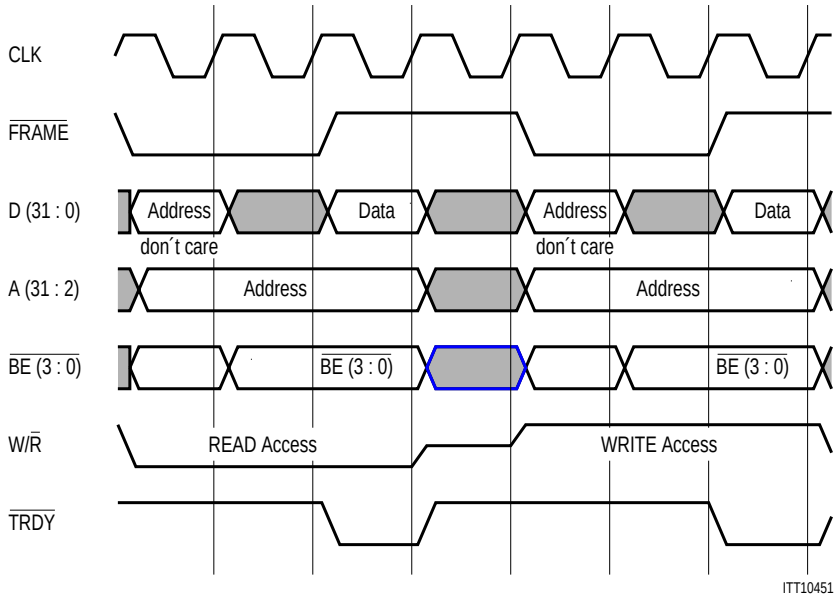


Figure 5-7 Master Single READ Transaction followed by a Master Single WRITE Transaction in De-multiplexed Bus Configuration

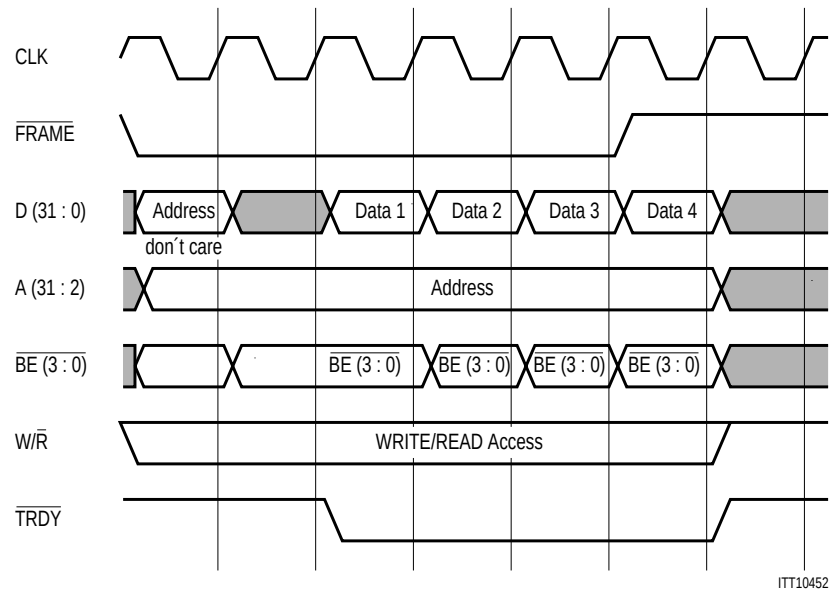


Figure 5-8 Master Burst WRITE/READ Access in De-multiplexed Bus Configuration

The timing provided in **Table 5-7** and **Table 5-8** can also be applied to the de-multiplexed bus interface.

Table 5-10 Additional De-multiplexed Interface Signal Characteristics

Parameter	Limit Values			Unit	Remarks
	min.	typ.	max.		
CLK to address bus signal valid delay			12	ns	
CLK to W/$\overline{R}$ signal valid delay			12	ns	
Address bus Input setup time to CLK	8			ns	
Address bus Input hold time to CLK	0			ns	
W/$\overline{R}$ signal Input setup time to CLK	8			ns	
W/$\overline{R}$ signal Input hold time to CLK	0			ns	

Note: The PCI parity signal PAR is not generated in de-multiplexed mode. It is driven active low by the MUNICH128X.

5.7.3 PCM Serial Interface Timing

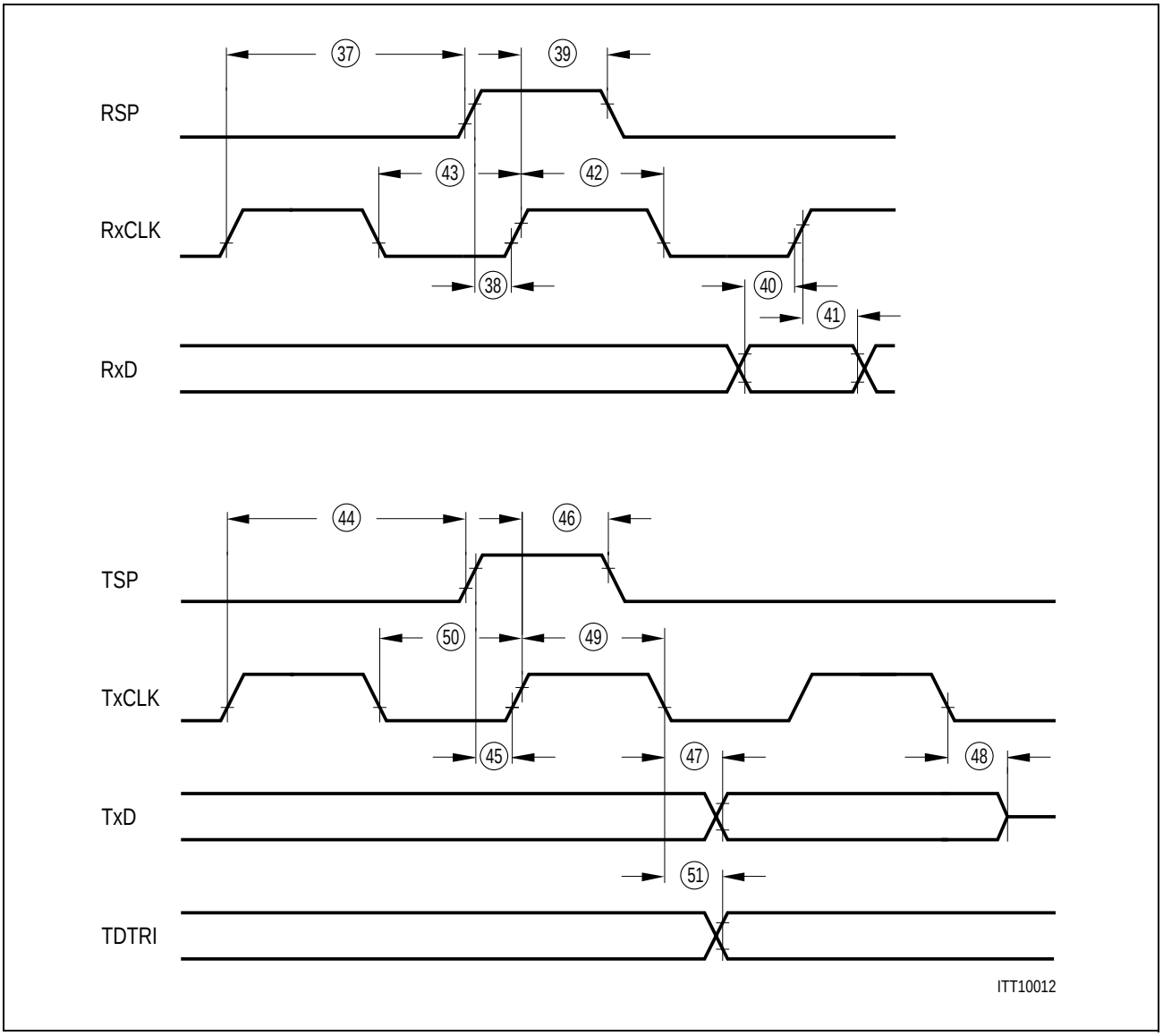


Figure 5-9 PCM Serial Interface Timing

Table 5-11 PCM Serial Interface Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
37	Receive strobe guard time	10		ns
38	Receive strobe setup	5		ns
39	Receive strobe hold	5		ns
40	Receive data setup	5		ns
41	Receive data hold	5		ns
42	Receive clock high width	30		ns
43	Receive clock low width	30		ns
44	Transmit strobe guard time	20		ns
45	Transmit strobe setup	5		ns
46	Transmit strobe hold	5		ns
47	Transmit data delay		25	ns
48	Transmit clock to high impedance		25	ns
49	Transmit clock high width	30		ns
50	Transmit clock low width	30		ns
51	Transmit tristate delay	25		ns

*Note: The frequency on the serial line **must** be smaller or equal to*
$^1/_8{}^{th}$ of the frequency on the µP bus for 1.536 MHz, 1.544 MHz, 2.048 MHz
$^1/_4{}^{th}$ of the frequency on the µP bus for 4.096 MHz.

Note: For complete internal or complete external loop t_{42} and t_{49} must be greater or equal to 3 times T.

5.7.4 System Interface Timing

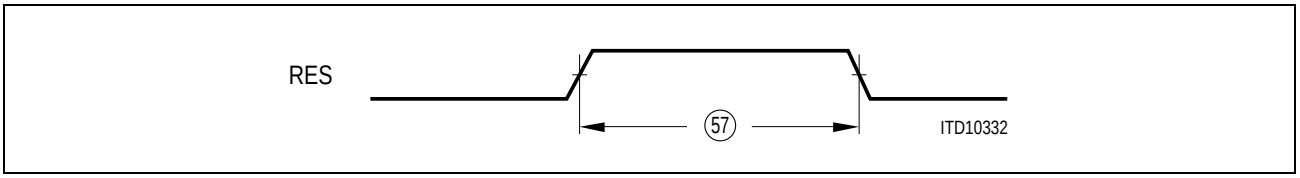


Figure 5-10 System Interface Timing

Table 5-12 System Interface Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
57	RESET pulse width	4 CLK cycles		

5.7.5 JTAG-Boundary Scan Timing

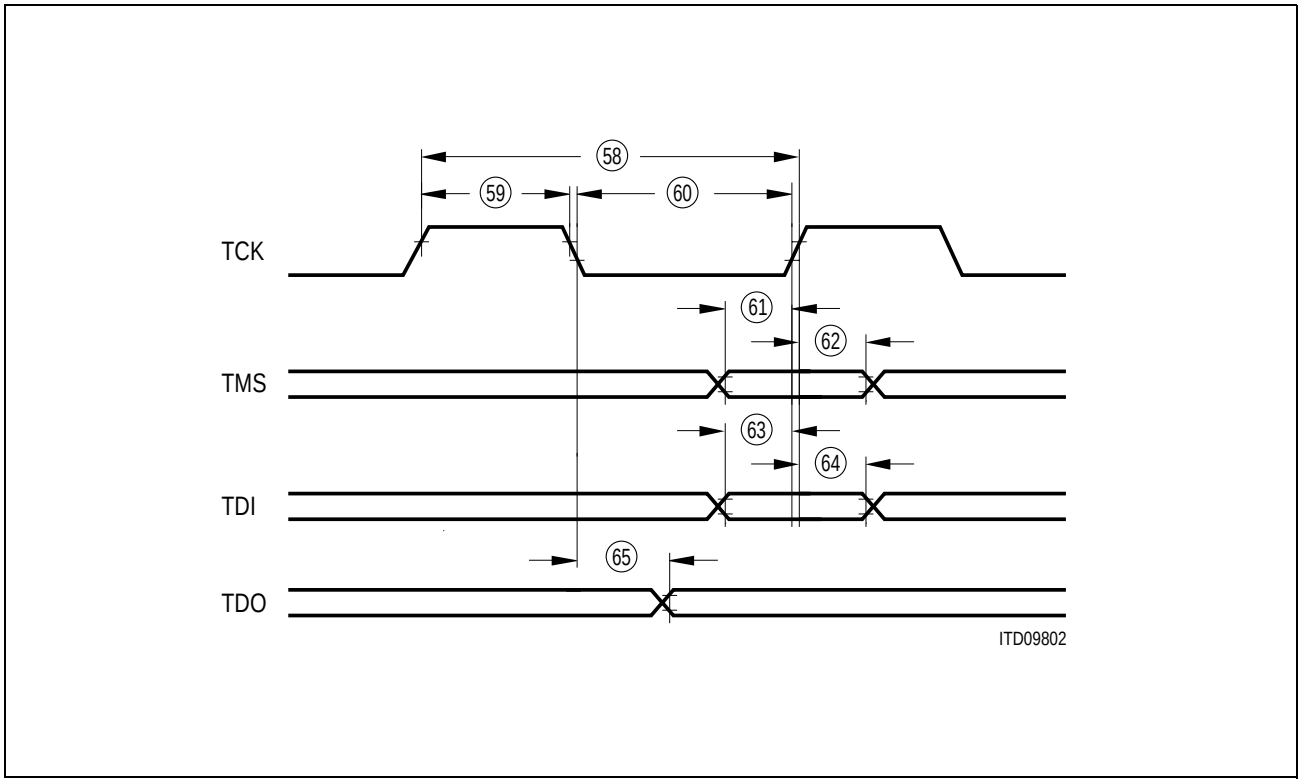


Figure 5-11 JTAG-Boundary Scan Timing

Table 5-13 JTAG-Boundary Scan Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
58	TCK period	166	∞	ns
59	TCK high time	80		ns
60	TCK low time	80		ns
61	TMS setup time	30		ns
62	TMS hold time	10		ns
63	TDI setup time	30		ns
64	TDI hold time	30		ns
65	TDO valid delay	60		ns

6 Test Modes

6.1 Boundary Scan Unit

In the MUNICH128X a Test Access Port (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard: IEEE 1149.1. **Figure 6-1** gives an overview.

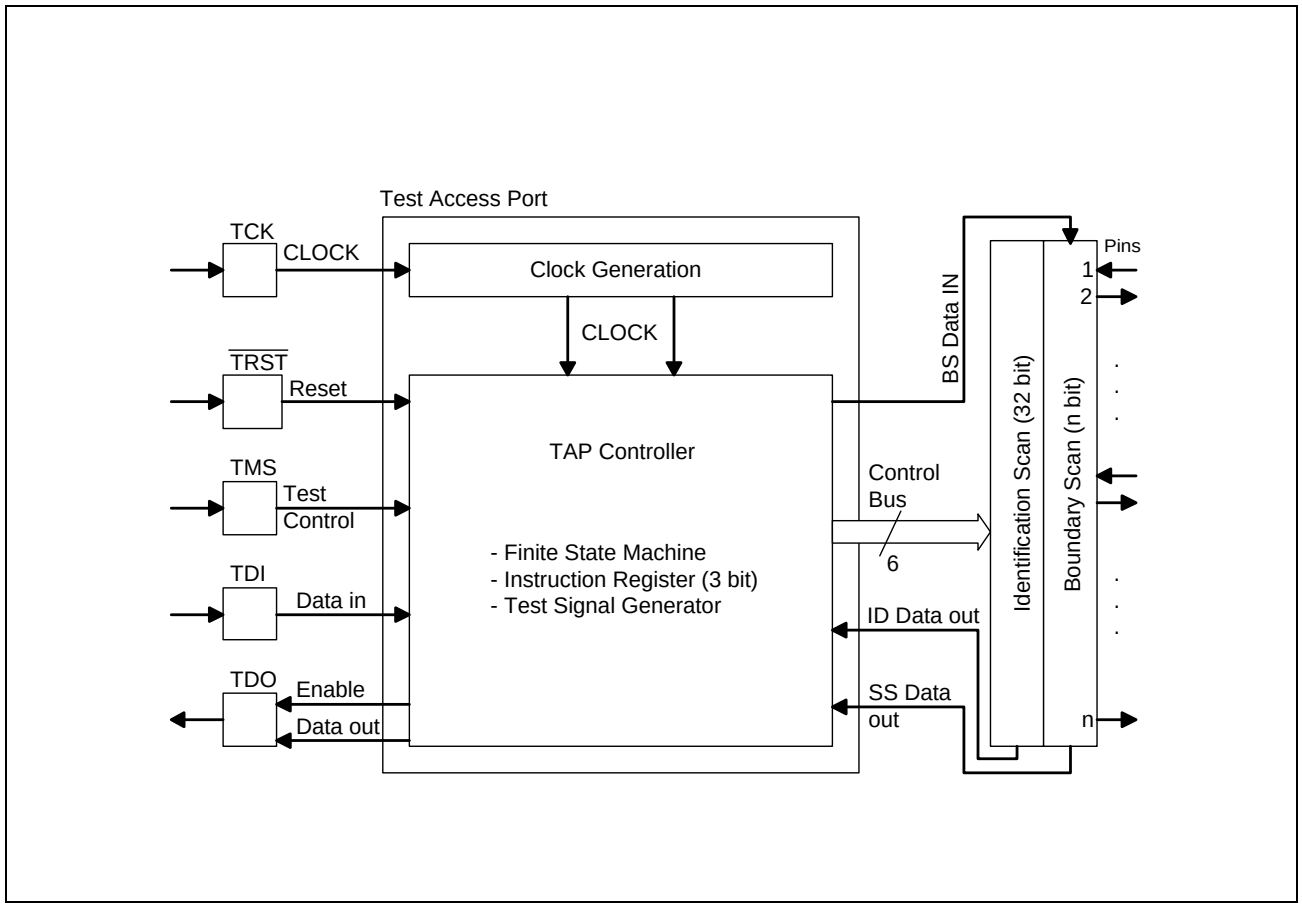


Figure 6-1 Block Diagram of Test Access Port and Boundary Scan

If no boundary scan operation is planned $\overline{\text{TRST}}$ has to be connected with V_{SS}. TMS and TDI do not need to be connected since pull-up transistors ensure high input levels in this case. Nevertheless it would be a good practice to put the unused inputs to defined levels. In this case, if the JTAG is not used:
TMS = TCK = '1' is recommended.

Test handling (boundary scan operation) is performed via the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output) when the TAP controller is not in its reset state, i.e. $\overline{\text{TRST}}$ is connected to V_{DD} or it remains unconnected due to its internal pull-up. Test data at TDI are loaded with a 4-MHz clock

signal connected to TCK. ‘1’ or ‘0’ on TMS causes a transition from one controller state to another; constant ’1’ on TMS leads to normal operation of the chip.

Table 6-1 Boundary Scan Sequence in MUNICH128X

TDI ->

Seq. No.	Pin	I/O	Number of Boundary Scan Cells	Constant Value In, Out, Enable
1	DPCI0	I	1	**0**
2	DPCI1	I	1	**0**
3	A27	I/O	3	**011**
4	A26	I/O	3	**000**
5	A25	I/O	3	**000**
6	A24	I/O	3	**100**
7	A23	I/O	3	**000**
8	A22	I/O	3	**001**
9	A21	I/O	3	**000**
10	A20	I/O	3	**010**
11	A19	I/O	3	**000**
12	A18	I/O	3	**110**
13	A17	I/O	3	000
14	A16	I/O	3	000
15	$\overline{\text{RST}}$	I/O	3	000
16	CLK	I	1	0
17	$\overline{\text{GNT}}$	I/O	3	000
18	$\overline{\text{REQ}}$	I/O	3	000
19	AD31	I/O	3	000
20	AD30	I/O	3	000
21	AD29	I/O	3	000
22	AD28	I/O	3	000
23	AD27	I/O	3	000
24	AD26	I/O	3	000
25	AD25	I/O	3	000

Seq. No.	Pin	I/O	Number of Boundary Scan Cells	Constant Value In, Out, Enable
26	AD24	I/O	3	000
27	$\overline{\text{C/BE3}}$	I/O	3	000
28	IDSEL	I/O	3	000
29	AD23	I/O	3	000
30	AD22	I/O	3	000
31	AD21	I/O	3	000
32	AD20	I/O	3	000
33	AD19	I/O	3	000
34	AD18	I/O	3	000
35	AD17	I/O	3	000
36	AD16	I/O	3	000
37	$\overline{\text{C/BE2}}$	I/O	3	000
38	$\overline{\text{FRAME}}$	I/O	3	000
39	$\overline{\text{IRDY}}$	I/O	3	000
40	$\overline{\text{TRDY}}$	I/O	3	000
41	$\overline{\text{DEVSEL}}$	I/O	3	000
42	$\overline{\text{STOP}}$	I/O	3	000
43	$\overline{\text{PERR}}$	I/O	3	000
44	$\overline{\text{SERR}}$	I/O	3	000
45	PAR	I/O	3	000
46	$\overline{\text{C/BE1}}$	I/O	3	000
47	AD15	I/O	3	000
48	AD14	I/O	3	000
49	AD13	I/O	3	000
50	AD12	I/O	3	000
51	AD11	I/O	3	000
52	AD10	I/O	3	000
53	AD9	I/O	3	000
54	AD8	I/O	3	000
55	$\overline{\text{C/BE0}}$	I/O	3	000

Seq. No.	Pin	I/O	Number of Boundary Scan Cells	Constant Value In, Out, Enable
56	AD7	I/O	3	000
57	AD6	I/O	3	000
58	AD5	I/O	3	000
59	AD4	I/O	3	000
60	AD3	I/O	3	000
61	AD2	I/O	3	000
62	AD1	I/O	3	000
63	AD0	I/O	3	000
64	$\overline{\text{INTA}}$	I/O	3	000
65	A15	I/O	3	000
66	A14	I/O	3	000
67	A13	I/O	3	000
68	A12	I/O	3	000
69	A11	I/O	3	000
70	A10	I/O	3	000
71	A9	I/O	3	000
72	A8	I/O	3	000
73	A7	I/O	3	000
74	A6	I/O	3	000
75	A5	I/O	3	000
76	A4	I/O	3	000
77	A3	I/O	3	000
78	A2	I/O	3	000
79	$\overline{\text{WR}}$	I/O	3	000
80	TCLK3	I	1	0
81	TSP3	I	1	0
82	TD3	I/O	3	000
83	$\overline{\text{TDEN3}}$	I/O	3	000
84	RD3	I	1	0
85	RSP3	I	1	0

Seq. No.	Pin	I/O	Number of Boundary Scan Cells	Constant Value In, Out, Enable
86	RCLK3	I	1	0
87	TCLK2	I	1	0
88	TSP2	I	1	0
89	TD2	I/O	3	000
90	$\overline{\text{TDEN2}}$	I/O	3	000
91	RD2	I	1	0
92	RSP2	I	1	0
93	RCLK2	I	1	0
94	TCLK1	I	1	0
95	TSP1	I	1	0
96	TD1	I/O	3	000
97	$\overline{\text{TDEN1}}$	I/O	3	000
98	RD1	I	1	0
99	RSP1	I	1	0
100	RCLK1	I	1	0
101	TCLK0	I	1	0
102	TSP0	I	1	0
103	TD0	I/O	3	000
104	$\overline{\text{TDEN0}}$	I/O	3	000
105	RD0	I	1	0
106	RSP0	I	1	0
107	RCLK0	I	1	0
	-> TDO			

An input pin (I) uses one boundary scan cell (data in), an output pin (O) uses two cells (data out, enable) and an I/O-pin (I/O) uses three cells (data in, data out, enable). Note that some output and input pins of the MUNICH128X are tested as I/O pins in boundary scan, hence using three cells. The boundary scan unit of the MUNICH128X contains a total of n = 275 scan cells.

The right column of **Table 6-1** gives the initialization values of the cells.

The desired test mode is selected by serially loading a 3-bit instruction code into the instruction register via TDI (LSB first); see **Table 6-2.**

Table 6-2 Boundary Scan Test Modes

Instruction (Bit 2 … 0)	Test Mode
000	EXTEST (external testing)
001	INTEST (internal testing)
010	SAMPLE/PRELOAD (snap-shot testing)
011	IDCODE (reading ID code)
111	BYPASS (bypass operation)
others	handled like BYPASS

EXTEST is used to examine the interconnection of the devices on the board. In this test mode at first all input pins **capture** the current level on the corresponding external interconnection line, whereas all output pins are held at constant values (‘0’ or ‘1’, according to **Table 6-1**). Then the contents of the boundary scan is **shifted** to TDO. At the same time the next scan vector is loaded from TDI. Subsequently all output pins are **updated** according to the new boundary scan contents and all input pins again capture the current external level afterwards, and so on.

INTEST supports internal testing of the chip, i.e. the output pins **capture** the current level on the corresponding internal line whereas all input pins are held on constant values (‘0’ or ‘1’, according to **Table 6-1**). The resulting boundary scan vector is **shifted** to TDO. The next test vector is serially loaded via TDI. Then all input pins are **updated** for the following test cycle.

Note: In capture IR-state the code ‘001’ is automatically loaded into the instruction register, i.e. if INTEST is wanted the shift IR-state does not need to be passed.

SAMPLE/PRELOAD is a test mode which provides a snap-shot of pin levels during normal operation.

IDCODE: A 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to ‘1’.

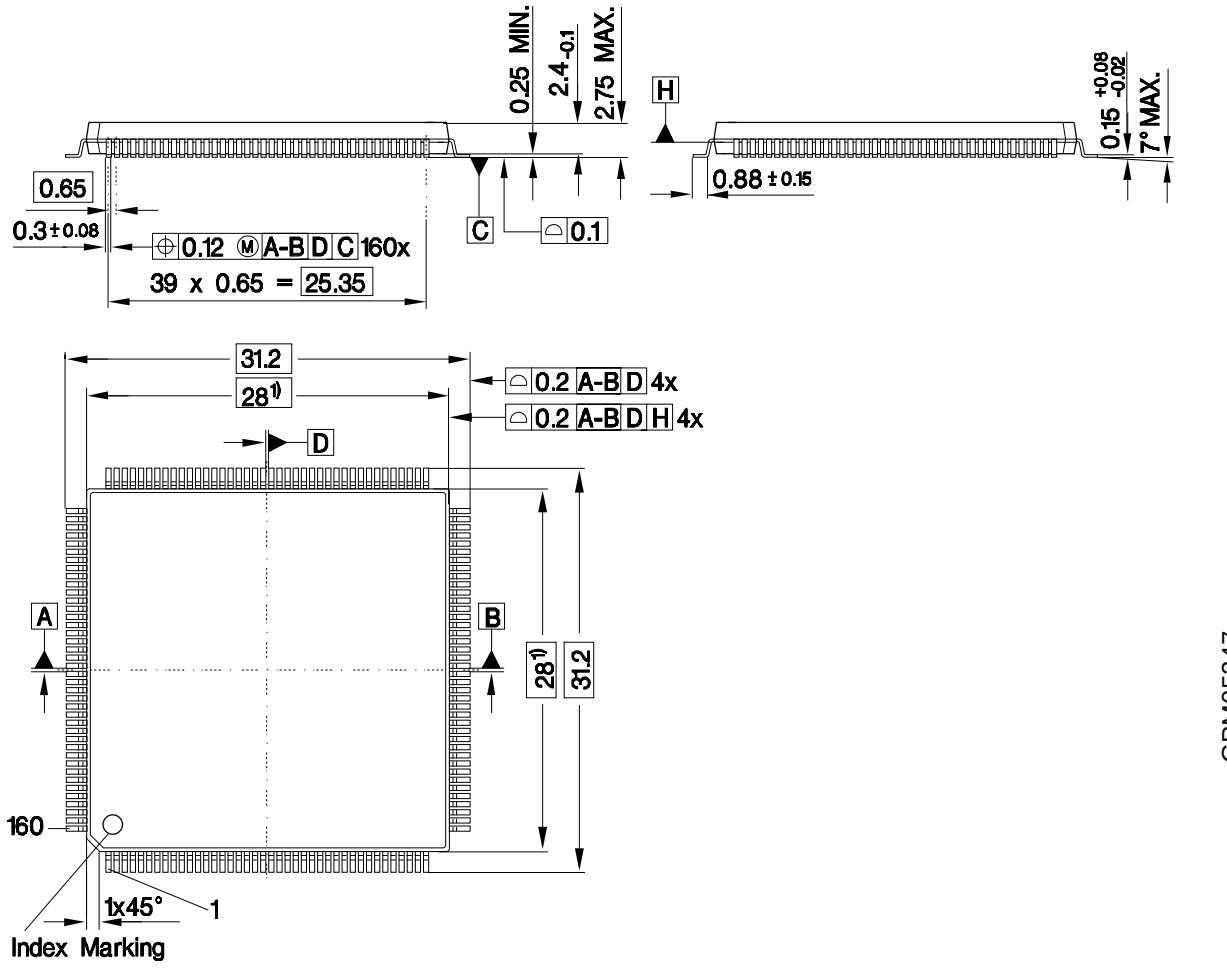
TDI ->	**0011**	0000 0000 0100 0100	0000 1000 001	1	-> TDO

Note: Since in test logic reset state the code ‘011’ is automatically loaded into the instruction register, the ID code can easily be read out in shift DR state which is reached by TMS = 0, 1, 0, 0.

BYPASS: A bit entering TDI is shifted to TDO after one TCK clock cycle.

7 Package Outlines

P-MQFP-160-1
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm