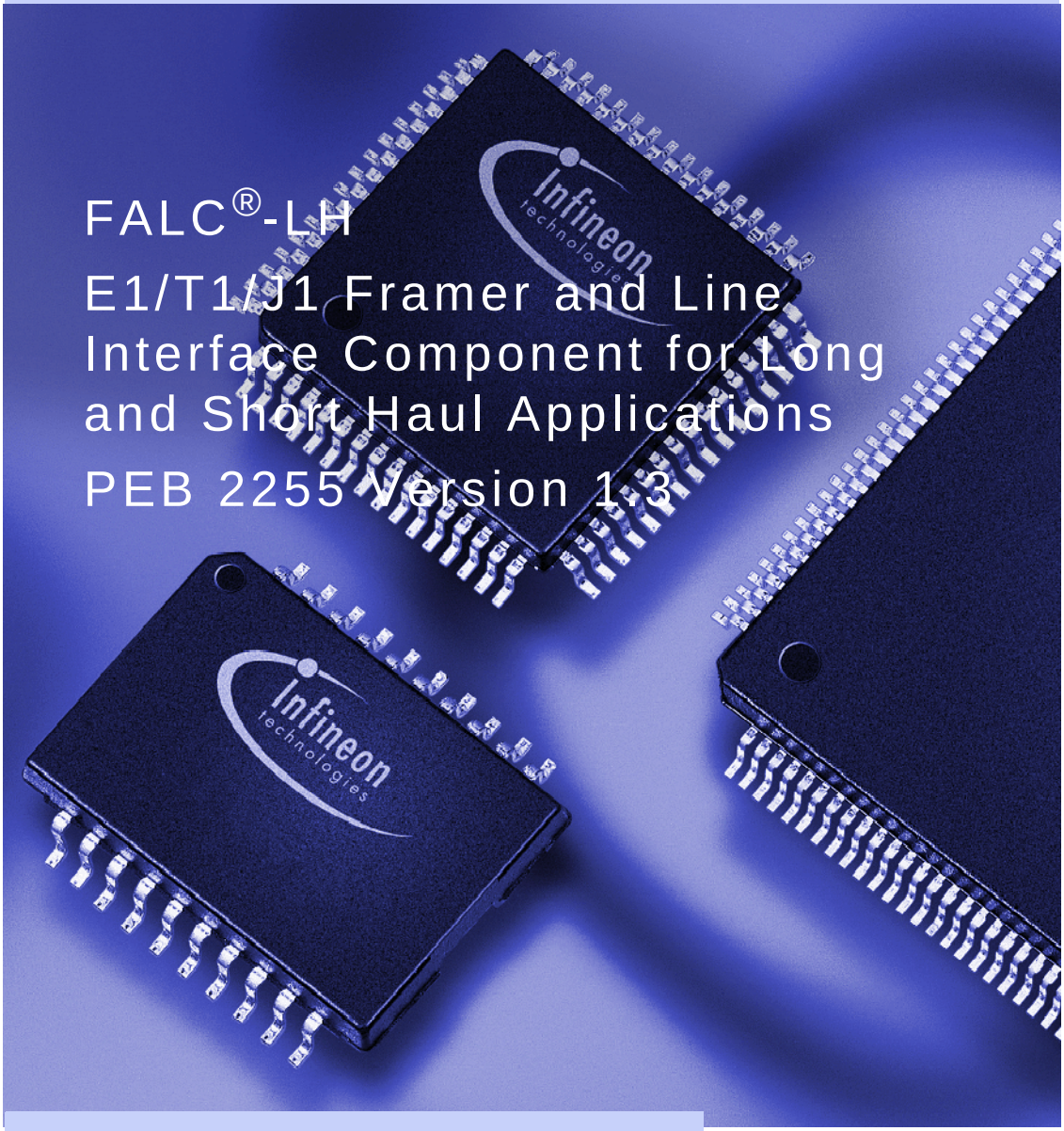
Data Sheet, DS 1, July 2000



FALC®-LH

E1/T1/J1 Framer and Line Interface Component for Long and Short Haul Applications

PEB 2255 Version 1.3

Datacom

Infineon technologies

Never stop thinking.

Edition 2000-07

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
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Revision History:	**2000-07**	DS 1
Previous Version:	Preliminary Data Sheet DS1	

Page	Subjects (major changes since last revision)

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Preface

The FALC®-LH framer and line interface component is designed to fulfill all required interfacing between an analog E1/T1/J1 line and the digital PCM system highway/H.100 bus.

The digital functions as well as the analog characteristics are configured via a flexible microprocessor interface.

Organization of this Document

This Data Sheet is organized as follows:

- **Chapter 1**, **Introduction**
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- **Chapter 2**, **Pin Descriptions**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3** to **Chapter 5**, **Functional Description E1/T1/J1**
  These chapters describe the functional blocks and principle operation modes, organized into separate sections for E1 and T1/J1 operation

- **Chapter 6** and **Chapter 7**, **Operational Description E1/T1/J1**
  Shows the operation modes and how they are to be initialized (separately for E1 and T1/J1).

- **Chapter 8**, **Signaling Controller Operating Modes**
  Describes signaling controller functions for both E1 and T1/J1 operation.

- **Chapter 9** and **Chapter 10**, **E1 Registers** and **T1/J1 Registers**
  Gives a detailed description of all implemented registers and how to use them in different applications/configurations.

- **Chapter 11**, **Electrical Characteristics**
  Specifies maximum ratings, DC and AC characteristics.

- **Chapter 12**, **Package Outlines**
  Shows the mechanical values of the device package.

- **Chapter 13**, **Appendix**
  Gives an example for overvoltage protection and information about application notes and other support.

- **Chapter 14**, **Glossary**

- **Index**

Related Documentation

This document refers to the following international standards (in alphabetical/numerical order):

ANSI/EIA-656
ANSI T1.102
ANSI T1.403
AT&T PUB 43802
AT&T PUB 54016
AT&T PUB 62411
ESD Ass. Standard EOS/ESD-5.1-1993
ETSI ETS 300 011
ETIS ETS 300 166
ETSI ETS 300 233
ETSI ETS 300 324
ETSI ETS 300 347
ETSI TBR12
ETSI TBR13
FCC Part68
GR-253-CORE
GR-499-CORE
GR-1089-CORE
H.100
H-MVIP
IEEE 1149.1
ITU-T G.703
ITU-T G.704
ITU-T G.705
ITU-T G.706
ITU-T G.732
ITU-T G.735
ITU-T G.736
ITU-T G.737
ITU-T G.738
ITU-T G.739
ITU-T G.823
ITU-T G.824
ITU-T G.962
ITU-T G.963
ITU-T G.964
ITU-T I.431
ITU-Q.703
JT-G703
JT-G704
JT-G706
JT-I431
MIL-Std. 883D
TR-TSY-000009
UL 1459

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device name (FALC®-LH), device number (PEB 2255), device version (Version 1.3),

and in the *body* of your e-mail:
document type (Data Sheet), issue date (2000-07) and document revision number (DS 1).

Table of Contents **Page**

Table of Contents **Page**

Table of Contents **Page**

Table of Contents **Page**

Table of Contents **Page**

List of Figures **Page**

List of Figures **Page**

List of Tables **Page**

List of Tables **Page**

1 Introduction

The FALC®-LH framer and line interface component is designed to fulfill all required interfacing between an analog E1/T1/J1 line and the digital PCM system highway, H.100 or H-MVIP bus for world market telecommunication systems.

Due to its multitude of implemented functions, it fits to a wide range of networking applications and fulfills the according international standards. The FALC®-LH offers a generic E1/T1/J1 analog line interface without the need to change external components. Optional crystal-less jitter attenuation reduces the amount of required external components.

Equipped with a flexible microprocessor interface, it connects to any control processor environment. A standard boundary scan interface is provided to support board level testing. Flat pack device packaging, small number of external components and low power consumption lead to reduced overall system costs.

Other members of the FALC® family are the FALC®54 for short haul applications, the FALC®56 for long haul and short haul applications as well as the QuadFALC™ supplying four long haul and short haul interfaces on one single chip.

E1/T1/J1 Framer and Line Interface Component for Long and Short Haul Applications
FALC®-LH

PEB 2255

Version 1.3

1.1 Features

P-MQFP-80-1

Line Interface

- High density, generic interface for all E1/T1/J1 applications
- Analog receive and transmit circuitry for long haul and short haul applications
- Data and clock recovery using an integrated digital phase locked loop
- Maximum line attenuation up to -43 dB at 1024 kHz (E1)
  and up to -36 dB at 772 kHz (T1/J1)
- Programmable transmit pulse shapes for E1 and T1/J1 pulse masks
- Programmable line build-out for CSU signals according to ANSI T1.403 + FCC68 in steps of 0 dB, -7.5 dB, -15 dB and -22.5 dB (T1/J1)
- Low transmitter output impedances for high transmit return loss
- Tristate function of the analog transmit line outputs
- Transmit line monitor protecting the device from damage
- Jitter specifications of ITU-T I.431, G.703, G.736 (E1), G.823 (E1) and AT&T TR62411 (T1/J1) are met
- Optional crystal-less wander and jitter attenuation/compensation
- Dual rail or single rail digital inputs and outputs
- Unipolar NRZ or CMI coding for interfacing fibre optical transmission routes
- Selectable line codes (E1: HDB3, AMI - T1/J1: B8ZS, AMI with ZCS) for analog interface
- Loss of signal indication with programmable thresholds according to ITU-T G.775 and ETS300233 (E1)/ANSI T1.403, T1.231(T1/J1)
- Clock generator for jitter free system/transmit clocks
- Local loop and remote loop for diagnostic purposes
- Only one type of transformer (ratio 1: $\sqrt{2}$) for E1 75/120 Ω and T1/J1 100/110 Ω

Type	Package
PEB 2255	P-MQFP-80-1

Frame Aligner

- Frame alignment/synthesis for 2048 kbit/s according to ITU-T G.704 (E1) and for 1544 kbit/s according to ITU-T G.704 and JT G.704 (T1/J1)
- Programmable frame formats :
  E1: Doubleframe, CRC Multiframe (E1)
  T1: 4-Frame Multiframe (F4,FT), 12-Frame Multiframe (F12, D3/4), Extended Superframe (F24, ESF), Remote Switch Mode (F72, SLC96)
- Selectable conditions for recover/loss of frame alignment
- CRC4 to non-CRC4 interworking of ITU-T G. 706 Annex B (E1)
- Error checking via CRC4 procedures according to ITU-T G. 706 (E1)
- Error checking via CRC6 procedures according to ITU-T G. 706 and JT G.706 (T1/J1)
- Performs synchronization in ESF format according to NTT requirements (J1)
- Alarm and performance monitoring per second
  16 bit counter for CRC-, framing errors, code violations, error monitoring via E bit and SA6 bit (E1), errored blocks, PRBS bit errors
- Insertion and extraction of alarm indication signals (AIS, Remote/Yellow Alarm, AUXP)
- IDLE code insertion for selectable channels
- 8.192 MHz/2.048 MHz (E1) or 8.192 MHz/1.544 MHz (T1/J1) system clock frequency
- Selectable 2048/4096 kbit/s backplane interface with programmable receive/transmit timeslot offset
- Programmable tristate function of 4096 kbit/s output via RDO
- Elastic store for receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication
- Programmable elastic buffer size: 2 frames/1 frame/short buffer/bypass
- Supports fractional E1 or T1 access
- Flexible transparent modes
- Programmable In-Band Loop Code detection and generation (TR62411)
- Channel loop back, line loop back or payload loop back capabilities (TR54016)
- Pseudo random bit sequence (PRBS) generator and monitor
- Provides loop-timed mode
- Clear channel capabilities (T1/J1)

Signaling Controller

- HDLC controller
  Bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions, programmable preamble
- DL-channel protocol for ESF format according to ANSI T1.403 or according to AT&T TR54016 (T1/J1)
- DL-channel protocol for F72 (SLC96) format
- CAS controller with last look capability, enhanced CAS- register access and freeze signaling indication
- Robbed bit signaling capability (T1/J1)

- Provides access to serial signaling data streams
- CAS Multiframe synchronization and synthesis according to ITU-T G.732
- Alarm insertion and detection (AIS and LOS in Timeslot 16)
- Transparent mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets.
- Time-slot assignment
  Any combination of time slots selectable for data transfer independent of signaling mode

Microprocessor Interface

- 8/16 bit microprocessor bus interface (Intel or Motorola type)
- All registers directly accessible (byte or word access)
- Multiplexed and non-multiplexed address bus operations
- Extended interrupt capabilities
- Hardware and software reset
- One second timer

General

- Boundary scan standard IEEE 1149.1
- P-MQFP-80 package; body size 14x14; pitch 0.65
- 5V power supply
- Typical power consumption 450 mW

Applications

- Wireless Basestations
- E1/T1/J1 ATM Gateways, Multiplexer
- E1/T1/J1 Channel & Data Service Units (CSU, DSU)
- E1/T1/J1 Internet Access Equipment
- LAN/WAN Router
- ISDN PRI, PABX
- Digital Access Cross Connect Systems (DACS)
- SONET/SDH Add/Drop Multiplexer

1.2 Logic Symbol

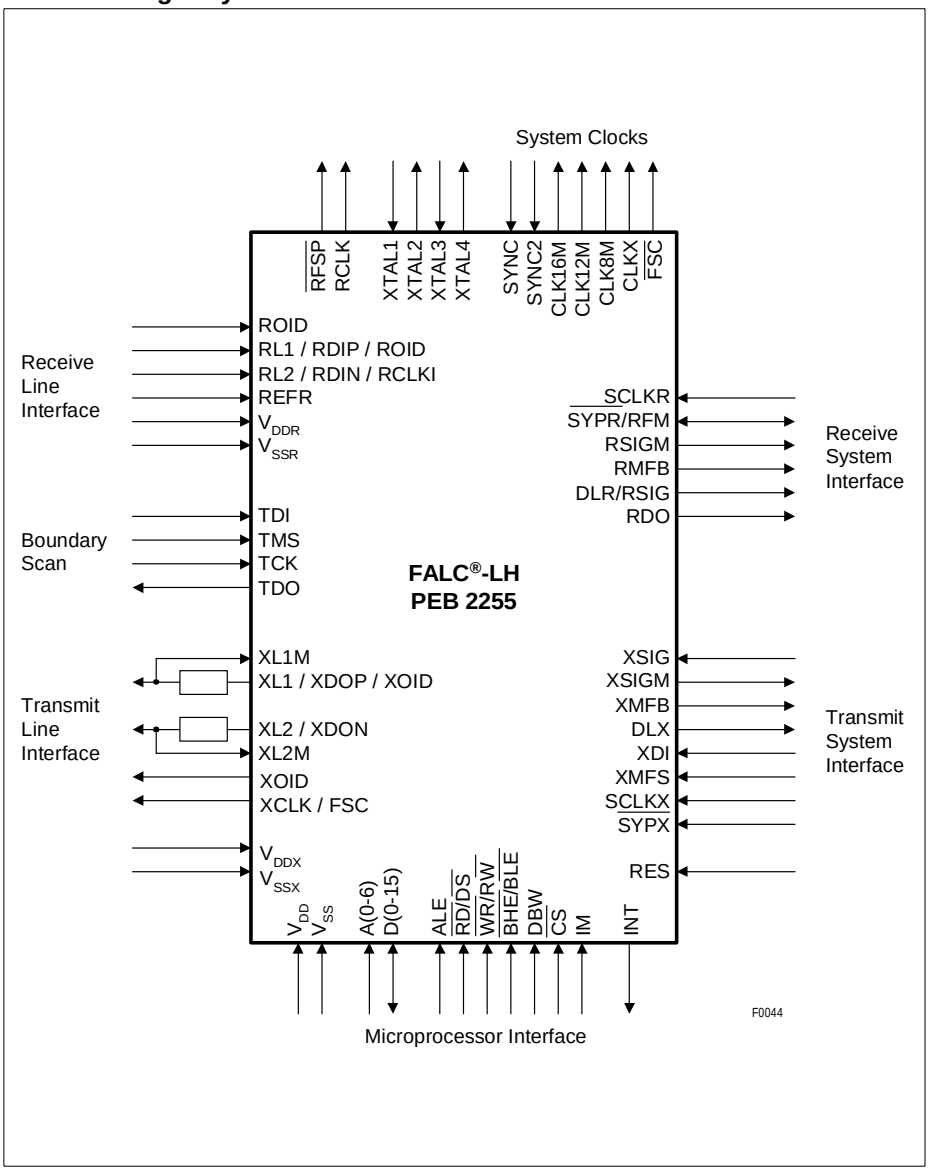


Figure 1 Logic Symbol

1.3 Typical Applications

The figures show a multiple link circuit for Frame Relay applications using the FALC-LH together with the 128 channel HDLC controller M128X and the Memory Timeswitch MTLS as well as an 8 channel interface to the ATM layer combined with n IWE8 device.

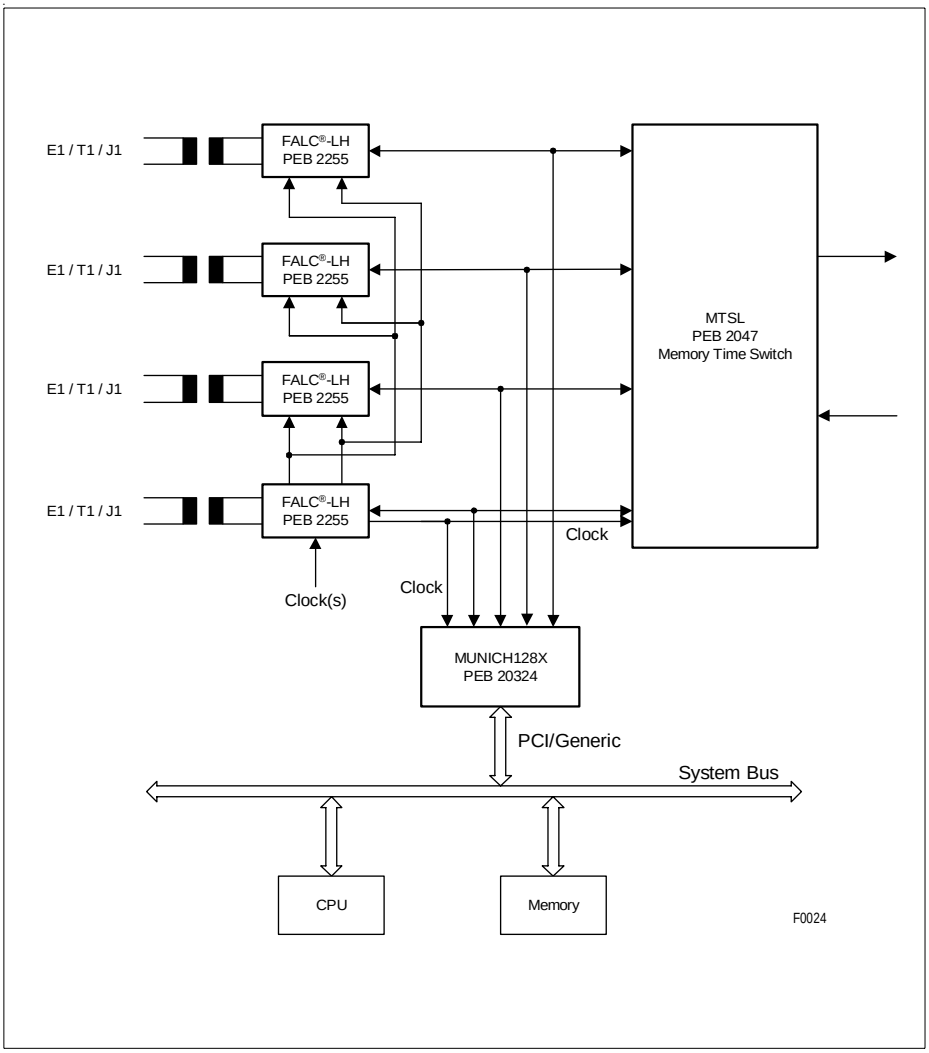


Figure 2 Multiple E1/T1/J1 Link over Frame Relay

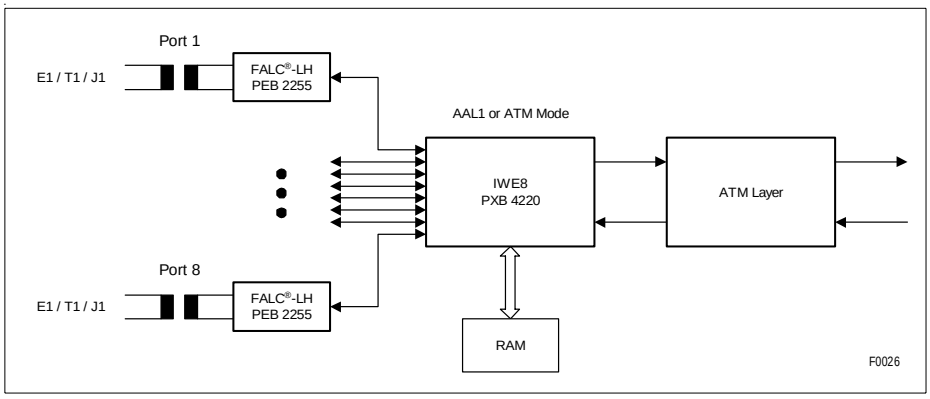


Figure 3 8 Channel E1/T1/J1 Interface to the ATM Layer

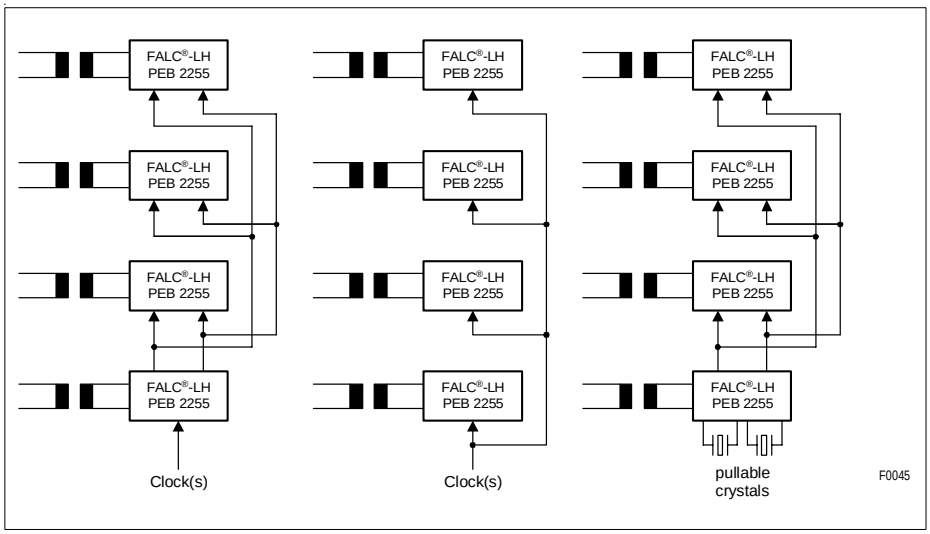


Figure 4 Multiple FALC Clocking Options

2 Pin Descriptions

2.1 Pin Diagram

(top view)

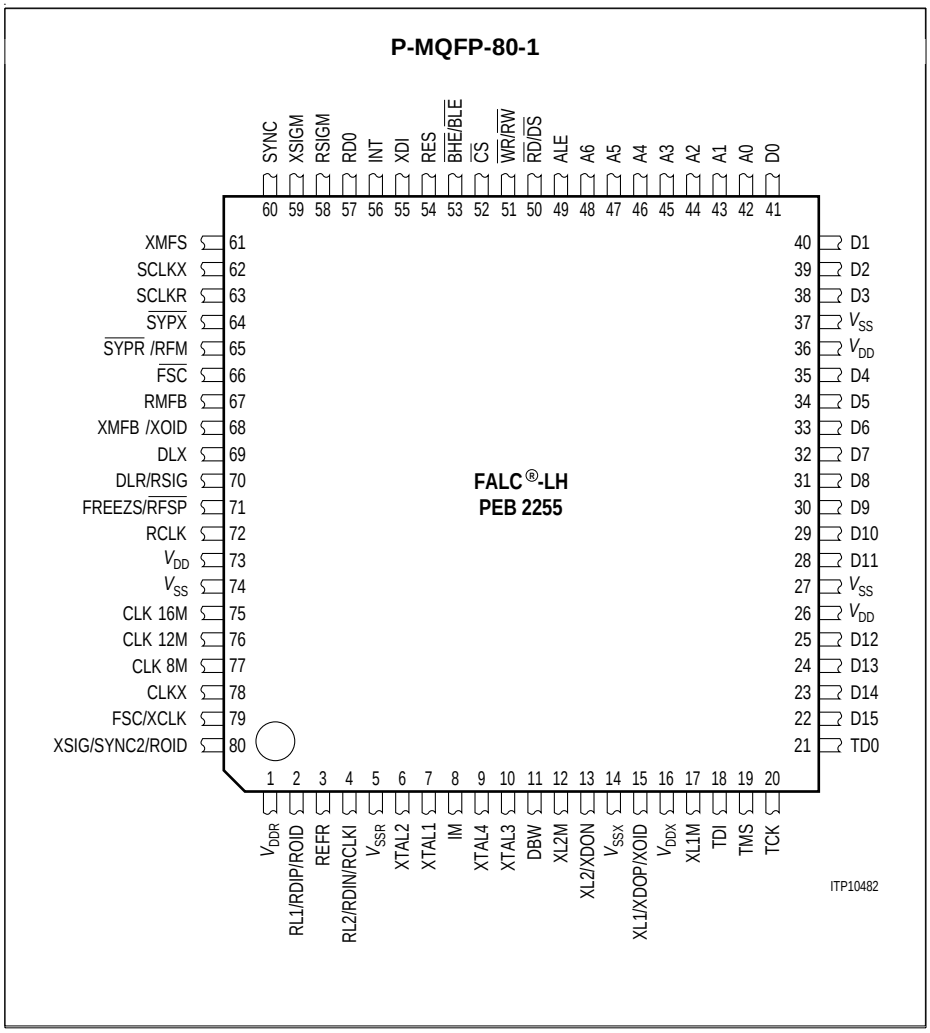


Figure 5 Pin Configuration

2.2 Pin Definitions and Functions

Table 1 Pin Definitions - Microprocessor Interface

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
42...48	A0 ... A6	I	**Address Bus** These inputs interface to seven bits of the system's address bus to select one of the internal registers for read or write.
41…38 35…28 25…22	D0…D3 D4…D11 D12..D15	I/O	**Data Bus** Bidirectional tristate data lines which interface to the system's data bus. Their configuration is controlled by the level of pin DBW: 8-bit mode (DBW = 0): D0 … D7 are active. D8 … D15 are in high impedance and have to be connected to V_{DD} or V_{SS}. 16-bit mode (DBW = 1): D0 … D15 are active. In case of byte transfers, the active half of the bus is determined by A0 and $\overline{BHE}$/$\overline{BLE}$ and the selected bus interface mode (via pin IM). The unused half is in high impedance state.
49	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus. The address information provided on lines A0 … A6 is internally latched with the falling edge of ALE. This function allows the FALC®-LH to be connected to a multiplexed address/data bus directly. In this case, pins A0 … A6 must be connected to the Data Bus pins externally. In case of demultiplexed mode this pin has to be connected to V_{DD} or V_{SS} directly.
52	$\overline{CS}$	I	**Chip Select** A low signal selects the FALC®-LH for read and write operations.

Table 1 Pin Definitions - Microprocessor Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
50	$\overline{RD}/\overline{DS}$	I	**Read Enable** (Intel bus mode) This signal indicates a read operation. When the FALC®-LH is selected via $\overline{CS}$, the $\overline{RD}$ signal enables the bus drivers to output data from an internal register addressed by A0 … A6 on to the Data Bus. **Data Strobe** (Motorola bus mode) This pin serves as input to control read/write operations. It is logically ored with pin $\overline{CS}$.
51	$\overline{WR}/R\overline{W}$	I	**Write Enable** (Intel bus mode) This signal indicates a write operation. When $\overline{CS}$ is active the FALC®-LH loads an internal register with data provided on the Data Bus. **Read/Write Enable** (Motorola bus mode) This signal distinguishes between read and write operation.
11	DBW	I	**Data Bus Width** (Bus Interface Mode) A low signal on this input selects the 8-bit bus interface mode. A high signal on this input selects the 16-bit bus interface mode. In this case word transfer to/from the internal registers is enabled. Byte transfers are implemented by using A0 and $\overline{BHE}/\overline{BLE}$.
8	IM	I	**Interface Mode** The level at this pin defines the bus interface mode: A low signal on this input selects the Intel interface mode. A high signal on this input selects the Motorola interface mode.

Table 1 **Pin Definitions - Microprocessor Interface** (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
53	$\overline{\text{BHE}}$/$\overline{\text{BLE}}$	I + PU	**Bus High Enable** (Intel bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the upper byte of the data bus (D8 … D15). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}. **Bus Low Enable** (Motorola bus mode) If 16-bit bus interface mode is enabled, this signal indicates a data transfer on the lower byte of the data bus (D0 … D7). In 8-bit bus interface mode this signal has no function and should be tied to V_{DD}.
56	INT	O/oD	**Interrupt Request** INT serves as general interrupt request which may include all interrupt sources. These interrupt sources can be masked via registers IMR0 … 5. Interrupt status is reported via registers GIS (Global Interrupt Status) and ISR0 … 3,5. Output characteristics (push-pull active low/ high, open drain) are determined by programming the IPC register. (oD = open drain output)

Table 2 Pin Definitions - Line Interface

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
			Line Interface Receive
2	RL1	I (analog)	**Line Receiver 1** Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIP	I	**Receive Data Input Positive** Digital input for received dual rail PCM(+) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The Duty cycle of the received signal has to be close to 50%. The Dual Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input polarity is selected by bit RC0.RDIS (after reset: active low).
	ROID	I	**Receive Optical Interface Data** Unipolar data received from fiber optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The Single Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 0.
80	ROID	I	**Receive Optical Interface Data** LOOP.SPN = 1 Unipolar data received from fiber optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1). Latching of data is done with the falling edge of RCLKI. Input polarity is selected by bit RC0.RDIS. The Single Rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 0. *Note: This pin contains multiple functions, see also SYNC2 and XSIG.*

Table 2 Pin Definitions - Line Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
4	RL2	I (analog)	**Line Receiver 2** Analog Input from the external transformer. Selected if LIM1.DRS = 0.
	RDIN	I	**Receive Data Input Negative** Input for received dual rail PCM(-) route signal which will be latched with the internal generated Receive Route Clock. An internal DPLL will extract the Receive Route Clock from the incoming data pulse. The duty cycle of the received signal has to be close to 50%. The dual rail mode is selected if LIM1.DRS = 1 and FMR0.RC1 = 1. Input polarity is selected by bit RC0.RDIS (after reset: active low).
	RCLKI	I	**Receive Clock Input** Receive clock input for the optical interface if LIM1.DRS = 1 and FMR0.RC1/0 = 00. Clock frequency: 2048 kHz (E1) or 1544 kHz (T1/J1).

Table 2 Pin Definitions - Line Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
			Line Interface Transmit
15	XL1	O (analog)	**Transmit Line 1** Analog output to the external transformer. Selected if LIM1.DRS = 0. After reset this pin is in a high impedance state until bit FMR0.XC1 is set.
	XDOP	O	**Transmit Data Output Positive** This digital output for transmitted dual rail PCM(+) route signals can provide - half bauded signals with 50% duty cycle (LIM0.XFB = 0) or - full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After reset this pin is in a high impedance state until register LIM1.DRS is set.
	XOID	O	**Transmit Optical Interface Data** Unipolar data sent to fiber optical interface with 2048 kbit/s (E1) or 1544 kbit/s (T1/J1) which will be clocked off on the positive transitions of XCLK. Clocking off data in NRZ code is done with 100% duty cycle. Data in CMI code (E1 only) are shifted out with 50% or 100% duty cycle according to the CMI coding. Output polarity is selected by bit LIM0.XDOS (after reset: data is sent active high). The single rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 0. After reset this pin is in a high impedance state until register LIM1.DRS is set. If LOOP.SPN = 1 this pin function is not defined and should be tristated by enabling XPM2.XLT.

Table 2 Pin Definitions - Line Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
17	XL1M	I	**Transmit Line 1 Monitor** Analog input from external transmit transformer (XL1). This pin must be connected, otherwise pin XL1 could be set into high impedance state automatically. If digital line interface mode is selected (LIM1.DRS = 1), this input has to be connected to V_{SSX}.
13	XL2	O (analog)	**Transmit Line 2** Analog output for the external transformer. Selected if LIM1.DRS = 0. After reset this pin is in a high impedance state until bit FMR0.XC1 is set.
	XDON	O	**Transmit Data Output Negative** This digital output for transmitted dual rail PCM(-) route signals can provide - half bauded signals with 50% duty cycle (LIM0.XFB = 0) or - full bauded signals with 100% duty cycle (LIM0.XFB = 1) The data will be clocked off on the positive transitions of XCLK in both cases. Output polarity is selected by bit LIM0.XDOS (after reset: active low). The dual rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 1. After reset this pin is in a high impedance state until register LIM1.DRS is set.
12	XL2M	I	**Transmit Line 2 Monitor** Analog input from external transmit transformer (XL2). This pin must be connected, otherwise pin XL2 could be set into high impedance state automatically. If digital line interface mode is selected (LIM1.DRS = 1), this input has to be connected to V_{SSX}.

Table 3 Pin Definitions - Clock Generation

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
7	XTAL1	I	**Crystal Connection 16.384 MHz** A pullable crystal of 16.384 MHz has to be provided at these pins, if jitter attenuation of the system clocks is done internally. If not, or if crystal-less jitter attenuation is used, either a regular crystal of 16.384 MHz has to be connected to XTAL1/XTAL2 or a 16.384-MHz clock must be connected to XTAL1 while XTAL2 is left open.
6	XTAL2	O	
10	XTAL3	I	**Crystal Connection** **16.384 MHz (E1)/12.352 MHz (T1/J1)** A pullable crystal of 16.384 MHz/12.352 MHz is only required at these pins, if jitter attenuation of the transmit clocks is done internally. If jitter attenuation is provided externally, the jitter attenuated clock of 16.384 MHz/12.352 MHz has to be applied to XTAL3 while XTAL4 is left open. If crystal-less jitter attenuation is used, either a regular crystal of16.384 MHz/12.352 MHz has to be connected to XTAL3/XTAL4 or a 16.384-MHz/12.352-MHz clock has to be connected to XTAL3 while XTAL4 is left open. E1 mode only: If no transmit jitter attenuation is required, XTAL3 should be connected to V_{DD} or V_{SS}, XTAL4 is to be left open.
9	XTAL4	O	
79	XCLK	O	**Transmit Clock** Transmit clock of 2.048 MHz (E1) or 1.544 MHz (T1/J1). This clock is driven from SCLKX or RCLK or generated internally.
	FSC	O	8 kHz Frame Synchronization Pulse is output on this pin, if LIM1.EFSC = 1 is selected. The synchronization pulse is active **high** for one cycle (pulse width = 488 ns) and derived from the clock supplied on pin CLK16M.

Table 3 Pin Definitions - Clock Generation (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
66	$\overline{\text{FSC}}$	O	**8 kHz Frame Synchronization Pulse** is output on this pin. The synchronization pulse is active **low** for one cycle (pulse width = 488 ns) and derived from the clock supplied on pin CLK16M.
75	CLK16M	O	**System Clock 16.384 MHz** Buffered XTAL1 clock (LIM3.CSC=1) or jitter attenuated clock (LIM3.CSC=0, if crystal-less jitter attenuation is used).
76	CLK12M	O	**System Clock 16.384 MHz (E1)/12.384 MHz (T1/J1)** Buffered XTAL3 clock (LIM3.CSC=1) or jitter attenuated clock (LIM3.CSC=0, if crystal-less jitter attenuation is used).
77	CLK8M	O	**System Clock 8.192 MHz** Clock derived from CLK16M reference.
78	CLKX	O	**System Clock Output** Output frequencies are 2.048 MHz or 4.096 MHz, inverted or non-inverted. The clock is derived from CLK16M, frequency and polarity in relation to $\overline{\text{FSC}}$ are selected by setting of LIM0.SCL1...0.
60	SYNC	I	**Clock Synchronization** If a clock is detected at the SYNC pin, the FALC®-LH synchronizes to this 2.048-MHz (E1)/ 2.048 or 1.544-MHz (T1/J1) clock if in master mode or if signal is lost in slave mode. This pin has to be connected to V_{SS}, if no clock is supplied.

Table 3 Pin Definitions - Clock Generation (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
80	SYNC2	I	**Clock Synchronization 2** Secondary reference clock for internal transmit clock generation. The clock frequency is 2.048-MHz (E1) or 2.048/ 1.544-MHz (T1/J1). This function is selected by setting LIM3.ESY=1 *Note: This pin contains multiple functions, see also ROID and XSIG.*
72	RCLK	O + PU	**Receive Clock** extracted from the incoming data pulses. Clock frequency: 2048 kHz (E1) or 1544 kHz (T1/J1) In case of loss of signal (LOS) the RCLK is derived from the clock that is provided on XTAL1. If LIM0.ELOS is set, RCLK is set high in case of loss of signal (FRS0.LOS = 1). If NRZ mode is selected, RCLK is the buffered RCLKI clock.

Table 4 Pin Definitions - System Interface

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
		System Interface Receive	
57	RDO	O	**Receive Data Out** Received data which is sent to the system highway at 4096 kbit/s, 2048 kbit/s or 1544 kbit/s (T1/J1 only). In 4096 kbit/s mode data is shifted out in the channel phase which is selected by RC0.SICS. During the other channel phase RDO is set into tristate. Clocking off data is done with the falling edge of SCLKR or RCLK, if the receive elastic store is bypassed. The delay between the beginning of time-slot 0 and the initial edge of SCLKR (after $\overline{\text{SYPR}}$ goes active) is determined by the values of registers RC1 and RC0.
70	DLR	O	**Data Link Bit Receive** E1 mode: Marks the S_A4...8 bits within the data steam on RDO. The S_A4...8 bit positions in time slot 0 of every frame not containing the frame alignment signal are selected by register XC0.SA4E-SA8E. T1/J1 mode: Provides a signal which marks the DL bit position within the data stream on RDO. It can be used as receive strobe signal for external data link controllers. In 4096 kbit/s mode DLR is active only during the channel phase selected by RCO.SICS.
	RSIG	O	**Receive Signaling Data** Output for receive signaling data sent to the signaling highway. This function is selected by setting LOOP.SPN = 1 LIM3.ESY = 1 XSP.CASEN = 0

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
71	$\overline{\text{RFSP}}$	O	**Receive Frame Synchronous Pulse** E1: FMR3.CFRZ = 0 T1/J1: XC0.SFRZ = 0 Active low framing pulse derived from the received PCM route signal. During loss of synchronization (bit FRS0.LFA) this pulse is suppressed (not influenced during alarm simulation). The pulse frequency is 8 kHz, pulse width is 488 ns (E1) or 648 ns (T1/J1).
		O	**PRBS Monitor Status** The status of the PRBS monitor is output on this pin, if FMR3.CFRZ = 0 (E1) or XC0.SFRZ = 1 (T1/J1) and LCR1.EPRM = 1. It is set high, if the PRBS monitor is in synchronous state.
	FREEZS	O	**Freeze Signaling (T1/J1)** If XC0.SFRZ = 1 (T1/J1) or FMR3.CFRZ = 1 (E1) and LCR1.EPRM = 0, the Freeze Signaling Status is indicated. Register access (LOOP.SPN=0 and LIM3.ESY=0): • E1: Bit FRS1.TSL16LFA = 1 • T1: FRS0.LFA/LMFA = 1 or a receive slip (positive or negative) occurred Serial signaling access (LOOP.SPN=1 and LIM3.ESY=1): • E1: Bit FRS1.TSL16LFA = 1 or FRS0.LOS=1 or a receive slip occurred • T1: FRS0.LFA/LMFA = 1 or FRS0.LOS=1 or a receive slip occurred The signal is cleared after an error-free superframe. During alarm simulation this signal gets active during simulation steps 2 and 6.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
65	$\overline{\text{SYPR}}$	I	**Synchronous Pulse Receive** SIC2.SRFSO = 0 (reset value): Defines the beginning of time slot 0 on system highway port RDO together with the values of RC0.RCO, RC0.RCOS and RC1.RTO. Sampling is done with the falling edge of SCLKR. The pulse cycle is an integer multiple of 125 µs.
	RFM	O	**Receive Frame Marker** SIC2.SRFSO = 1: This marker will be active high for one 2.048-MHz (E1)/1.544-MHz (T1/J1) cycle (SIC1.SRSC = 1; 2.048 Mbit/s PCM highway interface mode) or two 8.192-MHz cycles (SIC1.SRSC = 0; 4.096 Mbit/s PCM highway interface mode). It is clocked with the falling edge of SCLKR or RCLK, depending on the selected receive buffer size (SIC1).The marker can be activated within any bit position of a received frame (RC0/1).
63	SCLKR	I	**System Clock Receive** Working clock for the receive system interface with a frequency of 8.192 MHz (SIC1.SRSC = 0, SIC1.SXSC=0) or 2.048 MHz (E1)/1.544 MHz (T1/J1) (SIC1.SRSC = 1, SIC1.SXSC=1). If the receive elastic store is bypassed (SIC1.RBS1...0), the clock supplied on this pin is ignored. During reset phase, a clock has to be provided.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
58	RSIGM	O	**Receive Signaling Marker** E1/T1/J1 mode: Marks the time-slots which are defined by register RTR1-4 of every received frame on port RDO. T1/J1 CAS-BR mode: When using the CAS-BR signaling scheme, the robbed bit of each channel every six frames is marked, if it is enabled via register XC0.BRM = 1. General: In 4096 kbit/s mode RSIGM is active only during the channel phase selected by RCO.SICS.
67	RMFB	O	**Receive Multiframe Begin** RMFB marks the beginning of every received multiframe (RDO, first bit of the FAS word in frame 1 of a multiframe). Active high for one 2048 kbit/s period. In 4096 kbit/s mode RMFB is active during the first two bits of channel phase one of a multiframe. In T1/J1 mode the function depends on programming bit XC0.MFBS: MFBS = 1: RMFB marks the beginning of every received multiframe (RDO). MFBS = 0: Marks the beginning of every received superframe. Additional pulses every 12 frames are provided when using ESF/F24 or F72 format.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
		System Interface Transmit	
68	XMFB	O	**Transmit Multiframe Begin** E1 mode/LOOP.SPN = 0: Marks the begin of every transmitted multiframe (XDI). T1/J1 mode/XC0.MFBS = 1**:** XMFB marks the beginning of every transmitted multiframe (XDI). T1/J1 mode/XC0.MFBS = 0**:** XMFB marks the beginning of every transmitted superframe. Additional pulses every 12 frames are provided when using ESF/F24 or F72 format. General: This signal is always active high for one 2048 kbit/s period. In 4096 kbit/s mode, it is active during the first two bits of a multiframe.
	XOID	O	**Transmit Optical Interface Data** E1 mode only/LOOP.SPN = 1: Unipolar data sent to fiber optical interface with 2048 kbit/s which will be clocked off on the positive transitions of XCLK. Clocking off data in NRZ mode is done with a duty cycle of 100%. CMI code data is shifted out with a duty cycle of 50%/100% according to the CMI coding. Output polarity is selected by LIM0.XDOS (active high after reset). Single rail mode is selected if LIM1.DRS = 1 and FMR0.XC1 = 0.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
64	$\overline{\text{SYPX}}$	I	**Synchronous Pulse Transmit** Defines the beginning of time slot 0 at system highway port XDI together with the values of XC0.XCO, XC1.XTO and XC1.XCOS. Sampling is done with the falling edge of SCLKX. The pulse cycle is an integer multiple of 125 µs.
62	SCLKX	I	**System Clock Transmit** Working clock for the transmit system interface with a frequency of 8.192 MHz (SIC1.SXSC = 0, SIC1.SRSC = 0) or 2.048 MHz (E1)/1.544 MHz (T1/J1) (SIC1.SXSC = 1, SIC1.SRSC = 1).
55	XDI	I	**Transmit Data In** Transmit data received from the system highway. Latching of data is done with the falling transitions of SCLKX. E1 data rate (SCLKX = 8.192 MHz): FMR1.IMOD = 0: 4096 kbit/s FMR1.IMOD = 1: 2048 kbit/s E1 data rate (SCLKX = 2.048MHz): FMR1.IMOD = 1 & SIC1.SXSC = 1: 2048kbit/s T1/J1data rate (SCLKX = 8.192 MHz): FMR1.IMOD = 0: 4096 kbit/s FMR1.IMOD = 1 & SIC1.SXSC = 0: 2048 kbit/s T1/J1data rate (SCLKX = 1.544 MHz): FMR1.IMOD = 1 & SIC1.SXSC = 1: 1544 kbit/s The delay between the beginning of time slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is determined by the values of transmit time slot offset (XC1.XTO5-0), transmit clock slot offset (XC0.XCO2-0) and XC1.XCOS.

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
69	DLX	O	**Data Link Bit Transmit** E1 mode: Marks the S_A4...8 bits within the data stream on XDI. The S_A4...8 bit positions in time-slot 0 of every frame not containing the frame alignment signal are selected by register XC0.SA4E-SA8E. T1/J1 mode: This output provides a signal which marks the DL-bit position within the data stream on XDI. In 4096 kbit/s mode DLX is active only during the channel phase selected by RCO.SICS.
80	XSIG	I	**Transmit Signaling Data** Input for transmit signaling data received from the signaling highway. This function is selected by setting LOOP.SPN = 1 LIM3.ESY = 1 *Note: This pin contains multiple functions, see also SYNC2 and ROID.*

Table 4 Pin Definitions - System Interface (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
59	XSIGM	O	**Transmit Signaling Marker** Marks the transmit time slots which are defined by register TTR1-4 of every frame transmitted on port XDI. In 4096 kbit/s mode, XSIGM is active only during the channel phase which is selected by RC0.SICS. **T1 mode/CAS-BR:** If CAS-BR is selected by FMR1.SIGM = 1, the robbed bit of each channel every six frames is marked, if marker is enabled by setting XC0.BRM = 1.
61	XMFS	I	**Transmit Multiframe Synchronization** This port defines the first frame of the multiframe on the transmit system interface port XDI. **Note:** A new multiframe position has been settled at least one multiframe after pulse XMFS has been supplied. If this input is not used, it has to be connected to V_{SS}. In this case multiframe start is generated internally.

Table 5 Pin Definitions - Miscellaneous

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
Power Supply			
1	V_{DDR}	S	**Positive Power Supply** for the analog receiver
5	V_{SSR}	S	**Power Supply: Ground** for the analog receiver
16	V_{DDX}	S	**Positive Power Supply** for the analog transmitter
14	V_{SSX}	S	**Power Supply: Ground** for the analog transmitter
27, 37, 74	V_{SS}	S	**Power Supply: Ground** for digital subcircuits (0 V) For correct operation, all three pins have to be connected to ground.
26, 36, 73	V_{DD}	S	**Positive Power Supply** for the digital subcircuits (5.0 V) For correct operation, all three pins have to be connected to positive power supply.
Device Reset			
54	RES	I	**Reset** A high signal on this pin forces the FALC®-LH into reset state. During Reset the FALC®-LH needs active clocks on pins SCLKR, SCLKX, XTAL1 and XTAL3 (E1: XTAL3 only, if slicer mode selectable by LIM1.JATT/RL = 10 will be used). During Reset - all unidirectional output stages are in high-impedance state, except pins CLK16M, CLK12M, CLK8M, CLKX, $\overline{FSC}$, XCLK and RCLK (active clocks are required during reset on pins SCLKR, SCLKX, XTAL1 and XTAL3[1]) - all bidirectional output stages (data bus) are in input mode if signal $\overline{RD}$ is “high”

Table 5 Pin Definitions - Miscellaneous (cont'd)

Pin No.	Symbol	Input (I) Output (O) Supply (S)	Function
Analog Reference			
3	REFR	O	**Reference Resistance** of 12 kΩ +/- 1% and a capacitor of 680 pF (including external parasitic capacitances). Both have to be connected to pin V_{SSR} in parallel by short external connections.
Boundary Scan/Joint Test Access Group (JTAG)[2)]			
18	TDI	I + PU	**Test Data Input** for Boundary Scan according to IEEE Std. 1149.1 If not connected an internal pull-up transistor ensures high input level.
19	TMS	I + PU	**Test Mode Select** for Boundary Scan If not connected an internal pull-up transistor ensures high input level.
20	TCK	I + PU	**Test Clock** for Boundary Scan If not connected an internal pull-up transistor ensures high input level.
21	TDO	O	**Test Data Output** for Boundary Scan

1) XTAL3 not required in E1/bypass mode

2) Boundary scan reset is done automatically upon power up. No pin $\overline{TRS}$ is provided.

Note: Unused input pins have to be connected to a defined voltage level (V_{DD} or V_{SS}).

3 Functional Description E1/T1/J1

3.1 Functional Overview

The FALC®-LH device contains analog and digital function blocks, which are configured and controlled by an external microprocessor or microcontroller.

The main interfaces are

- Receive and Transmit Line Interface
- PCM System Highway Interface
- Microprocessor Interface
- Boundary Scan Interface

as well as several control lines for reset and clocking purpose.

The main internal functional blocks are

- Analog line receiver with equalizer network and digital clock/data recovery
- Analog line driver with programmable pulse shaper
- Clock generation
- Elastic buffers for receive and transmit direction
- Receive framer
- Receive line decoding, alarm detection, and PRBS monitoring
- Transmit framer
- Transmit line coding, alarm and PRBS generation
- Receive jitter attenuator
- Transmit jitter attenuator
- HDLC controller
- Loop switching (local, remote, payload, single channel)
- Register access interface
- Boundary scan control

3.2 Block Diagram

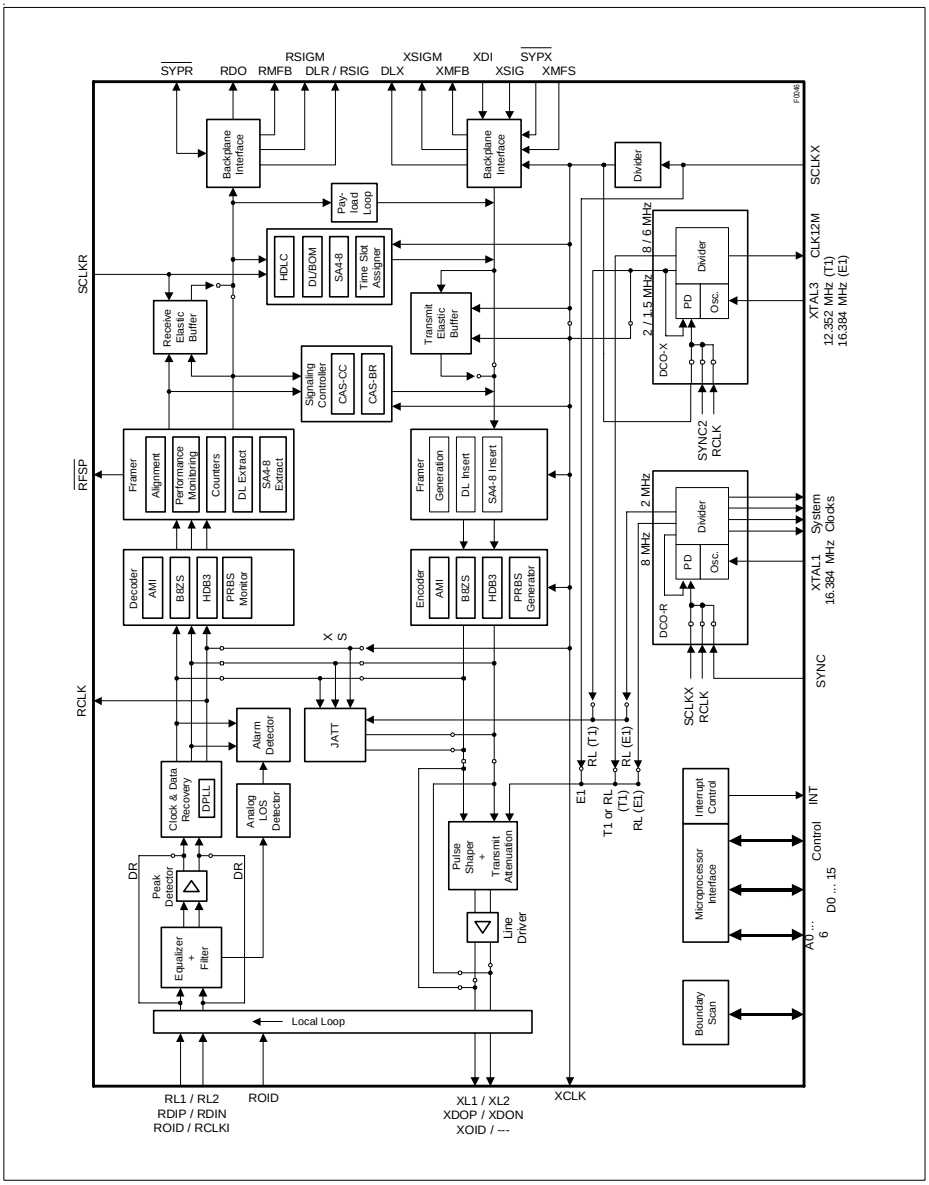


Figure 6 Block Diagram

3.3 Functional Blocks

3.3.1 Microprocessor Interface

The communication between the CPU and the FALC®-LH is done via a set of directly accessible registers. The interface may be configured as Intel or Motorola type with a selectable data bus width of 8 or 16 bits.

The CPU transfers data to/from the FALC®-LH (via 64 byte deep FIFOs per direction), sets the operating modes, controls function sequences, and gets status information by writing or reading control/status registers. All accesses can be done as byte or word accesses if enabled. If 16-bit bus width is selected, access to lower/upper part of the data bus is determined by address line A0 and signal $\overline{\text{BHE}}$/$\overline{\text{BLE}}$ as shown in **Table 6** and **Table 7**.

In **Table 8** is shown how the ALE (address latch enable) line is used to control the bus structure and interface type. The switching of ALE allows the FALC®-LH to be directly connected to a multiplexed address/data bus.

3.3.1.1 Mixed Byte/Word Access to the FIFOs

Reading from or writing to the internal FIFOs (RFIFO and XFIFO) can be done using a 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. Randomly mixed byte/word access to the FIFOs is allowed without any restrictions.

If byte access is used, high byte or low byte can be used as well. Any value written to high or low byte is placed in the FIFO in sequential order.

Table 6 Data Bus Access (16-Bit Intel Mode)

BHE	A0	Register Access	FALC®-LH Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0...D15
0	1	Register byte access (odd addresses)	D8...D15
1	0	Register byte access (even addresses)	D0...D7
1	1	No transfer performed	None

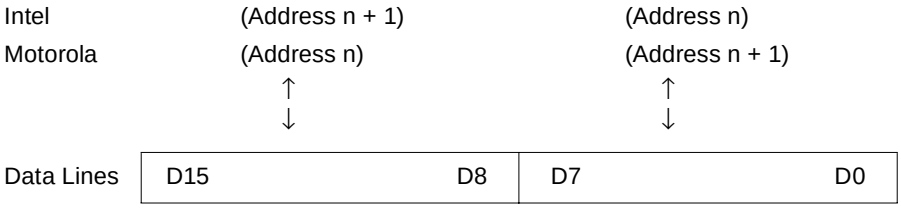
Table 7 Data Bus Access (16-Bit Motorola Mode)

BLE	A0	Register Access	FALC®-LH Data Pins Used
0	0	FIFO word access Register word access (even addresses)	D0...D15
0	1	Register byte access (odd addresses)	D0...D7
1	0	Register byte access (even addresses)	D8...D15
1	1	No transfer performed	None

Table 8 Selectable Bus and Microprocessor Interface Configuration

ALE	IM	Microprocessor interface	Bus Structure
GND/VDD	1	Motorola	demultiplexed
GND/VDD	0	Intel	demultiplexed
switching	0	Intel	multiplexed

The assignment of registers with even/odd addresses to the data lines in case of 16-bit register access depends on the selected microprocessor interface mode:



n: even address

3.3.1.2 FIFO Structure

In transmit and receive direction of the signaling controller 64-byte deep FIFOs are provided for the intermediate storage of data between the system internal highway and the CPU interface. The FIFOs are divided into two halves of 32-bytes. Only one half is accessible to the CPU at any time.

In case 16-bit data bus width is selected by fixing pin DBW to logical '1' word access to the FIFOs is enabled. Data output to bus lines D0-D15 as a function of the selected interface mode is shown in **Figure 7** and **Figure 8**. Of course, byte access is also allowed. The effective length of the accessible part of RFIFO can be changed from 32 bytes (RESET value) down to 2 bytes by programming CCR1.RFT1...0.

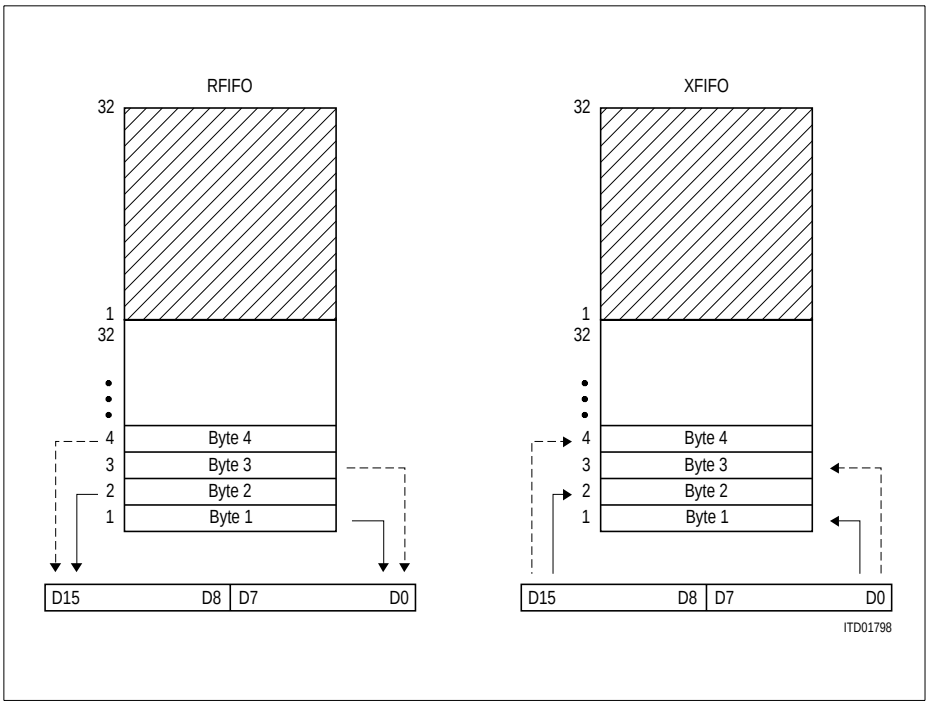


Figure 7 FIFO Word Access (Intel Mode)

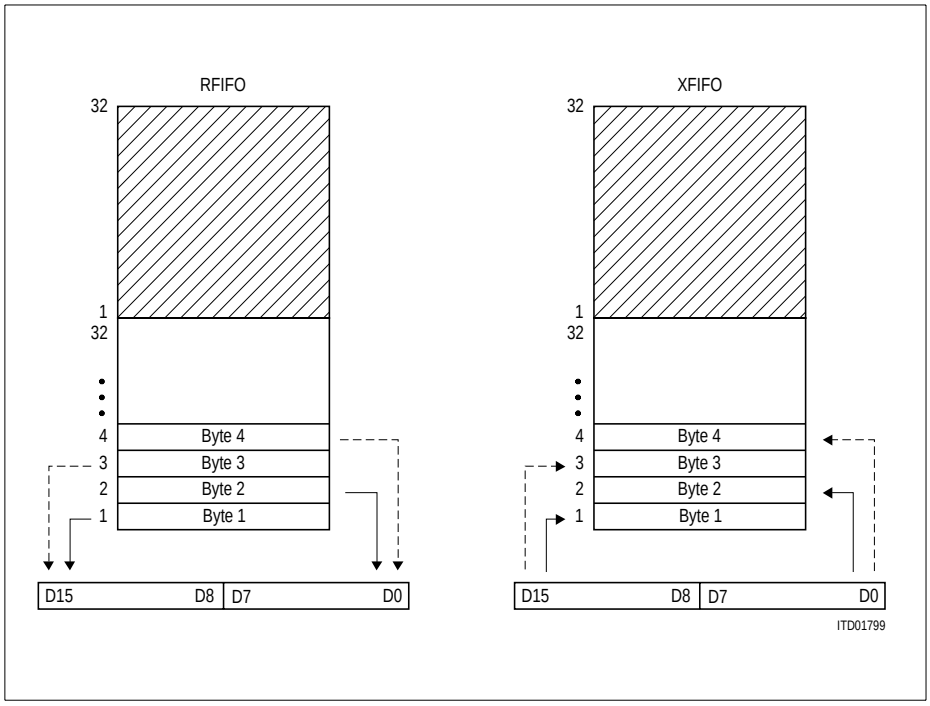


Figure 8 FIFO Word Access (Motorola Mode)

3.3.1.3 Interrupt Interface

Special events in the FALC®-LH are indicated by means of a single interrupt output with programmable characteristics (open drain, push-pull; IPC register), which requests the CPU to read status information from the FALC®-LH, or to transfer data from/to FALC®-LH.

Since only one INT request output is provided, the cause of an interrupt must be determined by the CPU by reading the FALC's interrupt status registers (GIS, ISR0...3, ISR5) that means the interrupt at pin INT and the interrupt status bits are reset by reading the interrupt status registers. Register ISR0...3,5 are from type "Clear on Read".

The structure of the interrupt status registers is shown in **Figure 9**.

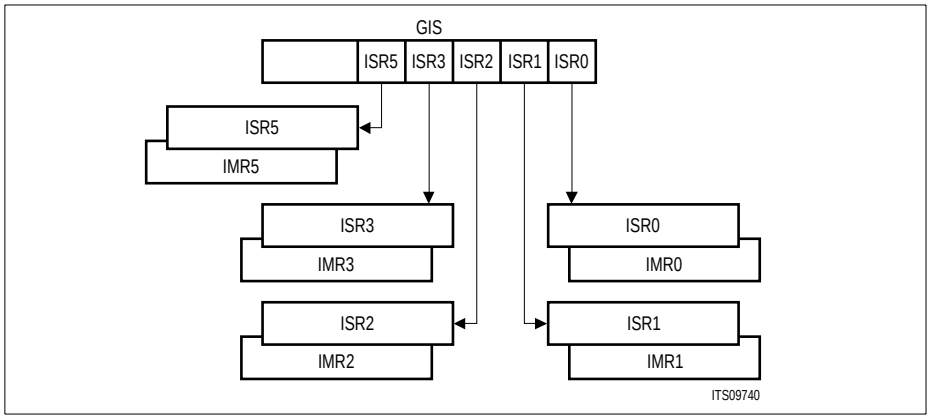


Figure 9 Interrupt Status Registers

Each interrupt indication of registers ISR0…3,5 can be selectively masked by setting the corresponding bit in the corresponding mask registers IMR0…3,5. If the interrupt status bits are masked they neither generate an interrupt at INT nor are they visible in ISR0 … 3,5.

GIS, the non-maskable Global Interrupt Status Register, serves as pointer to pending interrupts. After the FALC®-LH has requested an interrupt by activating its INT pin, the CPU should first read the Global Interrupt Status register GIS to identify the requesting interrupt source register. After reading the assigned interrupt status registers ISR0...ISR3 and ISR5, the pointer in register GIS is cleared or updated if another interrupt requires service.

If **all** pending interrupts are acknowledged by reading (GIS is reset), pin INT goes inactive.

Updating of interrupt status registers ISR0 … 3,5 and GIS is only prohibited during read access.

Masked Interrupts Visible in Status Registers

- The Global Interrupt Status register (GIS) indicates those interrupt status registers with active interrupt indications (GIS.ISR0...3,5).
- An additional mode can be selected via bit IPC.VIS.
- In this mode, masked interrupt status bits neither generate an interrupt at pin INT nor are they visible in GIS, **but are displayed in the respective interrupt status register(s) ISR0...3,5**.

This mode is useful when some interrupt status bits are to be polled in the individual interrupt status registers.

Note: In the visible mode, all active interrupt status bits, whether the corresponding actual interrupt is masked or not, are reset when the interrupt status register is read. Thus, when polling of some interrupt status bits is desired, care must be taken that unmasked interrupts are not lost in the process.

Note: All unmasked interrupt statuses are treated as before.

Please note that whenever polling is used, all interrupt status registers concerned have to be polled individually (no “hierarchical” polling possible), since GIS only contains information on actually generated - i.e. unmasked-interrupts.

3.3.2 Boundary Scan Interface

Identification Register: 32 bit

Version: 4 H

Part Number: 0042 H

Manufacturer:083 H

In FALC®-LH a Test Access Port (TAP) controller is implemented. The essential part of the TAP is a finite state machine (16 states) controlling the different operational modes of the boundary scan. Both, TAP controller and boundary scan, meet the requirements given by the JTAG standard: IEEE 1149.1. **Figure 10** gives an overview.

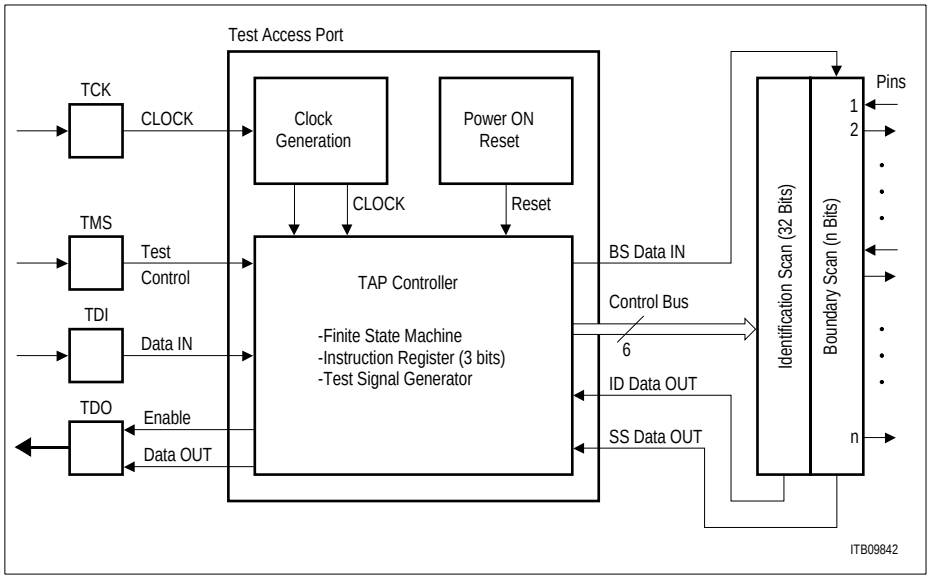


Figure 10 Block Diagram of Test Access Port and Boundary Scan

Test handling is performed via the pins TCK (Test Clock), TMS (Test Mode Select), TDI (Test Data Input) and TDO (Test Data Output). Test data at TDI are loaded with a 4-MHz clock signal connected to TCK. ‘1’ or ‘0’ on TMS causes a transition from one controller state to an other; constant ’1’ on TMS leads to normal operation of the chip.

If no boundary scan testing is planned TMS and TDI do not need to be connected since pull-up transistors ensure high input levels in this case. After switching on the device (power-on), a reset signal is generated internally, which forces the TAP controller into test logic reset state.

4 Functional Description E1

4.1 Receive Path in E1 Mode

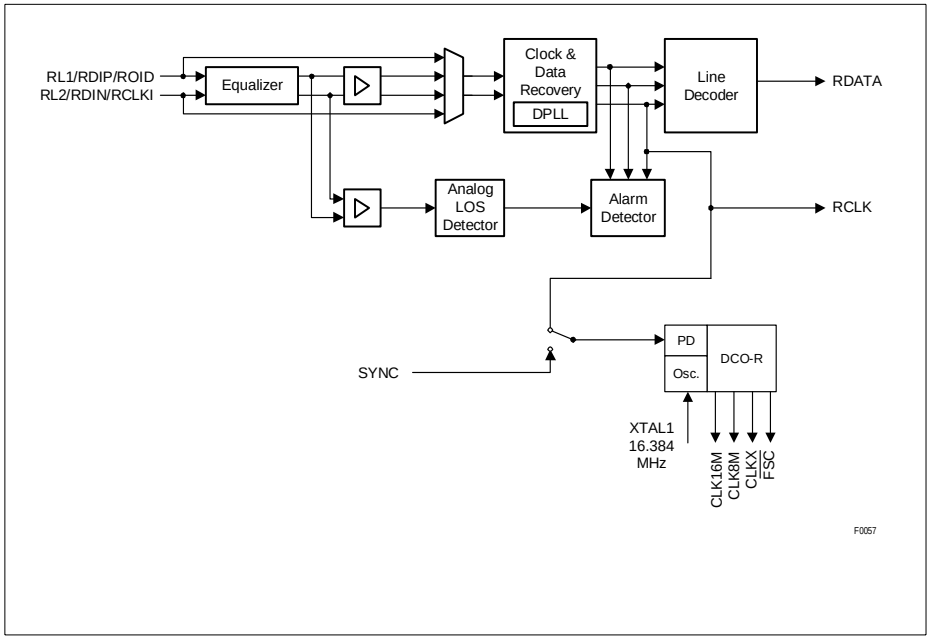


Figure 11 Receive Clock System (E1)

Receive Line Interface

For data input, three different data types are supported:

- Ternary coded signals received at multifunction ports RL1 and RL2 from a -10 dB (short haul, LIM0.EQON = 0) or -43 dB (long haul, LIM0.EQON = 1) ternary interface. The ternary interface is selected if LIM1.DRS is reset.

- Digital dual rail signals received on ports RDIP and RDIN. The dual rail interface is selected if LIM1.DRS and FMR0.RC1 is set.

- Unipolar data on port ROID received from a fiber optical interface. The optical interface is selected if LIM1.DRS is set and FMR0.RC1 is reset.

  Alternatively the optical interface can be switched to pin 68 (XMFB/XOID) and pin 80 (ROID) by setting bit LOOP.SPN.

Long Haul Interface

The FALC®-LH has an integrated short-haul and long-haul line interface, consisting of a receive equalization network and noise filtering.

4.1.1 Receive Equalization Network (E1)

The FALC®-LH automatically recovers the signals received on pins RL1/2 in a range of up to -43 dB. The maximum reachable length with a 22 AWG twisted-pair cable is 1500 m. After reset the FALC®-LH is in “Short Haul“ mode, received signals are recovered up to -10 dB of cable attenuation. Switching in “Long Haul“ mode is done by setting of register LIM0.EQON.
The integrated receive equalization network recovers signals with up to -43 dB of cable attenuation. Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak detected and sliced at 55% of the peak value to produce the digital data stream. The received data is then forwarded to the clock & data recovery unit.

The current equalizer status is indicated by register RES (Receive Equalizer Status) in long haul mode.

4.1.2 Receive Line Attenuation Indication (E1)

Status register RES reports the current receive line attenuation in a range of 0 to -43 dB in 25 steps of approximately 1.7 dB each. The least significant 5 bits of this register indicate the cable attenuation in dB. These 5 bits are only valid in conjunction with the two most significant bits (RES.EV1/0 = 01).

4.1.3 Receive Clock and Data Recovery (E1)

The analog received signal on port RL1/2 is equalized and then peak-detected to produce a digital signal. The digital received signal on port RDIP/N is directly forwarded to the DPLL. The receive clock and data recovery extracts the route clock RCLK from the data stream received at the RL1/2, RDIP/RDIN or ROID lines and converts the data stream into a single rail, unipolar bit stream. The clock and data recovery works with the clock frequency supplied by XTAL1. Normally the clock that is output via pin RCLK is the recovered clock from the signal provided on RL1/2 or RDIP/N and has a duty cycle close to 50 %. The free run frequency is defined by XTAL1 divided by 8 in periods with no signal. The intrinsic jitter generated in the absence of any input jitter is not more than 0.035 UI. In digital bipolar line interface mode the clock and data recovery accepts only HDB3 or AMI coded signals with 50% duty cycle.

4.1.4 Receive Line Coding (E1)

The HDB3 line code or the AMI coding is provided for the data received from the ternary or the dual rail interface. In case of the optical interface a selection between the NRZ code and the CMI Code (1T2B) with HDB3 postprocessing is provided. If CMI code

(1T2B) is selected the receive route clock is recovered from the data stream. The 1T2B decoder does not correct any errors. In case of NRZ coding data is latched with the falling edge of signal RCLKI. The HDB3 code is used along with double violation detection or extended code violation detection (selectable). In AMI code all code violations is detected.
The detected errors increment the code violation counter (16 bits length).

When using the optical interface with NRZ coding, the decoder is by-passed and no code violations are detected.

The signal at the ternary interface is received at both ends of a transformer.

The E1-operating modes 75 or 120 Ω are selectable by switching resistors in parallel. This selection does not require changing transformers.

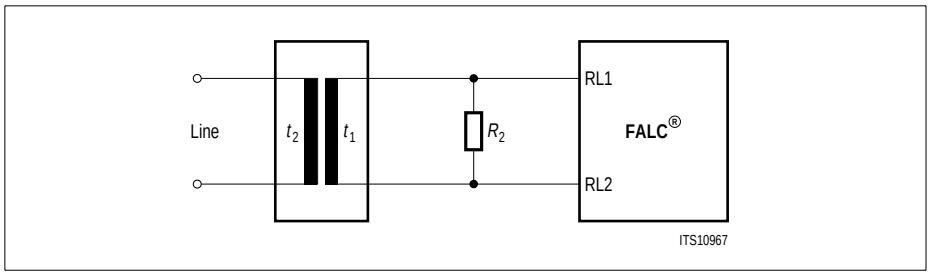


Figure 12 Receiver Configuration (E1)

Table 9 Recommended Receiver Configuration Values (E1)

Parameter	Characteristic Impedance [Ω]	
	120	**75**
R_2 (± 1 %) [Ω]	240	150
$t_2 : t_1$	1 : $\sqrt{2}$	1 : $\sqrt{2}$

4.1.5 Loss of Signal Detection (E1)

There are different definitions for detecting Loss of Signal (LOS) alarms in the ITU-T G.775 and ETS 300233. The FALC®-LH covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable via register IPC.SCI.

- Detection:
  An alarm is generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN/ROID. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS=0). In short haul mode (LIM0.EQON=0) the receive signal level Q is programmable via three control bits LIM1.RIL2...0 in a range of about 1400 to 200 mV differential voltage between pins RL1/2. In long haul mode (LIM0.EQON=1) the analog LOS criteria is defined by the equalizer status. The number N can be set via an 8 bit register PCD. The contents of the PCD register is multiplied by 16, which results in the number of pulse periods or better, the time which has to suspend until the alarm has to be detected. The range therefore results from 16 to 4096 pulse periods. ETS300233 requires detection intervals of at least 1 ms. This time period results always in a LFA (Loss of Frame Alignment) before a LOS is detected.

- Recovery:
  In general the recovery procedure starts after detecting a logical “one“ (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL2...0, LIM0.EQON=0) of the nominal pulse. The value in the 8 bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm. Additional recovery conditions may be programmed by register LIM2.

Note: In long haul mode, LOS alarm is declared either if “no pulses” are detected for the period defined in PCD or the signal level drops below typically about -35 dB of the nominal signal (“low signal level”). Additionally, the incoming data stream is cleared, if this “low signal level” is detected in order to generate a fixed data stream before first bit errors occur. Typically, this loss of signal threshold is about -35 dB.

For recovery this means, that at first the signal level has to increase and then the pulses are counted and compared to PCR to return from LOS indication.

Please also note, that this behavior is slightly different to FALC-LH V1.1.

4.1.6 Receive Jitter Attenuator (E1)

The receive jitter attenuator is placed in the receive path. The jitter attenuator meets the requirements of ITU-T I.431, G. 736-739, G.823 and ETSI TBR12/13.

The internal DCO-R generates a “jitter free“ output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock.The receive jitter attenuator can be either synchronized with the extracted receive clock RCLK or to a 2.048-MHz clock provided on pin SYNC. The received data is written into the receive elastic buffer with RCLK and are read out with the dejittered clock CLK8M/CLKX sourced by DCO-R if it is connected to SCLKR. Optionally a 8 kHz clock is provided on pin XCLK/ FSC or $\overline{\text{FSC}}$.

The DCO-R circuitry attenuates the incoming jittered clock starting at 2 Hz jitter frequency with 20 dB per decade fall off. Wander with a jitter frequency below 2 Hz is passed unattenuated. The intrinsic jitter in the absence of any input jitter is < 0.02 UI.

For some applications it might be useful starting of jitter attenuation at lower frequencies. Therefore the corner frequency is switchable by the factor of ten down to 0.2 Hz (LIM2.SCF).

Jitter attenuation can be achieved either using an external tunable crystal on pins XTAL1/XTAL2 or using the crystal-less jitter attenuation selected by LIM2.DJA1/2. In this case, a stable clock or regular crystal of 16.384 MHz has to be provided on pin XTAL1 (+/- 50 ppm). In crystal-less mode the system clock output on pin CLK16M can be either the dejittered or the non-dejittered clock (LIM3.CSC).

The DCO-R circuitry is automatically centered to the nominal bit rate if the reference clock on pin SYNC/RCLK is missed for two 2.048-MHz clock periods. In analog line interface mode the RCLK is always running. Only in digital line interface mode with single rail data a gapped clock at RCLKI may occur. In this case, DCO-R centers automatically.

The receive jitter attenuator works in two different modes:

- Slave mode
  In Slave mode (LIM0.MAS = 0) the DCO-R is synchronized with the recovered route clock. In case of LOS the DCO-R switches to Master mode automatically.
- Master mode
  In Master mode (LIM0.MAS = 1) the jitter attenuator is in free running mode if no clock on pin SYNC is supplied. If a 2.048 MHz clock at the SYNC input is applied the DCO-R synchronizes to this input.

The following table shows the clock modes with the corresponding synchronization sources.

Table 10 System Clocking (E1)

Mode	Internal LOS Active	SYNC Input	System Clocks generated by DCO-R
Master	independent	Fixed to VSS	Free running, DCO-R centered
Master	independent	2 MHz	Synchronized with SYNC input (external 2 MHz)
Slave	no	Fixed to VSS	Synchronized with Line RCLK
Slave	no	2 MHz	Synchronized with Line RCLK
Slave	yes	Fixed to VSS	Free running, DCO-R is centered
Slave	yes	2 MHz	Synchronized with SYNC input (external 2.048 MHz)

The jitter attenuator meets the jitter transfer requirements of the recommendations I.431 and G.735-739 (refer to **Figure 13**).

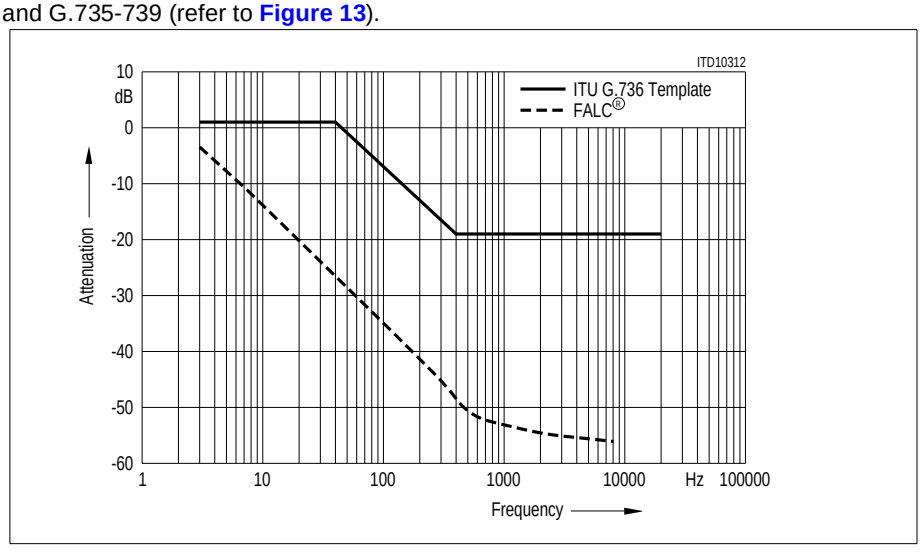


Figure 13 Jitter Attenuation Performance (E1)

Also the requirements of ETSI TBR12/13 are satisfied. Insuring adequate margin against TBR12/13 output jitter limit with 15 UI input at 20 Hz the DCO-R circuitry starts jitter attenuation at nearly 2 Hz.

4.1.7 Jitter Tolerance (E1)

The FALC®-LH receiver's tolerance to input jitter complies to ITU for CEPT application.

Figure 14 shows the curves of different input jitter specifications stated below as well as the FALC®-LH performance.

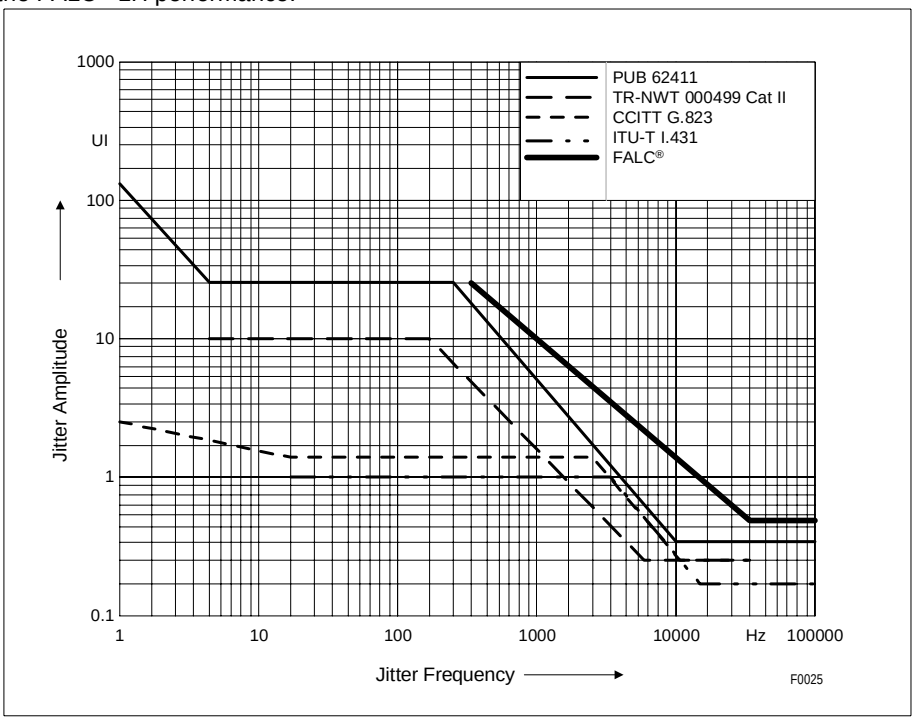


Figure 14 Jitter Tolerance (E1)

4.1.8 Output Jitter (E1)

In the absence of any input jitter the FALC®-LH generates the output jitter, which is specified in the**Table 11** below.

Table 11 Output Jitter (E1)

Specification	Measurement Filter Bandwidth		Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
ITU-T I.431	20 Hz	100 kHz	< 0.02
	700 Hz	100 kHz	< 0.02

4.1.9 Transmit Jitter Attenuator (E1)

The transmit jitter attenuator DCO-X circuitry generates a “jitter free“ transmit clock and meets the following requirements: ITU-T I.431, G. 703, G. 736-739, G.823 and ETSI TBR12/13. The DCO-X circuitry works internally with the same high frequency clock as the receive jitter attenuator it does. It synchronizes either to the working clock of the transmit backplane interface or the clock provided by pin SYNC2 or the receive clock RCLK (remote loop/loop-timed). The DCO-X attenuates the incoming clock jitter starting at 6 Hz with 20 dB per decade fall off. With the jitter attenuated clock, which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock, data is read from the transmit elastic buffer or from the JATT buffer (remote loop with JATT). Wander with a jitter frequency below 6 Hz is passed transparently.

The DCO-X accepts gapped clocks which are used in ATM or SDH/SONET applications. The jitter attenuated transmit clock is output by pin XCLK.

In the loop-timed clock configuration (LIM2.ELT) the DCO-X circuitry generates a transmit clock which is frequency synchronized with RCLK. In this configuration the transmit elastic buffer has to be enabled.

DCO-X can optionally be used with XTAL1 clock reference (selected by LIM1.TCD1 = 1). The dejittered transmit clock can be output on pin CLK16M. In this case the clocks CLKX, CLK8 and $\overline{\text{FSC}}$ are not synchronized with RCLK/SYNC.

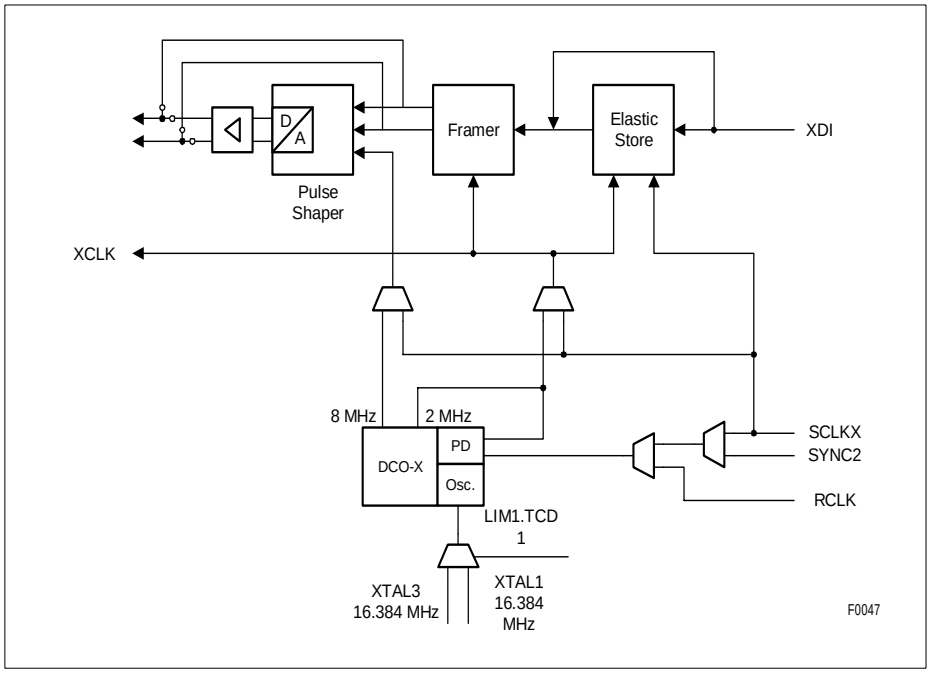


Figure 15 Transmit Clock System (E1)

Note: DR = Dual Rail Interface
DCO-R Digital Controlled Oscillator Receive
DCO-X Digital Controlled Oscillator Transmit

4.1.10 Framer/Synchronizer

The following functions are performed:

- Synchronization on pulse frame and multiframe
- Error indication when synchronization is lost. In this case, AIS is automatically sent to the system side and Remote Alarm to the remote end if en/disabled.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This can be done automatically by the FALC®-LH, or user controlled via the microprocessor interface.
- Detection of remote alarm indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in status registers.
- Generation of various maskable interrupt statuses of the receiver functions.

- Generation of control signals to synchronize the CRC checker and the receive elastic buffer.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC submultiframe according to the CRC 4 procedure (refer to ITU-T G704). These bits are compared with those check bits that are received during the next CRC submultiframe. If there is at least one mismatch, the CRC error counter (16 bit) is incremented.

4.1.11 Receive Elastic Buffer (E1)

The received bit stream is stored in the receive elastic buffer. The memory is organized as a two-frame elastic buffer with a maximum size of 64 × 8 bit. The size of the elastic buffer can be configured independently for the receive and transmit direction. Programming of the receive buffer size is done by SIC1.RBS1/0 :

- RBS1/0 = 00 : two frame buffer or 512 bits
  Maximum of wander amplitude (peak-to-peak): 190 UI (1 UI = 488 ns)
  average delay after performing a slip: about 1 frame

- RBS1/0 = 01 : one frame buffer or 256 bits
  Max. wander amplitude: 94 UI
  average delay after performing a slip: 128 bits, ($\overline{\text{SYPR}}$ = output)

- RBS1/0 = 10 : short buffer or 92 bits :
  Max. wander amplitude: 18 µs
  average delay after performing a slip: 46 bits, ($\overline{\text{SYPR}}$ = output)

- RBS1/0 = 11 : Bypass of the receive elastic buffer, ($\overline{\text{SYPR}}$ = output)

The functions are:

- Clock adaption between system clock (SCLKR) and internally generated route clock (RCLK).
- Compensation of input wander and jitter.
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel data which is circularly written to the elastic buffer using internally generated Receive Route Clock (RCLK).

Reading of stored data is controlled by the System Clock sourced by SCLKR and the Synchronous Pulse ($\overline{\text{SYPR}}$) in conjunction with the programmed offset values for the receive time slot/clock slot counters. After conversion into a serial data stream, the data

is given out via port RDO. If the receive buffer is bypassed, data is clocked off with RCLK instead of SCLKR.

In one frame or short buffer mode the delay through the receive buffer is reduced to an average delay of 128 or 46 bits. Slips are performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size.

The following table gives an overview of the receive buffer operating mode.

Note: Combinations of SIC1.RBS1...0 and LOOP.SFM other than described are not allowed. The use of LOOP.SFM = 1 is not recommended, but possible for FALC®54 compatibility.

Table 12 Receive Buffer Operating Modes (E1)

SIC1.RBS1...0	Buffer Size	TS Offset programing (RC1...0)	Slip performance
11 LOOP.SFM = 0	bypass[1)]	RFM ($\overline{\text{SYPR}}$ = output) must be selected; value of RC1...0 determines the position of RFM	no slips
10 LOOP.SFM = 0	short buffer	RFM ($\overline{\text{SYPR}}$ = output) must be selected; value of RC1...0 determines the position of RFM	yes
01 LOOP.SFM = 0	1 frame	RFM ($\overline{\text{SYPR}}$ = output) must be selected; value of RC1...0 determines the position of RFM	yes
00 LOOP.SFM = 1	1 frame	$\overline{\text{SYPR}}$ is input and determines the frame position together with RC1...0 offset.	Slip conditions are detected and reported, but no slip is performed. Slips have to be initiated by software (reprogramming of RC1...0).
00 LOOP.SFM = 0	2 frames	$\overline{\text{SYPR}}$ is input and determines the frame position together with RC1...0 offset.	yes Slips are performed on the frame boundary

1) In bypass mode the clock provided on pin SCLKR is ignored. Clocking is done with RCLK.

In single frame mode (SIC1. RBS), values of receive time slot offset (RC1/0) have to be specified great enough to prevent too great approach of frame begin (line side) and frame begin (system side).

Figure 16 gives an idea of operation of the receive elastic buffer:
A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive backplane interface. i.e. on the position of pointer R and W within the memory. A positive/negative slip is indicated in the interrupt status bits ISR3.RSP and ISR3.RSN.

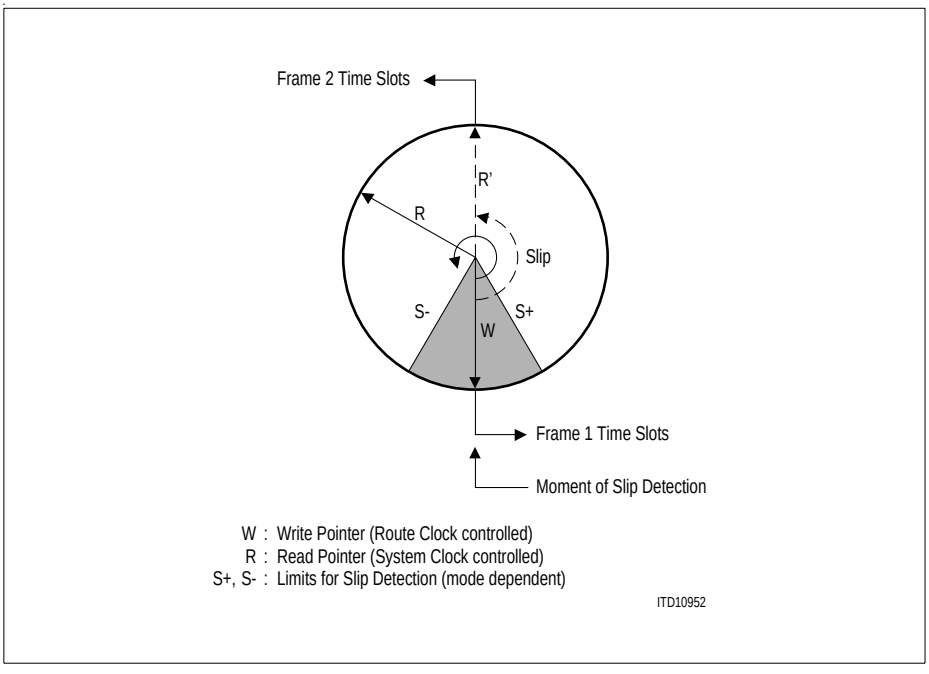


Figure 16 The Receive Elastic Buffer as Circularly Organized Memory

4.1.12 Receive Signaling Controller (E1)

The signaling controller can be programmed to operate in various signaling modes. The FALC®-LH performs the following signaling and data link methods:

4.1.12.1 HDLC or LAPD access

In case of common channel signaling the signaling procedure HDLC/SDLC or LAPD according to Q.921 is supported. The signaling controller of the FALC®-LH performs the FLAG detection, CRC checking, address comparison and zero bit-removing. The received data flow and the address recognition features can be performed in very flexible way, to satisfy almost any practical requirements. Depending on the selected address mode, the FALC®-LH performs a 1 or 2 byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address is interpreted as command/response bit (C/R) and is excluded from the address comparison. Buffering of receive data is done in a 64 byte deep RFIFO.
In signaling controller transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without FLAG recognition, CRC checking or bit-stuffing. This allows user specific protocol variations.
The FALC®-LH offers the flexibility to extract data during certain time slots. Any combination of time slots may be programmed independently for the receive and transmit direction.

4.1.12.2 S_a bit Access (E1)

The FALC®-LH supports the S_a bit signaling of time slot 0 of every other frame as follows:

- the access via register RSW
- the access via registers RSA4-8, capable of storing the information for a complete multiframe
- the access via the 64 byte deep receive FIFO of the signaling controller. This S_a bit access gives the opportunity to receive a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Any combination of S_a bits which should be extracted and stored in the RFIFO may be selected by XC0.SA8E-SA4E. The access to the RFIFO is supported by ISR0.RME/RPF.

4.1.12.3 Channel Associated Signaling CAS (E1, serial mode)

The signaling information is carried in time slot 16 (TS16). The signaling controller samples the bit stream on the receive system side (selected by setting LOOP.SPN=1, LIM3.ESY=1).

The complete CAS multiframe can be transmitted on pin RSIG. The signaling data is clocked with the working clock of the receive highway in conjunction with the receive synchronization pulse ($\overline{\text{SYPR}}$/RFM). Data on RSIG is transmitted in the last 4 bits per time slot and are aligned to the data on RDO. The first 4 bits per time slot can be optionally fixed high or low, except for time slot 0 and 16. In time slot 0 the FAS/NFAS word is transmitted, in time slot 16 the CAS multiframe pattern. Data on RSIG is valid only if the freeze signaling status is inactive. In case of freeze status, old data are repeated. With FMR1.SAIS = 1 an all-ones data stream may be transmitted on RDO and RSIG.

The signaling procedure is done as it is described in ITU-T G.704 and G.732.
The main functions are:

- Synchronization to a CAS multiframe
- Detection of AIS and remote alarm in CAS multiframes
- Separation of CAS service bits

Updating of the receive signaling information is controlled by the freeze signaling status. The freeze signaling status is output on pin $\overline{\text{RFSP}}$/FREEZS and is generated, if:

- Bit FRS1.TSL16LFA = 1 or
- FRS0.LOS=1 or
- a receive slip occurred

The receive signaling buffer is updated if the alarm remains inactive for at least one complete CAS multiframe. Setting of bit SIC2.FFS forces the freeze status active. The current freeze status could be read in register SIS.SFS. Optionally automatic freeze signaling may be disabled by setting bit SIC3.DAF.

The CAS controller acts on the PCM highway side of the receive buffer. Therefore slips disturb CAS data.

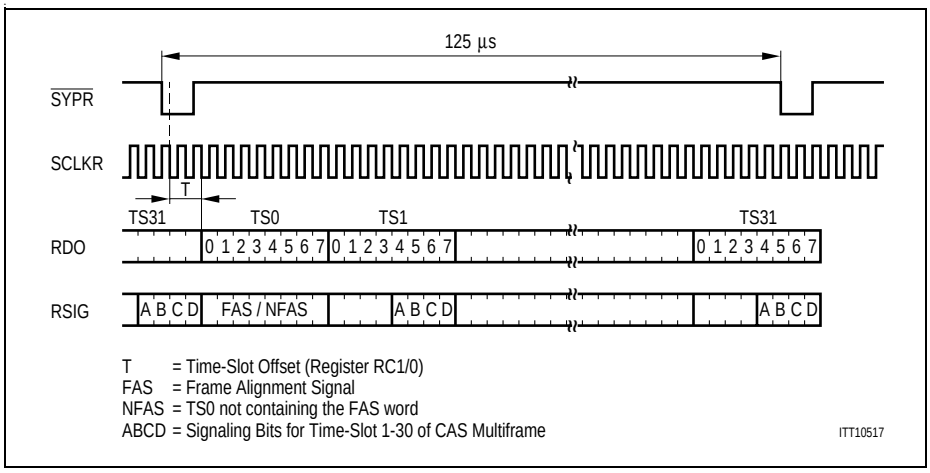


Figure 17 2.048 MHz Receive Signaling Highway (E1)

4.1.12.4 Channel Associated Signaling CAS (E1, µP access mode)

The signaling information is carried in time slot 16 (TS16). Receive data is stored in registers RS1-16 aligned to the CAS multiframe boundary. The signaling controller samples the bit stream on the receive line side.

The signaling procedure is done as it is described in ITU-T G.704 and G.732.
The main functions are:

- Synchronization to a CAS multiframe
- Detection of AIS and remote alarm in CAS multiframes
- Separation of CAS service bits
- Storing of received data in registers RS1...16 with last look capability

Updating of the receive signaling information is controlled by the freeze signaling status. If signaling information is frozen updating of the registers RS1...16 is disabled. The freeze signaling status is output on pin $\overline{\text{RFSP}}$/FREEZS and is generated, if:

- Bit FRS1.TSL16LFA = 1

The receive signaling buffer is updated if the alarm remains inactive for at least one complete CAS multiframe.

To relieve the µP load from always reading the complete RS1-16 buffer every 2 ms the FALC®-LH notifies the µP via interrupt ISR0.CASC only when signaling changes from one multiframe to the next.

The CAS controller acts on the PCM highway side of the receive buffer. Therefore slips disturb CAS data.

4.2 System Interface in E1 Mode

The FALC®-LH offers a flexible feature for system designers where for transmit and receive direction different system clocks and system pulses are necessary. The interface to the receive system highway is realized by two data buses, one for the data RDO and one for the signaling data RSIG. The receive highway is clocked via pin SCLKR/RCLK, while the interface to the transmit system highway is independently clocked via pin SCLKX. Selectable system clock and data rates and their valid combinations are shown in the table below.

Table 13 System Clock and Data Rates (E1)

System Data Rate	Clock Rate 2.048 MHz	Clock Rate 8.192 MHz
2.048 Mbit/s	x[1)]	x
4.096 Mbit/s	--	x

[1)] x = valid; -- = invalid

Generally the data or marker on the system interface are clocked off or latched on the falling edge of the SCLKR/X clock. 8.192-MHz clocking rate allows transmitting of time slots in different channel phases. The active channel phase is selected by RC0.SICS, during the inactive channel phase the output signal is tristated. The signals on pin $\overline{\text{SYPR}}$ in conjunction with the assigned timeslot offset in register RC0 and RC1 define the beginning of a frame on the receive system highway. The signal on pin $\overline{\text{SYPX}}$ in conjunction with the assigned timeslot offset in register XC0 and XC1 define the beginning of a frame on the transmit system highway.

Adjusting the frame begin (time slot 0, bit 0) relative to $\overline{\text{SYPR/X}}$ can be programmed in clock steps in the range of 0...125 µsec.

A receive frame marker RFM can be activated during any bit position of the entire frame. Programming is done with registers RC1/0. The pin function RFM is selected by SIC2.SRFS0. The receive frame marker is active high for one 2.048 MHz cycle (2.048 Mbit/s PCM highway interface mode) or two 8.192 MHz cycles (4.096 Mbit/s PCM highway interface mode) and is clocked off with the falling edge of the clock which is in/output on port SCLKR.

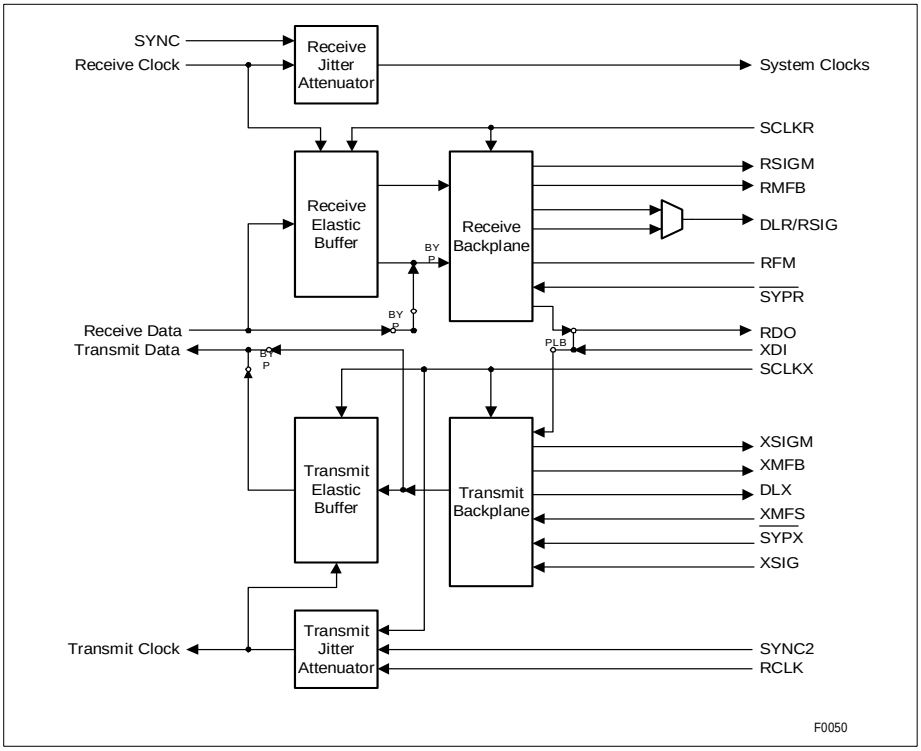


Figure 18 System Interface (E1)

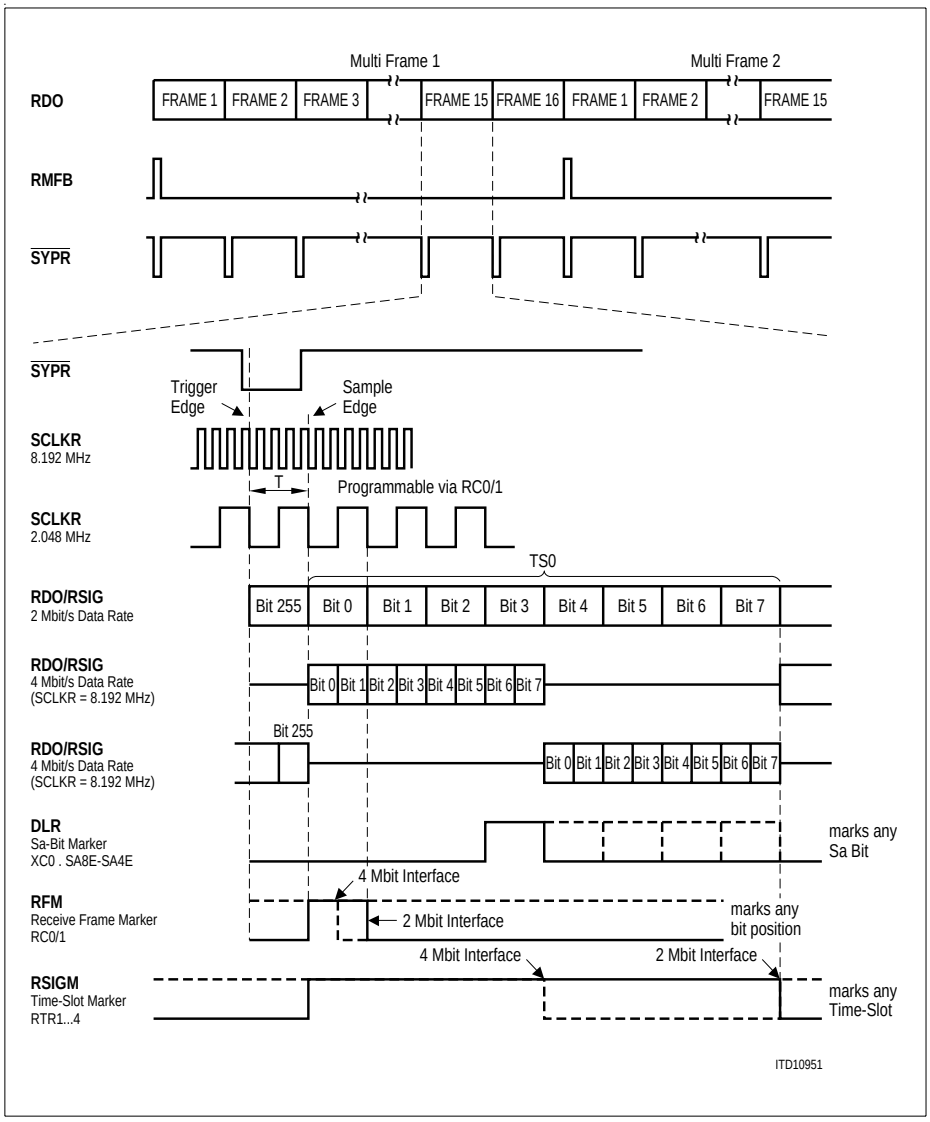


Figure 19 Receive System Interface Clocking (E1)

4.2.1 Time Slot Assigner (E1)

The FALC®-LH offers the flexibility to connect data during certain time slots, as defined by registers RTR1-4 and TTR1-4, to the RFIFO and XFIFO, respectively. Any combinations of time slots can be programmed for the receive and transmit directions. If CCR1.EITS = 1 the selected time slots (RTR1-4) are stored in the RFIFO of the signaling controller and the XFIFO contents are inserted into the transmit path as controlled by registers TTR1-4.

Table 14 Time Slot Assigner (E1)

Receive Time Slot Register	Transmit Time Slot Register	Time Slots	Receive Time Slot Register	Transmit Time Slot Register	Time Slots
RTR 1.7	TTR 1.7	0	RTR 3.7	TTR 3.7	16
RTR 1.6	TTR 1.6	1	RTR 3.6	TTR 3.6	17
RTR 1.5	TTR 1.5	2	RTR 3.5	TTR 3.5	18
RTR 1.4	TTR 1.4	3	RTR 3.4	TTR 3.4	19
RTR 1.3	TTR 1.3	4	RTR 3.3	TTR 3.3	20
RTR 1.2	TTR 1.2	5	RTR 3.2	TTR 3.2	21
RTR 1.1	TTR 1.1	6	RTR 3.1	TTR 3.1	22
RTR 1.0	TTR 1.0	7	RTR 3.0	TTR 3.0	23
RTR 2.7	TTR 2.7	8	RTR 4.7	TTR 4.7	24
RTR 2.6	TTR 2.6	9	RTR 4.6	TTR 4.6	25
RTR 2.5	TTR 2.5	10	RTR 4.5	TTR 4.5	26
RTR 2.4	TTR 2.4	11	RTR 4.4	TTR 4.4	27
RTR 2.3	TTR 2.3	12	RTR 4.3	TTR 4.3	28
RTR 2.2	TTR 2.2	13	RTR 4.2	TTR 4.2	29
RTR 2.1	TTR 2.1	14	RTR 4.1	TTR 4.1	30
RTR 2.0	TTR 2.0	15	RTR 4.0	TTR 4.0	31

4.3 Transmit Path in E1 Mode

Compared to the receive path the inverse functions are performed for the transmit direction.

The interface to the transmit system highway is realized by two data buses, one for the data XDI and one for the signaling data XSIG. The time slot assignment is equivalent to the receive direction.

Latching of data is controlled by the System Clock (SCLKX) and the Synchronous Pulse ($\overline{\text{SYPX}}$/XMFS) in conjunction with the programmed offset values for the Transmit Time slot/Clock slot Counters XC1/0. Refer also to **Table 13** on page **69**.
The received bit stream on ports XDI and XSIG can be multiplexed internally on a time slot basis, if enabled by SIC3.TTRF = 1, if not serial CAS mode is selected (see **Chapter 4.1.12.3** on page **66**). The data received on port XSIG can be sampled if the transmit signaling marker XSIGM is active high. Data on port XDI is sampled if XSIGM is low for the respective time slot. Programming the XSIGM marker is done with registers TTR1-4.

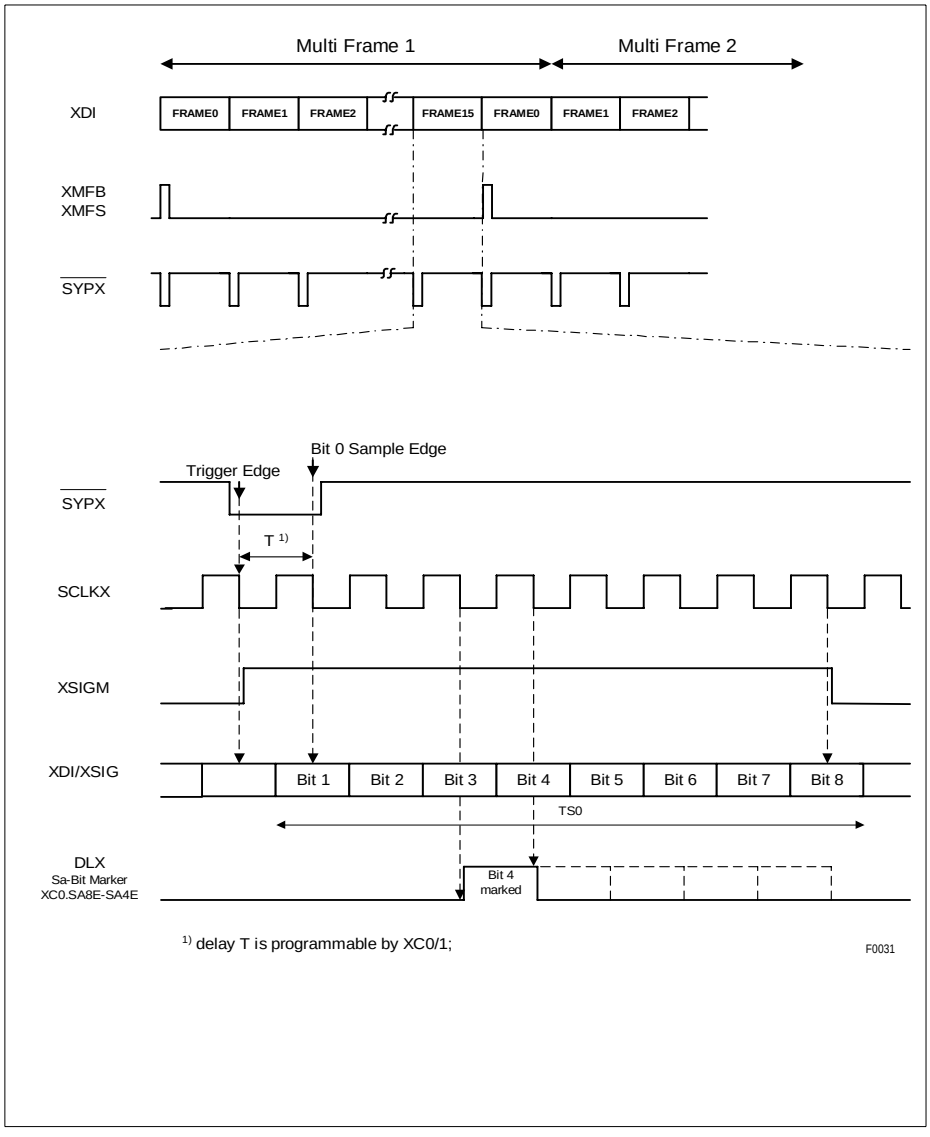


Figure 20 Transmit System Interface Clocking: 2.048 MHz (E1)

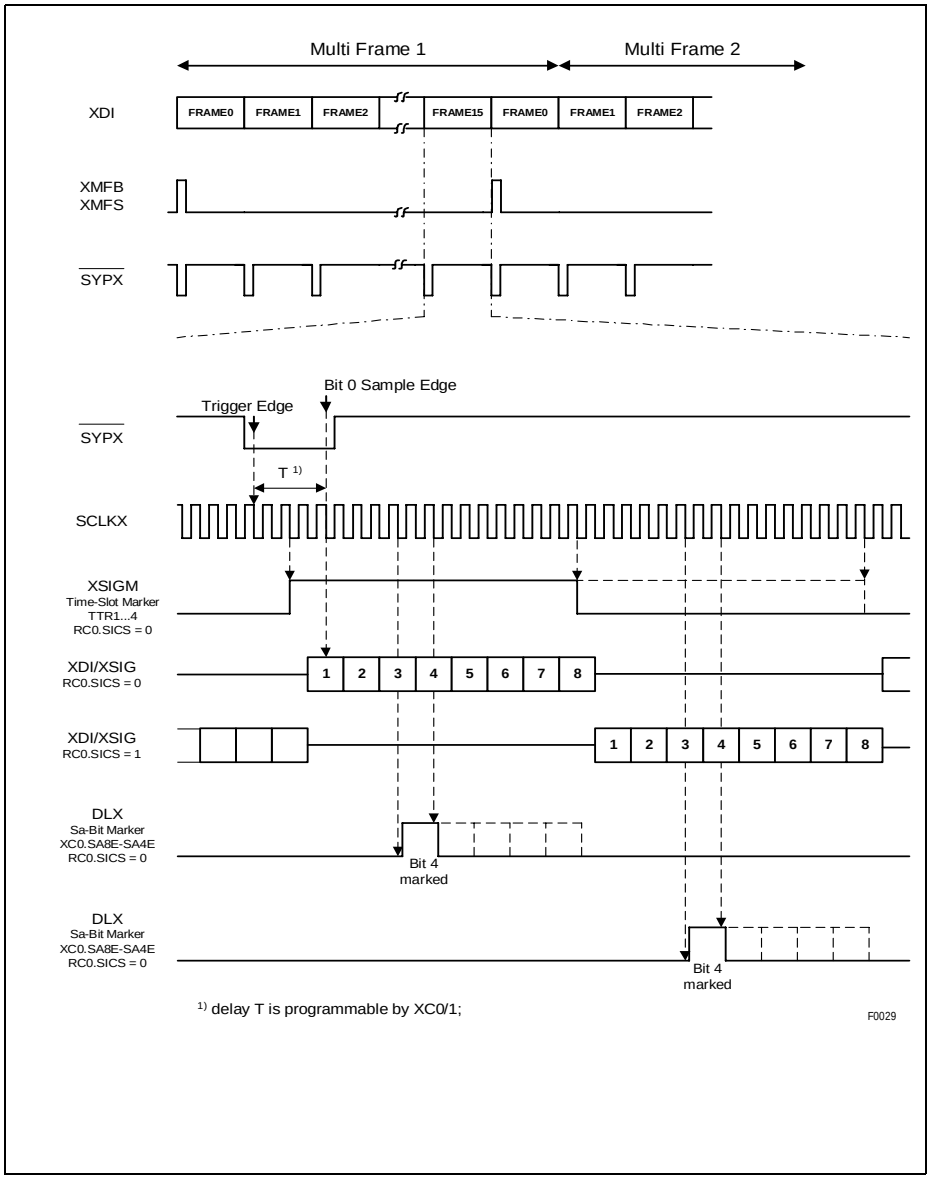


Figure 21 Transmit System Interface Clocking: 8.192 MHz/4.096 Mbit/s (E1)

4.3.1 Transmit Signaling Controller (E1)

Similar to the receive signaling controller the same signaling methods and the same time slot assignment is provided. The FALC®-LH performs the following signaling and data link methods:

4.3.1.1 HDLC or LAPD access

The transmit signaling controller of the FALC®-LH performs the FLAG generation, CRC generation, zero bit-stuffing and programmable IDLE code generation. Buffering of transmit data is done in the 64 byte deep XFIFO. The signaling information is internally multiplexed with the data applied to port XDI or XSIG.
In signaling controller transparent mode, fully transparent data transmission without HDLC framing is performed. Optionally the FALC®-LH supports the continuous transmission of the XFIFO contents.
The FALC®-LH offers the flexibility to insert data during certain time slots. Any combinations of time slots may be programmed separately for the receive and transmit directions.

4.3.1.2 S_a bit Access (E1)

The FALC®-LH supports the S_a bit signaling of time slot 0 of every second frame as follows:

- the access via register XSW
- the access via registers XSA4E...XSA8E, capable of storing the information for a complete multiframe
- the access via the 64 byte deep XFIFO of the signaling controller. This S_a bit access gives the opportunity to send a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Any combination of S_a bits which shall be inserted into the outgoing data stream may be selected by XC0.SA4E...SA8E.

4.3.1.3 Channel Associated Signaling CAS (E1, serial access mode)

In external signaling mode the signaling data is received on port XSIG. The signaling data is sampled with the working clock of the transmit system interface (SCLKX) in conjunction with the transmit synchronization pulse ($\overline{\text{SYPX}}$). Data on XSIG is latched in the bit positions 5...8 per time slot, bits 1...4 are ignored. Time slot 0 and 16 are sampled completely (bit 1...8). The received CAS multiframe is inserted frame aligned into the data stream on XDI. Data sourced by the internal signaling controller overwrites the external signaling data. CAS data is read from XSIG during the last frame of a multiframe, if CRC4/multiframe mode is selected. The CAS-multiframe is aligned to the CRC4-multiframe. Other frames are ignored.

If the FALC®-LH is optioned for no signaling, the data stream from the system interface passes the FALC®-LH undisturbedly.

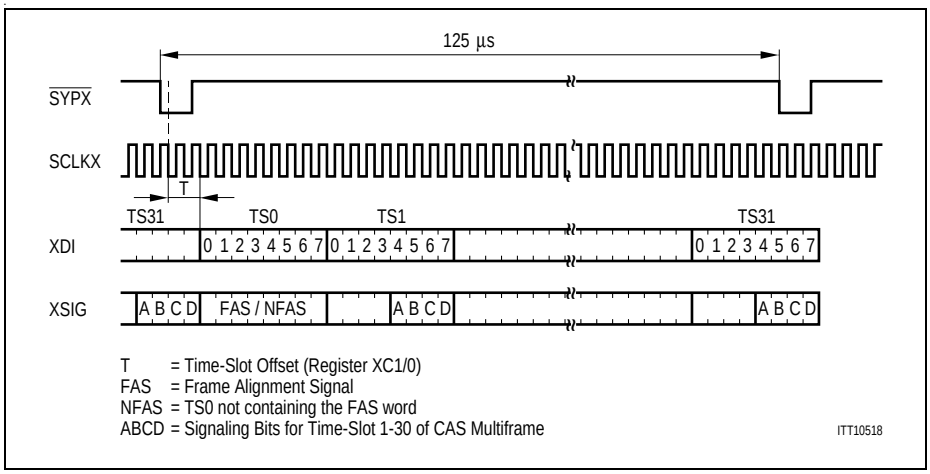


Figure 22 2.048 MHz Transmit Signaling Highway (E1)

4.3.1.4 Channel Associated Signaling CAS (E1, µP access mode)

Transmit data stored in registers XS1-16 is transmitted in time slot 16 aligned to the multiframe boundary. The signaling controller inserts the bit stream either on the transmit line side or if external signaling is enabled on the transmit system side via pin function XSIG.
Data sourced by the internal signaling controller overwrites the external signaling data.

If the FALC®-LH is optioned for no signaling, the data stream from the system interface passes the FALC®-LH undisturbedly.

4.3.2 Transmit Elastic Buffer (E1)

The received bit stream from pin XDI is optionally stored in the transmit elastic buffer. The memory is organized as the receive elastic buffer. The functions are also equal to the receive side. Programming of the transmit buffer size is done by SIC1.XBS1/0 :

- XBS1/0 = 00 : Bypass of the transmit elastic buffer
- XBS1/0 = 01 : one frame buffer or 256 bits
  Max. wander amplitude (peak-to-peak): 94 UI (1 UI = 488 ns)
  average delay after performing a slip: 128 bits
- XBS1/0 = 10 : two frame buffer or 512 bits
  Maximum of wander amplitude: 190 UI
  average delay after performing a slip: 1 frame or 256 bits

- XBS1/0 = 11 : short buffer or 92 bits :
  Max. wander amplitude: 18 µs
  average delay after performing a slip: 46 bits

The functions of the transmit buffer are:

- Clock adaption between system clock (SCLKX) and internally generated transmit clock (XCLK).
- Compensation of input wander and jitter.
- Frame alignment between system frame and transmit line frame
- Reporting and controlling of slips

Writing of received data from XDI is controlled by SCLKX and $\overline{\text{SYPX}}$/XMFS in conjunction with the programmed offset values for the transmit time slot/clock slot counters. Reading of stored data is controlled by the clock generated by DCO-X circuitry and the transmit framer. With the dejittered clock data is read from the transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is done according to the receive direction. Positive/negative slips are reported in interrupt status bits ISR5.XSP and ISR5.XSN. If the transmit buffer is bypassed data is directly transferred to the transmitter.

The following table gives an overview of the transmit buffer operating modes.

Table 15 Transmit Buffer Operating Modes (E1)

SIC1.XBS1...0	Buffer Size	TS Offset programming	Slip performance
00	bypass	enabled	no
11	short buffer	enabled	yes
01	1 frame	enabled	yes
10	2 frames	enabled	yes If XSW.XTM = 1, slip is performed on the frame boundary

4.3.3 Transmitter (E1)

The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the two selectable framing formats
- Insertion of service and data link information
- AIS generation (Alarm indication signal)
- Remote alarm generation
- CRC generation and insertion of CRC bits
- CRC bits inversion in case of a previously received CRC error
- IDLE code generation per DS0

- Auxiliary pattern generation

The frame/multiframe boundaries of the transmitter may be externally synchronized by using the $\overline{\text{SYPX}}$/XMFS pin. Any change of the transmit time slot assignment subsequently produces a change of the framing bit positions on the line side. This feature is required if signaling- and service- bits are routed through the switching network and are inserted in transmit direction via the system interface.

In loop-timed configuration (LIM2.ELT) disconnecting the control of the transmit system highway from the transmitter is done by setting XSW.XTM. The transmitter is now in a free running mode without any possibility to update the multiframe position in case of changing the transmit time slot assignment. The framing bits are generated independent of the transmit system interface. For proper operation the transmit elastic buffer size should be programmed to 2 frames.

The contents of selectable time slots can be overwritten by the pattern defined via register IDLE. The selection of “idle channels” is done by programming the four-byte registers ICB1 ... ICB4.

4.3.4 Transmit Line Interface (E1)

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided by the digital transmitter.

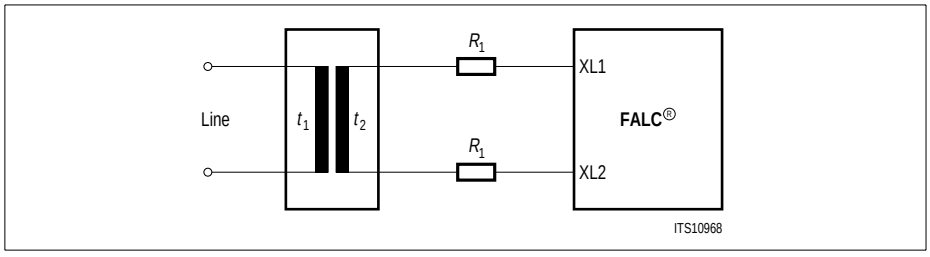


Figure 23 Transmitter Configuration (E1)

Table 16 Example Transmitter Configuration Values (E1)

Parameter[1)]	Characteristic Impedance [Ω]	
	120	75
R_1 (± 1 %) [Ω]	18	18
t2 : t1	1 : $\sqrt{2}$	1 : $\sqrt{2}$

1) includes all parasitics

Similar to the receive line interface three different data types are supported:

- Ternary Signal
  Single rail data is converted into a ternary signal which is output on pins XL1 and XL2. The HDB3 and AMI line code is employed. Selected by FMR0.XC1/0 and LIM1.DRS = 0.
- Dual rail data PCM(+), PCM(–) at multifunction ports XDOP/XDON with 50 % or 100 % duty cycle and with programmable polarity. Line coding is done in the same way as in the ternary interface. Selected by FMR0.XC1/0 and LIM1.DRS = 1.
- Unipolar data on port XOID is transmitted either in NRZ (Non Return to Zero) with 100 % duty cycle or in CMI (Code Mark Inversion or known as 1T2B) Code with or without (FMR3.CMI) preprocessed HDB3 coding to a fibre optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (2048 kHz) and with a programmable polarity. Selection is done by FMR0.XC1 = 0 and LIM1.DRS = 1.

4.3.5 Programmable Pulse Shaper (E1)

The analog transmitter includes a programmable pulse shaper to satisfy the requirements of ITU-T I.431. The amplitude and shape of the transmit pulses are completely programmable via registers XPM0...2 from the microprocessor interface.

The transmitter requires an external step up transformer to drive the line.

4.3.6 Transmit Line Monitor (E1)

The transmit line monitor compares the transmit line pulses on XL1 and XL2 with the transmit input signals received on pins XL1M and XL2M. The monitor detects faults on the primary side of the transformer and protects the device from damage by setting the transmit lines into high impedance state automatically. Faults on the secondary side can not be detected. To detect shorts, the configuration shown in **Figure 24** must be provided and the default (reset) value of registers XPM0...2 must be selected. Otherwise a short detection can not be guaranteed. Two conditions are detected by the monitor: “Transmit Line Ones Density“ (more than 31 consecutive zeroes) and “Transmit Line Shorted“. In both cases a transmit line monitor status change interrupt is provided.

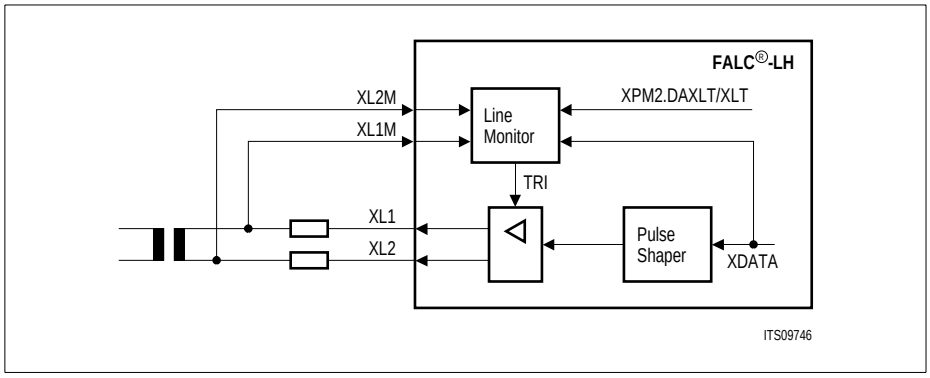


Figure 24 Transmit Line Monitor Configuration (E1)

4.4 Framer Operating Modes (E1)

4.4.1 General

Bit: FMR1.PMOD = 0

PCM line bit rate	:	2.048 Mbit/s
Single frame length	:	256 bit, No. 1 … 256
Framing frequency	:	8 kHz
HDLC controller	:	nx64 kbit/s, n = 1...32 or nx4 kbit/s, n=1...5
Organization	:	32 time slots, No. 0 … 31 with 8 bits each, No. 1 … 8

The operating mode of the FALC®-LH is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The FALC®-LH implements all of the standard framing structures for E1 or PCM 30 (CEPT, 2.048 Mbit/s) carriers. The internal HDLC- or CAS Controller supports all signaling procedures including signaling frame synchronization/synthesis and signaling alarm detection in all framing formats. The time slot assignment from the PCM line to the system highway and vice versa. is performed without any changes of numbering (TS0 ↔ TS0, … , TS31 ↔ TS31).

Summary of E1- Framing Modes

- Doubleframe format according to ITU-T G. 704
- Multiframe format according to ITU-T G. 704
- CRC4 processing according to ITU-T G. 706
- Multiframe format with CRC4 to non CRC4 interworking according to ITU-T G. 706
- Multiframe format with modified CRC4 to non CRC4 interworking
- Multiframe format with CRC4 performance monitoring

After RESET, the FALC®-LH is switched into doubleframe format automatically. Switching between the framing formats is done via bit FMR2.RFS1/0 and FMR3.EXTIW for the receiver and FMR1.XFS for the transmitter.

4.4.2 Doubleframe Format (E1)

The framing structure is defined by the contents of time slot 0 (refer to **Table 17**).)

Table 17 Allocation of Bits 1 to 8 of Time Slot 0 (E1)

Bit Number / Alternate Frames	1	2	3	4	5	6	7	8
Frame Containing the Frame Alignment Signal	S_i	0	0	1	1	0	1	1
	Note 1	Frame Alignment Signal						
Frame not Containing the Frame Alignment Signal or Service Word	S_i	1	A	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
	Note 1	Note 2	Note 3	Note 4				

Note:

1. *S_i bits: reserved for international use. If not used, these bits should be fixed to '1'. Access to received information via bits RSW.RSI and RSP.RSIF. Transmission is enabled via bits XSW.XSIS and XSP.XSIF.*
2. *Fixed to '1'. Used for synchronization.*
3. *Remote alarm indication: In undisturbed operation '0'; in alarm condition '1'.*
4. *S_a bits: Reserved for national use. If not used, they should be fixed at '1'. Access to received information via bits RSW.RY0 ... RY4. Transmission is enabled via bits XSW.XY0 ... XY4. HDLC-signaling in bits Sa4- Sa8 is selectable. (*)*

Note: (*) As a special extension for double frame format, the S_a-bit registers RSA4-8/XSA4-8 may be used optionally.

4.4.2.1 Transmit Transparent Modes

In transmit direction, contents of time slot 0 frame alignment signal of the outgoing PCM frame are normally generated by the FALC®-LH. However, transparency for the complete time slot 0 can be achieved by selecting the transparent mode XSP.TT0. With the Transparent Service Word Mask register TSWM the S_i-bits, A-bit and the SA4-8 bits can be selectively switched through transparently. XSW.XTM = 0 must be selected.

Table 18 Transmit Transparent Mode (Doubleframe E1)

Transmit Transparent Source for				
Enabled by	**Framing**	**A Bit**	**S_a Bits**	**S_i Bits**
–	(int. generated)	XSW.XRA[2)]	XSW.XY0 ... 4[3)]	XSW.XSIS,XSP.XSIF
XSP.TT0	via pin XDI[1)]	via pin XDI	via pin XDI	via pin XDI
TSWM.TSIF	(int. generated)	XSW.XRA	XSW.XY0 ... 4	via pin XDI
TSWM.TSIS	(int. generated)	XSW.XRA	XSW.XY0 ... 4	via pin XDI
TSWM.TRA	(int. generated)	via pin XDI	XSW.XY0 ... 4	XSW.XSIS,XSP.XSIF
TSWM.TSA4-8	(int. generated)	XSW.XRA	via pin XDI	XSW.XSIS,XSP.XSIF

1) pin XDI or XSIG or XFIFO-Buffer (signaling controller)

2) Additionally, automatic transmission of the A-bit is selectable

3) As a special extension for double frame format, the Sa-bit register may be used optionally.

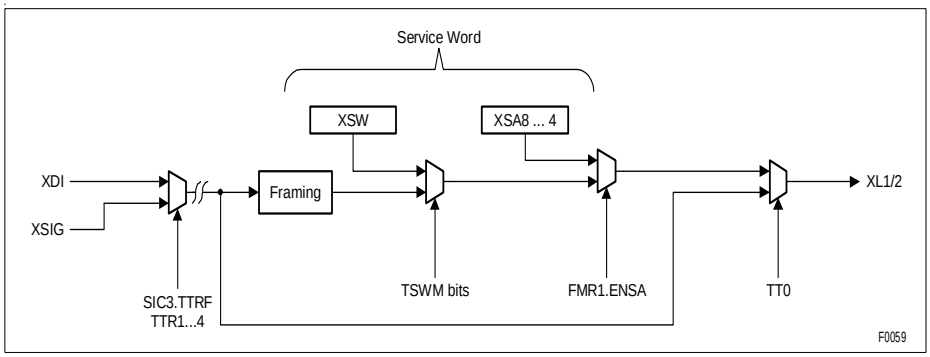


Figure 25 Data Flow in Transparent Mode

4.4.2.2 Synchronization Procedure

Synchronization status is reported via bit FRS0.LFA. Framing errors are counted by the Framing Error Counter (FEC). Asynchronous state is reached after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (bit 2 = 0 in time slot 0 of every other frame not containing the frame alignment word), the selection is done via bit RC1.ASY4. Additionally, the service word condition can be disabled. When the framer lost its synchronization an interrupt status bit ISR2.LFA is generated.

In asynchronous state, counting of framing errors and detection of remote alarm is stopped. AIS is automatically sent to the backplane interface (can be disabled via bit FMR2.DAIS).

Further on the updating of the registers RSA6S and RS1-16 is halted (remote alarm indication, S_a/S_i-Bit access).

The resynchronization procedure starts automatically after reaching the asynchronous state. Additionally, it may be invoked user controlled via bit: FMR0.FRS (Force Resynchronization: the FAS word detection is interrupted until the framer is in the asynchronous state. After that, resynchronization starts automatically).

Synchronous state is established after detecting:

- a correct FAS word in frame n,
- the presence of the correct service word (bit 2 = 1) in frame n + 1,
- a correct FAS word in frame n + 2.

If the service word in frame n + 1 or the FAS word in frame n + 2 or both are not found searching for the next FAS word starts in frame n + 2 just after the previous frame alignment signal.

Reaching the synchronous state causes a frame alignment recovery interrupt status ISR2.FAR if enabled. Undisturbed operation starts with the beginning of the next doubleframe.

4.4.2.3 A-Bit Access

If the FALC®-LH detects a remote alarm indication in the received data stream the interrupt status bit ISR2.RA is set. With setting of bit XSW.XRA a remote alarm (RAI) is send to the far end.

By setting FMR2.AXRA the FALC®-LH automatically transmit the remote alarm bit = 1 in the outgoing data stream if the receiver detects a loss of frame alignment FRS0.LFA = 1. If the receiver is in synchronous state FRS0.LFA = 0 the remote alarm bit is reset.

Note: The A-bit may be processed via the system interface. Setting bit TSWM.TRA enables transparency for the A bit in transmit direction (refer to ***Table Table 18****).*

4.4.2.4 S_a - Bit Access

As an extension for access to the S_a-bits via registers RSA4-8/XSA4-8 an option is implemented to allow the usage of internal S_a-bit registers RSA4-8/XSA4-8 in doubleframe format.

This function is enabled by setting FMR1.ENSA = 1 for the transmitter and FMR1.RFS1/0 = 01 for the receiver. The FALC®-LH works then internally with a 16-frame structure but no CRC multiframe alignment/generation is performed.

4.4.3 CRC-Multiframe (E1)

The multiframe structure shown in **Table 19** is enabled by setting bit: FMR2.RFS1/0 for the receiver and FMR1.XFS for the transmitter.

Multiframe	:	2 submultiframes = 2 × 8 frames
Frame alignment	:	refer to section Doubleframe Format
Multiframe alignment	:	bit 1 of frames 1, 3, 5, 7, 9, 11 with the pattern ‘001011’
CRC bits	:	bit 1 of frames 0, 2, 4, 6, 8, 10, 12, 14
CRC block size	:	2048 bit (length of a submultiframe)
CRC procedure	:	CRC4, according to ITU-T G.704, G.706)

Table 19 CRC-Multiframe Structure (E1)

	Sub-Multiframe	Frame Number	Bits 1 to 8 of the Frame							
			1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Multiframe	I	0	C_1	0	0	1	1	0	1	1
		1	0	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		2	C_2	0	0	1	1	0	1	1
		3	0	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		4	C_3	0	0	1	1	0	1	1
		5	1	1	A	S_{a4}	S_{a5}	S_{a63}	S_{a7}	S_{a8}
		6	C_4	0	0	1	1	0	1	1
		7	0	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}
	II	8	C_1	0	0	1	1	0	1	1
		9	1	1	A	S_{a4}	S_{a5}	S_{a61}	S_{a7}	S_{a8}
		10	C_2	0	0	1	1	0	1	1
		11	1	1	A	S_{a4}	S_{a5}	S_{a62}	S_{a7}	S_{a8}
		12	C_3	0	0	1	1	0	1	1
		13	E*	1	A	S_{a4}	S_{a5}	S_{a63}	S_{a7}	S_{a8}
		14	C_4	0	0	1	1	0	1	1
		15	E*	1	A	S_{a4}	S_{a5}	S_{a64}	S_{a7}	S_{a8}

E: Spare bits for international use. Access to received information via bits RSP.RS13 and RSP.RS15. Transmission is enabled via bits XSP.XS13 and XSP.XS15. Additionally, automatic transmission for submultiframe error indication is selectable.

S_a: Spare bits for national use. Additionally, Sa bit access via registers RSA4 … 8 and XSA4 … 8 is provided. HDLC-signaling in bits Sa4- Sa8 is selectable.

C_1 … C_4: Cyclic redundancy check bits.

A: Remote alarm indication. Additionally, automatic transmission of the A-bit is selectable.

For transmit direction, contents of time slot 0 are additionally determined by the selected transparent mode (see also **Figure 25**):

Table 20 Transmit Transparent Mode (CRC Multiframe E1)

	Transmit Transparent Source for			
enabled by	**Framing + CRC**	**A Bit**	**Sa Bits**	**E Bits**
–	(int. generated)	XSW.XRA[2)]	XSW.XY0 … 4[3)]	XSP.XS13/XS15[4)]
XSP.TT0	via pin XDI[1)]	via pin XDI	via pin XDI	via pin XDI
TSWM.TSIF	via pin XDI	XSW.XRA[1)]	XSW.XY0 … 4[2)]	(int. generated)
TSWM.TSIS	via pin XDI	XSW.XRA[1)]	XSW.XY0 … 4[2)]	via pin XDI
TSWM.TRA	(int. generated)	via pin XDI	XSW.XY0 … 4[2)]	XSP.XS13/XS15[3)]
TSWM.TSA4–8	(int. generated)	XSW.XRA[1)]	via pin XDI	XSP.XS13/XS15[3)]

1) pin XDI or XSIG or XFIFO buffer (signaling controller)

2) Automatic transmission of the A-bit is selectable

3) The S_a-bit register XSA4-8 may be used optionally

4) Additionally, automatic transmission of submultiframe error indication is selectable

The CRC procedure is automatically invoked when the multiframe structure is enabled. CRC errors in the received data stream are counted by the 16 bit CRC Error Counter CEC (one error per submultiframe, maximum).

Additionally a CRC4 error interrupt status ISR0.CRC4 may be generated if enabled by IMR0.CRC4.

All CRC bits of one outgoing submultiframe are automatically inverted in case a CRC error is flagged for the previous received submultiframe. This function is enabled via bit RC0.CRCI. Setting the bit RC0.XCRCI inverts the CRC bits before transmission to the distant end. The function of RC0.XCRCI and RC0.CRCI are logically ored.

4.4.3.1 Synchronization Procedure

Multiframe alignment is assumed to have been lost if doubleframe alignment has been lost (flagged on status bit FRS0.LFA). The rising edge of this bits causes an interrupt.

The multiframe resynchronization procedure starts when doubleframe alignment has been regained which is indicated by an interrupt status bit ISR2.FAR. For doubleframe synchronization refer to section doubleframe format. It may also be invoked by the user by setting

- bit FMR0.FRS for complete doubleframe **and** multiframe re-synchronization
- bit FMR1.MFCS for multiframe re-synchronization only.

The CRC checking mechanism is enabled after the first correct multiframe pattern has been found. However, CRC errors are not counted in asynchronous state.

In doubleframe asynchronous state, counting of framing errors, CRC4 bit errors and detection of remote alarm is stopped. AIS is automatically sent to the backplane interface (can be disabled via bit FMR2.DAIS). Further on the updating of the registers RSA6S and RS1-16 is halted (remote alarm indication, S_a/S_i-bit access).

The multiframe synchronous state is established after detecting two correct multiframe alignment signals at an interval of n × 2 ms (n = 1, 2, 3 ...). The Loss of multiframe alignment flag FRS0.LMFA is reset. Additionally an interrupt status multiframe alignment recovery bit ISR2.MFAR is generated with the falling edge of bit FRS0.LMFA.

4.4.3.2 Automatic Force Resynchronization (E1)

In addition, a search for Doubleframe alignment is automatically initiated if two multiframe pattern with a distance of n × 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained (bit FMR1.AFR). A new search for frame alignment is started just after the previous frame alignment signal.

4.4.3.3 Floating Multiframe Alignment Window (E1)

After reaching doubleframe synchronization a 8 ms timer is started. If a multiframe alignment signal is found during the 8 ms time interval the internal timer is reset to remaining 6 ms in order to find the next multiframe signal within this time. If the multiframe signal is not found for a second time an interrupt status ISR0.T8MS is provided. This interrupt usually occurs every 8 ms until multiframe synchronization is achieved.

4.4.3.4 CRC4 Performance Monitoring (E1)

In the synchronous state checking of multiframe pattern is disabled. However, with bit FMR2.ALMF an automatic multiframe resynchronization mode can be activated. If 915 out of 1000 errored CRC submultiframes are found then a false frame alignment is assumed and a search for double- and multiframe pattern is initiated. The new search for frame alignment is started just after the previous basic frame alignment signal.

4.4.3.5 Modified CRC4 Multiframe Alignment Algorithm (E1)

The modified CRC4 multiframe alignment algorithm allows an automatic interworking between framers with and without a CRC4 capability. The interworking is realized as it is described in ITU-T G.706 Appendix B and shown in **Figure 4.5** on **page 93**.

If doubleframe synchronization is consistently present but CRC4 multiframe alignment is not achieved within 400 ms it is assumed that the distant end is initialized to doubleframe format. The CRC4 to non-CRC4 interworking is enabled via FMR2.RFS1/0 = 11 and is activated only if the receiver has lost its synchronization. If doubleframe alignment (basic frame alignment) is established a 400 ms timer and searching for multiframe alignment is started. A research for basic frame alignment is initiated if the CRC4 multiframe

synchronization could not be achieved within 8 ms and is started just after the previous frame alignment signal. The research of the basic frame alignment is done in parallel and is independent of the synchronization procedure of the primary basic frame alignment signal. During the parallel search all receiver functions are based on the primary frame alignment signal, like framing errors, S_a-, S_i-, A-bits ...). All subsequent multiframe searches are associated with each basic framing sequence found during the parallel search.

If the CRC4 multiframe alignment sequence was not found within the time interval of 400 ms, the receiver is switched into a non-CRC4 mode indicated by setting the bit FRS0.NMF (No Multiframing Found) and ISR2.T400MS. In this mode checking of CRC bits is disabled and the received E-bits are forced to low. The transmitter framing format is not changed. Even if multiple basic FAS resynchronizations have been established during the parallel search, the receiver is maintained to the initially determined primary frame alignment signal location.

However, if the CRC4 multiframe alignment could be achieved within the 400 ms time interval assuming a CRC4 to CRC4 interworking, then the basic frame alignment sequence associated to the CRC4 multiframe alignment signal is chosen. If necessary, the primary frame alignment signal location is adjusted according to the multiframe alignment signal. The CRC4 performance monitoring is started if enabled by FMR2.ALMF and the received E-bits are processed in accordance with ITU-T G.704.

Switching into the doubleframe format (non CRC4) mode after 400 ms can be disabled by setting of FMR3.EXTIW. In this mode the FALC®-LH continues search for multiframing. In the interworking mode setting of bit FMR1.AFR is not allowed.

4.4.3.6 A-Bit Access (E1)

If the FALC®-LH detects a remote alarm indication (bit 2 in TS0 not containing the FAS word) in the received data stream the interrupt status bit ISR2.RA is set. With the deactivation of the remote alarm the interrupt status bit ISR2.RAR is generated.

By setting FMR2.AXRA the FALC®-LH automatically transmits the remote alarm bit = 1 in the outgoing data stream if the receiver detects a loss of frame alignment (FRS0.LFA = 1). If the receiver is in synchronous state (FRS0.LFA = 0) the remote alarm bit is reset in the outgoing data stream.

Additionally, if bit FMR3.EXTIW is set and the multiframe synchronous state could not be achieved within the 400 ms after finding the primary basic framing, the A-bit is transmitted active high to the remote end until the multiframing is found.

*Note: The A-bit may be processed via the system interface. Setting bit TSWM.TRA enables transparency for the A bit in transmit direction (refer to **Table 20**).*

4.4.3.7 S_a - Bit Access (E1)

Due to signaling procedures using the five S_a bits (S_{a4} … S_{a8}) of every other frame of the CRC multiframe structure, three possibilities of access via the microprocessor are implemented.

- The standard procedure allows reading/writing the S_a-bit registers RSW, XSW without further support. The S_a-bit information is updated every other frame.
- The advanced procedure, enabled via bit FMR1.ENSA, allows reading/writing the S_a-bit registers RSA4 … 8, XSA4 … 8.

A transmit or receive multiframe begin interrupt (ISR0.RMB or ISR1.XMB) is provided.

Registers RSA4-8 contains the service word information of the previously received CRC-multiframe or 8 doubleframes (bit slots 4-8 of every service word). These registers are updated with every multiframe begin interrupt ISR0.RMB.

With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of this registers XSA4-8 are copied into shadow registers. The contents is subsequently sent out in the service words of the next outgoing CRC multiframe (or every doubleframes) if none of the time slot 0 transparent modes is enabled. The transmit multiframe begin interrupt XMB request that these registers should be serviced. If requests for new information is ignored, current contents is repeated.

- The extended access via the receive and transmit FIFOs of the signaling controller. In this mode it is possible to transmit/receive a HDLC frame or a transparent bit stream in any combination of the S_a bits. Enabling is done by setting of bit CCR1.EITS and the corresponding bits XC0.SA8E-4E/TSWM.TSA8-4 and resetting of registers TTR1-4, RTR1-4 and FMR1.ENSA. The access to and from the FIFOs is supported by ISR0.RME,RPF and ISR1.XPR,ALS.

SA6-Bit Detection according to ETS 300233

Four consecutive received SA6-bits are checked on the by ETS 300233 defined SA6-bit combinations. The FALC®-LH detects following fixed SA6-bit combinations: SA61, SA62, SA63,SA64 = 1000; 1010; 1100; 1110; 1111. All other possible 4-bit combinations are grouped to status “X”.

A valid SA6-bit combination must occur three times in a row. The corresponding status bit in register RSA6S is set. Register RSA6S is from type “Clear on Read”. With any change of state of the SA6-bit combinations an interrupt status ISR0.SA6SC is generated.

During the basic frame asynchronous state updating of register RSA6S and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the SA6-bit combinations can be done either synchronous or asynchronous to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synchronous state (FRS0.LMFA=0). In asynchronous detection mode updating is independent to the multiframe synchronous state.

Sa6 Bit Error Indication Counters

The Sa6 bit error indication counter CRC2L/H (16 bits) counts the received Sa6 bit sequence 0001 or 0011 in every CRC submultiframe. In the primary rate access digital section this counter option gives information about CRC errors reported from the TE via Sa6 bit. Incrementing is only possible in the multiframe synchronous state.

The Sa6 bit error indication counter CRC3L/H (16 bits) counts the received Sa6 bit sequence 0010 or 0011 in every CRC submultiframe. In the primary rate access digital section this counter option gives information about CRC errors detected at T-reference point and reporting them via the Sa6 bit. Incrementing is only possible in the multiframe synchronous state.

4.4.3.8 E-Bit Access (E1)

Due to signaling requirements, the E bits of frame 13 and frame 15 of the CRC multiframe can be used to indicate received errored submultiframes:

Submultiframe I status E- Bit located in frame 13
Submultiframe II status E- Bit located in frame 15

no CRC error: : E = 1

CRC error: : E = 0

Standard Procedure

After reading the Submultiframe Error Indication RSP.SI1 and RSP.SI2, the microprocessor has to update contents of register XSP (XS13, XS15). Access to these registers has to be synchronized with Transmit or Receive Multiframe Begin Interrupts (ISR0.RMB or ISR1.XMB).

Automatic Mode

In the multiframe synchronous state the E-bits are processed according to ITU-T G.704 independently of bit XSP.EBP (E-bit polarity selection).

By setting bit XSP.AXS status information of received submultiframes is automatically inserted in the E-bit position of the outgoing CRC multiframe without any further interventions of the microprocessor.

In the doubleframe and multiframe asynchronous state the E-bits are set or cleared, depending on the setting of bit XSP.EBP.

Submultiframe Error Indication Counter

The EBC (E-Bit) Counter EBCL and EBCH (16 bits) counts zeros in E-bit position of frame 13 and 15 of every received CRC Multiframe. This counter option gives information about the outgoing transmit PCM line if the E bits are used by the remote end

for submultiframe error indication. Incrementing is only possible in the multiframe synchronous state.

*Note: E-bits may be processed via the system interface. Setting bit TSWM.TSIS enables transparency for E bits in transmit direction (refer to **Table 20**).*

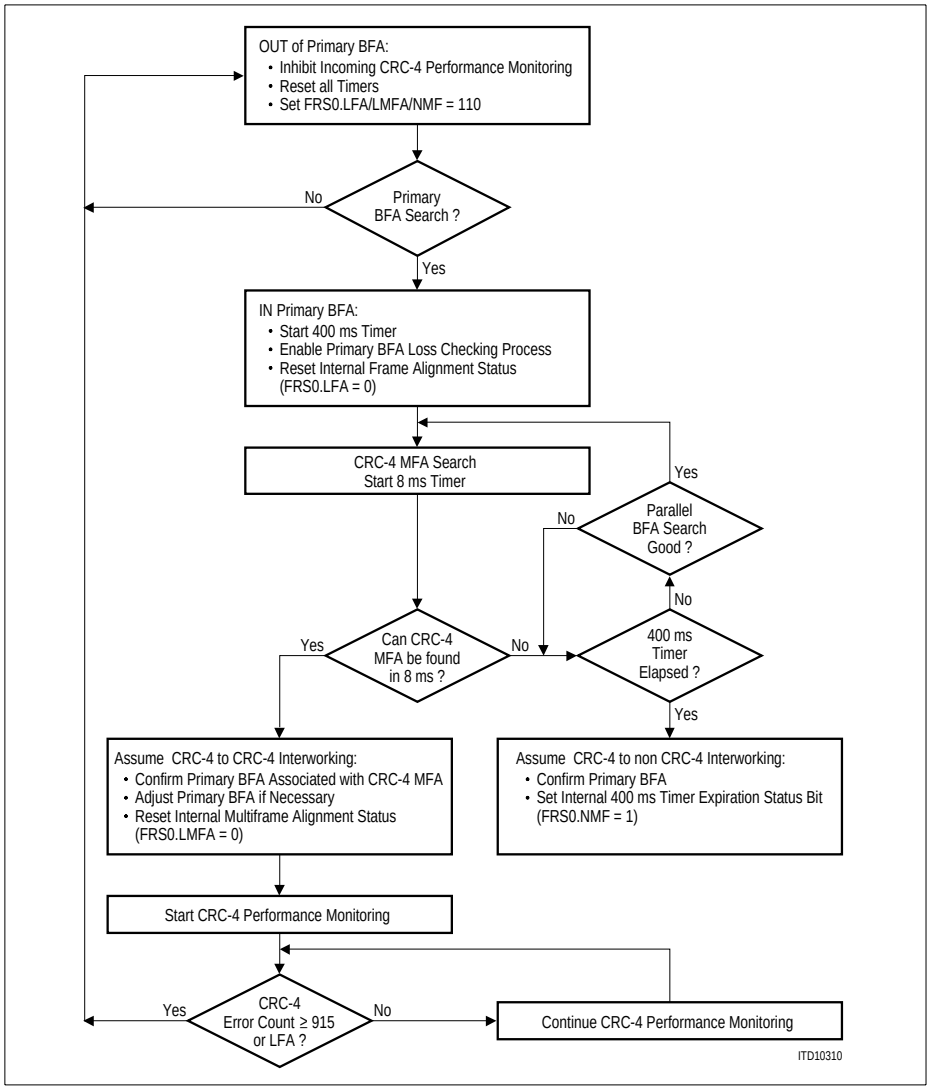


Figure 26 CRC4 Multiframe Alignment Recovery Algorithms

4.5 Additional Functions (E1)

4.5.1 Error Performance Monitoring and Alarm Handling

Alarm Indication Signal: Detection and recovery is flagged by bit FRS0.AIS and ISR2.AIS. Transmission is enabled via bit FMR1.XAIS.

Loss of Signal: Detection and recovery is flagged by bit FRS0.LOS and ISR2.LOS.

Remote Alarm Indication: Detection and release is flagged by bit FRS0.RRA, RSW.RRA and ISR2.RA/RAR. Transmission is enabled via bit XSW.XRA.

AIS in time slot 16: Detection and release is flagged by bit FRS1.TS16AIS and ISR3.AIS16. Transmission is enabled by writing all ones in registers XS1-16.

LOS in time slot 16: Detection and release is flagged by bit FRS1.TS16LOS. Transmission is enabled by writing all zeros in registers XS1-16.

Remote Alarm in time slot 16: Detection and release is flagged by bit FRS1.TS16RA and ISR3.RA16. Transmission is enabled via bit CCR1.XTS16RA or XS1.2.

Transmit Line Shorted: Detection and release is flagged by bit FRS1.XLS and ISR1.XLSC.

Transmit Ones Density: Detection and release is flagged by bit FRS1.XLO and ISR1.XLSC.

Table 21 Summary of Alarm Detection and Release (E1)

Alarm	Detection Condition	Clear Condition
Loss of Signal (LOS)	no transitions (logical zeros) in a programmable time interval of 16...4096 consecutive pulse periods. Programmable receive input signal threshold	programmable number of ones (1-256) in a programmable time interval of 16...4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold.
Alarm Indication Signal (AIS)	FMR0.ALM = 0: less than 3 zeros in 250 µs and loss of frame alignment declared FMR0.ALM = 1: less than 3 zeros in each of two consecutive 250 µs periods	FMR0.ALM = 0: more than 2 zeros in 250 µs FMR0.ALM = 1: more than 2 zeros in each of two consecutive 500 µs periods
Remote Alarm (RRA)	bit 3 = 1 in time slot 0 not containing the FAS word	set conditions no longer detected.

Table 21 Summary of Alarm Detection and Release (E1) (cont'd)

Alarm	Detection Condition	Clear Condition
Remote Alarm in time slot 16 (TS16RA)	Y-bit = 1 received in CAS multiframe alignment word	Y-bit = 0 received in CAS multiframe alignment word
Loss of Signal in time slot 16 (TS16LOS)	all zeros for at least 16 consecutively received time slots 16	receiving a one in time slot 16
Alarm Indication Signal in time slot 16 (TS16AIS)	time slot 16 containing less than 4 zeros in each of two consecutive CAS multiframes periods	time slot 16 containing more than 3 zeros in each of two consecutive CAS multiframes periods
Transmit Line Short (XLS)	If XL1 and XL2 are shortened for at least 32 pulses; pins XL1 and XL2 are forced into a high impedance state automatically, if bit XPM2.DAXLT is reset.	After 32 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still existing, the outputs XL1/2 are switched into high impedance state again. When the short disappears pins XL1/2 are activated automatically.
Transmit Ones Density (XLO)	32 consecutive zeros in the transmit data stream on XL1/2	Cleared with each transmitted pulse

4.5.2 Auto Modes

- Automatic remote alarm access
  If the receiver has lost its synchronization a remote alarm can be sent automatically, if enabled by bit FMR2.AXRA to the distant end. The remote alarm bit is set automatically in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit is removed.
- Automatic E bit access
  By setting bit XSP.AXS status information of received submultiframes is automatically inserted in E-bit position of the outgoing CRC Multiframe without any further interventions of the microprocessor.
- Automatic AIS to system interface
  In asynchronous state the synchronizer enforces automatically an AIS to the receive system interface. However, received data can be transparently switched through if bit FMR2.DAIS is set.

- Automatic clock source switching
  In Slave mode (LIM0.MAS = 0) the DCO-R synchronizes to the recovered route clock. In case of Loss of Signal LOS the DCO-R switches automatically to Master mode.
- Automatic freeze signaling:
  Updating of the received signaling information is controlled by the freeze signaling status. Optionally automatic freeze signaling can be disabled by setting bit SIC3.DAF.

4.5.3 Error Counter

The FALC®-LH offers six error counters each of them has a length of 16 bit. They record code violations, framing bit errors, E-bit errors, CRC4 bit errors and CRC4 error events which are flagged in the different SA6 bit combinations. Each of the error counter is buffered. Updating the buffer is done in two modes:

- one second accumulation
- on demand via handshake with writing to the DEC register

In the one second mode an internal one second timer updates these buffers and reset the counter to accumulate the error events in the next one second period. The error counter can not overflow. Error events occurring during reset are not lost.

4.5.4 Errored Second

The FALC®-LH supports the error performance monitoring by detecting the following alarms or error events in the received data:
framing errors, CRC errors, code violations, loss of frame alignment, loss of signal, alarm indication signal, E bit error, receive and transmit slips.
With a programmable interrupt mask register IMR4 all these alarms or error events can generate an Errored Second Interrupt (ISR3.ES) if enabled.

4.5.5 Second Timer

Additionally a one second timer interrupt is generated internally to indicate that the enabled alarm status bits or the error counters have to be checked. The clock is derived from signal RCLK.

4.5.6 In-Band Loop Generation and Detection

The FALC®-LH generates and detects a framed or unframed in-band loop up/activate and down/deactivate pattern with bit error rates up to1/100. Framed or unframed in-band loop code is selected by LCR1.FLLB. Replacing transmit data with the in-band loop codes is done by FMR3.XLD/XLU.
The FALC®-LH also offers the ability to generate and detect a flexible in-band loop up and down pattern (if LCR1.LLBP = 1) or a default pattern 00001 for up and 001 for down (if LCR1.LLBP = 0).

The user defined loop up and loop down pattern is programmable individually from 2 to 8 bit in length (LCR1.LAC1/0 and LCR1.LDC1/0). Programming of loop codes is done in registers LCR2 and LCR3.
Status and interrupt status bits inform the user whether a loop up or loop down code was detected.

4.5.7 Time Slot 0 Transparent Mode

The transparent modes are useful for loopbacks or for routing data unchanged through the FALC®-LH.

In receive direction, transparency for ternary or dual/single rail unipolar data is always achieved if the receiver is in the synchronous state. In asynchronous state the data may be transparently switched through if bit FMR2.DAIS is set. However, correct time slot assignment can not be guaranteed due to missing frame alignment between line and system side.
Setting of bit FMR2.RTM disconnects control of the internal elastic store from the receiver. The elastic buffer is now in a “free running” mode without any possibility to update the time slot assignment to a new frame position in case of re-synchronization of the receiver. Together with FMR2.DAIS this function can be used to realize undisturbed transparent reception.

Transparency in transmit direction can be achieved by activating the time slot 0 transparent mode (bit XSP.TT0 or TSWM.7-0). If XSP.TT0 = 1 all internal information of the FALC®-LH (framing, CRC, S_a/S_i bit signaling, remote alarm) is ignored. With register TSWM the S_i-bits, A-bit or the S_a4-8 bits can be selectively enabled to send data transparent from port XDI to the far end. For complete transparency the internal signaling controller, IDLE code generation and AIS alarm generation, single channel and payload loop back has to be disabled.

4.6 Test Functions (E1)

4.6.1 Pseudo-Random Bit Sequence Generation and Monitor

The FALC®-LH has the ability to generate and monitor 2^{15}-1 and 2^{20}-1 pseudo-random bit sequences (PRBS). The generated PRBS pattern is transmitted optionally inverted or not to the remote end via pins XL1/2 or XDOP/N. Generating and monitoring of PRBS pattern is done according to ITU-T O. 151.
The PRBS monitor senses the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error increments an error counter (CEC2). Synchronization is reached within 400 ms with a probability of 99.9% and a bit error rate of 1/10. If an 'all 0' or 'all 1' signal is detected, synchronous state is indicated, too.

4.6.2 Remote Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON via the analog or digital transmitter. As in normal mode they are also processed by the synchronizer and then sent to the system interface.The remote loopback mode is selected by setting the respective control bits LIM1.RL+JATT. Received data may be looped with or without the transmit jitter attenuator (FIFO = JATT).

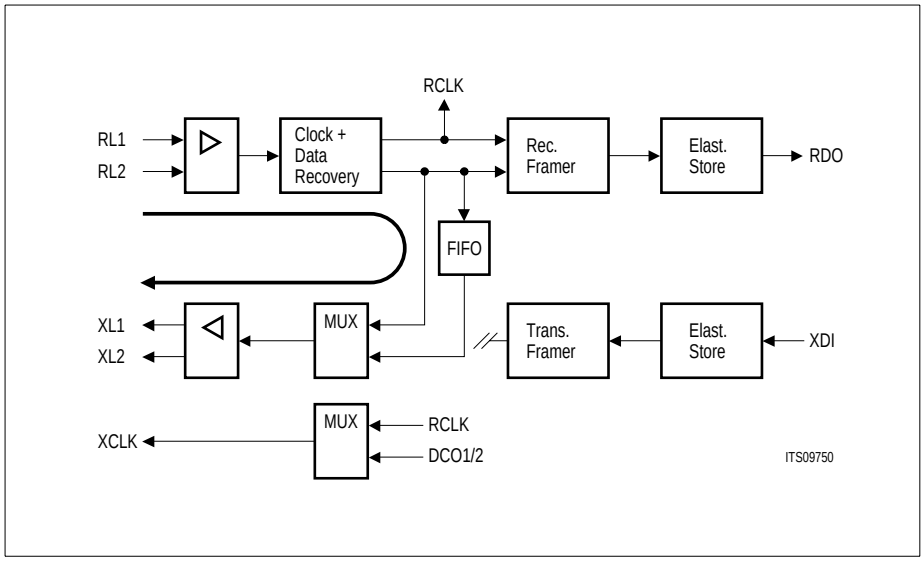


Figure 27 Remote Loop (E1)

4.6.3 Payload Loop Back

To perform an effective circuit test a payload loop is implemented. The payload loop back (FMR2.PLB) loops the data stream from the receiver section back to transmitter section. The looped data passes the complete receiver including the wander and jitter compensation in the receive elastic store and were output on pin RDO. Instead of the data an AIS (FMR2.SAIS) can be sent to the system interface.

The framing bits, CRC4 and Spare bits are not looped, if XSP.TT0 =0. They are originated by the FALC®-LH transmitter. If the PLB is enabled the transmitter and the data on pins XL1/2 or XDOP/XDON are clocked with SCLKR/RCLK instead of SCLKX. If XSP.TT0 = 1 the received time slot 0 is sent transparently back to the line interface. Data on the following pins are ignored: XDI, XSIG, SCLKX, $\overline{\text{SYPX}}$ and XMFS. All the received data is processed normally.

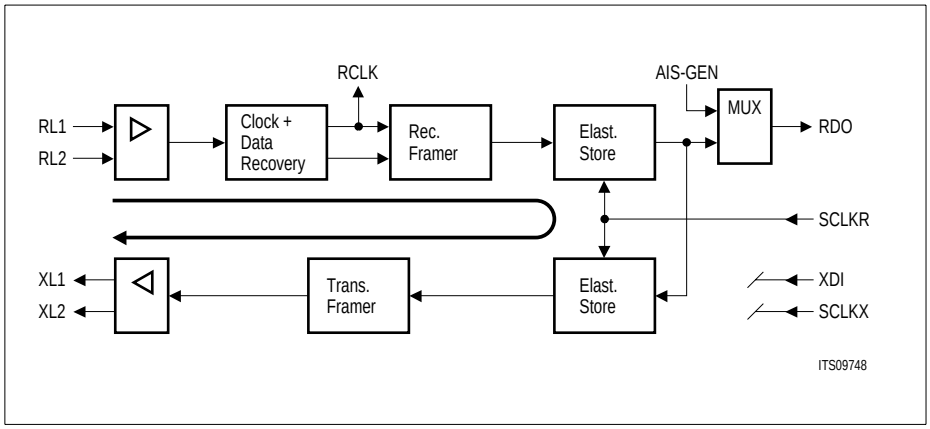


Figure 28 Payload Loop (E1)

Note: Returned data is not multiframe synchronous.

4.6.4 Local Loop

The local loopback mode, selected by LIM0.LL = 1, disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. However, the bit stream is transmitted undisturbedly on the line. However an AIS to the distant end can be enabled by setting FMR1.XAIS without influencing the data looped back to the system interface.

Note that enabling the local loop usually invokes an out of frame error until the receiver can resynchronize with the new framing. The serial codes for transmitter and receiver have to be identical.

In digital interface NRZ mode, a clock must be provided on pin RCLKI (=RL2) to enable switching into local loop mode.

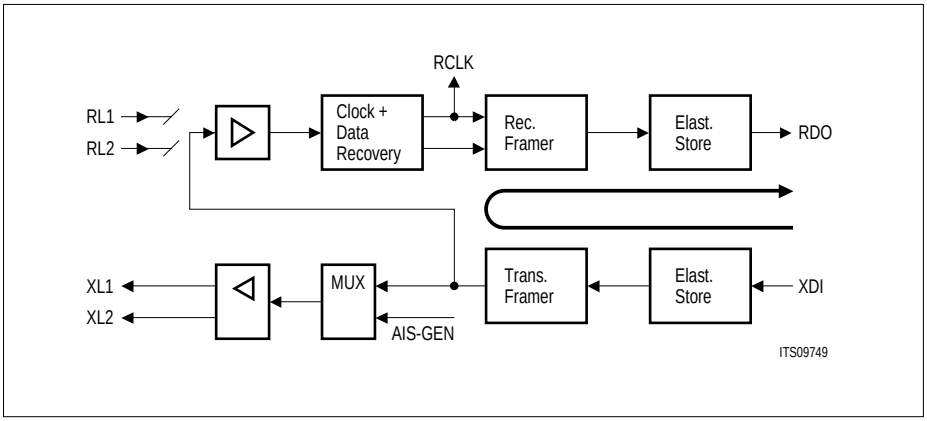


Figure 29 Local Loop (E1)

4.6.5 Single Channel Loop Back

Each of the 32 time slots may be selected for loopback from the system PCM input (XDI) to the system PCM output (RDO). This loopback is programmed for one time slot at a time selected by register LOOP. During loopback, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route time slot.

For the time slot test, sending sequences of test patterns like a 1 kHz check signal should be avoided. Otherwise, an increased occurrence of slips in the tested time slot disturbs testing. These slips do not influence the other time slots and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

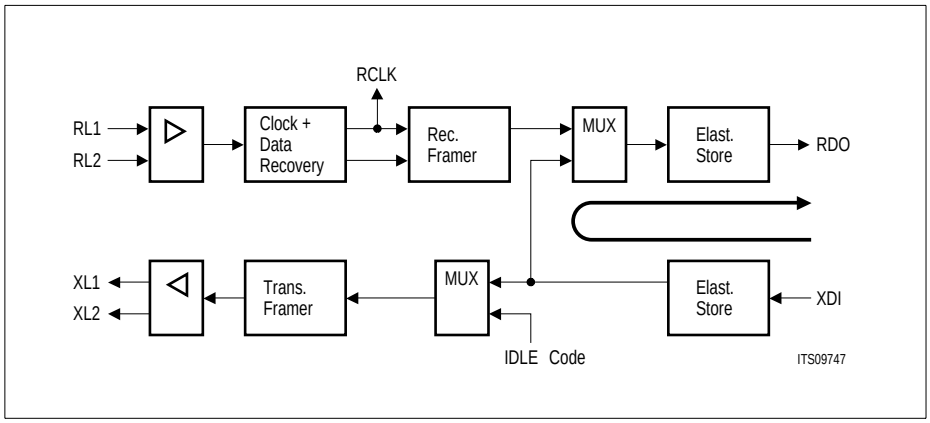


Figure 30 Single Channel Loopback (E1)

4.6.6 Alarm Simulation (E1)

Alarm simulation does not affect the normal operation of the device, i.e. all time slots remain available for transmission. However, possible ‘real’ alarm conditions are not reported to the processor when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss of Signal
- Alarm Indication Signal (AIS)
- Loss of pulse frame
- Remote alarm indication
- Receive and transmit slip indication
- Framing error counter
- Code violation counter (HDB3 Code)
- CRC4 error counter
- E-Bit error counter
- CEC2 counter
- CEC3 counter

Some of the above indications are only simulated if the FALC®-LH is configured in a mode where the alarm is applicable (e.g. no CRC4 error simulation when doubleframe format is enabled).

Setting of the bit FMR0.SIM initiates alarm simulation, interrupt status bits is set. Error counting and indication occurs while this bit is set. After it is reset all simulated error conditions disappear, but the generated interrupt statuses are still pending until the corresponding interrupt status register is read. Alarms like AIS and LOS are cleared automatically. Interrupt status register and error counters are automatically cleared on read.

5 Functional Description T1/J1

5.1 Receive Path in T1/J1 Mode

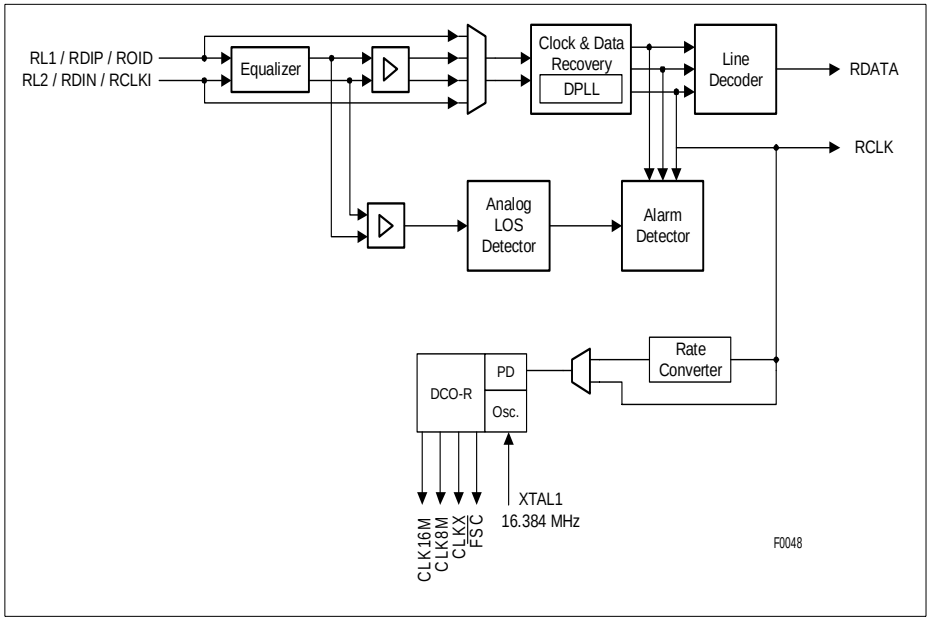


Figure 31 Receive Clock System (T1/J1)

Receive Line Interface (T1/J1)

For data input, three different data types are supported:

- Ternary coded signals received at multifunction ports RL1 and RL2 from a -10 dB (short haul, LIM0.EQON = 0) or -36 dB (long haul, LIM0.EQON = 1) ternary interface. The ternary interface is selected if LIM1.DRS is reset.

- Digital dual rail signals received on ports RDIP and RDIN. The dual rail interface is selected if LIM1.DRS and FMR0.RC1 is set.

- Unipolar data on port ROID received from a fiber optical interface. The optical interface is selected if LIM1.DRS is set and FMR0.RC1...0 = 00.

  Alternatively the optical interface can be switched to pin 68 (XMFB/XOID) and pin 80 (ROID) by setting bit LOOP.SPN.

Receive Short and Long Haul Interface (T1/J1)

The FALC®-LH has now an integrated short-haul and long-haul line interface, consisting of a receive equalization network, noise filtering and programmable line build-outs (LBO).

5.1.1 Receive Equalization Network (T1/J1)

The FALC®-LH automatically recovers the signals received on pins RL1/2 in a range of up to -36 dB. The maximum reachable length with a 22 AWG twisted-pair cable is 2000 m. After Reset the FALC®-LH is in “Short Haul“ mode, received signals are recovered up to -10 dB of cable attenuation. Switching in “Long Haul“ mode is done by setting of register LIM0.EQON.
The integrated receive equalization network recovers signals with up to -36 dB of cable attenuation. Noise filters eliminate the higher frequency part of the received signals. The incoming data is peak detected and sliced at 55% of the peak value to produce the digital data stream. The received data is then forwarded to the clock & data recovery unit.

5.1.2 Receive Line Attenuation Indication (T1/J1)

Status register RES reports the current receive line attenuation in a range of 0 to -36 dB in 25 steps of approximately 1.4 dB each. The least significant 5 bits of this register indicate the cable attenuation in dB. These 5 bits are only valid in conjunction with the two most significant bits (RES.EV1/0 = 01).

5.1.3 Receive Clock and Data Recovery (T1/J1)

The analog received signal on port RL1/2 is equalized and then peak-detected to produce a digital signal. The digital received signal on port RDIP/N is directly forwarded to the DPLL. The receive clock and data recovery extracts the route clock RCLK from the data stream received at the RL1/2, RDIP/RDIN or ROID lines and converts the data stream into a single rail, unipolar bit stream. Normally the clock that is output via pin RCLK is the recovered clock from the signal provided by RL1/2 or RDIP/N has a duty cycle close to 50 %. The free run frequency is defined by XTAL3 divided by 8 in periods with no signal. The intrinsic jitter generated in the absence of any input jitter is not more than 0.035 UI. In digital bipolar line interface mode the clock and data recovery accepts only B8ZS or AMI coded signals with 50 % duty cycle.

5.1.4 Receive Line Coding (T1/J1)

The B8ZS line code or the AMI (ZCS) coding is provided for the data received from the ternary or the dual rail interface. All code violations that do not correspond to zero substitution rules are detected. The detected errors increment the code violation counter (16 bits length). In case of the optical interface mode NRZ coding is performed automatically and data is latched with the falling edge of pin RCLKI. When using the

optical interface with NRZ coding, the decoder is by-passed and no code violations are detected.

Additionally, the receive line interface contains the alarm detection for Alarm Indication Signal AIS (Blue Alarm) and the Loss of Signal LOS (Red Alarm).

Pulse density violations are detected and indicated via bit FRS1.PDEN.

The signal at the ternary interface is received at both ends of a transformer.

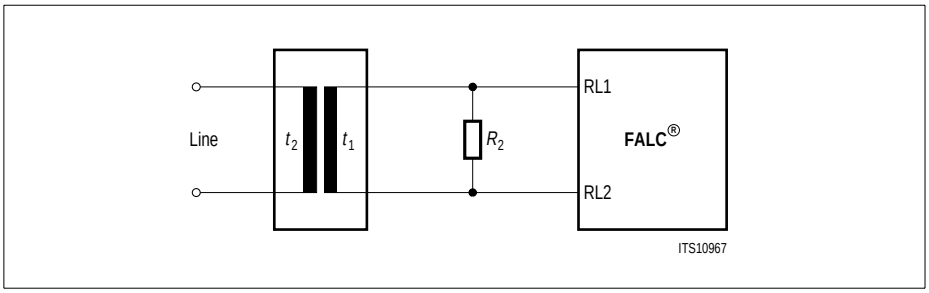


Figure 32 Receiver Configuration (T1/J1)

Table 22 Recommended Receiver Configuration Values (T1/J1)

Parameter	Characteristic Impedance	
	100 Ω	**110 Ω**
	T1	**J1**
R_2 (± 1 %) [Ω]	200	220
$t_2 : t_1$	1 : $\sqrt{2}$	1 : $\sqrt{2}$

5.1.5 Loss of Signal Detection (T1/J1)

There are different definitions for detecting Loss of Signal alarms (LOS) in the ITU-T G.775 and AT&T TR 54016. The FALC®-LH covers all these standards. The LOS indication is performed by generating an interrupt (if not masked) and activating a status bit. Additionally a LOS status change interrupt is programmable via register IPC.SCI.

- Detection:
  An alarm is generated if the incoming data stream has no pulses (no transitions) for a certain number (N) of consecutive pulse periods. “No pulse” in the digital receive interface means a logical zero on pins RDIP/RDIN/ROID. A pulse with an amplitude less than Q dB below nominal is the criteria for “no pulse” in the analog receive interface (LIM1.DRS=0). In short haul mode (LIM0.EQON = 0), the receive signal level Q is programmable via three control bits LIM1.RIL2...0 in a range of about 1400 to 200 mV differential voltage between pins RL1/2 (see **Chapter 11.3** on page **357**). In long

haul mode (LIM0.EQON = 1) the analog LOS criteria is defined by the equalizer status. The number N may be set via a 8 bit register PCD. The contents of the PCD register is multiplied by 16, which results in the number of pulse periods, or better, the time which has to suspend until the alarm has to be detected. The range therefore results from 16 to 4096 pulse periods.

- Recovery:
  In general the recovery procedure starts after detecting a logical “one“ (digital receive interface) or a pulse (analog receive interface) with an amplitude more than Q dB (defined by LIM1.RIL2...0) of the nominal pulse. The value in the 8 bit register PCR defines the number of pulses (1 to 255) to clear the LOS alarm. Additional recovery conditions may be programmed by register LIM2.

Note: In long haul mode, LOS alarm is declared either if “no pulses” are detected for the period defined in PCD or the signal level drops below typically about -35 dB of the nominal signal (“low signal level”). Additionally, the incoming data stream is cleared, if this “low signal level” is detected in order to generate a fixed data stream before first bit errors occur. Typically, this loss of signal threshold is about -36 dB. Because the DS1 signal varies at 3.0V +/- 20%, this loss of signal threshold correlates directly to the transmitted pulse amplitude. It changes to -33 dB, if the generated maximum transmit amplitude at the remote end is not more than 2.4V

For recovery this means, that at first the signal level has to increase and then the pulses are counted and compared to PCR to return from LOS indication.

Please also note, that this behavior is slightly different to FALC-LH V1.1.

5.1.6 Receive Jitter Attenuator (T1/J1)

The receive jitter attenuator is placed in the receive path. The jitter attenuator meets the requirements of PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431, G.703 and G. 824.

The internal DCO-R generates a “jitter free“ output clock which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock. The receive jitter attenuator can be either synchronized with the extracted receive clock RCLK or to a 1.544 or 2.048-MHz clock provided on pin SYNC. Received data are written into the receive elastic buffer with RCLK and are read out with SCLKR. Optionally an 8 kHz clock is provided on pin XCLK/FSC or $\overline{\text{FSC}}$.

The DCO-R circuitry attenuates the incoming jittered clock starting at 6 Hz jitter frequency with 20 dB per decade fall off. Wander with a jitter frequency below 6 Hz is passed unattenuated. The intrinsic jitter in the absence of any input jitter is < 0.02UI.

For some applications it might be useful starting of jitter attenuation at lower frequencies. Therefore the corner frequency is switchable by the factor of ten down to 0.6 Hz (LIM2.SCF).

Jitter attenuation can be achieved either using an external tunable crystal on pins XTAL1/XTAL2 or using the crystal-less jitter attenuation selected by LIM2.DJA1/2. In this case, a stable clock or regular crystal of 16.384 MHz has to be provided on pin XTAL1 (+/- 50 ppm). In crystal-less mode the system clock output on pin CLK16M can be either the dejittered or the non-dejittered clock (LIM3.CSC).

The DCO-R circuitry is automatically centered to the nominal bit rate if the reference clock on pin SYNC/RCLK is missed for two 2.048 or 1.544-MHz clock periods. In analog line interface mode the RCLK is always running. Only in digital line interface mode with single rail data (NRZ) a gapped clock on pin RCLK may occur.

The receive jitter attenuator works in two different modes:

- Slave mode
  In Slave mode (LIM0.MAS = 0) the DCO-R is synchronized with the recovered route clock. In case of LOS the DCO-R switches to Master mode automatically.
- Master mode
  In Master mode (LIM0.MAS = 1) the jitter attenuator is in free running mode if on pin SYNC no clock is supplied. If an external clock on the SYNC input is applied, the DCO-R synchronizes to this input. The external frequency can be 1.544 MHz (LIM1.DCOC=0) or 2.048 MHz (LIM1.DCOC=1).

The following table shows the clock modes with the corresponding synchronization sources.

Table 23 System Clocking (T1/J1)

Mode	Internal LOS Active	SYNC Input	System Clocks
Master	independent	Fixed to VSS	free running (oscillator centered)
Master	independent	1.544 MHz	Synchronized with SYNC input (LIM1.DCOC=0)
Master	independent	2.048 MHz	Synchronized with SYNC input (LIM1.DCOC=1)
Slave	no	Fixed to VSS	Synchronized with Line RCLK
Slave	no	1.544 MHz or 2.048 MHz	Synchronized with Line RCLK

Table 23 System Clocking (T1/J1) (cont'd)

Mode	Internal LOS Active	SYNC Input	System Clocks
Slave	yes	Fixed to VSS	Free running (oscillator centered)
Slave	yes	1.544 MHz	Synchronized with SYNC (LIM1.DCOC = 0)
Slave	yes	2.048 MHz	Synchronized with SYNC (LIM1.DCOC = 1)

The jitter attenuator meets the jitter transfer requirements of the PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499, I.431 and G. 703.(refer to **Figure 33**).

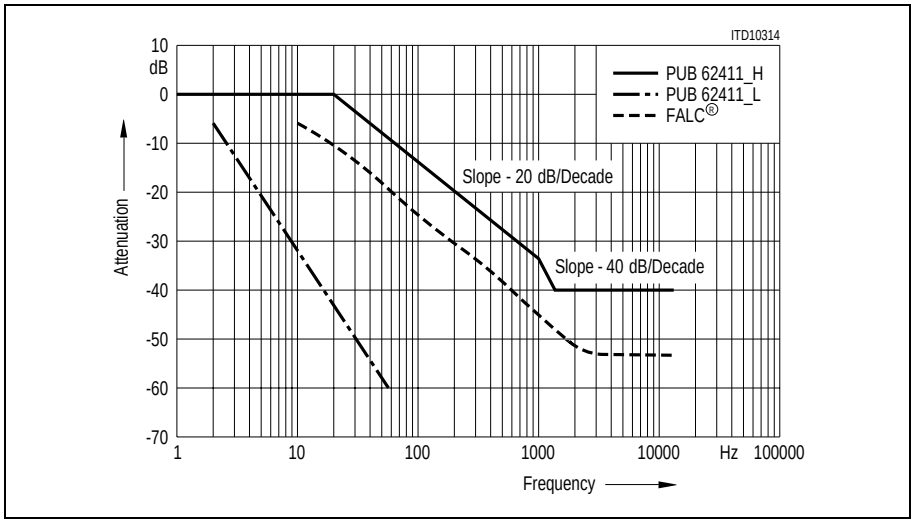


Figure 33 Jitter Attenuation Performance (T1/J1)

5.1.7 Jitter Tolerance (T1/J1)

The FALC®-LH receiver's tolerance to input jitter complies to ITU and Bellcore requirements for T1 applications.

Figure 34 shows the curves of different input jitter specifications stated below as well as the FALC®-LH performance.

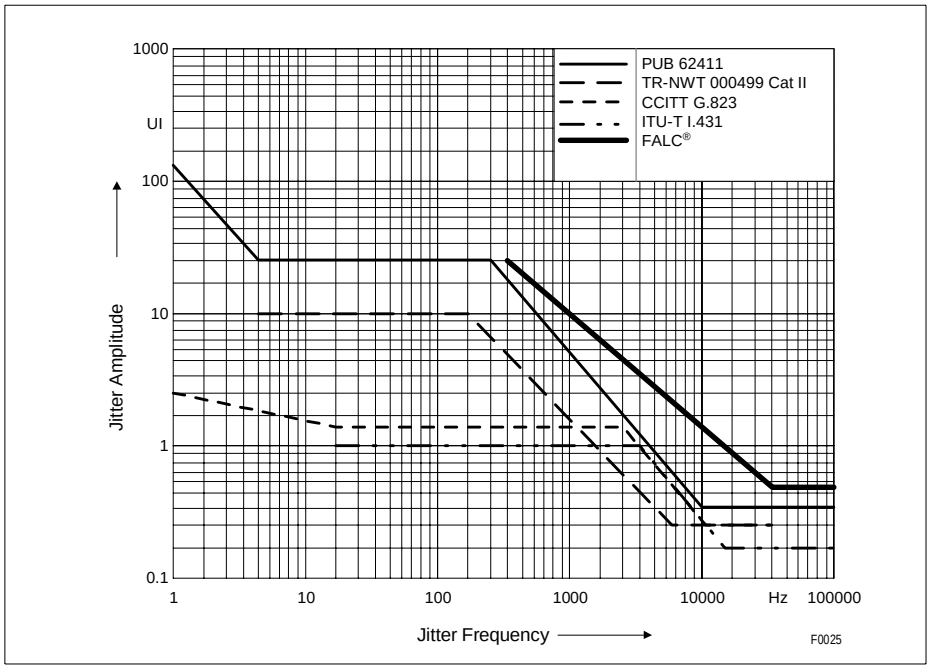


Figure 34 Jitter Tolerance (T1/J1)

5.1.8 Output Jitter (T1/J1)

According to the input jitter defined by PUB62411 the FALC®-LH generates the output jitter, which is specified in **Table 24Table** below.

Table 24 Output Jitter (T1/J1)

Specification	Measurement Filter Bandwidth		Output Jitter (UI peak to peak)
	Lower Cutoff	Upper Cutoff	
PUB 62411	10 Hz	8 kHz	< 0.02
	8 kHz	40 kHz	< 0.02
	10 Hz	40 kHz	< 0.02
	Broadband		< 0.02

5.1.9 Transmit Jitter Attenuator (T1/J1)

The transmit jitter attenuator DCO-X circuitry generates a “jitter free“ transmit clock and meets the following requirements: PUB 62411, PUB 43802, TR-TSY 009,TR-TSY 253, TR-TSY 499 and ITU-T I.431 and G.703. The DCO-X circuitry works internally with the same high frequency clock as the receive jitter attenuator it does. It synchronizes either to the working clock of the transmit backplane interface or the clock provided by pin SYNC2 (1.544 MHz if LIM1.DCOC=0 or 2.048 MHz if LIM1.DCOC=1) or the receive clock RCLK (remote loop with JATT/loop-timed). The DCO-X attenuates the incoming jitter starting at 6 Hz with 20 dB per decade fall off. With the jitter attenuated clock, which is directly dependent on the phase difference of the incoming clock and the jitter attenuated clock, data is read from the transmit elastic buffer (2 frames) or from the JATT buffer (2 frames, remote loop with JATT) Wander with a jitter frequency below 6 Hz is passed transparently.

The DCO-X accepts gapped clocks which are used in ATM or SDH/SONET applications. The jitter attenuated clock is output on pin XCLK.

The transmit jitter attenuator can be disabled.

In the loop-timed clock configuration (LIM2.ELT) the DCO-X circuitry generates a transmit clock which is frequency synchronized with RCLK. In this configuration the transmit elastic buffer has to be enabled.

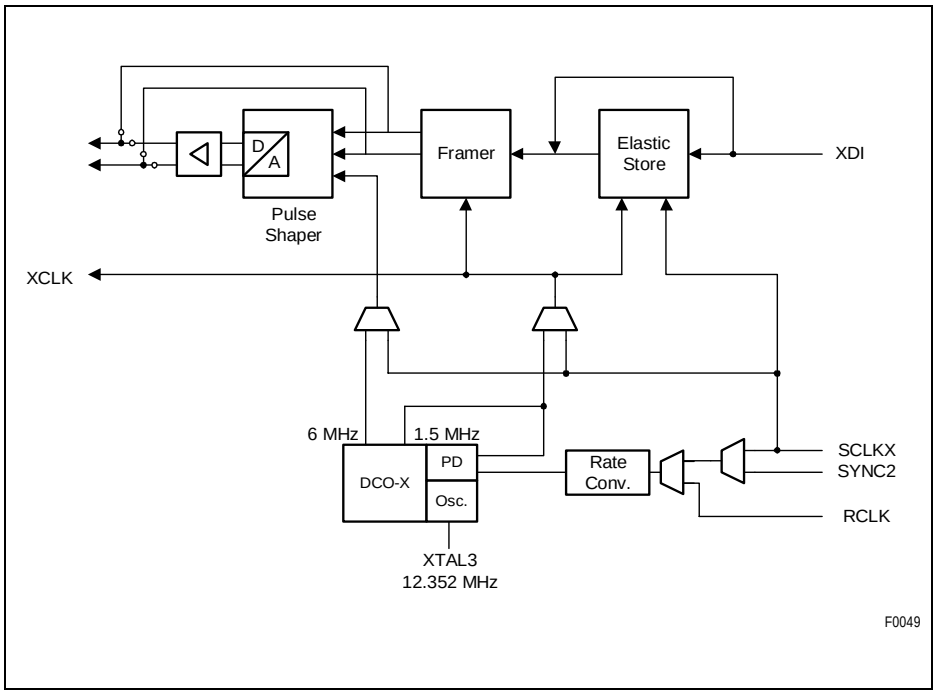


Figure 35 Transmit Clock System (T1/J1)

Note: DR = Dual Rail Interface; DCO-X = Digital Controlled Oscillator Transmit

5.1.10 Framer/Synchronizer (T1/J1)

The following functions are performed:

- Synchronization on pulse frame and multiframe
- Error indication when synchronization is lost. In this case, AIS is sent to the system side automatically and Remote Alarm to the remote end if en/disabled.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This can be done automatically by the FALC®-LH or user controlled via the microprocessor interface.
- Detection of remote alarm (yellow alarm) indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in special status registers.
- Detection of framed or unframed In Band Loop Up/Down Code
- Generation of various maskable interrupt statuses of the receiver functions.

- Generation of control signals to synchronize the CRC checker and the receive elastic buffer.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC multiframe according to the CRC 6 procedure (refer to ITU-T G.704). These bits are compared with those check bits that are received during the next CRC multiframe. If there is at least one mismatch, the CRC error counter (16 bit) is incremented.

5.1.11 Receive Elastic Buffer (T1/J1)

The received bit stream is stored in the receive elastic buffer. The memory is organized as a two-frame elastic buffer with a maximum size of 48 × 8 bit. The size of the elastic buffer can be configured independently for the receive and transmit direction. Programming of the receive buffer size is done by SIC1.RBS1/0 :

- RBS1/0 = 00 : two frame buffer or 384 bits
  Maximum of wander amplitude (peak-to-peak): (1 UI = 648 ns)
  System interface clocking rate: 8.192 MHz:
  142 UI in channel translation mode 0
  78 UI in channel translation mode 1
  System interface clocking rate: 1.544 MHz:
  max. wander: 126 UI
  average delay after performing a slip: 1 frame or 193 bits
- RBS1/0 = 01 : one frame buffer or 193 bits
  System interface clocking rate: 8.192 MHz:
  Max. wander : 80 UI in channel translation mode 0
  Max. wander : 50 UI in channel translation mode 1
  System interface clocking rate: 1.544 MHz:
  max. wander: 74 UI
  average delay after performing a slip: 96 bits
- RBS1/0 = 10 : short buffer or 96 bits :
  System interface clocking rate: 8.192 MHz:
  Max. wander : 28 UI in channel translation mode 0; channel translation mode 1 not supported
  System interface clocking rate: 1.544 MHz:
  max. wander: 38 UI
  average delay after performing a slip: 48 bits
- RBS1/0 = 11 : Bypass of the receive elastic buffer

The functions of the receive elastic buffer are:

- Clock adaption between system clock (SCLKR) and internally generated route clock (RCLK).
- Compensation of input wander and jitter.

- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel, time slot serial data which is circularly written to the elastic buffer using the internally generated Receive Route Clock (RCLK).

Reading of stored data is controlled by the System Clock sourced by SCLKR and the Synchronous Pulse ($\overline{\text{SYPR}}$) in conjunction with the programmed offset values for the receive time slot/clock slot counters. After conversion into a serial data stream, the data is given out via port RDO. If the receive buffer is bypassed, data is clocked off with RCLK instead of SCLKR.

If 8.192 MHz reference frequency is used, one of two channel translation modes has to be selected. The 24 received time slots (T1/J1) can be translated into the 32 system time slots (E1) in two different channel translation modes (selected by FMR1.CTM). Unequipped time slots are set to 'FF_H'. Refer to **Table 26**.

In one frame or short buffer mode the delay through the receive buffer is reduced to an average delay of 96 or 48 bits. In this case $\overline{\text{SYPR}}$ to be programmed as input is not allowed. Slips are performed in all buffer modes except the bypass mode. After a slip is detected the read pointer is adjusted to one half of the current buffer size. The following table gives an overview of the receive buffer operating mode.

Table 25 Receive Buffer Operating Modes (T1/J1)

SIC1.RBS1...0	Buffer Size	TS Offset programing (RC1...0)	Slip performance
11	bypass[1)]	RFM ($\overline{\text{SYPR}}$ = output) must be selected; value of RC1...0 determines the position of RFM	no slips
10	short buffer	RFM ($\overline{\text{SYPR}}$ = output) must be selected; value of RC1...0 determines the position of RFM	yes
01	1 frame	RFM ($\overline{\text{SYPR}}$ = output) must be selected; value of RC1...0 determines the position of RFM	yes
00	2 frames	$\overline{\text{SYPR}}$ is input and determines the frame position together with RC1...0 offset.	yes Slips are performed on the frame boundary

1) In bypass mode the clock provided on pin SCLKR is ignored. Clocking is done with RCLK.

Figure 36 gives an idea of operation of the receive elastic buffer:
A slip condition is detected when the write pointer (W) and the read pointer (R) of the memory are nearly coincident, i.e. the read pointer is within the slip limits (S +, S –). If a slip condition is detected, a negative slip (one frame or one half of the current buffer size is skipped) or a positive slip (one frame or one half of the current buffer size is read out twice) is performed at the system interface, depending on the difference between RCLK and the current working clock of the receive backplane interface. i.e. on the position of pointer R and W within the memory. A positive/negative slip is indicated in the interrupt status bits ISR3.RSP and ISR3.RSN.

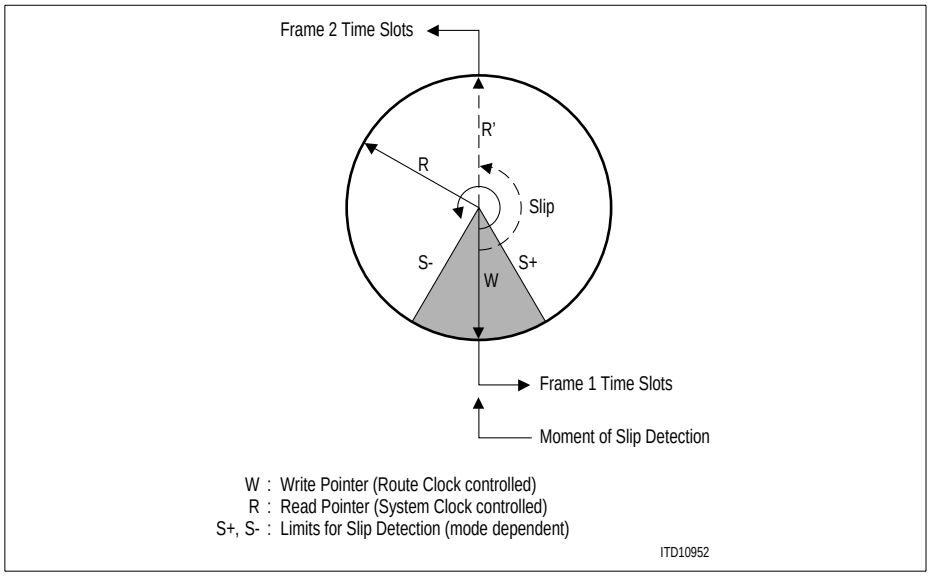


Figure 36 The Receive Elastic Buffer as Circularly Organized Memory

Table 26 Channel Translation Modes (T1/J1)

Speech Channels		Time Slots
C. Translation Mode 0	C. Translation Mode 1	
FS/DL	FS/DL	0
1	1	1
2	2	2
3	3	3
–	4	4

Table 26 Channel Translation Modes (T1/J1) (cont'd)

Speech Channels		Time Slots
C. Translation Mode 0	**C. Translation Mode 1**	
4	5	5
5	6	6
6	7	7
–	8	8
7	9	9
8	10	10
9	11	11
–	12	12
10	13	13
11	14	14
12	15	15
–	16	16
13	17	17
14	18	18
15	19	19
–	20	20
16	21	21
17	22	22
18	23	23
–	24	24
19	–	25
20	–	26
21	–	27
–	–	28
22	–	29
23	–	30
24	–	31

- : FF_H

5.1.12 Receive Signaling Controller (T1/J1)

The signaling controller may be programmed to operate in various signaling modes. The FALC®-LH performs the following signaling and data link methods.

5.1.12.1 HDLC/SDLC or LAPD Access

In case of common-channel signaling the signaling procedure HDLC/SDLC or LAPD according to Q.921 is supported. The signaling controller of the FALC®-LH performs the FLAG detection, CRC checking, address comparison and zero bit-removing. The received data flow and the address recognition features may be performed in very flexible way, to satisfy almost any practical requirements. Depending on the selected address mode, the FALC®-LH may perform a 1 or 2 byte address recognition. If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address is interpreted as command/response bit (C/R) and is excluded from the address comparison. Buffering of receive data is done in a 64 byte deep RFIFO.
In signaling controller transparent mode, fully transparent data reception without HDLC framing is performed, i.e. without FLAG recognition, CRC checking or bit-stuffing. This allows user specific protocol variations.
The FALC®-LH offers the flexibility to extract data during certain time slots. Any combination of time slots may be programmed independently for the receive and transmit direction.

5.1.12.2 CAS Bit-robbing (T1/J1, serial access mode)

The signaling information is carried in the LSB of every sixth frame for each time slot. The signaling controller samples the bit stream on the receive system side.

The complete CAS multiframe is transmitted on pin RSIG. The signaling data is clocked out with the working clock of the receive highway in conjunction with the receive synchronization pulse ($\overline{\text{SYPR}}$). Data on RSIG is transmitted in the last 4 bits per time slot and are time slot aligned to the data on RDO. In ESF format the A,B,C,D bits are placed in the bit positions 5-8 per time slot. In F12/72 format the A and B bits are repeated in the C and D bit positions. The first 4 bits per time slot can be optionally fixed high or low. The FS/DL time slot is transmitted on RDO and RSIG. During IDLE time slots no signaling information is transmitted. Data on RSIG are only valid if the freeze signaling status is inactive. With FMR1.SAIS an all ones may be transmitted on RDO and RSIG.
Update of the receive signaling information is controlled by the freeze signaling status. If signaling information is frozen updating of the registers RS1-16 is disabled. The freeze signaling status is output on pin $\overline{\text{RFSP}}$/FREEZS and is generated, if:

- FRS0.LFA/LMFA = 1 or
- FRS0.LOS=1 or

- a receive slip occurred

5.1.12.3 CAS Bit-robbing (T1/J1, µP access mode)

The signaling information is carried in the LSB of every sixth frame for each time slot. The signaling controller samples the bit stream on the receive line side. Receive signaling data is stored in the registers RS1-12.

To relieve the µP load from always reading the complete RS1-12 buffer every 3 ms the FALC®-LH notifies the µP via interrupt ISR0.RSC only when signaling changes from one multiframe to the next.

5.1.12.4 Bit Oriented Messages in ESF-DL Channel (T1/J1)

The FALC®-LH supports the DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016. The HDLC- and Bit Oriented Message (BOM)-Receiver may be switched ON/OFF independently. If the FALC®-LH is used for HDLC formats only, the BOM receiver has to be switched off. If HDLC- and BOM-receiver has been switched on (MODE.HRAC/BRAC), an automatic switching between HDLC and BOM mode is enabled. If eight or more consecutive ones are detected, the BOM mode is entered. Upon detection of a flag in the data stream, the FALC®-LH switches back to HDLC-mode. In BOM-mode, the following byte format is assumed (the left most bit is received first): 111111110xxxxxx0
Two different BOM reception modes can be programmed (CCR1.BRM).

5.1.12.5 Data Link Access in F72 Format (T1/J1)

The DL-channel protocol is supported as follows:
- access is done on a multiframe basis via registers RDL1-3,
- the DL bit information from frame 26 to 72 is stored in the Receive FIFO of the signaling controller.

5.2 System Interface in T1/J1 Mode

The interface to the receive system highway is realized by two data buses, one for the data RDO and one for the signaling data RSIG. The receive highway is clocked via pin SCLKR, while the interface to the transmit system highway is independently clocked via pin SCLKX. The frequency of these working clocks and the data rate for the receive and transmit system interface is programmable by SIC1.SRSC and SIC1.SXSC. Transmit and receive clock frequencies have to be the same. Selectable system clock and data rates and their valid combinations are shown in the table below.

Table 27 System Clock and Data Rates (T1/J1)

System Data Rate	Clock Rate 1.544 MHz	Clock Rate 8.192 MHz
1.544 Mbit/s	x	--
2.048 Mbit/s	--	x
4.096 Mbit/s	--	x

x = valid, -- = invalid

Generally the data or marker on the system interface are clocked off or latched on the falling edge of the SCLKR/SCLKX clock independently.

The signal on pin $\overline{\text{SYPR}}$ in conjunction with the assigned timeslot offset in register RC0 and RC1 define the beginning of a frame on the receive system highway.

The signal on pin $\overline{\text{SYPX}}$ in conjunction with the assigned timeslot offset in register XC0 and XC1 define the beginning of a frame on the transmit system highway.

Adjusting the frame begin (time slot 0, bit 0) relative to $\overline{\text{SYPR/X}}$ is possible in the range of 0...125 µsec.

A receive frame marker RFM can be activated (SIC2.SRFSO = 1) during any bit position of the entire frame. Programming is done with registers RC1/0. The receive frame marker is active high for one 1.544/2.048 MHz cycle and is clocked off with the falling edge of the clock which is input on port SCLKR or RCLK.

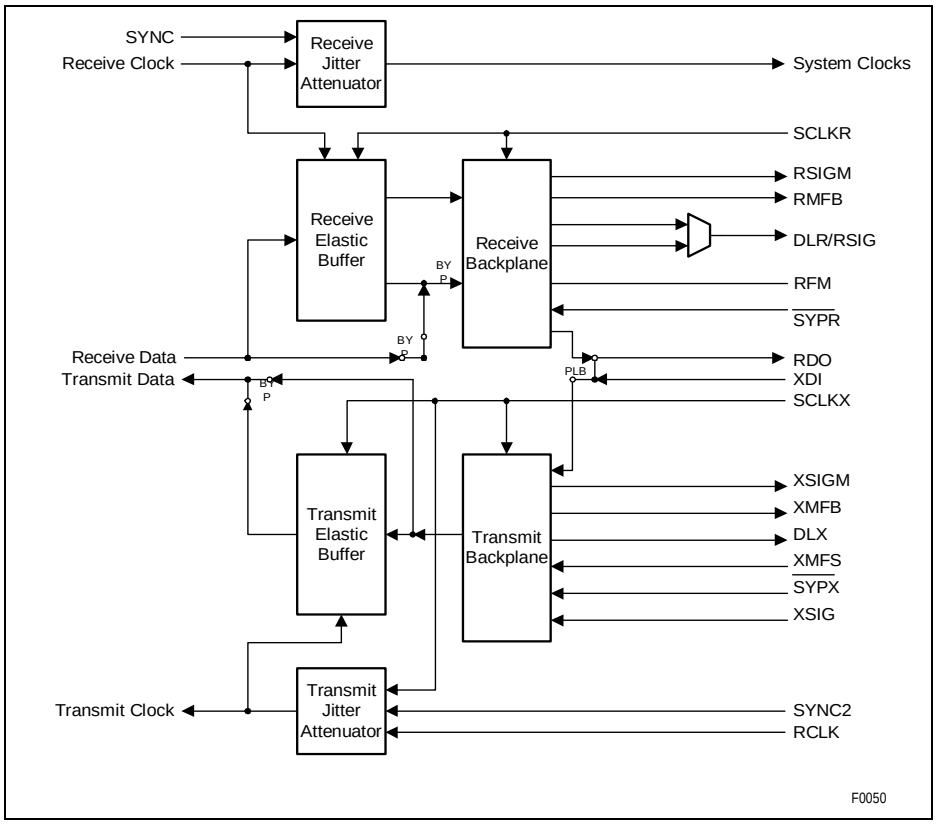


Figure 37 System Interface (T1/J1)

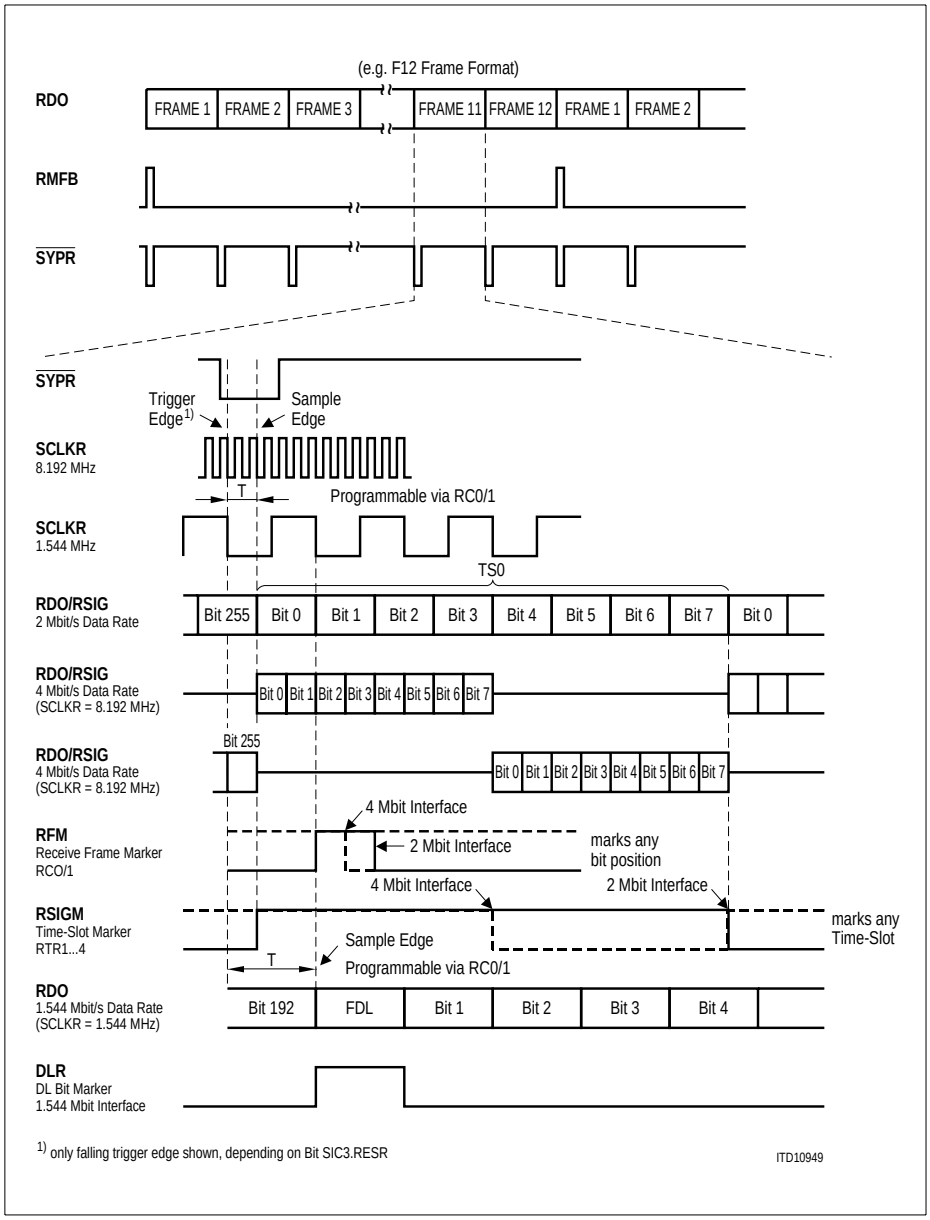


Figure 38 Receive System Interface Clocking (T1/J1)

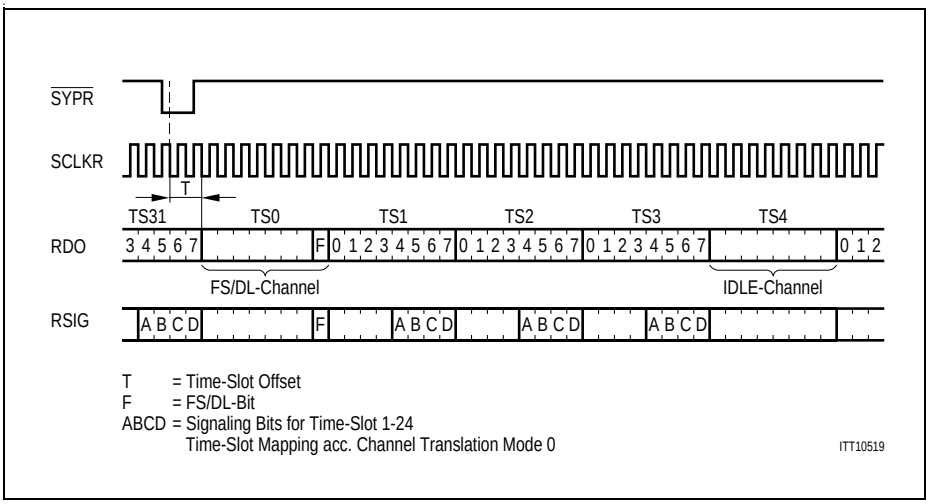


Figure 39 2.048 Mbit/s Receive Signaling Highway (T1/J1)

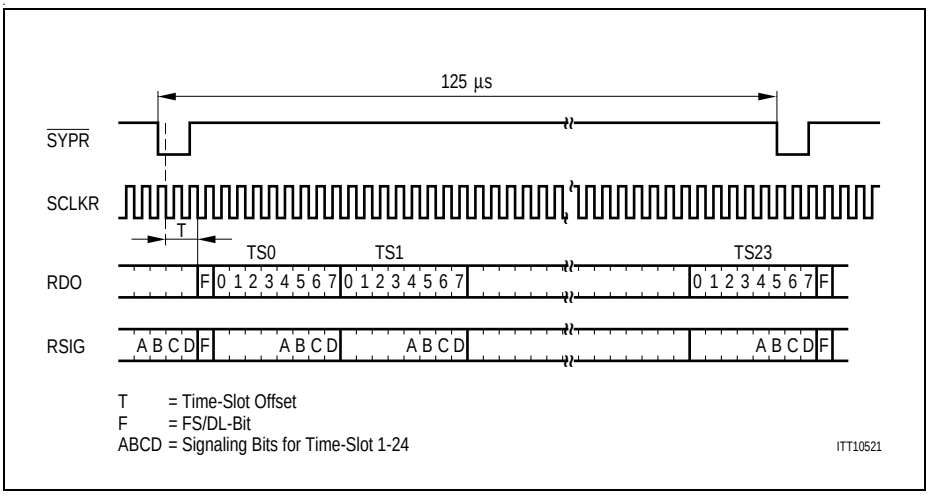


Figure 40 1.544 Mbit/s Receive Signaling Highway (T1/J1)

5.2.1 Time Slot Assigner (T1/J1)

The FALC®-LH offers the flexibility to connect data during certain time slots, as defined by registers RTR1-4 and TTR1-4, to the RFIFO and XFIFO, respectively. Any combinations of time slots can be programmed for the receive and transmit directions. If CCR1.EITS = 1 the selected time slots (RTR1-4) are stored in the RFIFO of the signaling controller and the XFIFO contents is inserted into the transmit path as controlled by registers TTR1-4.

Table 28 Time Slot Assigner (T1/J1)

Receive Time Slot Register	Transmit Time Slot Register	Time Slots	Receive Time Slot Register	Transmit Time Slot Register	Time Slots
RTR 1.7	TTR 1.7	0	RTR 3.7	TTR 3.7	16
RTR 1.6	TTR 1.6	1	RTR 3.6	TTR 3.6	17
RTR 1.5	TTR 1.5	2	RTR 3.5	TTR 3.5	18
RTR 1.4	TTR 1.4	3	RTR 3.4	TTR 3.4	19
RTR 1.3	TTR 1.3	4	RTR 3.3	TTR 3.3	20
RTR 1.2	TTR 1.2	5	RTR 3.2	TTR 3.2	21
RTR 1.1	TTR 1.1	6	RTR 3.1	TTR 3.1	22
RTR 1.0	TTR 1.0	7	RTR 3.0	TTR 3.0	23
RTR 2.7	TTR 2.7	8	RTR 4.7	TTR 4.7	24
RTR 2.6	TTR 2.6	9	RTR 4.6	TTR 4.6	25
RTR 2.5	TTR 2.5	10	RTR 4.5	TTR 4.5	26
RTR 2.4	TTR 2.4	11	RTR 4.4	TTR 4.4	27
RTR 2.3	TTR 2.3	12	RTR 4.3	TTR 4.3	28
RTR 2.2	TTR 2.2	13	RTR 4.2	TTR 4.2	29
RTR 2.1	TTR 2.1	14	RTR 4.1	TTR 4.1	30
RTR 2.0	TTR 2.0	15	RTR 4.0	TTR 4.0	31

In receive direction, transparency for ternary or dual/single rail unipolar data is always achieved if the receiver is in the synchronous state and bit FMR5.RTF is set. All bits in the F-bit position of the incoming multiframe are forwarded to RDO and inserted in the FS/DL time-slot or in the F-bit position.
In asynchronous state the received data may be transparently switched through if bit FMR2.DAIS is set.
For the receive path bit FMR5.RTF has the same function as bit FMR4.TM.

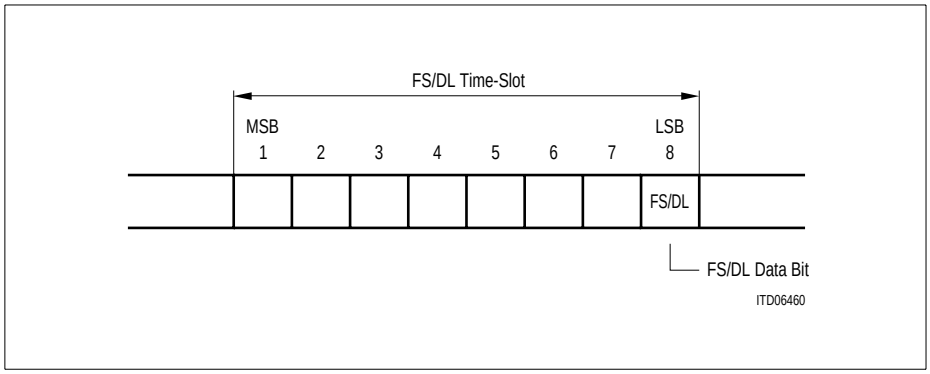


Figure 41 Receive FS/DL Bits in Time Slot 0 on RDO (T1/J1)

5.3 Transmit Path in T1/J1 Mode

Compared to the receive paths the inverse functions are performed for the transmit direction.

The interface to the transmit system highway is realized by two data buses, one for the data XDI and one for the signaling data XSIG. The time slot assignment is equivalent to the receive direction. All unequipped (idle) time slots are ignored.

Latching of data is controlled by the System Clock (SCLKX) and the Synchronous Pulse ($\overline{\text{SYPX}}$/XMFS) in conjunction with the programmed offset values for the Transmit Time slot/Clock slot Counters XC1/0. The frequency of the working clock for the transmit system interface is programmable by SIC1.SXSC. Refer also to **Table 27** on page **117**.

The received bit stream on ports XDI and XSIG can be multiplexed internally on a time slot basis, if enabled by SIC3.TTRF = 1, if not serial CAS mode is selected (see **Chapter 5.1.12.2** on page **115**). The data received on port XSIG can be sampled if the transmit signaling marker XSIGM is active high. Data on port XDI is sampled if XSIGM is low for the respective time slot. Programming the XSIGM marker is done with registers TTR1-4.

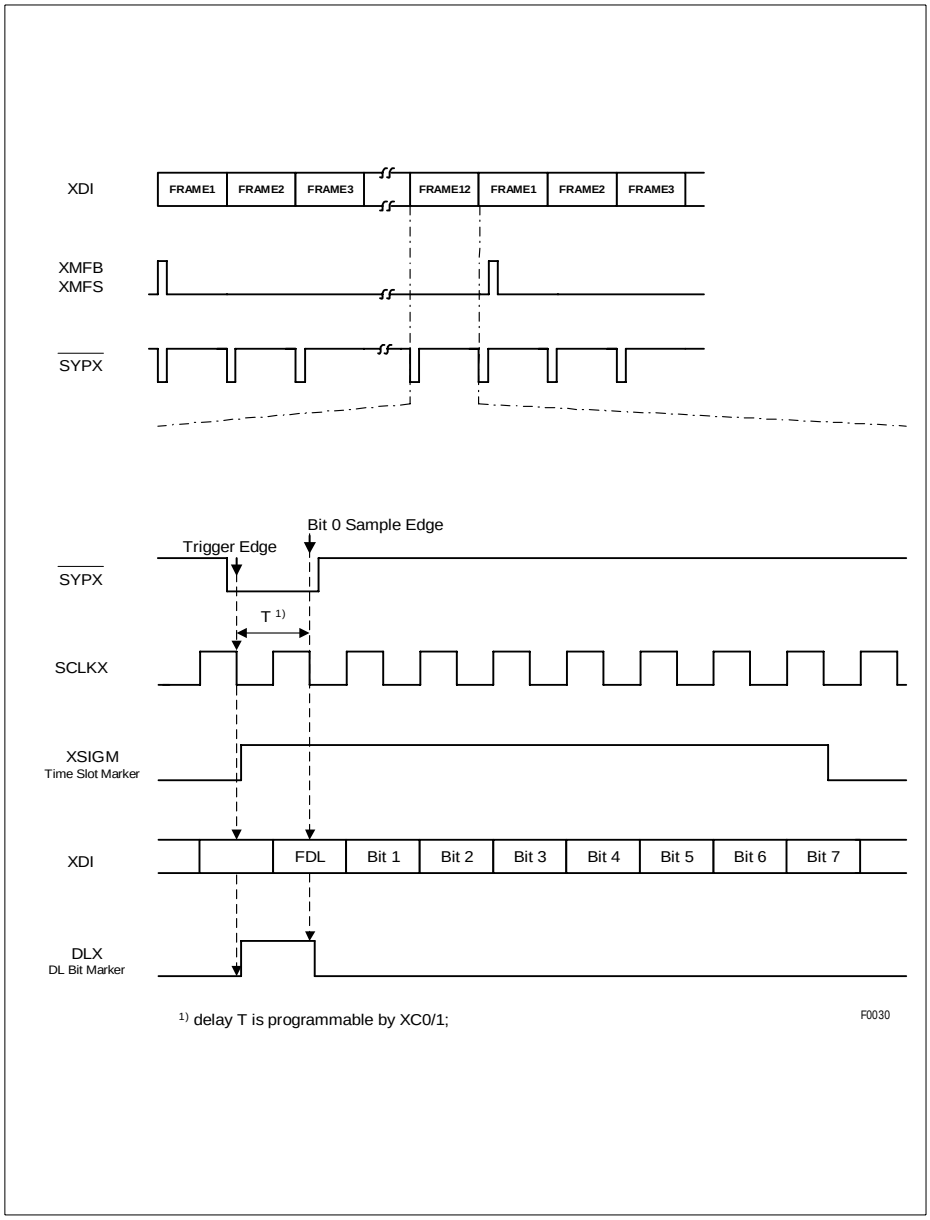


Figure 42 Transmit System Interface Clocking: 1.544 MHz (T1/J1)

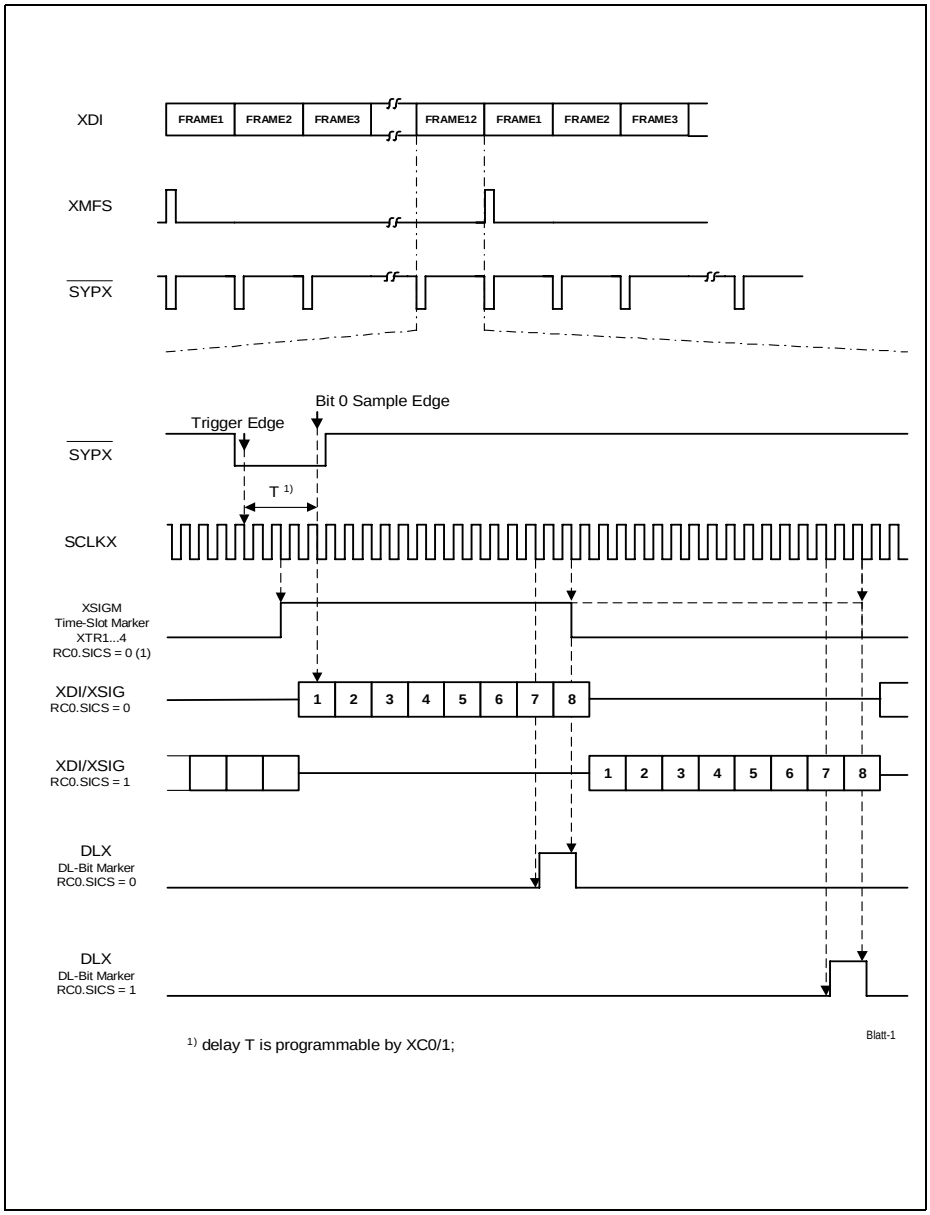


Figure 43 Transmit System Interface Clocking: 8 MHz/4 Mbit/s (T1/J1)

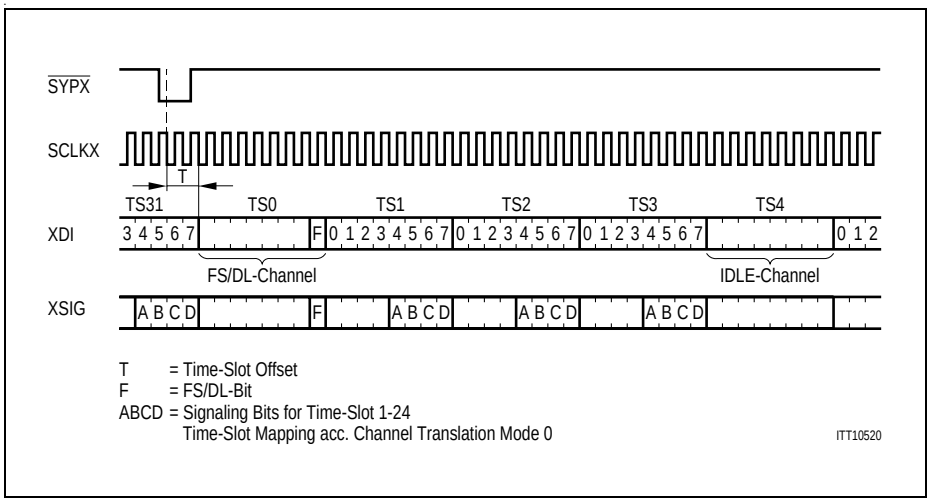


Figure 44 2.048 Mbit/s Transmit Signaling Clocking (T1/J1)

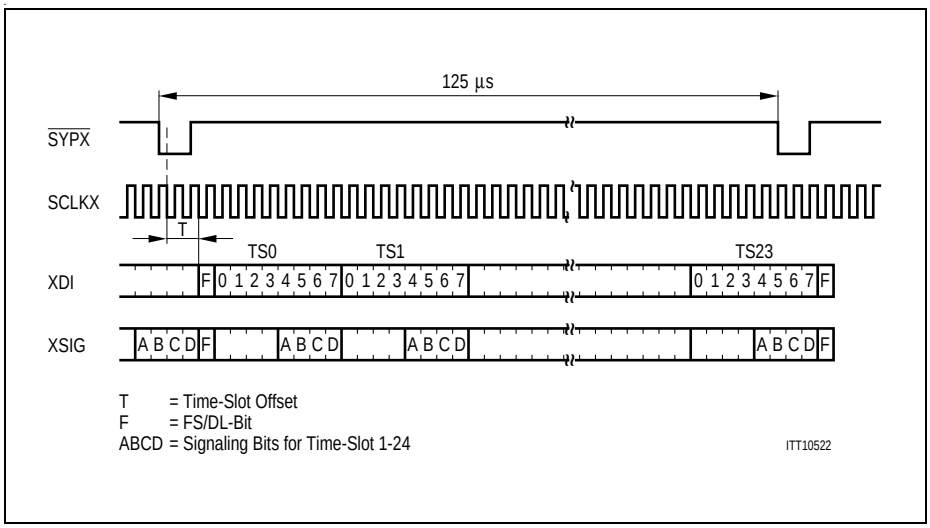


Figure 45 1.544 Mbit/s Transmit Signaling Highway (T1/J1)

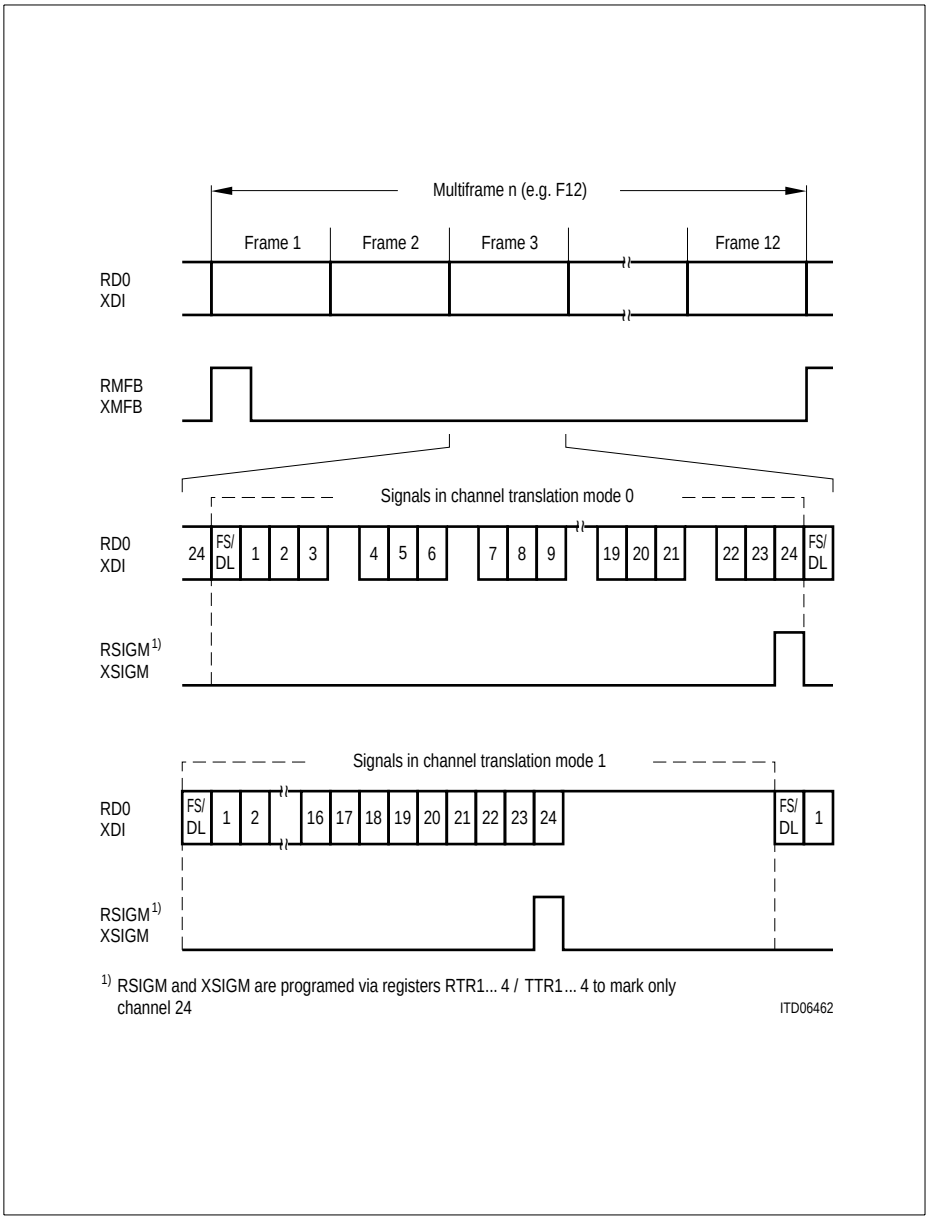


Figure 46 Signaling Marker for CAS/CAS-CC Applications (T1/J1)

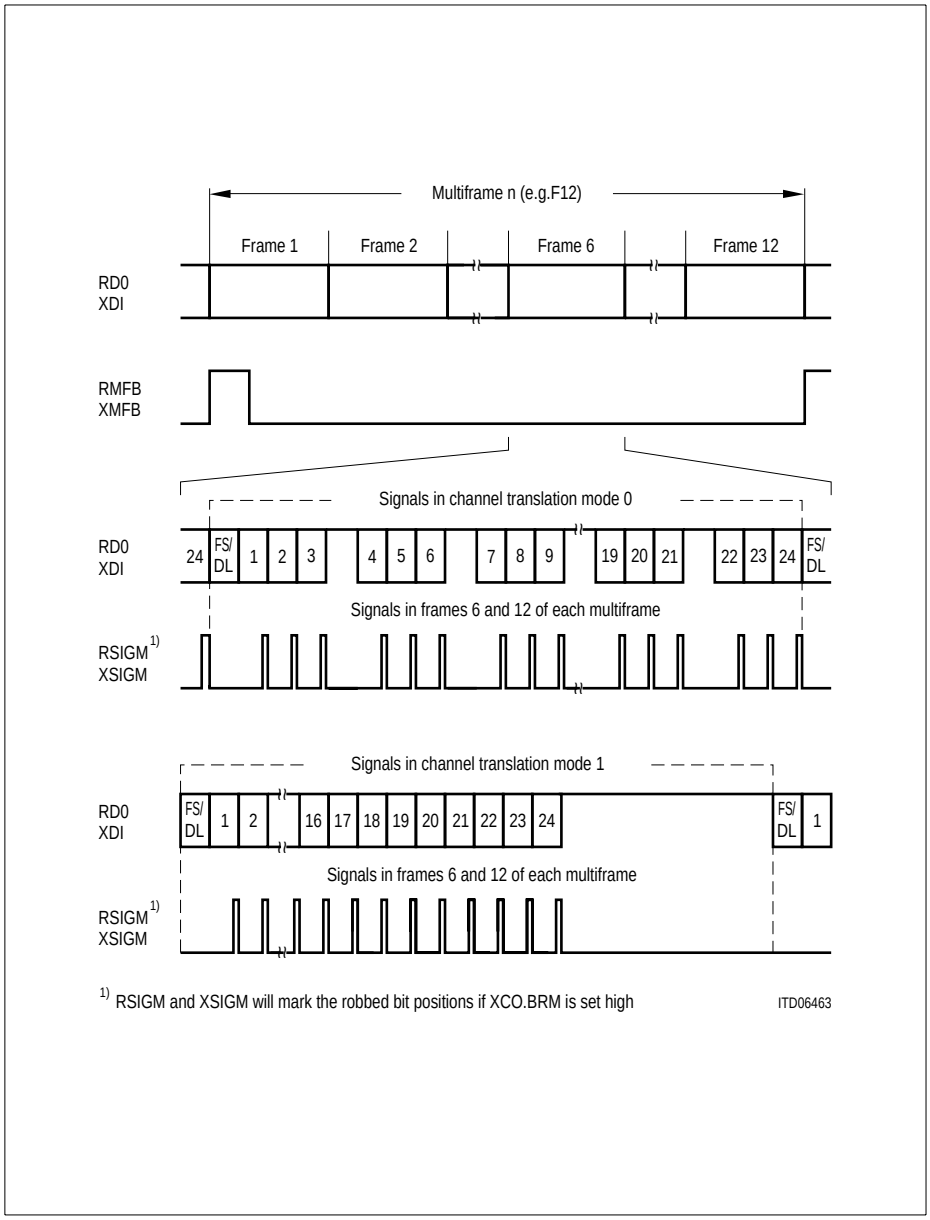


Figure 47 Signaling Marker for CAS-BR Applications (T1/J1)

Transmit Direction

FS/DL data on system transmit highway (XDI), time slot 0.

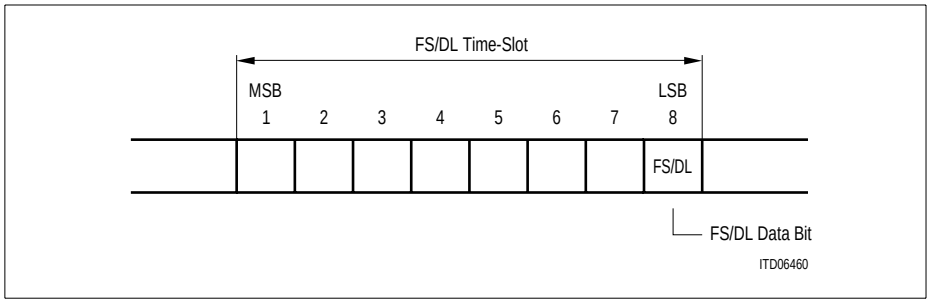


Figure 48 Transmit FS/DL Bits on XDI (T1/J1)

5.3.1 Transmit Signaling Controller (T1/J1)

Similar to the receive signaling controller the same signaling methods and the same time slot assignment are provided. The FALC®-LH performs the following signaling and data link methods.

5.3.1.1 HDLC or LAPD access

The transmit signaling controller of the FALC®-LH performs the FLAG generation, CRC generation, zero bit-stuffing and programmable IDLE code generation. Buffering of transmit data is done in the 64 byte deep XFIFO. The signaling information is multiplexed internally with the data applied on port XDI or XSIG.
In signaling controller transparent mode, fully transparent data transmission without HDLC framing is performed. Optionally the FALC®-LH supports the continuous transmission of the XFIFO contents.
Operating in HDLC or BOM mode “flags” or “idle” may be transmitted as interframe timefill. The FALC®-LH offers the flexibility to insert data during certain time slots. Any combinations of time slots may be programmed separately for the receive and transmit directions.

5.3.1.2 CAS Bit-robbing (T1/J1)

The signaling controller inserts the bit stream either on the transmit line side or if external signaling is enabled on the transmit system side. Signaling data may be sourced internally from registers XS1-12 or externally on port XSIG.
In external signaling mode the signaling data is sampled with the working clock of the transmit system interface (SCLKX) in conjunction with the transmit synchronous pulse ($\overline{\text{SYPX}}$). Data on XSIG is latched in the bit positions 5-8 per time slot, bits 1-4 are

ignored. The FS/DL bit is sampled on port XSIG and inserted in the outgoing data stream. The received CAS multiframe is inserted frame aligned into the data stream on XDI. Data sourced by the internal signaling controller overwrites the external signaling data.
Internal multiplexing of data and signaling data may be disabled on a per time slot basis (Clear Channel Capability). This is also valid when using the internal and external signaling mode.

5.3.1.3 Data Link Access in ESF/F24 and F72 Format (T1/J1)

The DL-channel protocol is supported as follows:
- access is done on a multiframe basis via registers XDL1-3 or
- HDLC access or transparent transmission (non HDLC mode) from XFIFO

The signaling information stored in the XFIFO is inserted in the DL bits of frame 26 to 72 in F72 format or in every other frame in ESF format. Operating in HDLC or BOM mode “flags” or “idle” may be transmitted as interframe timefill.

5.3.2 Transmit Elastic Buffer (T1/J1)

The transmit elastic store with a size of max. 2×193 bit (two frames) serves as a temporary store for the PCM data to adapt the system clock (SCLKX) to the internally generated clock for the transmit data, and to re-translate time slot structure used in the system to that of the line side. Its optimal start position is initiated when programming the transmit time slot offset values. A difference in the effective data rates of system side and transmit side may lead to an overflow/underflow of the transmit memory: thus, errors in data transmission to the remote end may occur. This error condition (transmit slip) is reported to the microprocessor via interrupt status registers.
The received bit stream from pin XDI is optionally stored in the transmit elastic buffer. The memory is organized as the receive elastic buffer. Programming of the transmit buffer size is done by SIC1.XBS1/0 :

- XBS1/0 = 00 : bypass of the transmit elastic buffer
- XBS1/0 = 01 : one frame buffer or 193 bits
  Maximum of wander amplitude (peak-to-peak): (1 UI = 648 ns)
  System interface clocking rate: 8.192 MHz:
  Max. wander : 80 UI in channel translation mode 0
  Max. wander : 50 UI in channel translation mode 1
  System interface clocking rate: 1.544 MHz:
  max. wander: 74 UI
  average delay after performing a slip: 96 bits
- XBS1/0 = 10 : two frame buffer or 386 bits
  System interface clocking rate: 8.192 MHz:
  142 UI in channel translation mode 0
  78 UI in channel translation mode 1
  System interface clocking rate: 1.544 MHz:
  max. wander: 126 UI
  average delay after performing a slip: 193 bits
- XBS1/0 = 11 : short buffer or 96 bits :
  System interface clocking rate: 8.192 MHz:
  Max. wander : 28 UI in channel translation mode 0; channel translation mode 1 not supported
  System interface clocking rate: 1.544 MHz:
  max. wander: 38 UI
  average delay after performing a slip: 48 bits

The functions of the transmit buffer are:

- Clock adaption between system clock (SCLKX) and internally generated transmit route clock (XCLK).
- Compensation of input wander and jitter.
- Frame alignment between system frame and transmit route frame

- Reporting and controlling of slips

Writing of received data from XDI is controlled by SCLKX and $\overline{\text{SYPX}}$/XMFS in conjunction with the programmed offset values for the transmit time slot/clock slot counters. Reading of stored data is controlled by the clock generated by DCO-X circuitry and the transmit framer. With the dejittered clock data is read from the transmit elastic buffer and are forwarded to the transmitter. Reporting and controlling of slips is automatically done according to the receive direction. Positive/negative slips are reported in interrupt status bits ISR5.XSP and ISR5.XSN.

A re-initialization of the transmit memory is done by re-programming the transmit time slot counter XC1 and with the next $\overline{\text{SYPX}}$ pulse. After that, this memory has its optimal start position.

The frequency of the working clock for the transmit system interface is programmable by SIC1.SXSC and SIC1.SRSC to be 1.544 or 8.192 MHz.
Generally the data or marker on the system interface are clocked off or latched on the falling edge of the SCLKX clock.

The following table gives an overview of the transmit buffer operating modes.

Table 29 Transmit Buffer Operating Modes (T1/J1)

SIC1.XBS1...0	Buffer Size	TS Offset programming	Slip performance
00 SCLKX=1.544 MHz	bypass	enabled	no
00 SCLKX=8.192 MHz	1 frame	enabled	yes[1)]
01	short buffer	enabled	yes
10	1 frame	enabled	yes
11	2 frames	enabled	yes If XSW.XTM = 1, slip is performed on the frame boundary

1) compatible with FALC®54

5.3.3 Transmitter (T1/J1)

The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the four selectable framing formats
- Insertion of service and data link information
- AIS generation (Blue Alarm)
- Remote alarm (yellow alarm) generation
- CRC generation and insertion of CRC bits
- CRC bits inversion in case of a previously received CRC error or in case of activating per control bit
- Generation of Loop Up/Down code
- IDLE code generation per DS0

The frame/multiframe boundaries of the transmitter may be externally synchronized by using the $\overline{\text{SYPX}}$/XMFS pin. Any change of the transmit time slot assignment subsequently produces a change of the framing bit positions on the line side. This feature is required if signaling and data link bits are routed through the switching network and are inserted in transmit direction via the system interface.

In loop-timed configuration (LIM2.ELT = 1) disconnecting the control of the transmit system highway from the transmitter is done by setting FMR5.XTM. The transmitter is now in a free running mode without any possibility to update the multiframe position in case of changing the transmit time slot assignment. The FS/DL bits are generated independently of the transmit system interface. For proper operation the transmit elastic buffer size must be programmed to 2 frames.

The contents of selectable time slots may be overwritten by the pattern defined via register IDLE. The selection of “idle channels” is done by programming the three-byte registers ICB1 … ICB3.

If AMI coding with zero code suppression (B7-stuffing) is selected, “clear channels” without B7-stuffing can be defined by programming registers CCB1 … CCB3.

5.3.4 Transmit Line Interface (T1/J1)

The analog transmitter transforms the unipolar bit stream to ternary (alternate bipolar) return to zero signals of the appropriate programmable shape. The unipolar data is provided by pin XDI and the digital transmitter.

Similar to the receive line interface three different data types are supported:

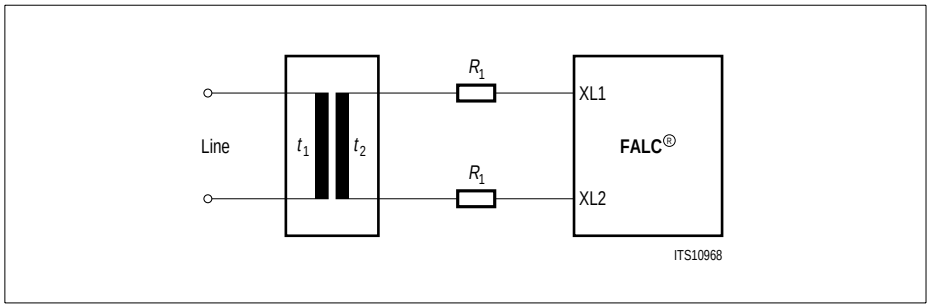


Figure 49 Transmitter Configuration (T1/J1)

Table 30 Example Transmitter Configuration Values (T1/J1)

Parameter	T1	J1
Characteristic Impedance [Ω]	100	110
R_1 (± 1 %) [Ω]	5	5
t2 : t1	1 : $\sqrt{2}$	1 : $\sqrt{2}$

- Ternary Signal
  Single rail data is converted into a ternary signal which is output on pins XL1 and XL2. Selection between B8ZS or simple AMI coding with zero code suppression (B7 stuffing) is provided. B7 stuffing may be disabled on a per time slot basis (Clear Channel capability). Selected by FMR0.XC1/0 and LIM1.DRS = 0.
- Dual rail data PCM(+), PCM(-) at multifunction ports XDOP and XDON with 50 % or 100 % duty cycle and with programmable polarity. Line coding is done in the same way as in the ternary interface. Selected by FMR0.XC1=1 and LIM1.DRS = 1.
- Unipolar data on port XOID is transmitted in NRZ (Non Return to Zero) with 100 % duty cycle to a fibre optical interface. Clocking off data is done with the rising edge of the transmit clock XCLK (1544 kHz) and with a programmable polarity. Selection is done by FMR0.XC1...0 = 00 and LIM1.DRS = 1.

5.3.5 Programmable Pulse Shaper and Line Build-Out (T1/J1)

In long haul applications the transmit pulse masks are optionally generated according to FCC68 and ANSI T1. 403. To reduce the crosstalk on the received signals the FALC®-LH offers the ability to place a transmit attenuator in the data path. Transmit attenuation is selectable from 0, -7.5, -15 or -22.5 dB (register LIM2.LBO2/1).
ANSI T1. 403 defines only 0...-15 dB.

The FALC®-LH includes a programmable pulse shaper to satisfy the requirements of ANSI T1. 102, also various DS1, DSX-1 specifications are met. The amplitude of the pulse shaper is programmable individually via the microprocessor interface to allow a maximum of different pulse templates. The line length is selected by programming the registers XPM2...0 as shown for typical values in the table below. The values with transformer ratio: 1:$\sqrt{2}$; cable: PULP 22AWG (100 Ω); serial resistors: 5 Ω. The XPM register values are given in decimal.

Table 31 Pulse Shaper Programming (T1/J1)

Range in m	Range in ft.	XPM0	XPM1	XPM2	XP04-XP00	XP14-XP10	XP24-XP20	XP34-XP30
		hexadecimal			decimal			
0...40	0...133	19	9B	01	25	24	6	3
40...81	133...266	5B	9F	01	27	26	7	3
81...122	266...399	7D	AB	01	29	27	10	3
122...162	399...533	7F	B7	01	31	27	13	3
162...200	533...655	5F	BB	01	31	26	14	3

The transmitter requires an external step up transformer to drive the line. The required programming values might vary between applications and have to be optimized according to external component values, parasitics, and so on.

5.3.6 Transmit Line Monitor (T1/J1)

The transmit line monitor compares the transmit line pulses on XL1 and XL2 with the transmit input signals received on pins XL1M and XL2M. The monitor detects faults on the primary side of the transformer and protects the device from damage by setting the transmit lines into high impedance state automatically. Faults on the secondary side can not be detected. To detect shorts, the configuration shown in **Figure 50** must be provided and the default (reset) value of registers XPM0...2 must be selected. Otherwise a short detection can not be guaranteed. Two conditions are detected by the monitor: “Transmit Line Ones Density“ (more than 31 consecutive zeroes) and “Transmit Line Shorted“. In both cases a transmit line monitor status change interrupt is provided.

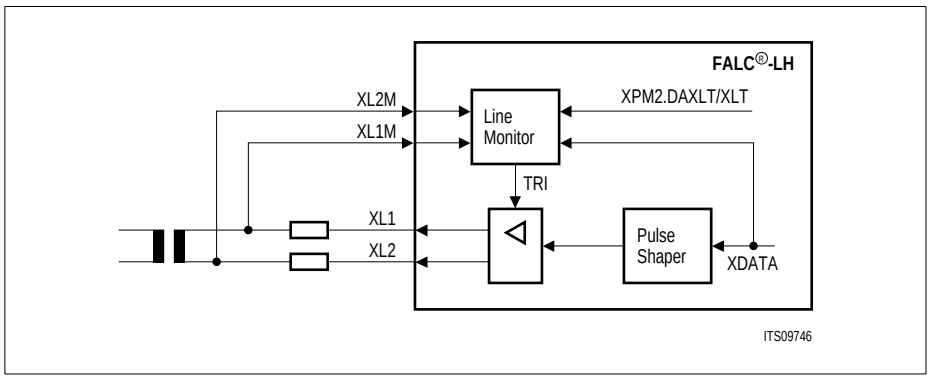


Figure 50 Transmit Line Monitor Configuration (T1/J1)

5.4 Framer Operating Modes (T1/J1)

5.4.1 General

Activated with bit FMR1.PMOD = 1.

PCM line bit rate	:	1.544 Mbit/s
Single frame length	:	193 bit, No. 1 … 193
Framing frequency	:	8 kHz
Organization	:	24 time slots, No. 1 … 24 with 8 bits each, No. 1 … 8 and one preceding F bit

Selection of one of the four permissible framing formats is performed by bits FMR4.FM1...0. These formats are:

F4 : 4-frame multiframe
F12 : 12-frame multiframe (D4)
ESF : Extended Superframe (F24)
F72 : 72-frame multiframe (SLC96)

The operating mode of the FALC®-LH is selected by programming the carrier data rate and characteristics, line code, multiframe structure, and signaling scheme.

The FALC®-LH implements all of the standard and/or common framing structures PCM 24 (T1, 1.544 Mbit/s) carriers. The internal HDLC-Controller supports all signaling procedures including signaling frame synchronization/synthesis in all framing formats.

After RESET, the FALC®-LH must be programmed with FMR1.PMOD = 1 to enable the T1(PCM24) mode. Switching between the framing formats is done via bit FMR4.FM1/0 for the receiver and for the transmitter.

5.4.2 General Aspects of Synchronization

Synchronization status is reported via bit FRS0.LFA (Loss Of Frame Alignment). Framing errors (pulse frame and multiframe) are counted by the Framing Error Counter FEC.

Loss of Frame Alignment (FRS0.LFA or opt. FRS0.LMFA) is declared if:
2 out of 4 framing bits or
2 out of 5 framing bits or
2 out of 6 framing bits in F4/12/72 format or
2 out of 6 framing bits per multiframe period in ESF format or
4 consecutive multiframe pattern in ESF format are incorrect.

It depends on the selected multiframe format and optionally on bit FMR2.SSP which framing bits are observed:
F4:FT bits → FRS0.LFA
F12, F72:SSP = 0: FT bits → FRS0.LFA: FS bits → FRS0.LFA

and FRS0.LMFA SSP = 1:FT → FRS0.LFA
FS → FRS0.LMFA
ESF:ESF framing bits → FRS0.LFA

The resynchronization procedure may be controlled by either one of the following procedure:

- Automatically (FMR4.AUTO = 1). Additionally, it may be triggered by the user by setting/resetting one of the bits FMR0.FRS (Force Resynchronization) or FMR0.EXLS (External Loss of Frame).
- User controlled, exclusively, via above control bits in the non-auto-mode (FMR4.AUTO = 0).

FT and FS bit conditions, i.e. pulse frame alignment and multiframe alignment can be handled separately if programmed via bit FMR2.SSP. Thus, a multiframe re-synchronization can be automatically initiated after detecting 2 errors out of 4/5/6 consecutive multiframing bits without influencing the state of the terminal framing.

In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state is reached if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.

In asynchronous state, the function of FMR0.EXLS is the same as above. Setting bit FMR0.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. Otherwise, a new frame search is started. This is useful in case the framing pattern that defines the pulseframe position is imitated periodically by a pattern in one of the speech/data channels.

The control bit FMR0.EXLS should be used first because it starts the synchronizer to search for a definite framing candidate.

To observe actions of the synchronizer, the Frame Search Restart Flag FRS0.FSRF is implemented. It toggles at the start of a new frame search if no candidate has been found at previous attempt.

When resynchronization is initiated, the following values apply for the time required to achieve the synchronous state in case there is one definite framing candidate within the data stream:

Table 32 Resynchronization Timing (T1/J1)

Frame Mode	Average	Maximum	Units
F4	1.0	1.5	ms
F12	3.5	4.5	ms
ESF	3.4	6.125	ms
F72	13.0	17.75	ms

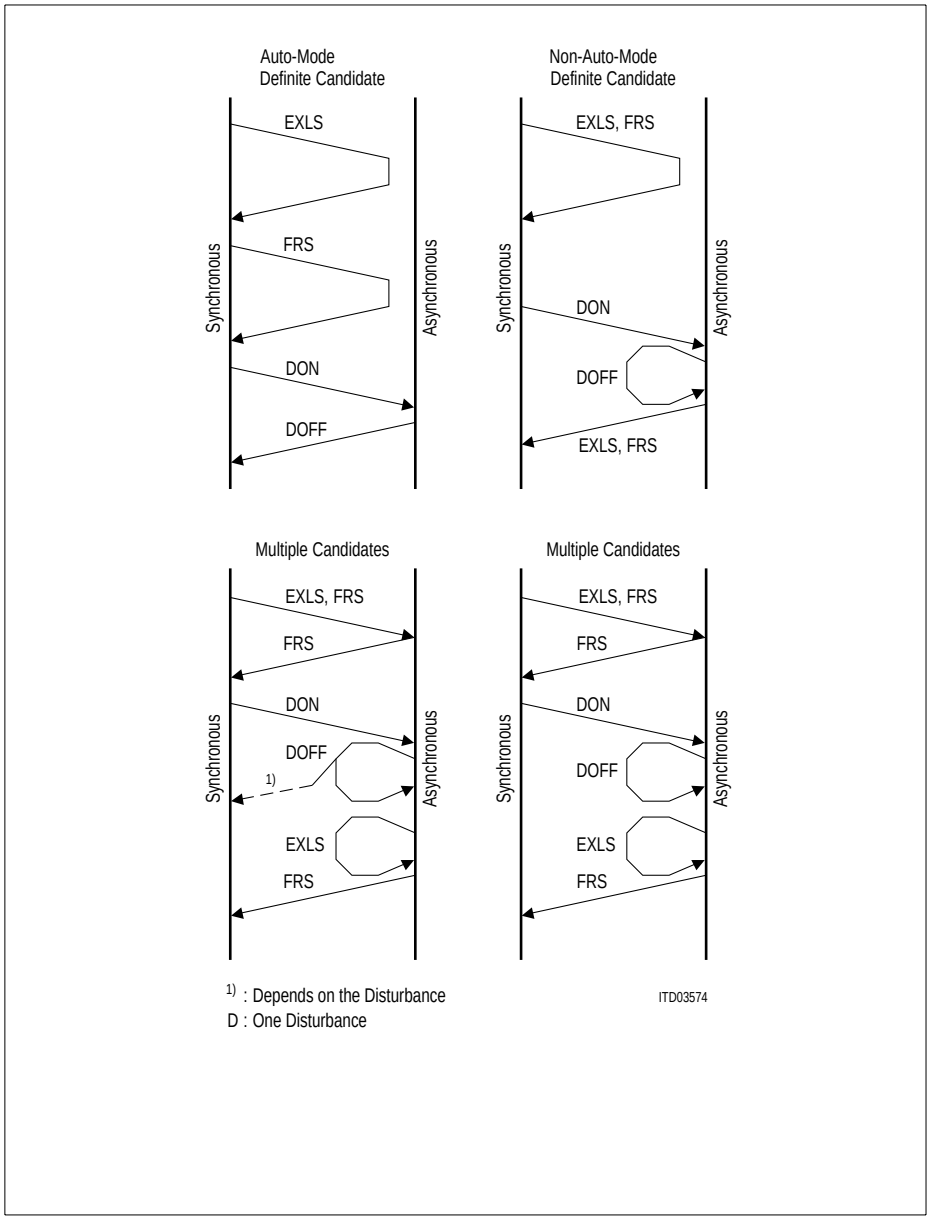


Figure 51 Influences on Synchronization Status (T1/J1)

Figure 51 gives an overview of influences on synchronization status for the case of different external actions. Activation of auto-mode and non-auto mode is performed via bit FMR4.AUTO. Generally, for initiating resynchronization it is recommended to use bit: FMR0.EXLS first. In case where the synchronizer remains in the asynchronous state, bit FMR0.FRS may be used to enforce it to lock onto the next framing candidate, although it might be a simulated one.

5.4.3 4-Frame Multiframe (F4 Format, T1/J1)

The allocation of the FT bits (bit 1 of frames 1 and 3) for frame alignment signal is shown in **Table 33**.
Remote alarm (yellow alarm) is indicated by setting bit 2 to ‘0’ in each time slot.

Table 33 4-Frame Multiframe Structure (T1/J1)

Frame Number	F_T	F_S
1	1	
2	–	Service bit
3	0	
4	–	Service bit

5.4.3.1 Synchronization Procedure

For multiframe synchronization, the terminal framing bits (FT bits) are observed. The synchronous state is reached if at least one terminal framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

5.4.4 12-Frame Multiframe (D4 or SF Format, T1/J1)

Normally, this kind of multiframe structure only makes sense when using the CAS Robbed Bit Signaling. The multiframe alignment signal is located at the FS-bit position of every other frame (refer to **Table 34**).

There are two possibilities of remote alarm (yellow alarm) indication:

- Bit 2 = 0 in each time slot of a frame, selected with bit FMR0.SRAF = 0
- The last bit of the multiframe alignment signal (bit 1 of frame 12) changes from ‘0’ to ‘1’, selected with bit FMR0.SRAF = 1.

Table 34 12-Frame Multiframe Structure (T1/J1)

Frame Number	F_T	F_S	Signaling Channel Designation
1	1	–	
2	–	0	
3	0	–	
4	–	0	
5	1	–	
6	–	1	A
7	0	–	
8	–	1	
9	1	–	
10	–	1	
11	0	–	
12	–	0/RA[1)]	B

[1)] This bit can be used for remote alarm indication, if FMR0.SRAF = 1 is set. In this case, this FS bit is not used to regain synchronization.

5.4.4.1 Synchronization Procedure

In the synchronous state terminal framing (FT bits) and multiframing (FS bits) are observed, independently. Further reaction on framing errors depends on the selected synchronization/resynchronization procedure (via bit FMR2.SSP):

- FMR2.SSP = ‘0’: terminal frame and multiframe synchronization are combined.
  Two errors within 4/5/6 framing bits (via bits FMR4.SSC1/0) of one of the above leads to the asynchronous state for terminal framing **and** multiframing. Additionally to the bit FRS0.LFA, loss of multiframe alignment is reported via bit FRS0.LMFA.
  The resynchronization procedure starts with synchronizing upon the terminal framing. If the pulse framing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.
- FMR2.SSP = ‘1’: terminal frame and multiframe synchronization are separated
  Two errors within 4/5/6 terminal framing bits lead to the same reaction as described above for the “combined” mode.
  Two errors within 4/5/6 multiframing bits lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported via bit FRS0.LMFA. The state of terminal framing is not influenced.
  Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

5.4.5 Extended Superframe (F24 or ESF Format, T1/J1)

The use of the first bit of each frame for the multiframe alignment word, the data link bits, and the CRC bits is shown in **Table 35** on page **142**.

Table 35 Extended Superframe Structure (F24, ESF; T1/J1)

Multiframe Frame Number	F Bits				Signaling Channel Designation
	Multiframe Bit Number	Assignments			
		FAS	DL	CRC	
1	0	–	m	–	
2	193	–	–	e_1	
3	386	–	m	–	
4	579	0	–	–	
5	772	–	m	–	
6	965	–	–	e_2	A
7	1158	–	m	–	
8	1351	0	–	–	
9	1544	–	m	–	
10	1737	–	–	e_3	
11	1930	–	m	–	
12	2123	1	–	–	B
13	2316	–	m	–	
14	2509	–	–	e_4	
15	2702	–	m	–	
16	2895	0	–	–	
17	3088	–	m	–	
18	3231	–	–	e_5	C
19	3474	–	m	–	
20	3667	1	–	–	
21	3860	–	m	–	
22	4053	–	–	e_6	
23	4246	–	m	–	
24	4439	1	–	–	D

5.4.5.1 Synchronization Procedures

For multiframe synchronization the FAS bits are observed. Synchronous state is reached if at least one framing candidate is definitely found, or the synchronizer is forced to lock onto the next available candidate (FMR0.FRS).

In the synchronous state the framing bits (FAS bits) are observed. The following conditions selected by FMR4.SSC1/0 lead to the asynchronous state:

- two errors within 4/5 framing bits

- two or more erroneous framing bits within one ESF multiframe
- 4 incorrect (1 out of 6) consecutive multiframes independent of CRC6 errors.

There are four multiframe synchronization modes selectable via FMR2.MCSP and FMR2.SSP.

- FMR2.MCSP/SSP = 00
  In the synchronous state, the setting of FMR0.FRS or FMR0.EXLS resets the synchronizer and initiates a new frame search. The synchronous state is reached again, if there is only one definite framing candidate. In the case of repeated apparent simulated candidates, the synchronizer remains in the asynchronous state.
  In asynchronous state, setting bit FMR0.FRS induces the synchronizer to lock onto the next available framing candidate if there is one. At the same time the internal framing pattern memory is cleared and other possible framing candidates are lost.

- FMR2.MCSP/SSP = 01
  Synchronization is achieved when 3 consecutive multiframe pattern are correctly found independent of the occurrence of CRC6 errors. If only one or two consecutive multiframe pattern were detected the FALC®-LH stays in the asynchronous state, searching for a possible additionally available framing pattern. This procedure is repeated until the framer has found three consecutive multiframe pattern in a row.

- FMR2.MCSP/SSP = 10
  This mode has been added in order to be able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS leads to synchronization on the next candidate available. However, only the previously assumed candidate is discarded in the internal framing pattern memory. The latter procedure can be repeated until the framer has locked on the right pattern (no extensive CRC errors).
  The synchronizer is completely reset and initiates a new frame search, if there is no multiframing found. In this case bit FSR0.FSRF toggles.

- FMR2.MCSP/SSP = 11
  Synchronization including automatic CRC6 checking
  Synchronization is achieved when framing pattern are correctly found and the CRC6 checksum is received without an error. If the CRC6 check failed on the assumed framing pattern the FALC®-LH stays in the asynchronous state, searching for a possible available framing pattern. This procedure is repeated until the framer has locked on the right pattern. This automatic synchronization mode has been added in order to reduce the microprocessor load.

5.4.5.2 Remote Alarm (yellow alarm) Generation/Detection

Remote alarm (yellow alarm) is indicated by the periodical pattern ‘1111 1111 0000 0000 …’ in the DL bits. Remote alarm is declared even in the presence of BER 1/1000. The alarm is reset when the “yellow alarm pattern“ no longer is detected.

Depending on bit RC1.SJR the FALC®-LH generates and detect the Remote Alarm according to JT G. 704. In the DL-bit position 16 continuos “1“ are transmitted if FMR0.SRAF=0 and FMR4.XRA=1.

Alternatively remote alarm can be indicated by setting bit 2 of every time slot after selecting FMR0.SRAF = 1.

5.4.5.3 CRC6 Generation and Checking (T1/J1)

Generation and checking of CRC6 bits transmitted/received in the e1-e6 bit positions is done according to ITU-T G.706. The CRC6 checking algorithm is enabled via bit FMR1.CRC. If not enabled, all check bits in the transmit direction are set. In the synchronous state received CRC6 errors are accumulated in a 16 bit error counter and are additionally indicated by an interrupt status.

- CRC6 Inversion

If enabled by bit RC0.CRCI, all CRC bits of one outgoing extended multiframe are automatically inverted in case a CRC error is flagged for the previous received multiframe. Setting the bit RC0.XCRCI inverts the CRC bits before transmitted to the distant end. This function is logically ored with RC0.CRCI.

- CRC6 Generation/Checking According to JT G. 706

Setting of RC1.SJR the FALC®-LH generates and check the CRC6 bits according to JT G. 706. The CRC6 checksum is calculated including the FS/DL bits. In synchronous state CRC6 errors increment an error counter.

5.4.6 72-Frame Multiframe (SLC96 Format, T1/J1)

The 72-multiframe is an alternate use of the FS-bit pattern and is used for carrying data link information. This is done by stealing some of redundant multiframing bits after the transmission of the 12-bit framing header (refer to **Figure 36** on page **146**). The position of A and B signaling channels (robbed bit signaling) is defined by zero-to-one and one-to-zero transitions of the FS bits and is continued when the FS bits are replaced by the data link bits.

Remote Alarm (Yellow Alarm) is indicated by setting bit 2 to zero in each time slot. An additional use of the D bits for alarm indication is user defined and must be done externally.

5.4.6.1 Synchronization Procedure

In the synchronous state terminal framing (FT bits) and multiframing (FS bits of the framing header) are observed independently. Further reaction on framing errors depends on the selected synchronization/resynchronization procedure (via bit FMR2.SSP):

- FMR2.SSP = ‘0’: terminal frame and multiframe synchronization are combined

  Two errors within 4/5/6 framing bits (via bits FMR4.SSC1/0) of one of the above lead to the asynchronous state for terminal framing **and** multiframing. Additionally to the resynchronization procedure starts with synchronizing upon the terminal framing. If the pulse framing has been regained, the search for multiframe alignment is initiated. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

- FMR2.SSP = ‘1’: terminal frame and multiframe synchronization are separated

  Two errors within 4/5/6 terminal framing bits lead to the same reaction as described above for the “combined” mode.
  Two errors within 4/5/6 multiframing bits lead to the asynchronous state only for the multiframing. Loss of multiframe alignment is reported via bit FRS0.LMFA. The state of terminal framing is not influenced.
  Now, the resynchronization procedure includes only the search for multiframe alignment. Multiframe synchronization has been regained after two consecutive correct multiframe patterns have been received.

Table 36 72-Frame Multiframe Structure (T1/J1)

Frame Number	F_T	F_S	Signaling Channel Designation
1	1	–	
2	–	0	B
3	0	–	
4	–	0	
5	1	–	
6	–	0	
7	0	–	
8	–	1	A
9	1	–	
10	–	1	
11	0	–	
12	–	1	
13	1	–	
14	–	0	B
15	0	–	
16	–	0	
17	1	–	
18	–	0	
19	0	–	
20	–	1	A
21	1	–	
22	–	1	
23	0	–	
24	–	1	
25	1	–	
26	–	D	
27	.	.	B
28	.	.	
.	1	–	
66	–	D	
67	0	–	
68	–	D	A
69	1	–	
70	–	D	
71	0	–	
72	–	D	

5.4.7 Summary of Frame Conditions (T1/J1)

Table 37 Summary Frame Recover/Out of Frame Conditions (T1/J1)

Format	Frame Recover Condition	Out of Frame Condition
F4	only one FT pattern found, optional forcing on next available FT framing candidate	2 out of 4/5/6 incorrect FT bits
F12 (D4) and F72 (SLC96)	FMR2.SSP = 0: Combined FT + FS framing search: First searching for FT pattern with optional forcing on next available framing candidates and then for 2 consecutive correct FS pattern[1]. FMR2.SSP = 1: Separated FT + FS pattern search: Loss of FT framing at first starts searching for FT and then for 2 consecutive correct FS pattern[1]. Loss of FS framing starts only the FS pattern[1]. search.	FMR2.SSP=0 : 2 out of 4/5/6 incorrect FT or FS bits FMR2.SSP= 1 : 2 out of 4/5/6 incorrect FT bits search FT and FS framing bits, 2 out of 4/5/6 incorrect FS bits search only the FS framing.
F24 (ESF)	FMR2.MCSP/SSP = 00: only one FAS pattern found, optional forcing on next available FAS framing candidate with discarding of all remaining framing candidates. FMR2.MCSP/SSP = 01: 3 consecutive correct multiframing found independent of CRC6 errors. FMR2.MCSP/SSP = 10: choosing multiple framing pattern step by step, optional forcing on next available FAS framing pattern with discarding only of the previous assumed framing candidate. FMR2.MCSP/SSP = 11: FAS framing correctly found and CRC6 check error free.	2 out of 4/5 incorrect FAS bits or 2 out of 6 incorrect FAS bits per multiframe or 4 consecutive incorrect multiframing pattern

[1] In F12 (D4) format bit 1 in frame 12 is excluded from the synchronization process, if FMR0.SRAF = 1.

5.5 Additional Functions (T1/J1)

5.5.1 Error Performance Monitoring and Alarm Handling

Alarm Indication Signal: Detection and recovery is flagged by bit FRS0.AIS and ISR2.AIS. Transmission is enabled via bit FMR1.XAIS.

Loss of Signal: Detection and recovery is flagged by bit FRS0.LOS and ISR2.LOS.

Remote Alarm Indication: Detection and release is flagged by bit FRS0.RRA and ISR2.RA/RAR. Transmission is enabled via bit FMR4.XRA.

Excessive Zeros: Detection is flagged by bit FRS1.EXZD.

Pulse Density Violation: Detection is flagged by bit FRS1.PDEN and ISR0.PDEN.

Transmit Line Shorted: Detection and release is flagged by bit FRS1.XLS and ISR1.XLSC.

Transmit Ones Density: Detection and release is flagged by bit FRS1.XLO and ISR1.XLSC.

Table 38 Summary of Alarm Detection and Release (T1/J1)

Alarm	Detection Condition	Clear Condition
Red Alarm or Loss of Signal (LOS)	no transitions (logical zeros) in a programmable time interval of 16 to 4096 consecutive pulse periods programmable receive input signal threshold	programmable number of ones (1-256) in a programmable time interval of 16 to 4096 consecutive pulse periods. A one is a signal with a level above the programmed threshold. or optionally the pulse density is fulfilled and no more than 15 or 99 contiguous zeros during the recovery interval are detected.
Blue Alarm or Alarm Indication Signal (AIS)	FMR4.AIS3 = 0: less than 3 zeros in 12 frames or 24 frames (ESF), FMR4.AIS3 = 1: less than 4 zeros in 12 frames or less than 6 zeros in 24 frames (ESF)	active for at least one multiframe. FMR4.AIS3 = 0: more than 2 zeros in 12 or 24 frames (ESF), FMR4.AIS3 = 1: more than 3 zeros in 12 frames or more than 5 zeros in 24 frames (ESF)

Table 38 Summary of Alarm Detection and Release (T1/J1) (cont'd)

Alarm	Detection Condition	Clear Condition
Yellow Alarm or Remote Alarm (RRA)	RC1.RRAM = 0: bit 2 = 0 in 255 consecutive time slots or FS bit = 1 of frame12 in F12 (D4) format or 8x1,8x0 in the DL channel (ESF) RC1.RRAM = 1: bit 2 = 0 in every time slot per frame or FS bit = 1 of frame12 in F12 (D4) format or 8x1,8x0 in the DL channel (ESF)	RC1.RRAM = 0: set conditions no longer detected. RC1.RRAM = 1: bit 2 = 0 not detected in 3 consecutive frames or FS bit not detected in 3 consecutive multiframes or 8x1,8x0 not detected for 3 times in a row (ESF).
Excessive Zeros (EXZD)	more than 7 (B8ZS code) or more than 15 (AMI code) contiguous zeros	Latched Status: cleared on read
Pulse Density Violation (PDEN)	less than 23 ones received in a floating time window of 192 bits or more than 15 consecutive zeros (see **Chapter 5.5.9**)	
Transmit Line Short (XLS)	If XL1 and XL2 are shortened for at least 32 pulses; pins XL1 and XL2 are forced into a high impedance state automatically, if bit XPM2.DAXLT is reset.	After 32 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still existing, the outputs XL1/2 are switched into high impedance state again. When the short disappears pins XL1/2 are activated automatically.
Transmit Ones Density (XLO)	32 consecutive zeros in the transmit data stream on XL1/2	Cleared with each transmitted pulse

RRA detection operates in the presence of 10^{-3} bit error rate.

5.5.2 Auto Modes

- Automatic remote alarm (Yellow Alarm) access
  If the receiver has lost its synchronization (FRS0.LFA) a remote alarm (yellow alarm) can be sent to the distant end automatically, if enabled by bit FMR2.AXRA. In synchronous state the remote alarm bit is removed.
- Automatic AIS to system interface
  In asynchronous state the synchronizer enforces an AIS to the receive system interface automatically. However, received data may be switched through transparently if bit FMR2.DAIS is set.
- Automatic clock source switching
  In Slave mode (LIM0.MAS = 0) the DCO-R synchronizes to the recovered route clock. In case of Loss of Signal LOS the DCO-R switches to Master mode automatically.
- Automatic freeze signaling:
  Updating of the received signaling information is controlled by the freeze signaling status. Optionally automatic freeze signaling can be disabled by setting bit SIC3.DAF.

5.5.3 Error Counter

The FALC®-LH offers five error counters where each of them has a length of 16 bit. They record code violations, framing bit errors, CRC6 bit errors, errored blocks and PRBS bit errors. Each of the error counters is buffered. Updating the buffer is done in two modes:

- one second accumulation
- on demand via handshake with writing to the DEC register

In the one second mode an internal one second timer updates these buffers and reset the counter to accumulate the error events in the next one second period. The error counter can not overflow. Error events occurring during reset are not lost.

5.5.4 Errored Second

The FALC®-LH supports the error performance monitoring by detecting the following alarms or error events in the received data:
framing errors, CRC errors, code violations, loss of frame alignment, loss of signal, alarm indication signal, receive and transmit slips.
With a programmable interrupt mask register IMR4 all these alarms or error events can generate an Errored Second Interrupt (ISR3.ES) if enabled.

5.5.5 Second Timer

Additionally a one second timer interrupt is generated internally to indicate that the enabled alarm status bits or the error counters have to be checked. The timing is derived from RCLK.

5.5.6 Clear Channel Capability

For support of common T1 applications, clear channels can be specified via the 3-byte register bank CCB1 ... CCB3. In this mode the contents of selected transmit time slots are not overwritten by internally or externally sourced bit-robbing and zero code suppression (B7 stuffing) information. Remote alarm signaling, however, overwrites cleared channels.

5.5.7 In-Band Loop Generation and Detection

The FALC®-LH generates and detects a framed or unframed in-band loop-up/activate (00001) and loop-down/deactivate (001) pattern according to ANSI T1. 403 with bit error rates as high as 1/100. Framed or unframed in-band loop code is selected by LCR1.FLLB. Replacing the in-band loop codes with transmit data is done by FMR5.XLD/XLU.
The FALC®-LH also offers the ability generating and detecting of a flexible in-band loop up - and down pattern (LCR1.LLBP = 1). The loop up and loop down pattern is individual programmable from 2 to 8 bit in length (LCR1.LAC1/0 and LCR1.LDC1/0). Programming of loop codes is done in registers LCR2 and LCR3.
Status and interrupt-status bits inform the user whether a loop-up or loop-down code was detected.

5.5.8 Transparent Mode

The transparent modes are useful for loopbacks or for routing data unchanged through the FALC®-LH.

In receive direction, transparency for ternary or dual/single rail unipolar data is achieved if the receiver is in the synchronous state and FMR5.RTF has been selected. All bits in F-bit position of the incoming multiframe are forwarded to RDO and inserted in the FS/DL time slot or in the F-bit position. In asynchronous state the received data may be transparently switched through if bit FMR2.DAIS is set. Setting of bit LOOP.RTM disconnects control of the elastic buffer from the receiver. The elastic buffer is now in a “free running” mode without any possibility to update the time slot assignment to a new frame position in case of re-synchronization of the receiver. Together with FMR2.DAIS this function may be used to realize undisturbed transparent reception.

Setting bit FMR4.TM switches the FALC®-LH in transmit transparent mode:

In transmit direction bit 8 of the FS/DL time slot from the system highway (XDI) is inserted in the F-bit position of the outgoing frame. For complete transparency the internal signaling controller, IDLE code generation, AIS/RA alarm generation, single channel and payload loop back has to be disabled and “Clear Channels” have to be defined via registers CCB1…3.

5.5.9 Pulse Density Detection

The FALC®-LH examines the receive data stream on the pulse density requirement which is defined by ANSI T1. 403. More than 15 consecutive zeros or less than 23 ones in each and every time window of 193 data bits are detected. Violations of these rules are indicated by setting the status bit FRS1.PDEN and the interrupt status bit ISR0.PDEN. Generation of the interrupt status may be programmed either with the detection or with any change of state of the pulse density alarm (GCR.SCI).

5.6 Test Functions (T1/J1)

5.6.1 Pseudo-Random Bit Sequence Generation and Monitor

The FALC®-LH has the ability to generate and monitor a 2^{15}-1 and 2^{20}-1 pseudo-random bit sequences (PRBS). The generated PRBS pattern is transmitted optionally inverted or not to the remote end via pins XL1/2 or XDOP/N. Generating and monitoring of PRBS pattern is done according to ITU-T O. 151 and TR62411 with maximum 14 consecutive zero restriction.
The PRBS monitor senses the PRBS pattern in the incoming data stream. Synchronization is done on the inverted and non inverted PRBS pattern. The current synchronization status is reported in status and interrupt status registers. Enabled by bit LCR1.EPRM each PRBS bit error increments an error counter (BEC). Synchronization is reached within 400 ms with a probability of 99.9% and a BER of 1/10 (pattern defined by ITU-T O.151).

5.6.2 Remote Loop

In the remote loopback mode the clock and data recovered from the line inputs RL1/2 or RDIP/RDIN are routed back to the line outputs XL1/2 or XDOP/XDON via the analog or digital transmitter. As in normal mode they are also processed by the synchronizer and then sent to the system interface.The remote loopback mode is selected by setting the respective control bits LIM1.RL+JATT. Received data may be looped with or without the transmit jitter attenuator (FIFO).

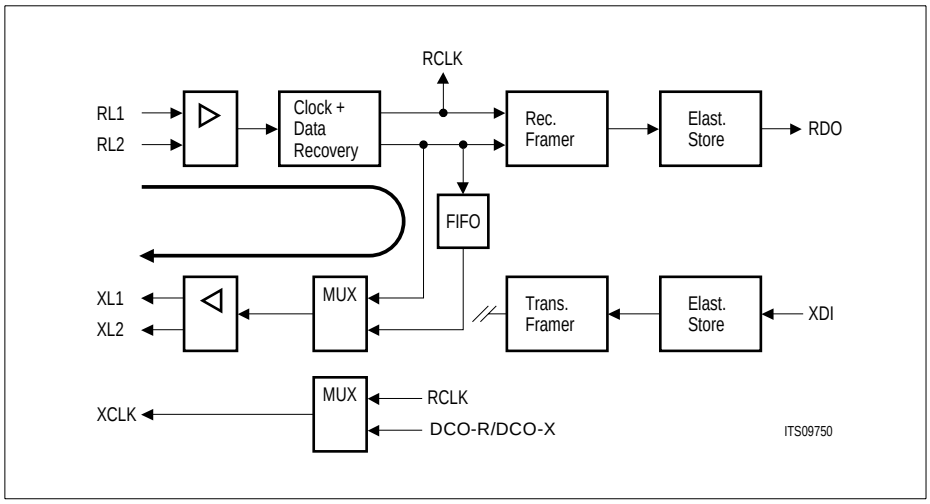


Figure 52 Remote Loop (T1/J1)

5.6.3 Payload Loop Back

To perform an effective circuit test a line loop is implemented.

If the payload loopback (FMR2.PLB) is activated the received 192 bits of payload data is looped back to the transmit direction. The framing bits, CRC6 and DL bits are not looped, if FMR4.TM = 0. They are originated by the FALC®-LH transmitter. If FMR4.TM= 1 the received FS/DL bit is sent transparently back to the line interface. Following pins are ignored: XDI, XSIG, SCLKX, $\overline{\text{SYPX}}$ and XMFS. All the received data is processed normally. With bit FMR2.SAIS an AIS can be sent to the system interface via pin RDO.

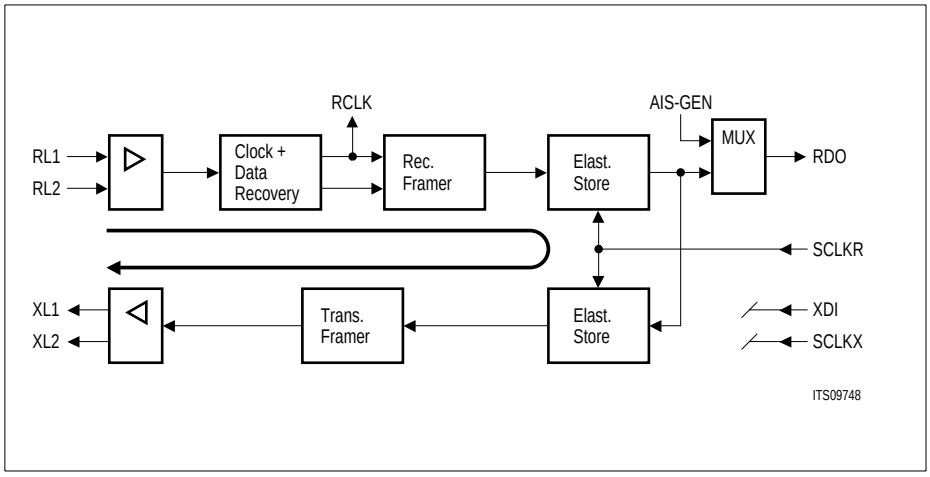


Figure 53 Payload Loop (T1/J1)

Note: Returned data is not multiframe synchronous.

5.6.4 Local Loop

The local loopback mode, selected by LIM0.LL = 1, disconnects the receive lines RL1/2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The bit stream is transmitted on the line undisturbedly. However, an AIS to the distant end can be enabled by setting FMR1.XAIS without influencing the data looped back to the system interface.

Note that enabling the local loop usually invokes an out of frame error until the receiver can resynchronize to the new framing. The serial codes for transmitter and receiver have to be identical.

In digital interface NRZ mode, a clock must be provided on pin RCLKI (=RL2) to enable switching into local loop mode.

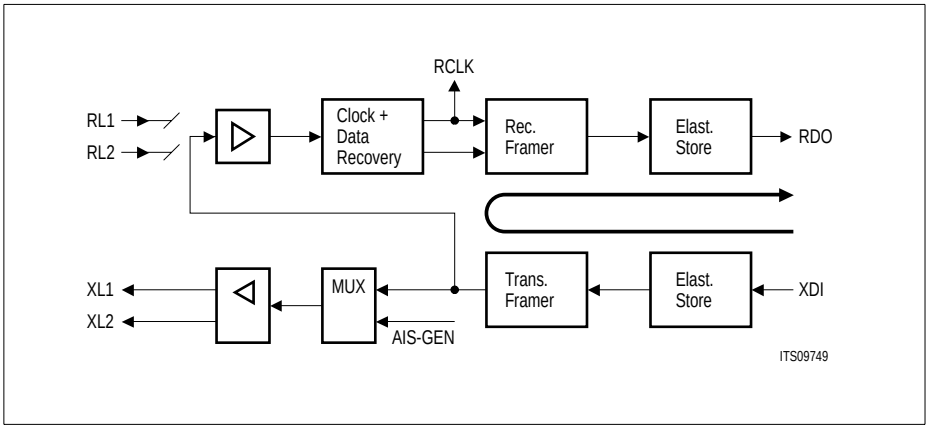


Figure 54 Local Loop (T1/J1)

5.6.5 Single Channel Loop Back (loopback of time slots)

The channel loopback is selected via LOOP.ECLB = 1.

Each of the 24 time slots may be selected for loopback from the system PCM input (XDI) to the system PCM output (RDO). This loopback is programmed for one time slot at a time selected by register LOOP. During loopback, an idle channel code programmed in register IDLE is transmitted to the remote end in the corresponding PCM route time slot.

For the time slot test, sending sequences of test patterns like a 1 kHz check signal should be avoided. Otherwise, an increased occurrence of slips in the tested time slot disturbs testing. These slips do not influence the other time slots and the function of the receive memory. The usage of a quasi-static test pattern is recommended.

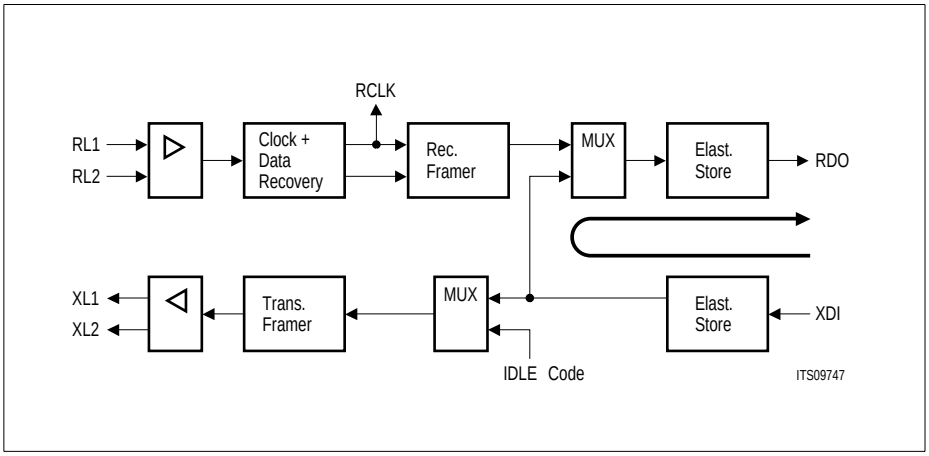


Figure 55 Channel Loopback (T1/J1)

5.6.6 Alarm Simulation (T1/J1)

Alarm simulation does not affect the normal operation of the device, i.e. all time slots remain available for transmission. However, possible “real“ alarm conditions are not reported to the processor or to the remote end when the device is in the alarm simulation mode.

The alarm simulation is initiated by setting the bit FMR0.SIM. The following alarms are simulated:

- Loss of Signal (red alarm)
- Alarm Indication Signal AIS (blue alarm)
- Loss of pulse frame
- Remote alarm (yellow alarm) indication
- Receive and transmit slip indication
- Framing error counter
- Code violation counter
- CRC6 error counter

Some of the above indications are only simulated if the FALC®-LH is configured in a mode where the alarm is applicable.

The alarm simulation is controlled by the value of the Alarm Simulation Counter: FRS2.ESC which is incremented by setting bit: FMR0.SIM.

Clearing of alarm indications:

- Automatically for LOS, remote (yellow) alarm, AIS, and loss of synchronization or
- User controlled for slips by reading the corresponding interrupt status register ISR3 or
- Error counter have been cleared by reading the corresponding counter registers.

Clearing is only possible at defined counter steps of FRS2.ESC. For complete simulation (FRS2.ESC = 0), eight simulation steps are necessary.

6 Operational Description E1

6.1 Operational Overview E1

The FALC®-LH in principle can be operated in two modes, which are either E1 mode or T1/J1 mode.

The device is programmable via a microprocessor interface which enables byte or word access to all control and status registers.

After reset the FALC®-LH must be initialized first. General guidelines for initialization are described in sections **“Device Initialization in E1 Mode” on page 158** and **“Device Initialization in T1/J1 Mode” on page 163**

The status registers are read-only and are updated continuously. Normally, the processor reads the status registers periodically to analyze the alarm status and signaling data.

6.2 Device Reset E1

The FALC®-LH is forced to the reset state if a high signal is input on pin RES for a minimum period of 20 µs. During reset the FALC®-LH needs an active clocks on pins SCLKR, SCLKX, XTAL1 and XTAL3. All output stages except of CLK16M, CLK12M, CLK8M, CLKX, $\overline{\text{FSC}}$, XCLK and RCLK are in a high impedance state, all internal flip-flops are reset and most of the control registers are initialized with default values.

SIgnals (for example RL1/2 receive line) should not be applied before the device is powered up.

After reset the device is initialized to E1 operation.

6.3 Device Initialization in E1 Mode

After reset, the FALC®-LH is initialized for doubleframe format with register values listed in the following table.

Table 39 Initial Values after Reset (E1)

Register	Reset Value	Meaning
FMR0	00_H	NRZ coding, no alarm simulation;XL1/2 stay tristate
FMR1 FMR2	00_H 00_H	PCM 30 – doubleframe format, 4.096 Mbit/s system data rate, no AIS transmission to remote end, payload loop off.
SIC1 SIC2 SIC3	00_H 00_H 00_H	8.192-MHz system clocking rate, receive buffer 2 frames, transmit buffer bypass, automatic freeze signaling

Table 39 Initial Values after Reset (E1) (cont'd)

Register	Reset Value	Meaning
LOOP	00_H	Channel loop back and single frame mode are disabled.
XSW	40_H	All bits of the transmitted service word are cleared (bit 2
XSP	00_H	excluded). Spare bit values are cleared.
TSWM	00_H	No transparent mode active.
XC0	00_H	The transmit clock offset is cleared.
XC1	$9C_H$	The transmit time slot offset is cleared.
RC0	00_H	The receive clock slot offset is cleared; 1st channel phase is active on PCM highway.
RC1	$9C_H$	The receive time slot offset is cleared.
IDLE	00_H	Idle channel code is cleared.
ICB 1 … 4	00_H	Normal operation (no 'Idle Channel' selected).
LIM0	00_H	Slave Mode, Local Loop off, CLKX=2.048 MHz active high, short haul mode, no LOS indication on RCLK
LIM1	00_H	Analog interface selected, Remote Loop off
PCD	00_H	Pulse Count for LOS Detection cleared
PCR	00_H	Pulse Count for LOS Recovery cleared
XPM2...0	$7B_H$,03_H,00_H	Transmit Pulse Mask
IMR0...4	FF_H,FF_H,FF_H, FF_H,FF_H,	All interrupts are disabled
RTR1...4	00_H,00_H,00_H,	No time slots selected
TTR1...4	00_H,	
MODE	00_H	Signaling controller disabled
PRE	00_H	Preamble cleared
RAH1/2	FD_H, FF_H	Compare register for receive address cleared
RAL1/2	FF_H, FF_H	

E1 Initialization

For a correct start up of the Primary Access Interface a set of parameters specific to the system and hardware environment must be programmed after reset goes inactive. Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T and ETSI recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 40** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational

set up, for example, may be programmed simultaneously. The bit FMR1.PMOD should always be kept low (otherwise T1/J1 mode is selected).

Table 40 Initialization Parameters (E1)

Basic Set Up	E1
Mode Select	FMR1.PMOD = 0
Specification of Line interface and clock generation	LIM0, LIM1, XPM2...0
Line interface coding	FMR0.XC1/0, FMR0.RC1/0
Loss of Signal detection/recovery conditions	PCD, PCR, LIM1, LIM2
System interface mode	FMR1.IMOD
Transmit offset counters	XC0.XCO, XC1.XTO
Receive offset counters	RC0.RCO, RC1.RTO
AIS to system interface	FMR2.DAIS/SAIS

Operational Set Up	E1
Select framing	FMR2.RFS1/0, FMR1.XFS
Framing additions	RC1.ASY4, RC1.SWD
Synchronization mode	FMR1.AFR, FMR2.ALMF
Signaling mode	XSP, XSW, FMR1.ENSA, XSA8...4, TSWM, MODE, CCR1, CCR3, PRE, RAH1/2, RAL1/2

Features like channel loop back, idle channel activation, extensions for signaling support, alarm simulation, … may be activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Note: Read access to unused register addresses: value should be ignored.
Write access to unused register addresses: should be avoided, or set to '00' hex.
All control registers (except XFIFO, XS1-16, CMDR, DEC) are of type: Read/ Write.

Specific E1 Register Settings

The following is a suggestion for a basic initialization to meet most of the E1 requirements. Depending on different applications and requirement any other initialization can be used.

Table 41 Line Interface Initialization (E1)

Register	Function
FMR0.XC0 FMR0.RC0 LIM1.DRS FMR3.CMI	The FALC®-LH supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI and HDB3 are supported. For the digital line interface modes (dual or single rail) the FALC®-LH supports AMI, HDB3, CMI (with and without HDB3 precoding) and NRZ.
PCD = $0A_H$	LOS detection after 176 consecutive “zeros” (fulfills G.775 spec).
PCR = 15_H	LOS recovery after 22 “ones” in the PCD interval. (fulfills G.775).
LIM1.RIL2-0 = 03_H	LOS threshold (fulfills G.775; see DC characteristics)

E1 Framer Initialization

The selection of the following modes during the basic initialization supports the ETSI requirements for E-Bit Access, Remote Alarm and Synchronization (please refer also to FALC®-LH driver code of the Reference System EASY2255-R1 and application notes) and helps to reduce the software load. They are very helpful especially to meet requirements as specified in ETS300 011.

Table 42 Framer Initialization (E1)

Register	Function
XSP.AXS = 1	ETS300 011 C4.x for instance requires the sending of E-Bits in TS0 if CRC4 errors have been detected. By programming XSP.AXS = 1 the submultiframe status is inserted automatically in the next outgoing multiframe.
XSP.EBP = 1	If the FALC®-LH has reached asynchronous state the E-Bit is cleared if XSP.EBP = 0 and set if XSP.EBP = 1. ETS300 011 requires that the E-Bit is set in asynchronous state.
FMR2.AXRA = 1	The transmission of RAI via the line interface is done automatically by the FALC®-LH in case of Loss of Frame Alignment (FRS0.LFA = 1). If basic framing has been reinstalled RAI is automatically reset.
FMR2.FRS1/2 = 10 FMR1.AFR = 1	In this mode a search of double framing is automatically reinitiated if no CRC4 multiframing could be found within 8ms. Together with FMR2.AXRA = 1 this mode is essential to meet ETS300 011 and reduces the processor load heavily.

Table 42 Framer Initialization (E1) (cont'd)

Register	Function
FMR2.ALMF = 1	The receiver initiates a new basic- and multiframing research if more than 914 CRC4 errors have been detected in one second.
FMR2.FRS1/0 = 11	In the interworking mode the FALC®-LH stays in double framing format if no multiframe pattern could be found in a time interval of 400 ms. This is also indicated by a 400 ms interrupt. Additionally the extended interworking mode (FMR3.EXTIW = 1) will activate after 400 ms the remote alarm (FMR2.AXRA = 1) and will still search the multiframing without switching completely to the double framing. A complete resynchronization in an 8 ms interval is not initiated.

Table 43 HDLC Controller Initialization (E1)

Register	Function
MODE = 88_H	HDLC Receiver active, no address comparison.
CCR1 = 18_H	Enable Signaling via TS0...31, Interframe Time Fill with continuous FLAGs.
IMR0.RME = 0 IMR0.RPF = 0 IMR1.XPR = 0	Unmask interrupts for HDLC processor requests.
RTR3.TS16 = 1 TTR3.TS16 = 1	Select TS16 for HDLC data reception and transmission.

Table 44 CAS-CC Initialization (E1)

Register	Function
XSP.CASEN = 1	Send CAS info stored in the XS1...16 registers.
IMR0.CASC = 0	Enable interrupt with any data change in the RS1...16 registers.

Note: After the device initialization a software reset should be executed by setting of bits CMDR.XRES/RRES.

7 Operational Description T1/J1

7.1 Operational Overview T1/J1

The FALC®-LH in principle can be operated in two modes, which are either E1 mode or T1/J1 mode. There are only minor differences between T1 and J1 mode which are described in **Table 48**.

The device is programmable via a microprocessor interface which enables byte or word access to all control and status registers.

After reset the FALC®-LH must be initialized first. General guidelines for initialization are described in sections **“Device Initialization in E1 Mode” on page 158** and **“Device Initialization in T1/J1 Mode” on page 163**

The status registers are read-only and are updated continuously. Normally, the processor reads the status registers periodically to analyze the alarm status and signaling data.

7.2 Device Reset T1/J1

The FALC®-LH is forced to the reset state if a high signal is input on pin RES for a minimum period of 20 µs. During reset the FALC®-LH needs an active clocks on pins SCLKR, SCLKX, XTAL1 and XTAL3. All output stages except of CLK16M, CLK12M, CLK8M, CLKX, $\overline{\text{FSC}}$, XCLK and RCLK are in a high impedance state, all internal flip-flops are reset and most of the control registers are initialized with default values.

SIgnals (for example RL1/2 receive line) should not be applied before the device is powered up.

After reset the device is initialized to E1 operation. Switching to T1/J1 mode is done by software (FMR1.PMOD = 1).

7.3 Device Initialization in T1/J1 Mode

After reset, the FALC®-LH is initialized for E1 doubleframe format. To initialize T1/J1 mode, bit FMR1.PMOD has to be set high. After the internal clocking is settled to T1/J1mode (takes up to 20 µs), the following register values are initialized:

Table 45 Initial Values after reset and FMR1.PMOD = 1 (T1/J1)

Register	Initiated Value	Meaning
FMR0	00_H	NRZ coding, no alarm simulation; XL1/2 stay tristate
FMR1 FMR2	10_H 00_H	PCM 24 mode, 4.096 Mbit/s system data rate, no AIS transmission to remote end or system interface, payload loop off, channel translation mode 0
SIC1 SIC2, SIC3	00_H 00_H 00_H	8.192-MHz system clocking rate, Receive Buffer 2 Frames, Transmit Buffer bypass, Automatic freeze signaling, data is active in the first channel phase
LOOP	00_H	Channel loop back is disabled.
FMR4 FMR5	00_H 00_H	Remote alarm indication towards remote end disabled. LFA condition: 2 out of 4 framing bits, Non-auto-synchronization mode, F12 multiframing, internal bit-robbing access disabled
XC0 XC1	00_H $9C_H$	The transmit clock slot offset is cleared. The transmit time slot offset is cleared.
RC0 RC1	00_H $9C_H$	The receive clock slot offset is cleared. The receive time slot offset is cleared.
IDLE ICB 1 … 3	00_H 00_H	Idle channel code is cleared. Normal operation (no “Idle Channels” selected).
CCB 1 … 3	00_H	Normal operation (no clear channel operation).
LIM0 LIM1 PCD PCR	00_H 00_H 00_H 00_H	Slave Mode, Local Loop off, CLKX=2.048 MHz active high, short haul mode, no LOS indication on RCLK Analog interface selected, Remote Loop off Pulse Count for LOS Detection cleared Pulse Count for LOS Recovery cleared
XPM2…0	$7B_H$,03_H,00_H	Transmit Pulse Mask
IMR0-4	FF_H	All interrupts are disabled
RTR1-4 TTR1-4	00_H	No time slots selected
MODE	00_H	Signaling controller disabled
RAH1/2 RAL1/2	FD_H,FF_H FF_H,FF_H	Compare register for receive address cleared

T1/J1 Initialization

For a correct start up of the Primary Access Interface a set of parameters specific to the system and hardware environment must be programmed after pin RES goes inactive (low). Both the basic and the operational parameters must be programmed **before** the activation procedure of the PCM line starts. Such procedures are specified in ITU-T recommendations (e.g. fault conditions and consequent actions). Setting optional parameters primarily makes sense when basic operation via the PCM line is guaranteed. **Table 46** gives an overview of the most important parameters in terms of signals and control bits which are to be programmed in one of the above steps. The sequence is recommended but not mandatory. Accordingly, parameters for the basic and operational set up, for example, may be programmed simultaneously. The bit FMR1.PMOD must always be kept high (otherwise E1 mode is selected).

Features like channel loop back, idle channel activation, clear channel activation, extensions for signaling support, alarm simulation, … may be activated later. Transmission of alarms (e.g. AIS, remote alarm) and control of synchronization in connection with consequent actions to remote end and internal system depend on the activation procedure selected.

Table 46 Initialization Parameters (T1/J1)

Basic Set Up	**T1/J1**
Mode Select	FMR1.PMOD = 1
Specification of Line interface and clock generation	LIM0, LIM1, XPM2-0
Line interface coding	FMR0.XC1/0, FMR0.RC1/0
Loss of Signal detection/recovery conditions	PCD, PCR, LIM1, LIM2
System interface mode	FMR1.IMOD
Channel translation mode	FMR1.CTM
Transmit offset counters	XC0.XCO, XC1.XTO
Receive offset counters	RC0.RCO, RC1.RTO
AIS to system interface	FMR2.DAIS/SAIS
Operational Set Up	**T1/J1**
Select framing	FMR4.FM1/0
Framing additions	FMR1.CRC, FMR0.SRAF
Synchronization mode	FMR4.AUTO, FMR4.SSC1/0, FMR2.MCSP, FMR2.SSP
Signaling mode	FMR1.SIGM, FMR5.EIBR, XC0.BRM, MODE, CCR1, CCR3, RAH1/2, RAL1/2

Note: Read access to unused register addresses: value should be ignored.
Write access to unused register addresses: should be avoided, or set to '00'hex.
All control registers (except XFIFO, XS1-12, CMDR, DEC) are of type: Read/Write

Specific T1/J1 Initialization

The following is a suggestion for a basic initialization to meet most of the T1/J1 requirements. Depending on different applications and requirements any other initialization can be used.

Table 47 Line Interface Initialization (T1/J1)

Register	Function
FMR0.XC0/1 FMR0.RC0/1 LIM1.DRS CCB1-3	The FALC®-LH supports requirements for the analog line interface as well as the digital line interface. For the analog line interface the codes AMI (with bit 7stuffing) and B8ZS are supported. For the digital line interface modes (dual or single rail) the FALC®-LH supports AMI (with bit 7 stuffing) and B8ZS.
PCD = 0x0A	LOS detection after 176 consecutive "zeros" (fulfills G.775 spec, Bellcore/AT&T)
PCR = 0x15	LOS recovery after 22 "ones" in the PCD interval. (fulfills G.775, Bellcore/AT&T)
LIM1.RIL2-0 = 0x03	LOS threshold (fulfills G.775, see DC characteristics).
GCR.SCI = 1	Additional Recovery Interrupts. Help to meet alarm activation and deactivation conditions in time.
LIM2.LOS2/1 = 01	Automatic pulse density check on 15 consecutive zeros for LOS recovery condition (Bellcore requirement)

Table 48 Framer Initialization (T1/J1)

Register	Function	
	T1	J1
FMR4.SSC1/0	Selection of framing sync conditions	
FMR4.FM1/0	Select framing format	
FMR2.AXRA = 1	The transmission of RAI via the line interface is done automatically by the FALC®-LH in case of Loss of Frame Alignment (FRS0.LFA = 1). If framing has been reinstalled RAI is automatically reset	

Table 48 Framer Initialization (T1/J1) (cont'd)

Register	Function	
	T1	**J1**
RCO.SJR[1)] = 1 FMR0.SRAF = 0 XSW.XRA = 1		Remote alarm handling via DL-channel according to ITU-T JG.704 using pattern "1111111111111111"
RCO.SJR[1)] = 0	CRC6 calculation without FS/DL bits	
RCO.SJR[1)] = 1		CRC6 calculation including FS/DL bits
FMR4.AUTO = 1	Automatic synchronization in case of definite framing candidate (FRS0.FSRF). In case of multiple framing candidates and CRC6 errors different resynchronization conditions can be programmed via FMR2.MCSP/SSP.	
FMR4.SSC1 = 1 FMR4.SSC0 = 1 FMR2.MCSP = 0 FMR2.SSP = 1		Synchronization and resynchronization conditions, for details see register description.

[1)] Remote alarm handling and CRC6 calculation are commonly selected by bit RCO.SJR

Table 49 Initialization of the HDLC controller (T1/J1)

Register	Function
MODE = 88_H	HDLC Receiver active, No address comparison
CCR1 = 18_H	Enable Signaling via time slot 0...31, Interframe Time Fill with continuous FLAGs
IMR0.RME = 0 IMR0.RPF = 0 IMR1.XPR = 0	Select interrupts for HDLC processor requests
RTR4.0 = 1 TTR4.0 = 1	Select time slot 24 for HDLC data reception and transmission

Table 50 Initialization of the CAS-BR Controller (T1/J1)

Register	Function
FMR5.EIBR = 1 FMR1.SIGM = 1	Enable CAS-BR Mode Send CAS-BR information stored in XS1...12
IMR1.CASE = 0 IMR0.RSC = 0	Enable interrupts which indicate the access to the XS1...12 CAS-BR registers and any data change in RS1...12

Note: After the device initialization a software reset should be executed by setting of bits CMDR.XRES/RRES.

8 Signaling Controller Operating Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus, the receive data flow and the address recognition features can be performed in a very flexible way, to satisfy almost any practical requirements.

There are 4 different operating modes which can be set via the MODE register.

8.1 HDLC Mode

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

Depending on the selected address mode, the FALC®-LH can perform a 1 or 2 byte address recognition (MODE.MDS0).

If a 2-byte address field is selected, the high address byte is compared with the fixed value FEH or FCH (group address) as well as with two individually programmable values in RAH1 and RAH2 registers. According to the ISDN LAPD protocol, bit 1 of the high byte address is interpreted as command/response bit (C/R) and is excluded from the address comparison to RAH1.

Similarly, two compare values can be programmed in special registers (RAL1, RAL2) for the low address byte. A valid address is recognized in case the high and low byte of the address field correspond to one of the compare values. Thus, the FALC®-LH can be called (addressed) with 6 different address combinations. HDLC frames with address fields that do not match any of the address combinations, are ignored by the FALC®-LH.

In case of a 1-byte address, RAL1 and RAL2 are used as compare registers. The HDLC control field, data in the I-field and an additional status byte are temporarily stored in the RFIFO. Additional information can also be read from a special register (RSIS).

As defined by the HDLC protocol, the FALC®-LH performs the zero bit insertion/deletion (bit-stuffing) in the transmit/receive data stream automatically. That means, it is guaranteed that at least a “0” will appear after 5 consecutive “1”s.

8.1.1 Non-Auto-Mode (MODE.MDS2...1 = 01)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

All frames with valid addresses are forwarded directly via the RFIFO to the system memory.

8.1.2 Transparent Mode 1 (MODE.MDS2...0 = 101)

Characteristics: address recognition, FLAG - and CRC generation/check, bit-stuffing

Only the high byte of a 2-byte address field is compared with registers RAH1/2. The whole frame excluding the first address byte is stored in RFIFO.

8.1.3 Transparent Mode 0 (MODE.MDS2...0 = 100)

Characteristics: FLAG and CRC generation/check, bit-stuffing
No address recognition is performed and each frame is stored in the RFIFO.

8.1.4 Receive Data Flow

The following figure gives an overview of the management of the received HDLC frames in the different operating modes.

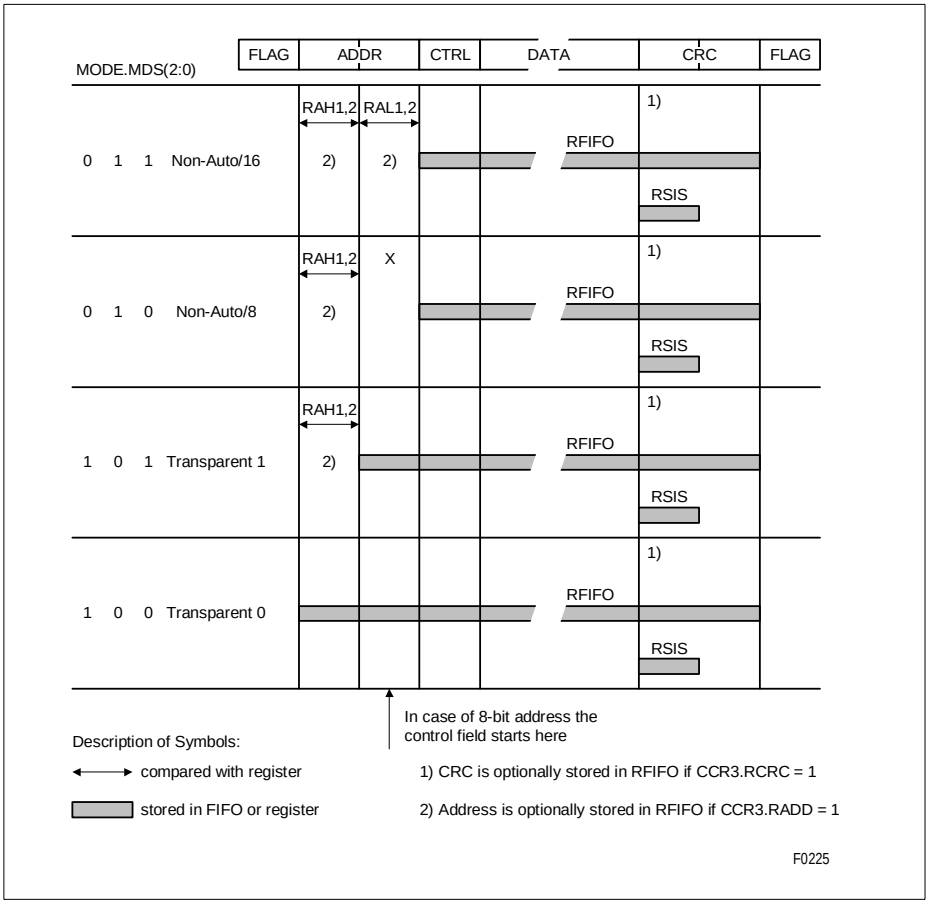


Figure 56 HDLC Receive Data Flow of FALC®-LH

8.1.5 Transmit Data Flow

The frames can be transmitted as shown below.

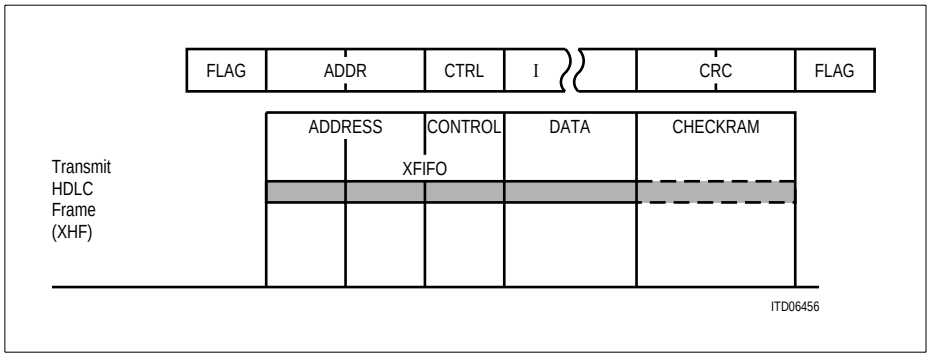


Figure 57 HDLC Transmit Data Flow of FALC®-LH

Transmitting a HDLC frame via register CMDR.XHF, the address, the control fields and the data field have to be entered in the XFIFO.

If CCR3.XCRC is set, the CRC checksum will not be generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame is closed automatically with a closing flag only.

The FALC®-LH does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

8.2 Extended Transparent Mode

Characteristics: fully transparent

In no HDLC mode, fully transparent data transmission/reception without HDLC framing is performed, i.e. without FLAG generation/recognition, CRC generation/check, or bit-stuffing. This feature can be profitably used e.g. for:

- Specific protocol variations
- Transmission of a BOM frame
- Test purposes

Data transmission is always performed out of the XFIFO. In transparent mode, the receive data is shifted into the RFIFO.

8.3 Signaling Controller Functions

8.3.1 Shared Flags

The closing Flag of a previously transmitted frame simultaneously becomes the opening Flag of the following frame if there is one to be transmitted. The Shared Flag feature is enabled by setting bit SFLG in control register CCR1.

8.3.2 Preamble Transmission

If enabled via register CCR3, a programmable 8-bit pattern (defined by register PRE) is transmitted with a selectable number of repetitions after Interframe Timefill transmission is stopped and a new frame is ready to be sent.

Zero bit insertion is disabled during preamble transmission. To guarantee correct function the programmed preamble value should be different to the Receive Address Byte values. Otherwise the preamble could be detected as valid address with shared flags.

In BOM mode the MSB of the preamble should be reset in order to achieve a faster synchronization at the BOM receiver. After the preamble has been sent, the transmitter inserts one sync byte (FF_H) automatically before sending the contents of the transmit FIFO.

8.3.3 Transparent Transmission and Reception

When programmed in the extended transparent mode via the MODE register (MDS2...0 = 111), the FALC®-LH performs fully transparent data reception without HDLC framing, i.e. without

- FLAG deletion
- CRC checking
- Bit-stuffing

In order to enable fully transparent data reception, bit MODE.HRAC has to be set and FF_H has to be written to RAH2.

Received data is always shifted into RFIFO.

Data transmission is always performed out of XFIFO by shifting the contents of XFIFO directly into the outgoing data stream. Transmission is initiated by setting CMDR.XTF. A sync byte FF_H is automatically sent before the first byte of the XFIFO is transmitted.

8.3.4 Cyclic Transmission (fully transparent)

If the extended transparent mode is selected, the FALC®-LH supports the continuous transmission of the contents of the transmit FIFO.

After having written 1 to 32 bytes to XFIFO, the command XREP and XTF via the CMDR register (bit 7 … 0 = '00100100' = 24_H) forces the FALC®-LH to transmit the data stored in XFIFO repeatedly to the remote end.

Note: The cyclic transmission continues until a reset command (CMDR: SRES) is issued or with resetting CMDR.XREP, after which continuous '1's are transmitted. During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

8.3.5 CRC ON/OFF Features

As an option in HDLC mode the internal handling of received and transmitted CRC checksum can be influenced via control bits CCR3.RCRC and CCR3.XCRC.

- Receive Direction

The received CRC checksum is always assumed to be in the 2 last bytes of a frame (CRC-ITU), immediately preceding a closing flag. If CCR3.RCRC is set, the received CRC checksum is written to RFIFO where it precedes the frame status byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If HDLC mode is selected, the limits for 'Valid Frame' check are modified (refer to description of bit RSIS.VFR).

- Transmit Direction

If CCR3.XCRC is set, the CRC checksum is not generated internally. The checksum has to be provided via the transmit FIFO (XFIFO) as the last two bytes. The transmitted frame will only be closed automatically with a closing flag.
The FALC®-LH does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

8.3.6 Receive Address pushed to RFIFO

The address field of received frames can be pushed to the receive FIFO (first one or two bytes of the frame). This function is useful with the extended address recognition. It is enabled by setting control bit CCR2.RADD.

8.3.7 HDLC Data Transmission

In transmit direction 2 × 32 byte FIFO buffers are provided. After checking the XFIFO status by polling bit SIS.XFW or after an interrupt ISR1.XPR (Transmit Pool Ready), up to 32 bytes may be entered by the CPU to the XFIFO.

The transmission of a frame can be started by issuing an XHF command via the command register. If enabled, a specified number of preambles (defined by register PRE) are sent optionally before transmission of the current frame starts. If the transmit command does not include an end of message indication (CMDR.XME), the FALC®-LH will repeatedly request for the next data block by means of an XPR interrupt as soon as

no more than 32 bytes are stored in the XFIFO, i.e. a 32-byte pool is accessible to the CPU.

This process is repeated until the CPU indicates the end of message by XME command, after which frame transmission is finished correctly by appending the CRC and closing flag sequence. Consecutive frames may be share a flag, or may be transmitted as back-to-back frames, if service of XFIFO is fast enough.

In case no more data is available in the XFIFO prior to the arrival of XME, the transmission of the frame is terminated with an abort sequence and the CPU is notified by interrupt ISR1.XDU. The frame may be aborted by software using CMDR.SRES.

The data transmission sequence from the CPU's point of view is outlined in **Figure 58**.

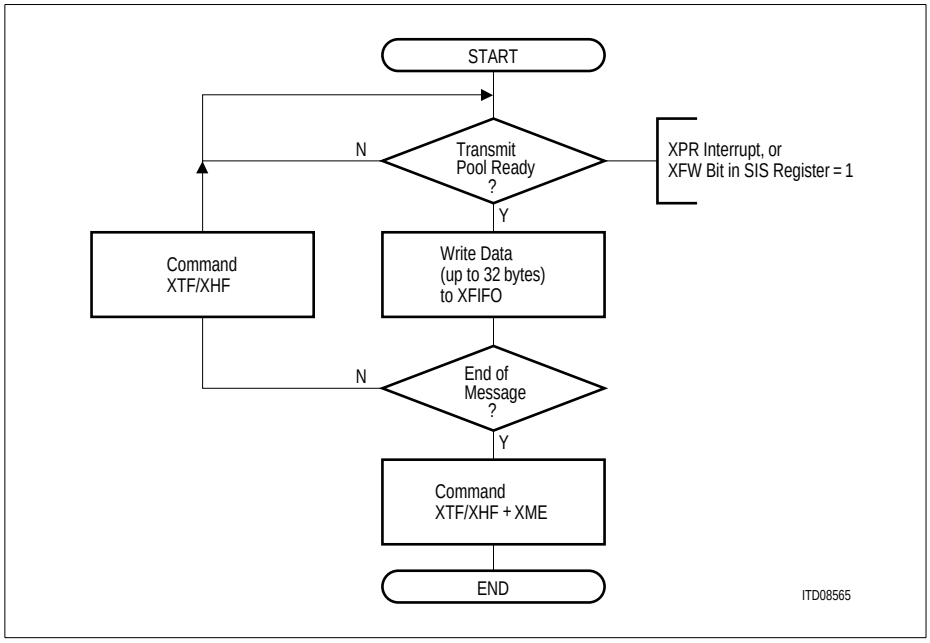


Figure 58 Interrupt Driven Data Transmission (flow diagram)

The activities at both serial and CPU interface during frame transmission (supposed frame length = 70 bytes) shown in **Figure 59**.

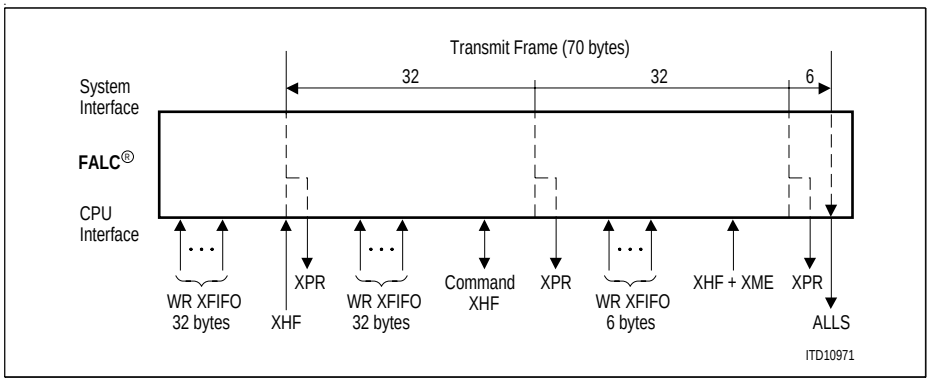


Figure 59 Interrupt Driven Transmission Example

8.3.8 HDLC Data Reception

2×32 byte FIFO buffers are also provided in receive direction. There are different interrupt indications concerned with the reception of data:

- RPF (Receive Pool Full) interrupt, indicating that a 32-byte block of data can be read from RFIFO and the received message is not yet complete.
- RME (Receive Message End) interrupt, indicating that the reception of one message is completed.

The following figure gives an example of a reception sequence, assuming that a “long” frame (66 bytes) followed by two short frames (6 bytes each) are received.

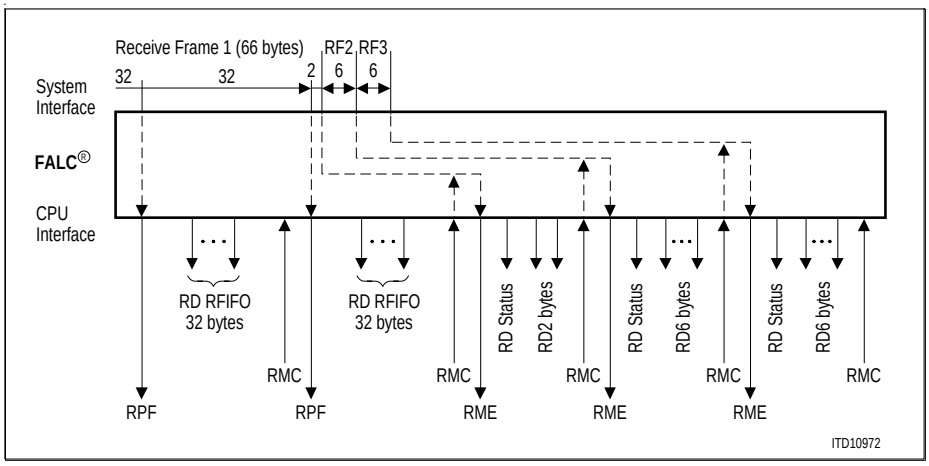


Figure 60 Interrupt Driven Reception Sequence Example

8.3.9 S_a bit Access (E1)

The FALC®-LH supports the S_a bit signaling of time slot 0 of every other frame as follows:

- access via registers RSW/XSW
- access via registers RSA8-4/XSA4-8
- capable of storing the information for a complete multiframe

the access via the 64 byte deep receive/transmit FIFO of the integrated signaling controller. This S_a bit access gives the opportunity to transmit/receive a transparent bit stream as well as HDLC frames where the signaling controller automatically processes the HDLC protocol. Enabling for receive direction is done by resetting of CCR1.EITS=0 and setting of registers XCO.SA4E...8E as required. For transmit direction bits TSWM.TSA4...8 have to be set as required, additionally.
Data written to the XFIFO will subsequently transmit in the S_a bit positions defined by register XC0.SA8E-4E and the corresponding bits of TSWM.TSA8-4. Any combination of S_a bits can be selected. After the data has been sent out completely, “all ones” or Flags (CCR1.ITF) are transmitted. The continuous transmission of a transparent bit stream, which is stored in the XFIFO, can be enabled.
With the setting of bit MODE.HRAC the received S_a bits can be forwarded to the receive FIFO.
The access to and from the FIFOs is supported by ISR0.RME/RPF and ISR1.XPR/ALS.

8.3.10 Bit Oriented Message Mode (T1/J1)

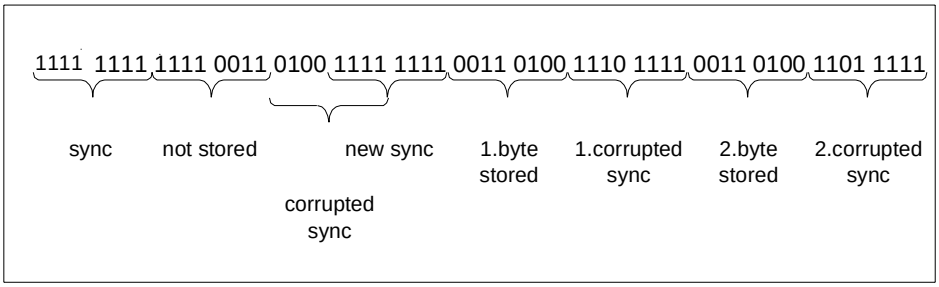
The FALC®-LH supports signaling and maintenance functions for T1/J1 - Primary Rate Interfaces using the Extended Super Frame format. The device supports the DL-channel protocol for ESF format according to T1.403-1989 ANSI or to AT&T TR54016 specification. The HDLC- and Bit Oriented Message (BOM) -Receiver can be switched on/off independently. If the FALC®-LH is used for HDLC formats only, the BOM receiver has to be switched off. If HDLC- and BOM-receiver has been switched on (MODE.HRAC/BRAC), an automatic switching between HDLC and BOM mode is enabled. Storing of received DL bit information in the RFIFO of the signaling controller and transmitting the XFIFO contents in the DL bit positions is enabled by CCR1.EDLX/EITS = 10. After hardware (pin RES = high) or software reset (CMDR.RRES = 1) the FALC®-LH operates in HDLC mode. If eight or more consecutive ones are detected, the BOM mode is entered. Upon detection of a flag in the data stream, the FALC®-LH switches back to HDLC-mode. Operating in BOM-mode, the FALC®-LH may receive an HDLC frame immediately, i.e. without any preceding flags.

In BOM-mode, the following byte format is assumed (the left most bit is received first).
111111110xxxxxx0

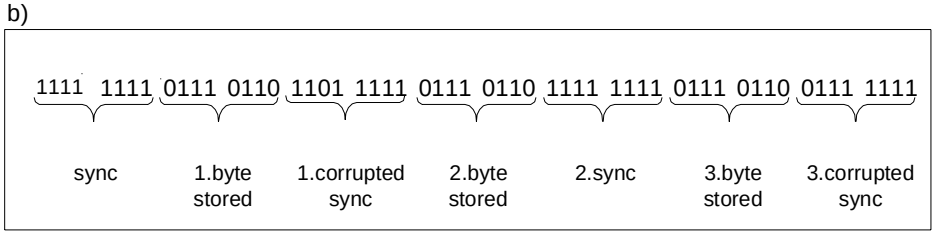
The FALC®-LH uses the FF_H byte for synchronization, the next byte is stored in RFIFO (first bit received: LSB) if it starts and ends with a ‘0’. Bytes starting and ending with a ‘1’ are not stored. If there are no 8 consecutive one’s detected within 32 bits, an interrupt ISR0.ISF is generated. However, byte sampling is not stopped.

Byte sampling in BOM Mode (T1/J1)

a)



b)



Two different BOM reception modes can be programmed (by CCR1.BRM).

10 byte packets: CCR1.BRM = 0
After storing 10 bytes in RFIFO the receive status byte marking a BOM frame (RSIS.HFR) is added as the eleventh byte and an interrupt (ISR0.RME) is generated. The sampling of data bytes continues and interrupts are generated every 10 bytes until an HDLC flag is detected.

Continuous reception: CCR1.BRM = 1
Interrupts are generated every 32 (16, 4, 2) bytes. After detecting an HDLC flag, byte sampling is stopped, the receive status byte is stored in RFIFO and an RME interrupt is generated.

The user may switch between these modes at any time. Byte sampling may be stopped by deactivating the BOM receiver (MODE.BRAC). In this case the receive status byte is added, an interrupt is generated and HDLC-mode is entered. Whether the FALC®-LH operates in HDLC or BOM mode may be checked by reading the Signaling Status Register (SIS.BOM).

8.3.10.1 Data Link Access in ESF/F72 Format (T1/J1)

The FALC®-LH supports the DL-channel protocol using the ESF or F72 (SLC96) format as follows:

- Sampling of DL bits is done on a multiframe basis and stored in the registers RDL1...3. A receive multiframe begin interrupt is provided to read the received data DL bits. The contents of registers XDL1...3 is subsequently sent out on the transmit multiframe basis if it is enabled via FMR1.EDL. A transmit multiframe begin interrupt requests for writing new information to the DL-bit registers.
- If enabled by CCR1.EDLX/EITS=10, the DL-bit information is stored in the Receive FIFO of the signaling controller. The DL-bits stored in the XFIFO are inserted into the outgoing data stream. If CCR1.EDLX is cleared, a HDLC- or a transparent- frame can be sent or received via the RFIFO/XFIFO.

Register Description

Due to the different device function in E1 and T1/J1 mode, several registers and register bits have dedicated functions according to the selected operation mode.

To maintain easy readability this chapter is divided into separate E1 and T1/J1 sections. Please choose the correct description according to your application (E1 or T1/J1).

9 E1 Registers

9.1 E1 Control Register Addresses

Table 51 E1 Control Register Address Arrangement

Address	Register	Type	Comment	Page
00	XFIFO	W	Transmit FIFO	183
01	XFIFO	W	Transmit FIFO	183
02	CMDR	W	Command Register	183
03	MODE	R/W	Mode Register	185
04	RAH1	R/W	Receive Address High 1	185
05	RAH2	R/W	Receive Address High 2	186
06	RAL1	R/W	Receive Address Low 1	186
07	RAL2	R/W	Receive Address Low 2	186
08	IPC	R/W	Interrupt Port Configuration	186
09	CCR1	R/W	Common Configuration Register 1	187
0A	CCR3	R/W	Common Configuration Register 3	189
0B	PRE	R/W	Preamble Register	190
0C	RTR1	R/W	Receive Timeslot Register 1	191
0D	RTR2	R/W	Receive Timeslot Register 2	191
0E	RTR3	R/W	Receive Timeslot Register 3	191
0F	RTR4	R/W	Receive Timeslot Register 4	191
10	TTR1	R/W	Transmit Timeslot Register 1	192
11	TTR2	R/W	Transmit Timeslot Register 2	192
12	TTR3	R/W	Transmit Timeslot Register 3	192
13	TTR4	R/W	Transmit Timeslot Register 4	192
14	IMR0	R/W	Interrupt Mask Register 0	193
15	IMR1	R/W	Interrupt Mask Register 1	193
16	IMR2	R/W	Interrupt Mask Register 2	193
17	IMR3	R/W	Interrupt Mask Register 3	193
18	IMR4	R/W	Interrupt Mask Register 4	193
19	IMR5	R/W	Interrupt Mask Register 5	193
1A	FMR0	R/W	Framer Mode Register 0	193

Table 51 E1 Control Register Address Arrangement (cont'd)

Address	Register	Type	Comment	Page
1B	FMR1	R/W	Framer Mode Register 1	195
1C	FMR2	R/W	Framer Mode Register 2	197
1D	LOOP	R/W	Channel Loop Back Register	199
1E	XSW	R/W	Transmit Service Word	200
1F	XSP	R/W	Transmit Spare Bits	201
20	XC0	R/W	Transmit Control 0	203
21	XC1	R/W	Transmit Control 1	203
22	RC0	R/W	Receive Control 0	204
23	RC1	R/W	Receive Control 1	206
24	XPM0	R/W	Transmit Pulse Mask 0	207
25	XPM1	R/W	Transmit Pulse Mask 1	207
26	XPM2	R/W	Transmit Pulse Mask 2	207
27	TSWM	R/W	Transparent Service Word Mask	208
29	IDLE	R/W	Idle Channel Code	209
2A	XSA4	R/W	Transmit SA4 Bit Register	210
2B	XSA5	R/W	Transmit SA5 Bit Register	210
2C	XSA6	R/W	Transmit SA6 Bit Register	210
2D	XSA7	R/W	Transmit SA7 Bit Register	210
2E	XSA8	R/W	Transmit SA8 Bit Register	210
2F	FMR3	R/W	Framer Mode Register 3	210
30	ICB1	R/W	Idle Channel Register 1	212
31	ICB2	R/W	Idle Channel Register 2	212
32	ICB3	R/W	Idle Channel Register 3	212
33	ICB4	R/W	Idle Channel Register 4	212
34	LIM0	R/W	Line Interface Mode 0	213
35	LIM1	R/W	Line Interface Mode 1	214
36	PCD	R/W	Pulse Count Detection	216
37	PCR	R/W	Pulse Count Recovery	216
38	LIM2	R/W	Line Interface Mode 2	217
39	LCR1	R/W	Loop Code Register 1	218

Table 51 E1 Control Register Address Arrangement (cont'd)

Address	Register	Type	Comment	Page
3A	LCR2	R/W	Loop Code Register 2	220
3B	LCR3	R/W	Loop Code Register 3	220
3C	SIC1	R/W	System Interface Control 1	221
3D	SIC2	R/W	System Interface Control 2	223
3E	LIM3	R/W	Line Interface Mode 3	224
40	SIC3	R/W	System Interface Control 3	224
60	DEC	W	Disable Error Counter	225
70	XS1	W	Transmit CAS Register 1	226
71	XS2	W	Transmit CAS Register 2	226
72	XS3	W	Transmit CAS Register 3	226
73	XS4	W	Transmit CAS Register 4	226
74	XS5	W	Transmit CAS Register 5	226
75	XS6	W	Transmit CAS Register 6	226
76	XS7	W	Transmit CAS Register 7	226
77	XS8	W	Transmit CAS Register 8	226
78	XS9	W	Transmit CAS Register 9	226
79	XS10	W	Transmit CAS Register 10	226
7A	XS11	W	Transmit CAS Register 11	226
7B	XS12	W	Transmit CAS Register 12	226
7C	XS13	W	Transmit CAS Register 13	226
7D	XS14	W	Transmit CAS Register 14	226
7E	XS15	W	Transmit CAS Register 15	226
7F	XS16	W	Transmit CAS Register 16	226

After 'RESET' all control registers except the XFIFO and XS1...16 are initialized to defined values.

Unused bits have to be cleared (set to logical '0').

9.2 Detailed Description of E1 Control Registers

Transmit FIFO (Write)

	7		0	
XFIFO	XF7		XF0	(00/01)

Writing data to XFIFO can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first.

Up to 32 bytes/16 words of transmit data can be written to the XFIFO following a XPR (or ALLS) interrupt.

Command Register (Write)

Value after RESET: 00_H

	7							0	
CMDR	RMC	RRES	XREP	XRES	XHF	XTF	XME	SRES	(02)

RMC… **Receive Message Complete**

Confirmation from CPU to FALC®-LH that the current frame or data block has been fetched following a RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

RRES… **Receiver Reset**

The receive line interface except the clock and data recovery unit (DPLL), the DCR-R circuitry, the receive framer, the one second timer and the receive signaling controller are reset. However the contents of the control registers is not deleted. RRES has to be given every time after a configuration change.

XREP… **Transmission Repeat**

If XREP is set together with XTF (write 24_H to CMDR), the FALC®-LH repeatedly transmits the contents of the XFIFO (1 … 32 bytes) without HDLC framing fully transparently, i.e. without FLAG,CRC.

The cyclic transmission is stopped with a SRES command or by resetting XREP.

Note: During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

XRES… **Transmitter Reset**

The transmit framer and transmit line interface including DCO-X are reset. However, the contents of the control registers is not deleted. XRES has to be given every time after a configuration change.

XHF… **Transmit HDLC Frame**

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.

XTF… **Transmit Transparent Frame**

Initiates the transmission of a transparent frame without HDLC framing.

XME… **Transmit Message End**

Indicates that the data block written last to the transmit FIFO completes the current frame. The FALC®-LH can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

SRES… **Signaling Transmitter Reset**

The transmitter of the signaling controller is reset. XFIFO is cleared of any data and an abort sequence (seven 1's) followed by interframe time fill is transmitted. In response to SRES a XPR interrupt is generated.

This command can be used by the CPU to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDR register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the CPU operates with a very high clock rate in comparison with the FALC®-LH's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.

Note: Bits are cleared automatically except of XREP

Mode Register (Read/Write)

Value after RESET: 00_H

	7							0	
MODE	MDS2	MDS1	MDS0		HRAC				(03)

MDS2...0… **Mode Select**

The operating mode of the HDLC controller is selected.

000… Reserved

001… Reserved

010… 1 byte address comparison mode (RAL1,2)

011… 2 byte address comparison mode (RAH1,2 and RAL1,2)

100… No address comparison

101… 1 byte address comparison mode (RAH1,2)

110… Reserved

111… No HDLC framing mode

HRAC… **HDLC Receiver Active**

Switches the HDLC receiver to operational or inoperational state.

0… Receiver inactive

1… Receiver active

Receive Address Byte High Register 1 (Read/Write)

Value after RESET: FD_H

	7							0	
RAH1							0		(04)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individually programmable values in RAH1 and RAH2.

RAH1… **Value of the First Individual High Address Byte**

Bit 1 (C/R-bit) is excluded from address comparison.

Receive Address Byte High Register 2 (Read/Write)
Value after RESET: FF_H

	7						0	
RAH2								(05)

RAH2… **Value of Second Individual High Address Byte**

Receive Address Byte Low Register 1 (Read/Write)
Value after RESET: FF_H

	7						0	
RAL1								(06)

RAL1… **Value of First Individual Low Address Byte**

Receive Address Byte Low Register 2 (Read/Write)
Value after RESET: FF_H

	7						0	
RAL2								(07)

RAL2... **Value of the second individually programmable low address byte.**

Interrupt Port Configuration (Read/Write)

Value after RESET: 00_H

	7							0	
IPC	VIS					SCI	IC1	IC0	(08)

Note: Unused bits have to be cleared.

VIS… **Masked Interrupts Visible**

0… Masked interrupt status bits are not visible
1… Masked interrupt status bits are visible

SCI… **Status Change Interrupt**

0… Interrupts ISR2.LOS, ISR2.AIS, ISR3.API and ISR3.LMFA16 are generated only on the rising edge of the corresponding status flag.
1… Interrupts ISR2.LOS, ISR2.AIS, ISR3.API and ISR3.LMFA16 are generated on the rising and falling edge of the corresponding status flag.

IC1...0… **Interrupt Port Configuration**

These bits define the function of the interrupt output stage (pin INT):

IC1	IC0	Function
X	0	Open drain output[1)]
0	1	Push/pull output, active low
1	1	Push/pull output, active high

[1)] an external pullup resistor is required at pin INT

Common Configuration Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
CCR1	SFLG	XTS16RA	CASM	EITS	ITF		RFT1	RFT0	(09)

SFLG… **Enable Shared Flags**

If this bit is set, the closing flag of a preceding HDLC frame simultaneously is used as the opening flag of the following frame.

0… Shared flag function disabled

1… Shared flag function enabled

XTS16RA… **Transmit Time Slot 16 Remote Alarm**

0… Standard operation

1… Sends remote alarm in time slot 16 towards remote end by setting the Y-bit in CAS multiframe alignment word. This bit is logically ored with the contents of register XS1.2

CASM… **CAS Synchronization Mode**

Determines the synchronization mode of the channel associated signaling multiframe alignment.

0… Synchronization is done in accordance to ITU-T G. 732

1… Synchronization is established when two consecutively correct multiframe alignment pattern are found.

EITS… **Enable Internal Time Slot 0-31 Signaling**

0… Internal signaling in time slots 0-31 defined via registers RTR1...4 or TTR1...4 is disabled.

1… Internal signaling in time slots 0-31 defined via registers RTR1...4 or TTR1...4 is enabled.

ITF… **Interframe Time Fill**

Determines the idle (= no data to send) state of the transmit data coming from the signaling controller.

0… Continuous logical ‘1’ is output

1… Continuous flag sequences are output (‘01111110’ bit patterns)

RFT1...0... **RFIFO Threshold Level**

The size of the accessible part of RFIFO can be determined by programming these bits. The number of valid bytes after a RPF interrupt is given in the following table:

RFT1	RFT0	Size of Accessible Part of RFIFO
0	0	32 bytes (RESET value)
0	1	16 bytes
1	0	4 bytes
1	1	2 bytes

The value of RFT1, 0 can be changed dynamically.

– If reception is not running or

– after the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer).

Note: It is seen that changing the value of RFT1, 0 is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH after a RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by a RMC command (see table below):

RFT1	RFT0	Bit Positions in RBCL Reset by a CMDR.RMC Command
0	0	RBC4 …. 0
0	1	RBC3 … 0
1	0	RBC1,0
1	1	RBC0

Common Configuration Register 3 (Read/Write)

Value after RESET: 00_H

	7							0	
CCR3	PRE1	PRE0	EPT	RADD		RCRC	XCRC		(0A)

Note: Unused bits have to be cleared.

PRE1...0… **Number of Preamble Repetitions**

If preamble transmission is enabled, the preamble defined by register PRE is transmitted:

00... 1 time

01... 2 times

10... 4 times

11... 8 times

EPT… **Enable Preamble Transmission**

This bit enables transmission of preamble. The preamble is started after interframe timefill transmission has been stopped and a new frame is to be transmitted. The preamble consists of an 8-bit pattern repeated a number of times. The pattern is defined by register PRE, the number of repetitions is selected by bits PRE0 and PRE1.

Note: The 'Shared Flag' feature is not influenced by preamble transmission. Zero bit insertion is disabled during preamble transmission.

RADD… **Receive Address Pushed to RFIFO**

If this bit is set, the received HDLC address information (1 or 2 bytes, depending on the address mode selected via MODE.MDS0) is pushed to RFIFO. See **Chapter 8.1** on page **169** for detailed description.

RCRC… **Receive CRC ON/OFF**

If this bit is set, the received CRC checksum is written to RFIFO (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO by the status information byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If non-auto mode is selected, the limits for “Valid Frame” check are modified (**refer to RSIS.VFR** and to **Chapter 8.1** on page **169**).

XCRC… **Transmit CRC ON/OFF**

If this bit is set, the CRC checksum is not generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO). The transmitted frame is closed automatically with a closing flag.

Note: The FALC®-LH does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Preamble Register (Read/Write)
Value after RESET: 00_H

	7						0	
PRE								(0B)

PRE7...0… **Preamble Register**

This register defines the pattern which is sent during preamble transmission (refer to CCR3). LSB is sent first.

Note: Zero bit insertion is disabled during preamble transmission.

Receive Timeslot Register 1...4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(0C)
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(0D)
RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(0E)
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(0F)

TS0…31… **Timeslot Register**

These bits define the received time slots on the system highway port RDO to be extracted to RFIFO and marked. Additionally these registers control the RSIGM marker which can be forced high during the respective time slots independently of bit CCR1.EITS.
A one in the RTR1...4 bits samples the corresponding time slots and send their data to the RFIFO of the signaling controller if bit CCR1.EITS is set.

Assignments:
TS0 → time slot 0
...
TS31→ time slot 31

0 …The corresponding time slot is not extracted and stored into the RFIFO.

1…The contents of the selected time slot is stored in the RFIFO. This function becomes active only if bit CCR1.EITS is set.
The corresponding time slot is forced high on marker pin RSIGM.

Transmit Timeslot Register 1...4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(10)
TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(11)
TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(12)
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(13)

TS0…31… **Transmit Timeslot Register**

These bits define the transmit time slots on the system highway to be inserted. Additionally these registers control the XSIGM marker which can be forced high during the respective time slots independently of bit CCR1.EITS.
A one in the TTR1...4 bits inserts the corresponding time slot sourced by the XFIFO in the data received on pin XDI, if bit CCR1.EITS is set. If SIC3.TTRF is set and CCR1.EITS is cleared insertion of data received on port XSIG is controlled by this registers.

Assignments:
TS0 → time slot 0

...
TS31 → time slot 31

0 …The selected time slot is not inserted into the outgoing data stream.

1…The contents of the selected time slot is inserted into the outgoing data stream from XFIFO. This function becomes active only if bit CCR1.EITS is set.
The corresponding time slot is forced high on marker pin XSIGM.

Interrupt Mask Register 0...5 (Read/Write)

Value after RESET: FF_H, FF_H, FF_H, FF_H, FF_H

	7							0	
IMR0	RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF	(14)
IMR1	LLBSC	RDO	ALLS	XDU	XMB		XLSC	XPR	(15)
IMR2	FAR	LFA	MFAR	T400MS	AIS	LOS	RAR	RA	(16)
IMR3	ES	SEC	LMFA16	AIS16	RA16	API	RSN	RSP	(17)
IMR4	LFA	FER	CER	AIS	LOS	CVE	SLIP	EBE	(18)
IMR5	XSP	XSN							(19)

IMR0...IMR5... **Interrupt Mask Register**

Each interrupt source can generate an interrupt signal on port INT (characteristics of the output stage are defined via register IPC). A ‘1’ in a bit position of IMR0...5 sets the mask active for the interrupt status in ISR0...3 and ISR5. Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they are

– not displayed in the Interrupt Status Register if bit IPC.VIS is cleared
– displayed in the Interrupt Status Register if bit IPC.VIS is set.

*Note: After RESET, all interrupts are **dis**abled.*

Framer Mode Register 0 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR0	XC1	XC0	RC1	RC0	EXTD	ALM	FRS	SIM	(1A)

XC1... 0… **Transmit Code**

Serial code for the transmitter is independent to the receiver.

00... NRZ (optical interface)

01... CMI (1T2B + HDB3), (see FMR3 on **page 210**)

10... AMI (ternary or digital dual rail interface)

11... HDB3 Code (ternary or digital dual rail interface)

RC1...0… **Receive Code**

Serial code for the receiver is independent to the transmitter.

00... NRZ (optical interface)

01... CMI (1T2B+HDB3), (optical interface)

10... AMI (ternary or digital dual rail interface)

11... HDB3 Code (ternary or digital dual rail interface)

EXTD… **Extended HDB3 Error Detection**

Selects error detection mode.

0… Only double violations are detected.

1… Extended code violation detection: 0000 strings are detected additionally. Thereafter, next increment of Code Violation Counter CVC is done after receiving additional four zeros.

ALM… **Alarm Mode**

Selects the AIS alarm detection mode.

0… The AIS alarm is detected according to ETS300233.
Detection: An AIS alarm is detected if the incoming data stream contains less than 3 zeros within a period of 512 bits and a Loss of Frame Alignment is indicated.
Recovery: The alarm is cleared if 3 or more zeros within 512 bits are detected or the FAS word is found.

1… The AIS alarm is detected according to ITU-T G.775
Detection: An AIS alarm is detected if the incoming data stream contains for two consecutive doubleframe periods (1024 bits) less than 3 zeros for each doubleframe period (512 bits).
Recovery: The alarm is cleared if within two consecutive doubleframe periods 3 or more zeros for each period of 512 bits are detected.

FRS… **Force Resynchronization**

A transition from low to high initiates a resynchronization procedure of the pulse frame and the CRC-multiframe (if enabled via bit FMR2.RFS1) starting directly after the old framing candidate.

Note:FRS is not reset automatically.

SIM… **Alarm Simulation**

0… Normal operation.

1… Initiates internal error simulation of AIS, loss of signal, loss of synchronization, remote alarm, slip, framing errors, CRC errors, and code violations. The error counters FEC, CVC, CEC1 are incremented.

Framer Mode Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR1	MFCS	AFR	ENSA	PMOD	XFS	ECM	IMOD	XAIS	(1B)

MFCS… **Multiframe Force Resynchronization**

Only valid if CRC multiframe format is selected (FMR2.RFS1/0=10).

A transition from low to high initiates the resynchronization procedure for CRC-multiframe alignment without influencing doubleframe synchronous state. In case, “Automatic Force Resynchronization” (FMR1.AFR) is enabled and multiframe alignment can not be regained, a new search of doubleframe (and CRC multiframe) is automatically initiated.

Note:MFCS is not reset automatically.

AFR… **Automatic Force Resynchronization**

Only valid if CRC multiframe format is selected (FMR2.RFS1/0=10).

If this bit is set, a search of doubleframe alignment is automatically initiated if two multiframe patterns with a distance of n × 2 ms have not been found within a time interval of 8 ms after doubleframe alignment has been regained.

ENSA… **Enable S_a-Bit Access via Register XSA4...8**

0… Normal operation. The S_a-bit information is taken from bits XSW.XY0…4 and written to bits RSW.RY0…4.

1… S_a-bit register access. The S_a-bit information is taken from the registers XSA4...8. In addition, the received information is written to registers RSA4...8. Transmitting of the contents of registers XSA4...8 is disabled if one of time slot 0 transparent modes is enabled (XSP.TT0 or TSWM.SA4...8).

PMOD… **PCM Mode**

For E1 application this bit must be set low. Switching from E1 to T1 or vice versa the device needs up to 10 µs to settle up to the internal clocking.

0… PCM 30 or E1 mode.

1… PCM 24 or T1 mode.

XFS… **Transmit Framing Select**

Selection of the transmit framing format could be done independent of the receive framing format.

0… Doubleframe format enabled.

1… CRC4-multiframe format enabled.

ECM… **Error Counter Mode**

The function of the error counters is determined by this bit.

0… Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8 bit access the low byte of the error counter should always be read before the high byte. The error counters are reset with the rising edge of the corresponding bits in the DEC register.

1… Every second the error counters are latched and then automatically be reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided (do not access an error counter within 2 µs before or after the one-second interrupt occurs).

IMOD… **Select System Interface Mode**

0... 4.096 Mbit/s

1... 2.048 Mbit/s

XAIS… **Transmit AIS Towards Remote End**

Sends AIS via ports XL1, XL2, XOID towards the remote end. The outgoing data stream which could be looped back via the Local Loop to the system interface is not affected.

Framer Mode Register 2 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR2	RFS1	RFS0	RTM	DAIS	SAIS	PLB	AXRA	ALMF	(1C)

RFS1... 0... **Receive Framing Select**

00… Doubleframe format

01… Doubleframe format

10… CRC4 Multiframe format

11… CRC4 Multiframe format with modified CRC4 Multiframe alignment algorithm (Interworking according to ITU-T G.706 Annex B). Setting of FMR3.EXTIW changes the reaction after the 400 ms timeout.

RTM… **Receive Transparent Mode**

Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to update the time slot assignment to a new frame position in case of re-synchronization of the receiver. This function can be used in conjunction with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.
This bit should be enabled in case of unframed data reception mode. After resetting RTM to 0, the elastic buffer is adjusted after the next resynchronization.

DAIS… **Disable AIS to System Interface**

0… AIS is automatically inserted into the data stream to RDO if FALC®-LH is in asynchronous state.

1… Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.

SAIS… **Send AIS Towards System Interface**

Sends AIS via output RDO towards system interface. This function is not influenced by bit FMR2.DAIS.

PLB… **Payload Loopback**

0… Normal operation. Payload loop is disabled.

1... The payload loopback loops the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received on port XDI, XSIG, SYPX and XMFS is

ignored. With XSP.TT0=1 timeslot 0 is also looped. If XSP.TT0=0 timeslot 0 is generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit. It is recommended to write the actual value of XC1 into this register once again, because a write access to register XC1 sets the read/write pointer of the transmit elastic buffer into its optimal position to ensure a maximum wander compensation (the write operation forces a slip).

AXRA… **Automatic Transmit Remote Alarm**

0… Normal operation

1… The Remote Alarm bit is set automatically in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit is reset. Additionally in multiframe format FMR2.RFS1=1 and FMR3.EXTIW =1 and the 400 ms timeout has elapsed, the remote alarm bit is active in the outgoing data stream. In multiframe synchronous state the outgoing remote alarm bit is cleared.

ALMF… **Automatic Loss of Multiframe**

0… Normal operation

1… The receiver searches a new basic framing and multiframing if more than 914 CRC errors have been detected in a time interval of one second. The internal 914 CRC error counter is reset if the multiframe synchronization is found. Incrementing the counter is only enabled in the multiframe synchronous state.

Channel Loop Back Register (Read/Write)

Value after RESET: 00_H

	7							0	
LOOP	SPN	SFM	ECLB	CLA4	CLA3	CLA2	CLA1	CLA0	(1D)

SPN… **Select Additional Optical Pin Functions**

Together with bit LIM3.ESY the functionality of pin 80 is defined:

Programming of LOOP.SPN and LIM3.ESY and the corresponding pin function is shown below.

SPN/ESY:

00… function of pin 80 XSIG: If SIC3.TTRF = 1, transmit data from the system interface. Internal multiplexing with the XDI data stream is controlled by XSIGM. No input function defined for SIC3.TTRF = 0.

01… function of pin 80 SYNC2: external synchronization input for the DCO-X circuitry

10… function of pin 80 ROID: Receive Optical Interface Data (Input) and Pin 68: XMFB/**XOID** Transmit Optical Interface Data (Output). At the same time data received on pin 2 are ignored, data on pin XOID (pin 15) are undefined. Transmit data is clocked off with the positive transition of XCLK. After Reset the transmit multiframe begin marker is output on pin 68.

11… function of pin 80 XSIG: The signaling information from the transmit system interface is received on pin XSIG. Bit FMR5.EIBR should be cleared to disable internal signaling access from registers XS1...16. The signaling information from the line interface is transmitted on pin RSIG.

SFM… **Single Frame Mode**

Setting this bit reduces the receive speech memory from two to one frame length. In this case, clocks SCLKR and RCLK have to be phase locked to avoid slip conditions. However, slip detection still works but without any influence on data transmission.

Note:This mode is not recommended, but possible to be compatible with FALC®54. Newer FALC devices (e.g. FALC®56, QuadFALC™) don't support this any more.

ECLB… **Enable Channel Loop Back**

0... Disables the channel loop back.

1... Enables the channel loop back selected by this register.

CLA4...0… **Channel Address For Loop Back**

CLA = 0…31 selects the channel.

During looped back the contents of the assigned outgoing channel on ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed at register IDLE.

Transmit Service Word Pulseframe (Read/Write)

Value after RESET: 00_H

	7							0	
XSW	XSIS	XTM	XRA	XY0	XY1	XY2	XY3	XY4	(1E)

XSIS… **Spare Bit For International Use**

First bit of the service word. Only significant in doubleframe format. If not used, this bit should be fixed to ‘1’. If one of the time slot 0 transparent modes is enabled (bit XSP.TT0, or TSWM.TSIS), bit XSW.XSIS is ignored.

XTM… **Transmit Transparent Mode**

0…Ports $\overline{\text{SYPX}}$/XMFS define the frame/multiframe begin on the transmit system highway. The transmitter is usually synchronized on this externally sourced frame boundary and generates the FAS bits according to this framing. Any change of the transmit time slot assignment or a transmit slip subsequently produces a change of the FAS bit positions.

1… Disconnects the control of the transmit system interface from the transmitter. The transmitter is now in a free running mode without any possibility to update the multiframe position. The framing (FAS bits) generated by the transmitter are not disturbed (in case of changing the transmit time slot assignment or transmit slip) by the transmit system highway unless register XC1 is written. Useful in loop-timed applications. For correct operation the transmit elastic buffer (2 frames, SIC1.XBS1/0= 10) has to be enabled.

XRA… **Transmit Remote Alarm**

0… Normal operation.

1… Sends remote alarm towards remote end by setting bit 3 of the service word. If time slot 0 transparent mode is enabled via bit XSP.TT0 or TSWM.TRA bit is set, bit XSW.XRA is ignored.

XY0…4… **Spare Bits For National Use (Y-Bits, S_n-Bits, S_a-Bits)**

These bits are inserted in the service word of every other pulseframe if S_a-bit register access is disabled (FMR1.ENSA = 0). If not used, they should be fixed to ‘1’.

If one of the time slot 0 transparent modes is enabled (bit XSP.TT0 or TSWM.TSA4...8), bits XSW.XY0…4 is ignored.

Transmit Spare Bits (Read/Write)

Value after RESET: 00_H

	7							0	
XSP	XAP	CASEN	TT0	EBP	AXS	XSIF	XS13	XS15	(1F)

XAP… **Transmit Auxiliary Pattern towards Remote End**

0… Normal operation.

1… A one in this bit position causes the transmitter to send an alternating pattern 101010... towards the remote end. FMR1.XAIS = 1 overwrites the alternating pattern by a continuous one bit stream.

CASEN… **Channel Associated Signaling Enable**

0… Normal operation.

1… A one in this bit position causes the transmitter to send the CAS information stored in the XS1...16 registers in the corresponding time slots.

TT0… **Time Slot 0 Transparent Mode**

0… Normal operation.

1… All information for time slot 0 on port XDI is inserted in the outgoing pulseframe. All internal information of the FALC®-LH (framing, CRC, S_a/S_i bit signaling, remote alarm) is ignored. This function is mainly useful for system test applications (test

loops). Priority sequence of transparent modes: XSP.TT0 > TSWM.

EBP… **E-Bit Polarity**

0… In the basic framing or multiframe asynchronous state the E-bit is cleared.

1… In the basic framing or multiframe asynchronous state the E-bit is set.

If automatic transmission of sub-multiframe status is enabled by setting bit XSP.AXS and the receiver has been lost multiframe synchronization, the E bit with the programmed polarity is inserted automatically in S_i-bit position of every outgoing CRC multiframe (under the condition that time slot 0 transparent mode and transparent S_i bit in service word are both disabled).

AXS… **Automatic Transmission of Submultiframe Status**

Only applicable to CRC multiframe.

0… Normal operation.

1… Information of submultiframe status bits RSP.SI1 and RSP.SI2 is inserted automatically in S_i-bit positions of the outgoing CRC multiframe (RSP.SI1 $\rightarrow$ S_i-bit of frame 13; RSP.SI2 $\rightarrow$ S_i-bit of frame 15). Contents of XSP.XS13 and XSP.XS15 is ignored. If one of the time slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.AXS has no function.

XSIF… **Transmit Spare Bit For International Use (FAS Word)**

First bit in the FAS word. Only significant in doubleframe format. If not used, this bit should be fixed to ‘1’. If one of the time slot 0 transparent modes is enabled (bits XSP.TT0, or TSWM.TSIF), bit XSP.XSIF is ignored.

XS13… **Transmit Spare Bit (Frame 13, CRC-Multiframe)**

First bit in the service word of frame 13 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to ‘1’. The information of XSP.XS13 is shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe.

If automatic transmission of submultiframe status is enabled via bit XSP.AXS, or, if one of the time slot 0 transparent modes XSP.TT0 or TSWM.TSIS is enabled, bit XSP.XS13 is ignored.

XS15… **Transmit Spare Bit (Frame 15, CRC-Multiframe)**

First bit in the service word of frame 15 for international use. Only significant in CRC-multiframe format. If not used, this bit should be fixed to '1'. The information of XSP.XS15 is shifted into internal transmission buffer with beginning of the next following transmitted CRC multiframe.

If automatic transmission of submultiframe status is enabled via bit XSP.AXS, or, if one of the time slot 0 transparent modes XSP.TT0 or TSWM.TSIF is enabled, bit XSP.XS15 is ignored.

Transmit Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
XC0	SA8E	SA7E	SA6E	SA5E	SA4E	XCO2	XCO1	XCO0	(20)

SA8E...4E **SA Bit Signaling Enable**

0… Standard operation.

1… By setting this bit it is possible to send/receive a LAPD protocol in any combination of the SA8...SA4 bit positions in the outgoing/incoming data stream. The on chip signaling controller has to be configured in the HDLC/LAPD mode. In transmit direction together with these bits the TSWM.TSA8-4 bits must be set to enable transmission to the remote end transparently through the FALC®-LH.

XCO2...0… **Transmit Clock Slot Offset**

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse on port $\overline{\text{SYPX}}$ is active. Refer to register XC1. XCO0 must be cleared if SIC1.SXSC is set.

Transmit Control 1 (Read/Write)

Value after RESET: 00_H

	7							0	
XC1	XCOS		XTO5	XTO4	XTO3	XTO2	XTO1	XTO0	(21)

A write access to this address resets the transmit elastic buffer to its basic starting position. Therefore, updating the value should only be done when the FALC®-LH is

initialized or when the buffer should be centered. As a consequence a transmit slip occurs.

XCOS... **Transmit Clock Offset Shift**

Only valid if SIC1.SXSC = 0.

0... The delay T between the beginning of time slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is an even number in the range of 0 to 1022 SCLKX cycles.

1... The delay T is an odd number in the range of 1 to 1023 SCLKX cycles.

XTO5...0... **Transmit Time Slot Offset**

Initial value loaded into the transmit time slot counter at the trigger edge of SCLKX when the synchronous pulse on port $\overline{\text{SYPX}}$ is active.

Receive Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
RC0	RCOS	SICS	CRCI	XCRCI	RDIS	RCO2	RCO1	RCO0	(22)

RCOS... **Receive Clock Offset Shift**

0... The delay T between the beginning of time slot 0 and the initial edge of SCLKR (after $\overline{\text{SYPR}}$ goes active) is an even number in the range of 0 to 1022 SCLKR cycles.

1... The delay T is an odd number in the range of 1 to 1023 SCLKR cycles.

SICS... **System Interface Channel Select**

Only applicable for PCM highway configuration 8 MHz and 4 Mbit/s

0... Received data is output on port RDO in the first channel phase. Data line RDO is tristated in the second channel phase. Data on pin XDI is sampled in the first channel phase only. Data on XDI in the second channel phase is ignored.

1... Received data is output on port RDO in the second channel phase. Data line RDO is tristated in the first channel phase. Data on pin XDI is sampled in the second channel phase only. Data on XDI in the first channel phase is ignored.

CRCI… **Automatic CRC4 Bit Inversion**

If set, all CRC bits of one outgoing submultiframe are inverted in case a CRC error is flagged for the previous received submultiframe. This function is logically ORed with RC0.XCRCI.

XCRCI… **Transmit CRC4 Bit Inversion**

If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ORed with RC0.CRCI.

RDIS… **Receive Data Input Sense**

Only applicable for dual rail mode (LIM1.DRS = 1).

0… Inputs: RDIP, RDIN active low, input ROID is active high

1… Inputs: RDIP, RDIN active high, input ROID is active low

RCO2...0… **Receive Clock Slot Offset/Receive Frame Marker Offset**

Depending on bit SIC2.SRFSO this bit enables different functions:

Receive Clock-Slot Offset (SIC2.SRFSO = 0)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse on port $\overline{\text{SYPR}}$ is active.

Receive Frame Marker Offset (SIC2.SRFSO = 1)

Offset programming of the receive frame marker which is output on port $\overline{\text{SYPR}}$. The receive frame marker could be activated during any bit position of the current frame.

Calculation of the value X of the “Receive Counter Offset” register RC1/0 depends on the bit position BP which should be marked and SCLKR:
X = (2 + 2 BP) mod 512, for SCLKR = 2.048 MHz.

Receive Control 1 (Read/Write)

Value after RESET: 00_H

	7							0	
RC1	SWD	ASY4	RTO5	RTO4	RTO3	RTO2	RTO1	RTO0	(23)

SWD … **Service Word Condition Disable**

0… Standard operation. Three or four consecutive incorrect service words (depending on bit RC1.ASY4) causes loss of synchronization.

1… Errors in service words have no influence when in synchronous state. However, they are used for the resynchronization procedure.

ASY4 … **Select Loss of Sync Condition**

0… Standard operation. Three consecutive incorrect FAS words or three consecutive incorrect service words causes loss of synchronization.

1… Four consecutive incorrect FAS words or four consecutive incorrect service words causes loss of synchronization. The service word condition may be disabled via bit RC1.SWD.

RTO5...0… **Receive Time Slot Offset/Receive Frame Marker Offset**

Depending on bit SIC2.SRFSO this bit enables different functions:

Receive Time Slot Offset (SIC2.SRFSO = 0)
Initial value which is loaded into the receive time slot counter at the trigger edge of SCLKR when the synchronous pulse on port $\overline{\text{SYPR}}$ is active.

Receive Frame Marker Offset (SIC2.SRFSO = 1)

Offset programming of the receive frame marker which is output on port $\overline{\text{SYPR}}$. The receive frame marker could be activated during any bit position of the current frame.

Calculation of the value X of the “Receive Counter Offset” register RC1/0 depends on the bit position BP which should be marked and SCLKR:
X = (2 + 2 BP) mod 512, for SCLKR = 2.048 MHz.

Transmit Pulse-Mask 0...2 (Read/Write)

Value after RESET: $9C_H$, 03_H, 00_H

	7							0	
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00	(24)
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13	(25)
XPM2	XLHP	XLT	DAXLT		XP34	XP33	XP32	XP31	(26)

The transmit pulse shape which is defined in ITU-T G.703 is output on pins XL1 and XL2. The level of the pulse shape can be programmed via registers XPM2...0 to create a custom waveform. In order to get an optimized pulse shape for the external transformers each pulse shape is internally divided into four sub pulse shapes. In each sub pulse shape a programmed 5 bit value defines the level of the analog voltage on pins XL1/2. Together four 5 bit values have to be programmed to form one complete transmit pulse shape. The four 5 bit values are sent in the following sequence:

XP04-00: First pulse shape level
XP14-10: Second pulse shape level
XP24-20: Third pulse shape level
XP34-30: Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM2...0 changes the amplitude of the differential voltage on XL1/2 by approximately 110 mV.
Example:120 Ω interface and wired as shown in **Figure 23** on page **79**.

XPM04-00: $1D_H$ or 29 decimal
XPM14-10: $1D_H$ or 29 decimal
XPM24-20: 00_H
XPM34-30: 00_H

Programming values for XPM0...2: BD_H, 03_H, 00_H

XLHP… **Transmit Line High Power**

0… Normal operation

1… With this bit the output current capability of the transmit line XL1 and XL2 can be influenced. Connecting low impedances to the outputs XL1/XL2 this bit should be set to increase the possible output current. Setting this bit has no influence on the voltage levels of the pulse shape.

XLT... **Transmit Line Tristate**

0... Normal operation

1... Transmit line XL1/XL2 or XDOP/XDON are switched into high impedance state. If this bit is set the transmit line monitor status information is frozen.

DAXLT... **Disable Automatic Tristating of XL1/2**

0... Normal operation. If a short is detected on pins XL1/2 the transmit line monitor sets the XL1/2 outputs into a high impedance state.

1... If a short is detected on XL1/2 pins automatic setting these pins into a high impedance (by the XL-monitor) state is disabled.

Transparent Service Word Mask (Read/Write)

Value after RESET: 00_H

	7							0	
TSWM	TSIS	TSIF	TRA	TSA4	TSA5	TSA6	TSA7	TSA8	(27)

TSWM7...0... **Transparent Service Word Mask**

TSIS... **Transparent S_i-Bit in Service Word**

0... The S_i-Bit is generated internally.

1... The S_i-Bit in the service word is taken from port XDI and transparently passed through the FALC®-LH without any changes. The internal information of the FALC®-LH (register XSW) is ignored.

TSIF... **Transparent S_i Bit in FAS Word**

0... The S_i-Bit is generated internally.

1... The S_i-Bit in the FAS word is taken from port XDI and routed transparently through the FALC®-LH without any changes. The internal information of the FALC®-LH (register XSW) is ignored.

TRA… **Transparent Remote Alarm**

0… The Remote Alarm Bit is generated internally.

1… The A Bit is taken from port XDI and routed transparently through the FALC®-LH without any changes. The internal information of the FALC®-LH (register XSW) is ignored.

TSA4…8... **Transparent SA4...8 Bit**

0… The SA4...8 bits are generated internally.

1… The SA4...8 bits are taken from port XDI or from the internal signaling controller if enabled and transparently passed through the FALC®-LH without any changes. The internal information of the FALC®-LH (registers XSW and XSA4...8) is ignored.

Idle Channel Code Register (Read/Write)

Value after RESET: 00_H

	7						0	
IDLE	IDL7						IDL0	(29)

IDL7…0… **Idle Channel Code**

If channel loop back is enabled by programming LOOP.ECLB = 1, the contents of the assigned outgoing channel on ports XL1/XL2 or XDOP/XDON is set equal to the idle channel code selected by this register.

Additionally, the specified pattern overwrites the contents of all channels selected via the idle channel registers ICB1…ICB4. IDL7 is transmitted first.

Transmit SA4...8 Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H, 00_H

	7							0	
XSA4	XS47	XS46	XS45	XS44	XS43	XS42	XS41	XS40	(2A)
XSA5	XS57	XS56	XS55	XS54	XS53	XS52	XS51	XS50	(2B)
XSA6	XS67	XS66	XS65	XS64	XS63	XS62	XS61	XS60	(2C)
XSA7	XS77	XS76	XS75	XS74	XS73	XS72	XS71	XS70	(2D)
XSA8	XS87	XS86	XS85	XS84	XS83	XS82	XS81	XS80	(2E)

XSA8…XSA4… **Transmit S_a-Bit Data**

The Sa-bit register access is enabled by setting bit FMR1.ENSA = 1. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XSA4...8 is copied into a shadow register. The contents is subsequently sent out in the service words of the next outgoing CRC multiframe (or doubleframes) if none of the time slot 0 transparent modes is enabled. XS40 is sent out in bit position 4 in frame 1, XS47 in frame 15. The transmit multiframe begin interrupt XMB request that these registers should be serviced. If requests for new information are ignored, current contents is repeated.

Framer Mode Register 3 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR3			XLD	XLU	CMI	SA6SY	CFRZ	EXTIW	(2F)

XLD… **Transmit LLB Down Code**

0… Normal operation.

1… A one in this bit position causes the transmitter to replace normal transmit data with the LLB Down (Deactivate) Code continuously until this bit is reset. The LLB Down Code is optionally overwritten by the timeslot 0 depending on bit

LCR1.LLBF. For correct operation bit FMR3.XLU must be cleared.

XLU… **Transmit LLB UP Code**

0… Normal operation.

1… A one in this bit position causes the transmitter to replace normal transmit data with the LLB UP Code continuously until this bit is reset. The LLB UP Code is overwritten by the timeslot 0 depending on bit LCR1.LLBF. For correct operation bit FMR3.XLD must be cleared.

CMI… **Select CMI Precoding**

Only valid if CMI code (FMR0.XC1/0=01) is selected. This bit defines the CMI precoding and influences only the transmit data and not the receive data.

0… CMI with HDB3 precoding

1… CMI without HDB3 precoding

SA6SY… **Receive SA6 Access Synchronous Mode**

Only valid if multiframe format (FMR2.RFS1/0=1x) is selected.

0… The detection of the predefined SA6 bit pattern (refer to chapter SA6 Bit Detection according to ETS 300233) is done independently of the multiframe synchronous state.

1… The detection of the SA6 bit pattern is done synchronously to the multiframe.

CFRZ… **Enable CAS Freeze Output**

This bit selects the function of pin RFSPQ.

0… The receive frame synchronous pulse is output on pin RFSPQ.

1… The synchronous status of the integrated CAS controller (FRS1.TS16LFA) is output on pin $\overline{\text{RFSP}}$. If the CAS synchronizer lost its synchronization this pin is set high.

EXTIW… **Extended CRC4 to Non CRC4 Interworking**

Only valid in multiframe format. This bit selects the reaction of the synchronizer after the 400 ms timeout has been elapsed and starts transmitting a remote alarm if FMR2.AXRA is set.

0… The CRC4 to Non CRC4 interworking is done as described in ITU-T G. 706 Annex B.

1… The interworking is done according to ITU-T G. 706 with the exception that the synchronizer still searches for the multiframing even if the 400 ms timer is expired. Switching into doubleframe format is disabled. If FMR2.AXRA is set the remote alarm bit is active in the outgoing data stream until the multiframe is found.

Idle Channel Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
ICB1	IC0	IC1	IC2	IC3	IC4	IC5	IC6	IC7	(30)
ICB2	IC8	IC9	IC10	IC11	IC12	IC13	IC14	IC15	(31)
ICB3	IC16	IC17	IC18	IC19	IC20	IC21	IC22	IC23	(32)
ICB4	IC24	IC25	IC26	IC27	IC28	IC29	IC30	IC31	(33)

IC0…31… **Idle Channel Selection Bits**

These bits define the channels (time slots) of the outgoing PCM frame to be altered.
Assignments:
IC0 → time slot 0
IC1 → time slot 1
...
IC31 → time slot 31

0… Normal operation.

1… Idle channel mode. The contents of the selected time slot is overwritten by the idle channel code defined via register IDLE.

Note: Although time slot 0 can be selected by bit IC0, its contents is only altered if the transparent mode is selected (XSP.TT0).

Line Interface Mode 0 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM0	XFB	XDOS	SCL1	SCL0	EQON	ELOS	LL	MAS	(34)

XFB… **Transmit Full Bauded Mode**

Only applicable for dual rail mode (bit LIM1.DRS = 1).

0…Output signals XDOP/XDON are half bauded (normal operation).

1…Output signals XDOP/XDON are full bauded.

Note: If CMI coding is selected (FMR0.XC1/0=01) this bit has to be cleared.

XDOS… **Transmit Data Out Sense**

Only applicable for dual rail mode (bit LIM1.DRS = 1)

0… Output signals XDOP/XDON are active low. Output XOID is active high (normal operation).

1… Output signals XDOP/XDON are active high. Output XOID is active low.

Note: If CMI coding is selected (FMR0.XC1/0=01) this bit has to be cleared.

SCL1…0… **Select Clock Output**

00… Output frequency at pin CLKX: 2048 kHz active high

01… Output frequency at pin CLKX: 2048 kHz active low

10… Output frequency at pin CLKX: 4096 kHz active high

11… Output frequency at pin CLKX: 4096 kHz active low

EQON… **Receive Equalizer On**

0… -10 dB Receiver: short haul mode

1… -43 dB Receiver, long haul mode

ELOS **Enable Loss of Signal**

0… Normal operation. The extracted receive clock is output via pin RCLK.

1… In case of loss of signal (FRS0.LOS = 1) the RCLK is set high. If FRS0.LOS = 0 the received clock is output via RCLK.

LL... **Local Loop**

0... Normal operation

1... Local loop active. The local loopback mode disconnects the receive lines RL1/RL2 or RDIP/RDIN from the receiver. Instead of the signals coming from the line the data provided by system interface are routed through the analog receiver back to the system interface. The unipolar bit stream is transmitted undisturbedly on the line. Receiver and transmitter coding must be identical. Operates in analog and digital line interface mode. In analog line interface mode data is transferred through the complete analog receiver.

MAS... **Master Mode**

0... Slave mode

1 ... Master mode on. Setting this bit the DCO-R circuitry is frequency synchronized with the clock (2.048 MHz) supplied by SYNC. If this pin is connected to VSS the DCO-R circuitry is centered and no receive jitter attenuation is performed. The generated clocks are stable.

Line Interface Mode 1 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM1	EFSC	RIL2	RIL1	RIL0	TCD1	JATT	RL	DRS	(35)

EFSC... **Enable Frame Synchronization Pulse**

0... The transmit clock is output via pin XCLK.

1... Pin XCLK provides a 8 kHz frame synchronization pulse which is active high for one 2 MHz cycle (pulse width = 488 ns).

RIL2...0... **Receive Input Threshold**

Only valid if analog line interface in short haul mode is selected (LIM0.EQON=0 and LIM1.DRS=0).

Loss of signal is declared if the voltage between pins RL1 and RL2 drops below the limits programmed via bits RIL2...0 and the received data stream has no transition for a period defined in the PCD register.

The threshold where no signal is declared is programmable by the RIL2...0 bits, see **Table 58 "DC Parameters" on page 336** for detail.

Note: LIM1.RIL(2:0) must be programmed before LIM0.EQON = 1 is set.

TCD1… **Transmit Clock Generation DCO-X**

0… The transmit clock is sourced by the DCO-X circuitry, if the transmit elastic buffer is enabled. Reference clock is XTAL3.

1… The transmit clock is sourced by the DCO-X circuitry, if the transmit elastic buffer is enabled. Reference clock is XTAL1. DCO-R cannot be used in this configuration.

JATT…RL... **Transmit Jitter Attenuator/Remote Loop**

00… Normal operation. The transmit jitter attenuator is disabled. Transmit data bypasses the buffer.

01… Remote Loop active without transmit jitter attenuator enabled. Transmit data bypasses the buffer.

10… Transmit Slicer active.
FALC54 compatibility: Transmit data received on port XDI is first written into the transmit jitter attenuator and then sent jitter free on ports XL1/2 or XDOP/N or XOID.
For FALC-LH the same function even with a better support in case of slips is also provided if bits are set to
SIC1.XBS1/0 = 10.

11… Remote Loop and jitter attenuator active. Received data from pins RL1/2 or RDIP/N or ROID is sent 'jitter free' on ports XL1/2 or XDOP/N or XOID. The dejittered clock is generated by the DCO-X circuitry.

DRS… **Dual Rail Select**

0… The ternary interface is selected. Multifunction ports RL1/2 and XL1/2 become analog in/outputs.

1… The digital dual rail interface is selected. Received data is latched on multifunction ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Pulse Count Detection Register (Read/Write)

Value after RESET: 00_H

	7		0	
PCD	PCD7		PCD0	(36)

PCD7…0… **Pulse Count Detection**

A LOS alarm is detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable via the PCD register and can be calculated as follows:
$T = 16 \times (N+1)$; with $0 \leq N \leq 255$.

The maximum time is: 256 x 16 x 488 ns = 2 ms. Every detected pulse resets the internal pulse counter. The counter is clocked with the receive clock RCLK.

Pulse Count Recovery (Read/Write)

Value after RESET: 00_H

	7		0	
PCR	PCR7		PCR0	(37)

PCR7…0… **Pulse Count Recovery**

A LOS alarm is cleared if a pulse density is detected in the received bit stream. The number of pulses M which must occur in the predefined PCD time interval is programmable via the PCR register and can be calculated as follows:

$M = N+1$; with $0 \leq N \leq 255$.

The time interval starts with the first detected pulse transition. With every received pulse a counter is incremented and the actual counter is compared with the contents of PCR register. If the pulse number is $\geq$ the PCR value the LOS alarm is reset; otherwise the alarm stays active. In this case the next detected pulse transition starts a new time interval.

Line Interface Mode 2 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM2			DJA2	DJA1	SCF	ELT	LOS2	LOS1	(38)

DJA2… **Digital Jitter Attenuation DCO-X**

0… Jitter attenuation of the transmit clock is done using an external pullable crystal between pins XTAL3/4

1… Jitter attenuation of the transmit clock is done **without** using an external pullable crystal between pins XTAL3/4. Only a free running 16.384-MHz clock has top be provided at XTAL3 (+/- 50 ppm).

DJA1… **Digital Jitter Attenuation DCO-R**

0… Jitter attenuation of the system/transmit clock is done using an external pullable crystal between pins XTAL1/2

1… Jitter attenuation of the system/transmit clock is done **without** using an external pullable crystal between pins XTAL1/2. Only a free running 16.384-MHz clock has top be provided at XTAL1 (+/- 50 ppm).

SCF… **Select Corner Frequency of DCO-R**

Setting this bit reduces the corner frequency of the DCO-R circuit by the factor of ten to 0.2 Hz.

Note: Reducing the corner frequency of the DCO-R circuitry increases the synchronization time before the frequencies are synchronized.

ELT… **Enable Loop-Timed**

0… normal operation.

1… Transmit clock is generated from the clock supplied by XTAL3/4 which is synchronized with the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. Refer to register XSW.XTM.

LOS2...1… **Loss of Signal Recovery Condition**

00… The LOS alarm is cleared if the predefined pulse density (register PCR) is detected during the time interval which is defined by register PCD.

01… Additionally to the recovery condition described above a LOS alarm is only cleared if the pulse density is fulfilled and no more than 15 contiguous zeros are detected during the recovery interval. (according to TR-NWT 499).

10… Clearing a LOS alarm is done if the pulse density is fulfilled and no more than 99 contiguous zeros are detected during the recovery interval. (according to TR-NWT 820).

11… Not assigned.

Loop Code Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
LCR1	EPRM	XPRBS	LDC1	LDC0	LAC1	LAC0	FLLB	LLBP	(39)

EPRM… **Enable Pseudo Random Bit Sequence Monitor**

0… Pseudo random bit sequence (PRBS) monitor is disabled.

1… PRBS monitor is enabled. Setting this bit enables incrementing the CEC2 error counter with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR1.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit RSP.LLBAD. The expected PRBS sequence has to be selected by bit LCR1.LLBP.

The PRBS status signal is output on pin $\overline{\text{RFSP}}$, if FMR3.CFRZ=0 and LCR1.EPRM=1. It is set high, if the PRBS monitor is in synchronous state.

XPRBS… **Transmit Pseudo Random Bit Sequence**

A one in this bit position enables transmitting of a pseudo random bit sequence to the remote end. Depending on pit LLBP the PRBS is generated according to 2^{15}-1 or 2^{20}-1 with a maximum-14-zero restriction (ITU-T O. 151).

LDC1…0... **Length Deactivate (Down) Code**

These bits defines the length of the user programmable LLB deactivate code which is programmable in register LCR2.

00… length: 5 bit

01… length: 6 bit

10… length: 7 bit

11… length: 8 bit

If a shorter pattern length is required, select a multiple of the required length and repeat the pattern in LCR2.

LAC1…0... **Length Activate (Up) Code**

These bits defines the length of the user programmable LLB activate code which is programmable in register LCR3.

00… length: 5 bit

01… length: 6 bit

10… length: 7 bit

11… length: 8 bit

If a shorter pattern length is required, select a multiple of the required length and repeat the pattern in LCR3.

FLLB… **Framed Line Loopback/Invert PRBS**

Depending on bit LCR1.XPRBS this bit enables different functions:

LCR1.XPRBS=0:

0… The line loopback code is transmitted including framing bits.

1… The line loopback code is transmitted unframed.

Invert PRBS

LCR1.XPRBS=1:

0… The generated PRBS is transmitted not inverted.

1… The PRBS is transmitted inverted.

LLBP… **Line Loopback Pattern**

LCR1.XPRBS=0

0… Fixed line loopback code : 001 (loop down) or 00001 (loop up).

1… Enable user programmable line loopback code via register LCR2/3.

LCR1.XPRBS=1 or LCR1.EPRM = 1

0… 2^{15} -1

1… 2^{20} -1

Loop Code Register 2 (Read/Write)

Value after RESET: 00_H

	7						0	
LCR2	LDC7						LDC0	(3A)

LDC7…0… **Line Loopback Deactivate Code**

If enabled by bit FMR3.XLD the LLB deactivate code is repeated automatically until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmitted last. If the selected code length is less than 8 bit, the leftmost bits of LCR2 are ignored. For correct operations bit LCR1.XPRBS has to be cleared.

Loop Code Register 3 (Read/Write)

Value after RESET: 00_H

	7						0	
LCR3	LAC7						LAC0	(3B)

LAC7…0… **Line Loopback Activate Code**

If enabled by bit FMR3.XLU the LLB activate code is repeated automatically until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmitted last. If the selected code length is less than 8 bit, the leftmost bits of LCR3 are ignored. For correct operations bit LCR1.XPRBS has to be cleared.

System Interface Control 1 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC1	SRSC		RBS1	RBS0	SXSC		XBS1	XBS0	(3C)

SRSC… **Select Receive System Clock**

0… expected frequency on pin SCLKR: 8.192 MHz
Calculation of delay time T (SCLKR cycles) depends on the value X of the “Receive Counter Offset” register RC1/0 and of the programming of RC0.RCOS.

Delay T is an even number in the range of 0 to 1022:

RCOS = 0: X = 5 – T/2 if $0 \le T \le 10$

X = 517 – T/2 if $12 \le T \le 1022$

Delay T is an odd number in the range of 1 to 1023:

RCOS = 1: X = 5 – (T – 1)/2 if $1 \le T \le 11$

X = 517 – (T – 1)/2 if $13 \le T \le 1023$

1… expected frequency on pin SCLKR: 2.048 MHz
Calculation of delay time T (SCLKR cycles) depends on the value X of the “Receive Counter Offset” register RC1/0:
T = (260 – x/2) mod 256

Delay time T = time between beginning of time slot 0 at RDO and the initial edge of SCLKR after $\overline{\text{SYPR}}$ goes active.
If this bit is set FMR1.IMOD must be set also and bit RC0.0 must be cleared.

RBS1...0… **Receive Buffer Size**

00… buffer size : 2 frames

01… buffer size : 1 frame

10… buffer size : 92 bits

11… bypass of receive elastic store

SXSC… **Select Transmit System Clock**

0… expected frequency on pin SCLKX: 8.192 MHz
Calculation of delay time T (SCLKX cycles) depends on the value X of the “Transmit Counter Offset” register XC1/0 and of the programming of XC1.XCOS:

Delay T is an even number in the range of 0 to 1022:

XCOS = 0: X = 498 – T/2 if $0 \leq T \leq 996$

X = 1010 – T/2 if $998 \leq T \leq 1022$

Delay T is an odd number in the range of 1 to 1023:

XCOS = 1: X = 498 – (T – 1)/2 if $1 \leq T \leq 997$

X = 1010 – (T – 1)/2 if $999 \leq T \leq 1023$

1… expected frequency on pin SCLKX: 2.048 MHz
Calculation of delay time T (SCLKX cycles) depends on the value X of the “Transmit Counter Offset” register XC1/0:
T = (507 – x/2) mod 256

Delay time T = time between beginning of time slot 0 at XDI and the initial edge of SCLKX after $\overline{\text{SYPX}}$ goes active.
If this bit is set FMR1.IMOD must be set also and bit XC0.0 must be cleared.

XBS1...0… **Transmit Buffer Size**

00… By-pass of transmit elastic store

01… buffer size : 1 frame

10… buffer size : 2 frames

11… buffer size : 92 bits

System Interface Control 2 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC2	FFS	SSF						SRFSO	(3D)

FFS … **Force Freeze Signaling**

Setting this bit disables updating of the receive signaling buffer and current signaling information is frozen. After resetting this bit and receiving a complete superframe updating of the signaling buffer is started again. The freeze signaling status could be also automatically generated by detecting the Loss of Signal alarm or a Loss of CAS Frame Alignment or a receive slip (only if external register access via RSIG is enabled). This automatic freeze signaling function is logically ored with this bit.
The current internal freeze signaling status is available in register SIS.SFS.

SSF … **Serial Signaling Format**

Only applicable if pin function R/XSIG is selected.

0… Bits 1...4 in all time slots except time slots 0 +16 are cleared.

1… Bits 1...4 in all time slots except time slots 0 +16 are set high.

SRFSO… **Select Receive Frame Sync Output**

0… Pin $\overline{\text{SYPR}}$: Input

1… Pin $\overline{\text{SYPR}}$: Output
Setting this bit disables the timeslot assigner. With register RC1/0 the receive frame marker could be activated during any bit position of the current frame. This marker is active high for 2.048 MHz cycle and is clocked off with the falling edge of SCLKR or RCLK if the receive elastic store is bypassed.
If no $\overline{\text{SYPR}}$ has been activated since RESET or software reset CMDR.RES the outputs of the receive system interface assume an arbitrary alignment.
Calculation of the value X of the “Receive Counter Offset” register RC1/0 depends on SCLKR and on the bit position BP which should be marked:
X = (2 + 2BP) mod 512, for SCLKR = 2.048 MHz

Line Interface Mode 3 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM3							CSC	ESY	(3E)

CSC… **Configure System Clock CLK16M/CLK12M**

0… Dejittered XTAL1 or XTAL3 clock is output on CLK16M/ CLK12M.

1… Buffered XTAL1 or XTAL3 clock is output on CLK16M/ CLK12M.

ESY… **External Synchronization of DCO-X**

Together with bit LOOP.SPN the functionality of pin 80 is defined:

Programming of LOOP.SPN and LIM3.ESY and the corresponding pin function is shown below.

SPN/ESY:

00… function of pin 80 XSIG: If SIC3.TTRF = 1, transmit data from the system interface. No input function defined for SIC3.TTRF = 0.

01… function of pin 80 SYNC2: external synchronization input for the DCO-X circuitry.

10… function of pin 80 ROID: Receive Optical Interface Data.

11… function of pin 80 XSIG: Transmit signaling input from the transmit system interface.

System Interface Control 3 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC3							TTRF	DAF	(40)

TTRF… **TTR Register Function**

Setting this bit the function of the TTR1...4 registers are changed. A one in each TTR register forces the XSIGM marker high for the respective time slot and controls sampling of the time slots provided on pin XSIG. XSIG is selected by LOOP.SPN = 0 and LIM3.ESY = 0.

DAF… **Disable Automatic Freeze**

Valid only if serial signaling access is enabled.

0… Signaling is automatically frozen if one of the following alarms occurred: Loss of Signal (FRS0.LOS), Loss of CAS Frame Alignment (FRS1.TS16LFA) or receive slips (ISR3.RSP/N).

1… Automatic freezing of signaling data is disabled. Updating of the signaling buffer is also done if one of the above described alarm conditions is active. However, updating of the signaling buffer is stopped if SIC2.FFS is set.

Disable Error Counter (Write)

Value after RESET: 00_H

	7							0	
DEC			DCEC3	DCEC2	DCEC1	DEBC	DCVC	DFEC	(60)

DCEC3… **Disable CRC Error Counter 3**

DCEC2… **Disable CRC Error Counter 2**

DCEC1… **Disable CRC Error Counter**

DEBC … **Disable Errored Block Counter**

DCVC… **Disable Code Violation Counter**

DFEC… **Disable Framing Error Counter**

These bits are only valid if FMR1.ECM is cleared. They have to be set before reading the error counters. They are reset automatically if the corresponding error counter high byte has been read. With the rising edge of these bits the error counters are latched and then cleared.

Transmit CAS Registers (Write)

Value after RESET: not defined

	7							0	
XS1	0	0	0	0	X	Y	X	X	(70)
XS2	A1	B1	C1	D1	A16	B16	C16	D16	(71)
XS3	A2	B2	C2	D2	A17	B17	C17	D17	(72)
XS4	A3	B3	C3	D3	A18	B18	C18	D18	(73)
XS5	A4	B4	C4	D4	A19	B19	C19	D19	(74)
XS6	A5	B5	C5	D5	A20	B20	C20	D20	(75)
XS7	A6	B6	C6	D6	A21	B21	C21	D21	(76)
XS8	A7	B7	C7	D7	A22	B22	C22	D22	(77)
XS9	A8	B8	C8	D8	A23	B23	C23	D23	(78)
XS10	A9	B9	C9	D9	A24	B24	C24	D24	(79)
XS11	A10	B10	C10	D10	A25	B25	C25	D25	(7A)
XS12	A11	B11	C11	D11	A26	B26	C26	D26	(7B)
XS13	A12	B12	C12	D12	A27	B27	C27	D27	(7C)
XS14	A13	B13	C13	D13	A28	B28	C28	D28	(7D)
XS15	A14	B14	C14	D14	A29	B29	C29	D29	(7E)
XS16	A15	B15	C15	D15	A30	B30	C30	D30	(7F)

Transmit CAS Register 1...16

The transmit CAS register access is enabled by setting bit XSP.CASEN = 1. Each register except XS1 contains the CAS bits for two time slots. With the transmit multiframe begin ISR1.XMB the contents of these registers is copied into a shadow register. The contents is sent out subsequently in the time slots 16 of the outgoing data stream.

Note: If ISR1.XMB is not used and the write access to these registers is done exact in that moment when this interrupt is generated, data may be lost.

XS1.7 is sent out first and XS16.0 is sent last. The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information are ignored, current contents is repeated. XS1 has to be programmed with the multiframe pattern. This pattern must always stay low, otherwise the remote end loses its synchronization. With setting the Y-bit a remote alarm is transmitted to the far end. The Y-bit is logically ored with bit CCR1.XTS16RA.

The X bits (Spare bits) should be set if they are not used.

If access to these registers is done without control of the interrupt ISR1.XMB the registers should be written twice to avoid an internal data transfer error.

Note: A software reset (CMDR.XRES) resets these registers.

9.3 E1 Status Register Addresses

Table 52 E1 Status Register Address Arrangement

Address	Register	Type	Comment	Page
00	RFIFO	R	Receive FIFO	230
01	RFIFO	R	Receive FIFO	230
4B	RES	R	Receive Equalizer Status	230
4C	FRS0	R	Framer Receive Status 0	231
4D	FRS1	R	Framer Receive Status 1	234
4E	RSW	R	Receive Service Word	236
4F	RSP	R	Receive Spare Bits	236
50	FECL	R	Framing Error Counter Low	238
51	FECH	R	Framing Error Counter High	238
52	CVCL	R	Code Violation Counter Low	239
53	CVCH	R	Code Violation Counter High	239
54	CEC1L	R	CRC Error Counter 1 Low	240
55	CEC1H	R	CRC Error Counter 1 High	240
56	EBCL	R	E-Bit Error Counter Low	241
57	EBCH	R	E-Bit Error Counter High	241
58	CEC2L	R	CRC Error Counter 2 Low	242
59	CEC2H	R	CRC Error Counter 2 High	242
5A	CEC3L	R	CRC Error Counter 3 Low	243
5B	CEC3H	R	CRC Error Counter 3 High	243
5C	RSA4	R	Receive SA4 Bit Register	244
5D	RSA5	R	Receive SA5 Bit Register	244
5E	RSA6	R	Receive SA6 Bit Register	244
5F	RSA7	R	Receive SA7 Bit Register	244
60	RSA8	R	Receive SA8 Bit Register	244
61	RSA6S	R	Receive SA6 Bit Status Register	245
64	SIS	R	Signaling Status Register	246
65	RSIS	R	Receive Signaling Status Register	247
66	RBCL	R	Receive Byte Control Low	248
67	RBCH	R	Receive Byte Control High	249

Table 52 E1 Status Register Address Arrangement (cont'd)

Address	Register	Type	Comment	Page
68	ISR0	R	Interrupt Status Register 0	249
69	ISR1	R	Interrupt Status Register 1	251
6A	ISR2	R	Interrupt Status Register 2	253
6B	ISR3	R	Interrupt Status Register 3	254
6C	ISR5	R	Interrupt Status Register 5	256
6E	GIS	R	Global Interrupt Status	256
6F	VSTR	R	Version Status	256
70	RS1	R	Receive CAS Register 1	257
71	RS2	R	Receive CAS Register 2	257
72	RS3	R	Receive CAS Register 3	257
73	RS4	R	Receive CAS Register 4	257
74	RS5	R	Receive CAS Register 5	257
75	RS6	R	Receive CAS Register 6	257
76	RS7	R	Receive CAS Register 7	257
77	RS8	R	Receive CAS Register 8	257
78	RS9	R	Receive CAS Register 9	257
79	RS10	R	Receive CAS Register 10	257
7A	RS11	R	Receive CAS Register 11	257
7B	RS12	R	Receive CAS Register 12	257
7C	RS13	R	Receive CAS Register 13	257
7D	RS14	R	Receive CAS Register 14	257
7E	RS15	R	Receive CAS Register 15	257
7F	RS16	R	Receive CAS Register 16	257

9.4 Detailed Description of E1 Status Registers

Receive FIFO (Read)

	7							0	
RFIFO	RF7							RF0	(00/01)

Reading data from RFIFO can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface.

The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT 1 ... 0 (RFIFO threshold level). It can be reduced from 32 bytes (RESET value) down to 2 bytes (four values: 32, 16, 4, 2 bytes).

Data Transfer

Up to 32 bytes/16 words of received data can be read from the RFIFO following an RPF or an RME interrupt.
RPF Interrupt: A fixed number of bytes/words to be read (32, 16, 4, 2 bytes). The message is not yet complete.

RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers.

RFIFO is released by issuing the “Receive Message Complete” command (RMC).

Receive Equalizer Status (Read)

	7							0	
RES	EV1	EV0		RES4	RES3	RES2	RES1	RES0	(4B)

EV1…0... **Equalizer Status Valid**

These bits informs the user about the current state of the receive equalization network. Only valid if LIM1.EQON is set.

00… equalizer status not valid, still adapting

01… equalizer status valid

10… equalizer status not valid

11… equalizer status valid but high noise floor

RES4…0... **Receive Equalizer Status**

The current line attenuation status in steps of about 1.7 dB are displayed in these bits. Only valid if bits EV1...0 = 01 and LIM1.EQON=1. Accuracy: +/- 2 digit, based on temperature influence and noise amplitude variations.

00000… attenuation (0 dB)
...
11001… max. attenuation

Framer Receive Status Register 0 (Read)

	7							0	
FRS0	LOS	AIS	LFA	RRA	AUXP	NMF	LMFA		(4C)

LOS… **Loss of Signal**

Detection:
This bit is set when the incoming signal has “no transitions” (analog interface) or logical zeros (digital interface) in a time interval of T consecutive pulses, where T is programmable by register PCD.
Total account of consecutive pulses: 16 < T < 4096.

Analog interface: The receive signal level where “no transition” is declared is defined by the programmed value of LIM1.RIL2...0 (short haul mode only, LIM1.EQON = 0).

Recovery:
Analog interface: The bit is reset in short haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL2...0; short haul mode only) for at least M pulse periods defined by register PCR in the PCD time interval.

Digital interface: The bit is reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval.

With the rising edge of this bit an interrupt status bit (ISR2.LOS) is set. For additional recovery conditions see register LIM2.LOS2...1.
The bit is also set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

AIS... **Alarm Indication Signal**

The function of this bit is determined by FMR0.ALM.

FMR0.ALM = 0: This bit is set when two or less zeros in the received bit stream are detected in a time interval of 250 µs and the FALC®-LH is in asynchronous state (FRS0.LFA = 1). The bit is reset when no alarm condition is detected (according to ETSI standard).

FMR0.ALM = 1: This bit is set when the incoming signal has two or less Zeros in each of two consecutive double frame period (512 bits). This bit is cleared when each of two consecutive doubleframe periods contain three or more zeros or when the frame alignment signal FAS has been found. (according to ITU-T G.775 standard)

The bit is also set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

With the rising edge of this bit an interrupt status bit (ISR2.AIS) is set.

LFA... **Loss of Frame Alignment**

This bit is set after detecting 3 or 4 consecutive incorrect FAS words or 3 or 4 consecutive incorrect service words (can be disabled). With the rising edge of this bit an interrupt status bit (ISR2.LFA) is set. The specification of the loss of sync conditions is done via bits RC1.SWD and RC1.ASY4. After loss of synchronization, the frame aligner resynchronizes automatically.

The following conditions have to be detected to regain synchronous state:
– The presence of the correct FAS word in frame n.
– The presence of the correct service word (bit 2 = 1) in frame n + 1.
– For a second time the presence of a correct FAS word in frame n + 2.

The bit is cleared when synchronization has been regained (directly after the second correct FAS word of the procedure described above has been received).

If the CRC-multiframe structure is enabled by setting bit FMR2.RFS1, multiframe alignment is assumed to be lost if pulse-frame synchronization has been lost. The resynchronization procedure for multiframe alignment starts after the bit FRS0.LFA has been cleared.

Multiframe alignment has been regained if two consecutive CRC-multiframes have been received without a framing error (refer to FRS0.LMFA).

The bit is set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

If bit FRS0.LFA is cleared a loss of frame alignment recovery interrupt status ISR2.FAR is generated.

RRA… **Receive Remote Alarm**

Set if bit 3 of the received service word is set. An alarm interrupt status ISR2.RA can be generated if the alarm condition is detected.

FRS0.RRA is cleared when no alarm is detected. At the same time a remote alarm recovery interrupt status ISR2.RAR is generated.

The bit RSW.RRA has the same function.

Both status and interrupt status bits are set during alarm simulation.

AUXP… **Auxiliary Pattern Indication**

This bit is set when 254 or more ‘10’ are received in a time interval of 250 µs and the frame alignment is lost FRS0.LFA = 1. An interrupt status ISR3.API is generated if this bit is set.

The bit is reset when no auxiliary pattern condition is detected. The bit is also set during alarm simulation and reset if FMR0.SIM is cleared and no alarm condition exists.

NMF… **No Multiframe Alignment Found**

This bit is only valid if the CRC4 interworking is selected (FMR2.RFS1/0 = 11). Set if the multiframe pattern could not be detected in a time interval of 400 ms after the framer has reached the doubleframe synchronous state. The receiver is then automatically switched to doubleframe format.

This bit is reset if the basic framing has been lost.

LMFA… **Loss of Multiframe Alignment**

Not used in doubleframe format (FMR2.RFS1 = 0). In this case, LMFA is set.

In CRC-multiframe mode (FMR2.RFS1 = 1), this bit is set

– if force resynchronization is initiated by setting bit FMR0.FRS, or

– if multiframe force resynchronization is initiated by setting bit FMR1.MFCS, or

– if pulseframe alignment has been lost (FRS0.LFA).

It is reset if two CRC-multiframes have been received at an interval of n × 2 ms (n = 1, 2, 3…) without a framing error.

If bit FRS0.LMFA is cleared a loss of multiframe alignment recovery interrupt status ISR2.MFAR is generated.

Framer Receive Status Register 1 (Read)

	7						0	
FRS1		TS16RA	TS16LOS	TS16AIS	TS16LFA		XLS	XLO	(4D)

TS16RA… **Receive Timeslot 16 Remote Alarm**

This bit contains the actual information of the received remote alarm bit RS1.2 in time slot 16. Setting and resetting of this bit causes an interrupt status change ISR3.RA16.

TS16LOS… **Receive Timeslot 16 Loss of Signal**

This bit is set if the incoming TS16 data stream contains always zeros for at least 16 contiguously received time slots. A one in a time slot 16 resets this bit.

TS16AIS… **Receive Timeslot 16 Alarm Indication Signal**

The detection of the alarm indication signal in timeslot 16 is according to ITU-T G.775.

This bit is set if the incoming TS16 contains less than 4 zeros in each of two consecutive TS16 multiframe periods. This bit is cleared if two consecutive received CAS multiframe periods contains more than 3 zeros or the multiframe pattern was found in each of them. This bit is cleared if TS0 synchronization is lost.

TS16LFA… **Receive Timeslot 16 Loss of Multiframe Alignment**

0… The CAS controller is in synchronous state after frame alignment is accomplished.

1… This bit is set if the framing pattern ‘0000’ in 2 consecutive CAS multiframes were not found or in all TS16 of the preceding multiframe all bits were reset. An interrupt ISR3.LMFA16 is generated.

XLS… **Transmit Line Short**

Significant only if the ternary line interface is selected by LIM1.DRS=0.

0… Normal operation. No short is detected.

1… The XL1 and XL2 are shortened for at least 32 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high impedance state if bit XPM2.DAXLT is reset. After 32 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit is reset. With any change of this bit an interrupt ISR1.XLSC is generated. In case of XPM2.XLT is set this bit is frozen.

XLO… **Transmit Line Open**

0… Normal operation

1… This bit is set if at least 32 consecutive zeros were sent via pins XL1/XL2 or XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC is set. In case of XPM2.XLT is set this bit is frozen.

Receive Service Word Pulseframe (Read)

	7							0	
RSW	RSI		RRA	RY0	RY1	RY2	RY3	RY4	(4E)

RSI… **Receive Spare Bit for International Use**

First bit of the received service word. It is fixed to one if CRC-multiframe mode is enabled.

RRA… **Receive Remote Alarm**

Equivalent to bit FRS0.RRA.

RY0…RY4… **Receive Spare Bits for National Use (Y-Bits, S_n-Bits, S_a-Bits)**

Receive Spare Bits/Additional Status (Read)

	7							0	
RSP	SI1	SI2		LLBDD	LLBAD	RSIF	RS13	RS15	(4F)

SI1…SI2… **Submultiframe Error Indication 1, 2**

Not valid if doubleframe format is enabled. In this case, both bits are set.

When using CRC-multiframe format these bits are set to

0… If multiframe alignment has been lost, or
if the last multiframe has been received with CRC error(s). SI1 flags a CRC error in last sub-multiframe 1, SI2 flags a CRC error in last sub-multiframe 2.

1… If at multiframe synchronous state last assigned sub-multiframe has been received without a CRC error.

Both flags are updated with beginning of every received CRC multiframe.

If automatic transmission of sub-multiframe status is enabled by setting bit XSP.AXS, above status information is inserted automatically in S_i -bit position of every outgoing CRC multiframe (under the condition that time slot 0 transparent modes are both disabled):
SI1 $\rightarrow$ S_i -bit of frame 13, SI2 $\rightarrow$ S_i -bit of frame 15.

LLBDD… **Line Loop Back Deactivation Signal Detected**

This bit is set in case the LLB deactivate signal is detected and then received over a period of more than 25 ms with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the timeslot 0 is not taken into account for the error rate calculation.

Any change of this bit causes a LLBSC interrupt.

LLBAD… **Line Loop Back Activation Signal Detected**

Depending on bit LCR1.EPRM the source of this status bit changed.

LCR1.EPRM=0: This bit is set in case the LLB activate signal is detected and then received over a period of more than 25 ms with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the timeslot 0 is not taken into account for the error rate calculation.

Any change of this bit causes a LLBSC interrupt.

PRBS Status

LCR1.EPRM=1: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a BER 1/10. A data stream containing all zeros with/without framing bits is also a valid pseudo random bit sequence. The same applies to an all ones data stream.

RSIF… **Receive Spare Bit for International Use (FAS Word)**

First bit in FAS-word. Used only in doubleframe format, otherwise fixed to ‘1’.

RS13… **Receive Spare Bit (Frame 13, CRC Multiframe)**

First bit in service word of frame 13. Significant only in CRC-multiframe format, otherwise fixed to ‘0’. This bit is updated with beginning of every received CRC multiframe.

RS15… **Receive Spare Bit (Frame 15, CRC Multiframe)**

First bit in service word of frame 15. Significant only in CRC-multiframe format, otherwise fixed to ‘0’. This bit is updated with beginning of every received CRC multiframe.

Framing Error Counter (Read)

	7			0	
FECL	FE7			FE0	(50)

	7			0	
FECH	FE15			FE8	(51)

FE15…0… **Framing Errors**

This 16-bit counter is incremented when a FAS word has been received with an error.

Framing errors are counted during basic frame synchronous state only (but even if multiframe synchronous state is not reached yet). During alarm simulation, the counter is incremented every 250 µs up to its saturation. The error counter doesn't roll over.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DFEC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Code Violation Counter (Read)

	7			0	
CVCL	CV7			CV0	(52)

	7			0	
CVCH	CV15			CV8	(53)

CV15…0… **Code Violations**

No function if NRZ code has been enabled.

If the HDB3 or the CMI code is selected, the 16-bit counter is incremented when violations of the HDB3 code are detected. The error detection mode is determined by programming the bit FMR0.EXTD.

If simple AMI coding is enabled (FMR0.RC0/1 = 10) all bipolar violations are counted. The error counter doesn't roll over.

During alarm simulation, the counter is incremented every four bits received up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 1 (Read)

	7			0	
CEC1L	CR7			CR0	(54)

	7			0	
CEC1H	CR15			CR8	(55)

CR15…0… **CRC Errors**

No function if doubleframe format is selected.

In CRC-multiframe mode, the 16-bit counter is incremented when a CRC-submultiframe has been received with a CRC error. CRC errors don't count during asynchronous state. The error counter doesn't roll over.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC1 has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC1 is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

E Bit Error Counter (Read)

	7						0	
EBCL	EB7						EB0	(56)

	7						0	
EBCH	EB15						EB8	(57)

EB15…0… **E-Bit Errors**

If doubleframe format is selected, FEBEH/L has no function. If CRC-multiframe mode is enabled, FEBEH/L works as submultiframe error indication counter (16 bits) which counts zeros in S_i-bit position of frame 13 and 15 of every received CRC multiframe. The error counter doesn't roll over.

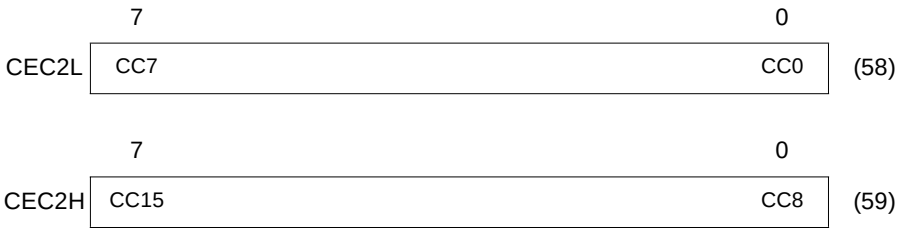
During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DEBC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 2 (Read)



CC15…0… **CRC Error Counter (Reported from TE via Sa6 -Bit)**

Depending on bit LCR1.EPRM the error counter increment is selected:

LCR1.EPRM=0:
If doubleframe format is selected, CEC2H/L has no function. If CRC-multiframe mode is enabled, CEC2H/L works as SA6 Bit error indication counter (16 bits) which counts the SA6 Bit sequence 0001 and 0011in every received CRC submultiframe.
Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = 0.

SA6 Bit sequence: SA61, SA62, SA63, SA64 = 0001 or 0011 where SA61 is received in frame 1 or 9 in every multiframe.

Pseudo Random Bit Sequence Error Counter

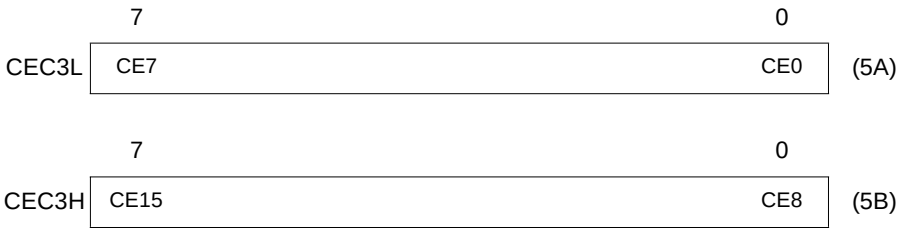
LCR1.EPRM=1:
This 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state RSP.LLBAD = 1. The error counter doesn't roll over.

During alarm simulation, the counter is incremented once per submultiframe up to its saturation.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC2 has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC2 is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter 3 (Read)



CE15…0… **CRC Error Counter (detected at T Ref. Point via Sa6 -Bit)**

If doubleframe format is selected, CEC3H/L has no function. If CRC-multiframe mode is enabled, CEC3H/L works as SA6 Bit error indication counter (16 bits) which counts the SA6 Bit sequence 0010 and 0011in every received CRC submultiframe.
Incrementing the counter is only possible in the multiframe synchronous state FRS0.LMFA = 0.

SA6 Bit sequence: $SA6_1$, $SA6_2$, $SA6_3$, $SA6_4$ = 0010 or 0011 where $SA6_1$ is received in frame 1 or 9 in every multiframe.

Clearing and updating the counter is done according to bit FMR1.ECM.

During alarm simulation, the counter is incremented once per multiframe up to its saturation.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC3 has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC3 is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Receive Sa4-Bit Register (Read)

	7		0	
RSA4	RS47		RS40	(5C)
RSA5	RS57		RS50	(5D)
RSA6	RS67		RS60	(5E)
RSA7	RS77		RS70	(5F)
RSA8	RS87		RS80	(60)

RS47…40… **Receive Sa4-Bit Data (Y-Bits)**

RS57…50… **Receive Sa5-Bit Data**

RS67…60… **Receive Sa6-Bit Data**

RS77…70… **Receive Sa7-Bit Data**

RS87…80… **Receive Sa8-Bit Data**

This register contains the information of the eight SAx bits (x = 4...8) of the previously received CRC multiframe. These registers are updated with every multiframe begin interrupt ISR0.RMB.

RS40 is received in bit-slot 4 of every service word in frame 1, RS47 in frame 15

RS50 is received in bit-slot 5, time slot 0, frame 1, RS57 in frame 15

RS60 is received in bit-slot 6, time slot 0, frame 1, RS67 in frame 15

RS70 is received in bit-slot 7, time slot 0, frame 1, RS77 in frame 15

RS80 is received in bit-slot 8, time slot 0, frame 1, RS87 in frame 15

Valid if CRC multiframe format is enabled by setting bits FMR2.RFS1 = 1 or FMR2.RFS1/0 = 01 (Doubleframe format).

Receive Sa6-Bit Status (Read)

	7							0	
RSA6S			S_X	S_F	S_E	S_C	S_A	S_8	(61)

Four consecutive received SA6-bits are checked on the by ETS 300233 defined SA6-bit combinations. The FALC®-LH detects the following “fixed” SA6-bit combinations:
SA61,SA62,SA63,SA64=1000; 1010; 1100; 1110; 1111. All other possible 4 bit combinations are grouped to status “X”.

A valid SA6-bit combination must occur three times in a row. The corresponding status bit in this register is set. Even if the detected status is active for a short time the status bit remains active until this register is read. Reading the register resets all pending status information.
With any change of state of the SA6-bit combinations an interrupt status ISR0.SA6SC is generated.
During the basic frame asynchronous state updating of this register and interrupt status ISR0.SA6SC is disabled. In multiframe format the detection of the SA6-bit combinations can be done either synchronous or asynchronous to the submultiframe (FMR3.SA6SY). In synchronous detection mode updating of register RSA6S is done in the multiframe synchronous state (FRS0.LMFA=0). In asynchronous state detection mode updating is independent of the multiframe synchronous state.

S_X... **Receive S_a6-Bit Status_X**

If none of the fixed SA6-bit combinations are detected this bit is set.

S_F... **Receive S_a6-Bit Status: “1111”**

Receive SA6-bit status “1111” is detected for three times in a row in the SA6-bit positions.

S_E... **Receive S_a6-Bit Status: “1110”**

Receive SA6-bit status “1110” is detected for three times in a row in the SA6-bit positions.

S_C... **Receive S_a6-Bit Status: “1100”**

Receive SA6-bit status “1100” is detected for three times in a row in the SA6-bit positions.

S_A… **Receive Sa6-Bit Status: “1010”**

Receive SA6-bit status “1010” is detected for three times in a row in the SA6-bit positions.

S_8… **Receive Sa6-Bit Status: “1000”**

Receive SA6-bit status “1000” is detected for three times in a row in the SA6-bit positions.

Signaling Status Register (Read)

	7							0	
SIS	XDOV	XFW	XREP		RLI	CEC	SFS		(64)

XDOV… **Transmit Data Overflow**

More than 32 bytes have been written to the XFIFO.
This bit is reset by:

– a transmitter reset command XRES

– or when all bytes in the accessible half of the XFIFO have been moved in the inaccessible half.

XFW… **Transmit FIFO Write Enable**

Data can be written to the XFIFO.

XREP… **Transmission Repeat**

Status indication of CMDR.XREP.

RLI… **Receive Line Inactive**

Neither FLAGs as Interframe Time Fill nor frames are received via the signaling timeslot.

CEC… **Command Executing**

0… No command is currently executed, the CMDR register can be written to.

1… A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.

Note: CEC is active at most 2.5 periods of the current system data rate.

SFS… **Status Freeze Signaling**

0… freeze signaling status inactive.

1… freeze signaling status active

Receive Signaling Status Register (Read)

	7							0	
RSIS	VFR	RDO	CRC16	RAB	HA1	HA0		LA	(65)

RSIS relates to the last received HDLC frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

VFR… **Valid Frame**

Determines whether a valid frame has been received.

1… valid HDLC frame

0… invalid HDLC frame

An invalid frame is either

– a frame which is not an integer number of 8 bits (n × 8 bits) in length (e.g. 25 bits), or

– a frame which is too short taking into account the operation mode selected via MODE (MDS2...0) and the selection of receive CRC ON/OFF (CCR3.RCRC) as follows:

- MDS2...0 = 011 (16 bit Address),
  RCRC = 0 : 4 bytes; RCRC = 1 : 3-4 bytes
- MDS2...0 = 010 (8 bit Address),
  RCRC = 0 : 3 bytes; RCRC = 1 : 2-3 bytes

Note: Shorter frames are not reported.

RDO… **Receive Data Overflow**

A RFIFO data overflow has occurred during reception of the frame.

Additionally, an interrupt can be generated (refer to ISR1.RDO/ IMR1.RDO).

CRC16… **CRC16 Compare/Check**

0… CRC check failed; received frame contains errors.

1… CRC check o.k.; received frame is error-free.

RAB… **Receive Message Aborted**

The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.

HA1...0… **High Byte Address Compare**

Significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the FALC®-LH compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (broadcast address).

Dependent on the result of this comparison, the following bit combinations are possible:

00… RAH2 has been recognized

01… Broadcast address has been recognized

10… RAH1 has been recognized C/R = 0 (bit 1)

11… RAH1 has been recognized C/R = 1 (bit 1)

Note: If RAH1, RAH2 contain identical values, a match is indicated by '10' or '11'.

LA… **Low Byte Address Compare**

Significant in HDLC modes only.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two registers. (RAL1, RAL2).

0… RAL2 has been recognized

1… RAL1 has been recognized

Receive Byte Count Low (Read)

	7		0	
RBCL	RBC7		RBC0	(66)

Together with RBCH (bits RBC11...8) indicates the length of a received frame (1…4095 bytes). Bits RBC4-0 indicate the number of valid bytes currently in RFIFO. These registers must be read by the CPU following an RME interrupt.

Received Byte Count High (Read)

	7							0	
RBCH				OV	RBC11	RBC10	RBC9	RBC8	(67)

OV… **Counter Overflow**

More than 4095 bytes received.

RBC11...8… **Receive Byte Count (most significant bits)**

Together with RBCL (bits RBC7…RBC0) indicate the length of the received frame.

Interrupt Status Register 0 (Read)

Value after RESET: 00_H

	7							0	
ISR0	RME	RFS	T8MS	RMB	CASC	CRC4	SA6SC	RPF	(68)

All bits are reset when ISR0 is read.

If bit IPC.VIS is set, interrupt statuses in ISR0 may be flagged although they are masked via register IMR0. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

RME… **Receive Message End**

One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte.

The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC4...0. Additional information is available in the RSIS register.

RFS... **Receive Frame Start**

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS interrupt, the contents of

- RSIS-bits 3...1

is valid and can be read by the CPU.

T8MS... **Receive Time Out 8 msec**

Only active if multiframing is enabled.

The framer has found the doubleframing (basic framing) FRS0.LFA = 0 and is searching for the multiframing. This interrupt is set to indicate that no multiframing could be found within a time window of 8 msec. In multiframe synchronous state this interrupt is not generated. Refer also to Floating multiframe alignment window.

RMB... **Receive Multiframe Begin**

This bit is set with the beginning of a received CRC multiframe related to the internal receive line timing.

In CRC multiframe format FMR2.RFS1 = 1 or in doubleframe format FMR2.RFS1...0 = 01 this interrupt occurs every 2 msec. If FMR2.RFS1...0 = 00 this interrupt is generated every doubleframe (512 bits).

CASC... **Received CAS Information Changed**

This bit is set with the updating of a received CAS multiframe information in the registers RS1...16. If the last received CAS information is different to the previous received one, this interrupt is generated after update has been completed. This interrupt occurs only in TS0 and TS16 synchronous state. The registers RS1...16 should be read within the next 2 ms otherwise the contents may be lost.

CRC4... **Receive CRC4 Error**

0... No CRC4 error occurs.

1... The CRC4 check of a received submultiframe failed.

SA6SC... **Receive SA6-Bit Status Changed**

With every change of state of the received SA6-bit combinations this interrupt is set.

RPF… **Receive Pool Full**

32 bytes of a frame have arrived in the receive FIFO. The frame is not yet completely received.

Interrupt Status Register 1 (Read)

	7							0	
ISR1	LLBSC	RDO	ALLS	XDU	XMB		XLSC	XPR	(69)

All bits are reset when ISR1 is read.

If bit IPC.VIS is set, interrupt statuses in ISR1 may be flagged although they are masked via register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

LLBSC… **Line Loop Back Status Change**

Depending on bit LCR1.EPRM the source of this interrupt status changed:

LCR1.EPRM=0: This bit is set, if the LLB activate signal or the LLB deactivate signal, respectively is detected over a period of 25 ms with a bit error rate less than 1/100.

The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds 1/100.

The actual detection status can be read from the RSP.LLBAD and RSP.LLBDD, respectively.

PRBS Status Change

LCR1.EPRM=1: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in RSP.LLBAD.

RDO… **Receive Data Overflow**

This interrupt status indicates that the CPU did not respond fast enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again.

Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.

ALLS… **All Sent**

This bit is set if the last bit of the current frame has been sent out completely and XFIFO is empty.

XDU… **Transmit Data Underrun**

Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued.

Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are re-activated not before this interrupt status register has been read. Thus, XDU should not be masked via register IMR1.

XMB… **Transmit Multiframe Begin**

This bit is set every 2 ms with the beginning of a multiframe transmission and is related to the internal transmit line interface timing.
After setting this bit, registers XS1...16 are copied into the transmit shift registers. The registers XS1...16 are now ready for the next data and have to be updated; otherwise the contents is retransmitted during the next multiframe. A wait time of 3µs has to be observed between reading of XMB = 1 and start of reprogramming XS1...16.

XLSC… **Transmit Line Status Change**

XLSC is set with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS.

The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.

XPR… **Transmit Pool Ready**

A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2 (Read)

	7							0	
ISR2	FAR	LFA	MFAR	T400MS	AIS	LOS	RAR	RA	(6A)

All bits are reset when ISR2 is read.

If bit IPC.VIS is set, interrupt statuses in ISR2 may be flagged although they are masked via register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

FAR… **Frame Alignment Recovery**

The framer has reached doubleframe synchronization. Set when bit FSR0.LFA is reset. It is set also after alarm simulation is finished and the receiver is still synchronous.

LFA… **Loss of Frame Alignment**

The framer has lost synchronization and bit FRS0.LFA is set. It is set during alarm simulation.

MFAR… **Multiframe Alignment Recovery**

Set when the framer has found two CRC-multiframes at an interval of $n \times 2$ ms (n = 1, 2, 3, …) without a framing error. At the same time bit FRS0.LMFA is reset.

It is set also after alarm simulation is finished and the receiver is still synchronous. Only active if CRC-multiframe format is selected.

T400MS… **Receive Time Out 400 msec**

Only active if multiframing is enabled.

The framer has found the doubleframing (basic framing) FRS0.LFA = 0 and is searching for the multiframing. This interrupt is set to indicate that no multiframing could be found within a time window of 400 ms after basic framing has been achieved. In multiframe synchronous state this interrupt is not generated.

AIS… **Alarm Indication Signal**

This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. It is set during alarm simulation.
If IPC.SCI is set high this interrupt status bit is set with every change of state of FRS0.AIS.

LOS... **Loss of Signal**

This bit is set when a loss of signal alarm is detected in the received bit stream and FRS0.LOS is set. It is set during alarm simulation.
If IPC.SCI is set high this interrupt status bit is set with every change of state of FRS0.LOS.

RAR... **Remote Alarm Recovery**

Set if a remote alarm in TS0 is cleared and bit FRS0.RA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.

RA... **Remote Alarm**

Set if a remote alarm in TS0 is detected and bit FRS0.RA is set. It is set during alarm simulation.

Interrupt Status Register 3 (Read)

	7							0	
ISR3	ES	SEC	LMFA16	AIS16	RA16	API	RSN	RSP	(6B)

All bits are reset when ISR3 is read.

If bit IPC.VIS is set, interrupt statuses in ISR3 may be flagged although they are masked via register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

ES... **Errored Second**

This bit is set if at least one enabled interrupt source via IMR4 is set during the time interval of one second. Interrupt sources of IMR4 register:
LFA = Loss of frame alignment detected (FRS0.LFA)
FER = Framing error received
CER = CRC error received
AIS = Alarm indication signal (FRS0.AIS)
LOS = Loss of signal (FRS0.LOS)
CVE = Code violation detected
SLIP= Receive Slip positive/negative detected
EBE = E-Bit error detected (RSP.RS13/15)

SEC... **Second Timer**

The internal one second timer has expired. The timer is derived from clock RCLK.

LMFA16… **Loss of Multiframe Alignment TS 16**

Multiframe alignment of timeslot 16 has been lost if two consecutive multiframe pattern are not detected or if in 16 consecutive timeslot 16 all bits are reset.
If register IPC.SCI is high this interrupt status bit is set with every change of state of FRS1.TS16LFA.

AIS16… **Alarm Indication Signal TS 16 Status Change**

The alarm indication signal AIS in timeslot 16 for the 64 kbit/s channel associated signaling is detected or cleared. A change in bit FRS1.TS16AIS sets this interrupt (This bit is set if the incoming TS 16 signal contains less than 4 zeros in each of two consecutive TS16-multiframe periods.).

RA16… **Remote Alarm TS 16 Status Change**

A change in the remote alarm bit in CAS multiframe alignment word is detected.

API… **Auxiliary Pattern Indication**

This bit is set if the auxiliary pattern is detected in the received bit stream and bit FRS0.AUXP is set.
If register IPC.SCI is high this interrupt status bit is set with every change of state of FRS0.AUXP.

RSN… **Receive Slip Negative**

The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 2.048 MHz. It is set during alarm simulation.

In 2-frame buffer mode a frame is skipped.

RSP… **Receive Slip Positive**

The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 2.048 MHz. It is set during alarm simulation.

In 2-frame buffer mode a frame is repeated.

Interrupt Status Register 5 (Read)

	7							0	
ISR5	XSP	XSN							(6C)

All bits are reset when ISR5 is read.

If bit IPC.VIS is set, interrupt statuses in ISR4 may be flagged although they are masked via register IMR5. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

XSP… **Transmit Slip Positive**

The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 2.048 MHz.

In 2-frame buffer mode a frame is skipped.

XSN… **Transmit Slip Negative**

The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 2.048 MHz.

In 2-frame buffer mode a frame is repeated

Global Interrupt Status Register (Read)

Value after RESET: 00_H

	7							0	
GIS				ISR5	ISR3	ISR2	ISR1	ISR0	(6E)

This status register points to pending interrupts sourced by ISR5 and ISR3...ISR0.

Version Status Register (Read)

	7							0	
VSTR	VN7	VN6	VN5	VN4	VN3	VN2	VN1	VN0	(6F)

VN7...0… **Version Number of Chip**

10_H…Version 1.1

13_H…Version 1.3

Receive CAS Registers (Read)

Value after RESET: not defined

	7							0	
RS1	0	0	0	0	X	Y	X	X	(70)
RS2	A1	B1	C1	D1	A16	B16	C16	D16	(71)
RS3	A2	B2	C2	D2	A17	B17	C17	D17	(72)
RS4	A3	B3	C3	D3	A18	B18	C18	D18	(73)
RS5	A4	B4	C4	D4	A19	B19	C19	D19	(74)
RS6	A5	B5	C5	D5	A20	B20	C20	D20	(75)
RS7	A6	B6	C6	D6	A21	B21	C21	D21	(76)
RS8	A7	B7	C7	D7	A22	B22	C22	D22	(77)
RS9	A8	B8	C8	D8	A23	B23	C23	D23	(78)
RS10	A9	B9	C9	D9	A24	B24	C24	D24	(79)
RS11	A10	B10	C10	D10	A25	B25	C25	D25	(7A)
RS12	A11	B11	C11	D11	A26	B26	C26	D26	(7B)
RS13	A12	B12	C12	D12	A27	B27	C27	D27	(7C)
RS14	A13	B13	C13	D13	A28	B28	C28	D28	(7D)
RS15	A14	B14	C14	D14	A29	B29	C29	D29	(7E)
RS16	A15	B15	C15	D15	A30	B30	C30	D30	(7F)

Receive CAS Register 1...16

Each register except RS1 contains the received CAS bits for two time slots. The received CAS multiframe is compared with the previously received one. If the contents changed a CAS multiframe changed interrupt (ISR0.CASC) is generated and informs the user that a new multiframe has to be read within the next 2 ms. If requests for reading the RS1...16 register are ignored, the received data may be lost. RS1 contains frame 0 of the CAS multiframe. MSB is received first.

10 T1/J1 Registers

10.1 T1/J1 Control Register Addresses

Table 53 T1/J1 Control Register Address Arrangement

Address	Register	Type	Comment	Page
00	XFIFO	W	Transmit FIFO	261
01	XFIFO	W	Transmit FIFO	261
02	CMDR	W	Command Register	261
03	MODE	R/W	Mode Register	263
04	RAH1	R/W	Receive Address High 1	264
05	RAH2	R/W	Receive Address High 2	264
06	RAL1	R/W	Receive Address Low 1	264
07	RAL2	R/W	Receive Address Low 2	265
08	IPC	R/W	Interrupt Port Configuration	265
09	CCR1	R/W	Common Configuration Register 1	266
0A	CCR3	R/W	Common Configuration Register 3	268
0B	PRE	R/W	Preamble Register	269
0C	RTR1	R/W	Receive Timeslot Register 1	270
0D	RTR2	R/W	Receive Timeslot Register 2	270
0E	RTR3	R/W	Receive Timeslot Register 3	270
0F	RTR4	R/W	Receive Timeslot Register 4	270
10	TTR1	R/W	Transmit Timeslot Register 1	271
11	TTR2	R/W	Transmit Timeslot Register 2	271
12	TTR3	R/W	Transmit Timeslot Register 3	271
13	TTR4	R/W	Transmit Timeslot Register 4	271
14	IMR0	R/W	Interrupt Mask Register 0	272
15	IMR1	R/W	Interrupt Mask Register 1	272
16	IMR2	R/W	Interrupt Mask Register 2	272
17	IMR3	R/W	Interrupt Mask Register 3	272
18	IMR4	R/W	Interrupt Mask Register 4	272
19	IMR5	R/W	Interrupt Mask Register 5	272
1A	FMR0	R/W	Framer Mode Register 0	272

Table 53 T1/J1 Control Register Address Arrangement (cont'd)

Address	Register	Type	Comment	Page
1B	FMR1	R/W	Framer Mode Register 1	274
1C	FMR2	R/W	Framer Mode Register 2	276
1D	LOOP	R/W	Channel Loop Back Register	278
1E	FMR4	R/W	Framer Mode Register 4	279
1F	FMR5	R/W	Framer Mode Register 5	281
20	XC0	R/W	Transmit Control 0	283
21	XC1	R/W	Transmit Control 1	284
22	RC0	R/W	Receive Control 0	284
23	RC1	R/W	Receive Control 1	286
24	XPM0	R/W	Transmit Pulse Mask 0	288
25	XPM1	R/W	Transmit Pulse Mask 1	288
26	XPM2	R/W	Transmit Pulse Mask 2	288
29	IDLE	R/W	Idle Channel Code	289
2A	XDL1	R/W	Transmit DL-Bit Register 1	290
2B	XDL2	R/W	Transmit DL-Bit Register 2	290
2C	XDL3	R/W	Transmit DL-Bit Register 3	290
2D	CCB1	R/W	Clear Channel Register 1	290
2E	CCB2	R/W	Clear Channel Register 2	290
2F	CCB3	R/W	Clear Channel Register 3	290
30	ICB1	R/W	Idle Channel Register 1	291
31	ICB2	R/W	Idle Channel Register 2	291
32	ICB3	R/W	Idle Channel Register 3	291
34	LIM0	R/W	Line Interface Mode 0	291
35	LIM1	R/W	Line Interface Mode 1	293
36	PCD	R/W	Pulse Count Detection	294
37	PCR	R/W	Pulse Count Recovery	295
38	LIM2	R/W	Line Interface Register 2	295
39	LCR1	R/W	Loop Code Register 1	297
3A	LCR2	R/W	Loop Code Register 2	299
3B	LCR3	R/W	Loop Code Register 3	299

Table 53 T1/J1 Control Register Address Arrangement (cont'd)

Address	Register	Type	Comment	Page
3C	SIC1	R/W	System Interface Control 1	300
3D	SIC2	R/W	System Interface Control 2	301
3E	LIM3	R/W	Line Interface Register 3	302
40	SIC3	R/W	System Interface Control 3	303
60	DEC	W	Disable Error Counter	304
70	XS1	W	Transmit Signaling Register 1	305
71	XS2	W	Transmit Signaling Register 2	305
72	XS3	W	Transmit Signaling Register 3	305
73	XS4	W	Transmit Signaling Register 4	305
74	XS5	W	Transmit Signaling Register 5	305
75	XS6	W	Transmit Signaling Register 6	305
76	XS7	W	Transmit Signaling Register 7	305
77	XS8	W	Transmit Signaling Register 8	305
78	XS9	W	Transmit Signaling Register 9	305
79	XS10	W	Transmit Signaling Register 10	305
7A	XS11	W	Transmit Signaling Register 11	305
7B	XS12	W	Transmit Signaling Register 12	305

After 'RESET' all control registers except the XFIFO and XS1...12 are initialized to defined values.

Unused bits have to be cleared (set to logical '0').

10.2 Detailed Description of T1/J1 Control Registers

Transmit FIFO (Write)

	7		0	
XFIFO	XF7		XF0	(00/01)

Writing data to XFIFO can be done in 8-bit (byte) or 16-bit (word) access. The LSB is transmitted first.

Up to 32 bytes/16 words of transmit data can be written to the XFIFO following an XPR (or ALLS) interrupt.

Command Register (Write)

Value after RESET: 00_H

	7							0	
CMDR	RMC	RRES	XREP	XRES	XHF	XTF	XME	SRES	(02)

RMC… **Receive Message Complete**

Confirmation from CPU to FALC®-LH that the current frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

RRES… **Receiver Reset**

The receive line interface except the clock and data recovery unit (DPLL), the receive framer, the one second timer and the receive signaling controller are reset. However the contents of the control registers is not deleted. Receiver reset shall be done after every new device initialization.

XREP… **Transmission Repeat**

If XREP is set together with XTF (write 24H to CMDR), the FALC®-LH repeatedly transmits the contents of the XFIFO (1…32 bytes) without HDLC framing fully transparently, i.e. without FLAG,CRC.

The cyclic transmission is stopped with an SRES command or by resetting XREP.

Note:During cyclic transmission the XREP-bit has to be set with every write operation to CMDR.

XRES… **Transmitter Reset**

The transmit framer and transmit line interface excluding the pulse shaper is reset. However the contents of the control registers is not deleted. Transmitter reset shall be done after every new device initialization.

XHF… **Transmit HDLC Frame**

After having written up to 32 bytes to the XFIFO, this command initiates the transmission of a HDLC frame.

XTF… **Transmit Transparent Frame**

Initiates the transmission of a transparent frame without HDLC framing.

XME… **Transmit Message End**

Indicates that the data block written last to the transmit FIFO completes the current frame. The FALC®-LH can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

SRES… **Signaling Transmitter Reset**

The transmitter of the signaling controller is reset. XFIFO is cleared of any data and an abort sequence (seven 1's) followed by interframe time fill is transmitted. In response to XRES an XPR interrupt is generated. Signaling transmitter reset shall be done after every new device initialization.

This command can also be used by the CPU to abort a frame currently in transmission.

Note: The maximum time between writing to the CMDR register and the execution of the command takes 2.5 periods of the current system data rate. Therefore, if the CPU operates with a very high clock rate in comparison with the FALC®-LH's clock, it is recommended that bit SIS.CEC should be checked before writing to the CMDR register to avoid any loss of commands.

All bits except XREP are cleared automatically.

Mode Register (Read/Write)

Value after RESET: 00_H

	7							0	
MODE	MDS2	MDS1	MDS0	BRAC	HRAC				(03)

MDS2...0… **Mode Select**

The operating mode of the HDLC controller is selected.

000… Reserved
001… Reserved
010… 1 byte address comparison mode (RAL1, 2)
011… 2 byte address comparison mode (RAH1, 2 and RAL1, 2)
100… No address comparison
101… 1 byte address comparison mode (RAH1, 2)
110… Reserved
111… No HDLC framing mode 1

BRAC… **BOM Receiver Active**

Switches the BOM receiver to operational or inoperational state.

0… Receiver inactive

1… Receiver active

HRAC… **HDLC Receiver Active**

Switches the HDLC receiver to operational or inoperational state.

0… Receiver inactive
1… Receiver active

Receive Address Byte High Register 1 (Read/Write)
Value after RESET: FD_H

	7			1	0	
RAH1				0		(04)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individually programmable values in RAH1 and RAH2.

RAH1… **Value of the First Individual High Address Byte**
Bit 1 (C/R-bit) is excluded from address comparison.

Receive Address Byte High Register 2 (Read/Write)
Value after RESET: FF_H

	7					0	
RAH2							(05)

RAH2… Value of Second Individual High Address Byte

Receive Address Byte Low Register 1 (Read/Write)
Value after RESET: FF_H

	7					0	
RAL1							(06)

RAL1… Value of First Individual Low Address Byte

Receive Address Byte Low Register 2 (Read/Write)
Value after RESET: FF_H

	7						0	
RAL2								(07)

RAL2... **Value of the second individually programmable low address byte.**

Interrupt Port Configuration (Read/Write)
Value after RESET: 01_H

	7							0	
IPC	VIS					SCI	IC1	IC0	(08)

Unused bits have to be cleared.

VIS… **Masked Interrupts Visible**

0… Masked interrupt status bits are not visible
1… Masked interrupt status bits are visible

SCI… **Status Change Interrupt**

0… Interrupts ISR2.LOS, ISR2.AIS and ISR0.PDEN is generated only on the rising edge of the corresponding status flag.
1… Interrupts ISR2.LOS, ISR2.AIS and ISR0.PDEN is generated on the rising and falling edge of the corresponding status flag.

IC1...0… **Interrupt Port Configuration**

These bits define the function of the interrupt output stage (pin INT):

IOC1	IOC0	Function
X	0	Open drain output[1)]
0	1	Push/pull output, active low
1	1	Push/pull output, active high

[1)] an external pullup resistor is required at pin INT

Common Configuration Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
CCR1	SFLG	BRM	EDLX	EITS	ITF		RFT1	RFT0	(09)

SFLG… **Enable Shared Flags**

If this bit is set, the closing flag of a preceding HDLC frame simultaneously is used as the opening flag of the following frame.

0… Shared flag function disabled

1… Shared flag function enabled

BRM… **BOM Receive Mode (significant in BOM mode only)**

0… 10 byte packets

1… Continuous reception

EDLX… **Enable DL Bit Access via the Transmit FIFO**

A one in this bit position enables the internal DL-bit access via the receive/transmit FIFO of the signaling controller. FMR1.EDL has to be cleared.

EITS… **Enable Internal Time Slot 0-31 Signaling**

0… Internal signaling in time slots 0-31 defined via registers RTR1...4 or TTR1...4 is disabled.

1… Internal signaling in time slots 0-31 defined via registers RTR1...4 or TTR1...4 is enabled.

ITF… **Interframe Time Fill**

Determines the idle (= no data to send) state of the transmit data coming from the signaling controller.

0… Continuous logical ‘1’ is output

1… Continuous FLAG sequences are output (‘01111110’ bit patterns)

RFT1...0… **RFIFO Threshold Level**

The size of the accessible part of RFIFO can be determined by programming these bits. The number of valid bytes after an RPF interrupt is given in the following table:

RFT1	RFT0	Size of Accessible Part of RFIFO
0	0	32 bytes (RESET value)
0	1	16 bytes
1	0	4 bytes
1	1	2 bytes

The value of RFT 1,0 can be changed dynamically

– If reception is not running or

– after the current data block has been read, but before the command CMDR.RMC is issued (interrupt controlled data transfer).

*Note:It is seen that changing the value of RFT1,0 is possible even during the reception of one frame. The total length of the received frame can be always read directly in RBCL, RBCH after an RPF interrupt, except when the threshold is increased during reception of that frame. The real length can then be inferred by noting which bit positions in RBCL are reset by an RMC command (see **table below**):*

RFT1	RFT0	Bit Positions in RBCL Reset by a CMDR.RMC Command
0	0	RBC4 …. 0
0	1	RBC3 … 0
1	0	RBC1,0
1	1	RBC0

Common Configuration Register 3 (Read/Write)

Value after RESET: 00_H

	7							0	
CCR3	PRE1	PRE0	EPT	RADD		RCRC	XCRC		(0A)

Unused bits have to be cleared.

PRE1...0… **Number of Preamble Repetitions**

If preamble transmission is enabled, the preamble defined by register PRE is transmitted:

00... 1 time

01... 2 times

10... 4 times

11... 8 times

EPT… **Enable Preamble Transmission**

This bit enables transmission of preamble. The preamble is started after interframe timefill transmission has been stopped and a new frame is to be transmitted. The preamble consists of an 8-bit pattern repeated a number of times. The pattern is defined by register PRE, the number of repetitions is selected by bits PRE0 and PRE1.

Note: The 'Shared Flag' feature is not influenced by preamble transmission.
Zero bit insertion is disabled during preamble transmission.

RADD… **Receive Address Pushed to RFIFO**

If this bit is set, the received HDLC address information (1 or 2 bytes, depending on the address mode selected via MODE.MDS0) is pushed to RFIFO. See **Chapter 8.1** on page **169** for detailed description.

RCRC… **Receive CRC ON/OFF**

If this bit is set, the received CRC checksum is written to RFIFO (CRC-ITU-T: 2 bytes). The checksum, consisting of the 2 last bytes in the received frame, is followed in the RFIFO by the status information byte (contents of register RSIS). The received CRC checksum is additionally checked for correctness. If non-auto mode is selected, the limits for "Valid Frame" check are modified (refer to **RSIS.VFR** and to **Chapter 8.1** on page **169**).

XCRC… **Transmit CRC ON/OFF**

If this bit is set, the CRC checksum is not generated internally. It has to be written as the last two bytes in the transmit FIFO (XFIFO). The transmitted frame is closed automatically with a closing flag.

Note: The FALC®-LH does not check whether the length of the frame, i.e. the number of bytes to be transmitted makes sense or not.

Preamble Register (Read/Write)
Value after RESET: 00_H

	7						0	
PRE								(0B)

PRE0...7… **Preamble Register**

This register defines the pattern which is sent during preamble transmission (refer to CCR3). LSB is sent first.

Note: Zero bit insertion is disabled during preamble transmission.

Receive Timeslot Register 1...4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
RTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(0C)
RTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(0D)
RTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(0E)
RTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(0F)

TS0…TS31… **Timeslot Register**

These bits define the received time slots on the system highway port RDO to be extracted. Additionally these registers control the RSIGM marker which can be forced high during the respective time slots independently of bit CCR1.EITS.
A one in the RTR1...4 bits samples the corresponding time slot in the RFIFO of the signaling controller, if bit CCR1.EITS is set.

Assignments:
SIC1.SRSC = 0 : (SCLKR = 8.192 MHz)
TS0 → time slot 0
…

TS31 → time slot 31

SIC1.SRSC = 1 : (SCLKR = 1.544 MHz)
TS0 → time slot 1
…

TS23 → time slot 24

0 … normal operation.
1… The contents of the selected time slot is stored in the RFIFO. Although the idle time slots can be selected. This function is activated, if bit CCR1.EITS is set.
The corresponding time slot is forced high on pin RSIGM.

Transmit Timeslot Register 1...4 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
TTR1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7	(10)
TTR2	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	(11)
TTR3	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	(12)
TTR4	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	(13)

TS0…TS31… **Transmit Timeslot Register**

These bits define the transmit time slots on the system highway to be inserted. Additionally these registers control the XSIGM marker which can be forced high during the respective time slots independently of bit CCR1.EITS.
A one in the TTR1...4 bits inserts the corresponding time slot sourced by the XFIFO in the data received on pin XDI, if bit CCR1.EITS is set. If SIC3.TTRF is set and CCR1.EDLX/EITS=00, insertion of data received on port XSIG is controlled by this registers.

Assignments:
SIC1.SRSC = 0 : (SCLKR = 8.192 MHz)
TS0 → time slot 0
…

TS31 → time slot 31

SIC1.SRSC = 1 : (SCLKR = 1.544 MHz)
TS0 → time slot 1
…

TS23 → time slot 24

0 … normal operation

1… The contents of the selected time slot is inserted into the outgoing data stream from XFIFO. This function is activated only, if bit CCR1.EITS is set.
The corresponding time slot is forced high on marker pin XSIGM.

Interrupt Mask Register 0...5

Value after RESET: FF_H, FF_H, FF_H, FF_H,FF_H

	7							0	
IMR0	RME	RFS	ISF	RMB	RSC	CRC6	PDEN	RPF	(14)
IMR1	CASE	RDO	ALLS	XDU	XMB		XLSC	XPR	(15)
IMR2	FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA	(16)
IMR3	ES	SEC	XSLP		LLBSC		RSN	RSP	(17)
IMR4	LFA	FER	CER	AIS	LOS	CVE	SLIP		(18)
IMR5	XSP	XSN							(19)

IMR0...5... **Interrupt Mask Register**

Each interrupt source can generate an interrupt signal on port INT (characteristics of the output stage are defined via register IPC). A ‘1’ in a bit position of IMR0…5 sets the mask active for the interrupt status in ISR0…3 and ISR5. Masked interrupt statuses neither generate a signal on INT, nor are they visible in register GIS. Moreover, they are

– not displayed in the Interrupt Status Register if bit IPC.VIS is cleared

– displayed in the Interrupt Status Register if bit IPC.VIS is set.

After RESET, all interrupts are **dis**abled.

Framer Mode Register 0 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR0	XC1	XC0	RC1	RC0	FRS	SRAF	EXLS	SIM	(1A)

XC1…0… **Transmit Code**

Serial code transmitter is independent to the receiver.

00… NRZ (optical interface)
01… Not assigned

10…AMI coding with Zero Code Suppression (ZCS, B7-Stuffing). Disabling of the ZCS is done by activating the clear channel mode via register CCB1...3. (ternary or digital interface)

11…B8ZS Code (ternary or digital dual rail interface)

RC1…0… **Receive Code**

Serial code receiver is independent to the transmitter.

00… NRZ (optical interface)
01… Not assigned
10… AMI coding (ternary or digital dual rail interface)
11… B8ZS Code (ternary or digital dual rail interface)

FRS… **Force Resynchronization**

A transition from low to high forces the frame aligner to execute a resynchronization of the pulse frame. In the asynchronous state, a new frame position is assumed at the next candidate if there is one. Otherwise, a new frame search with the meaning of a general reset is started. In the synchronous state this bit has the same meaning as bit FMR0.EXLS except if FMR2.MCSP=1. This bit is not reset automatically.

SRAF… **Select Remote (Yellow) Alarm Format for F12 and ESF Format**

0… F12: bit2 = 0 in every channel. ESF: pattern '1111 1111 0000 0000…' in data link channel.
1… F12: FS bit of frame 12. ESF: bit2 = 0 in every channel

EXLS… **External Loss Of Frame**

With a low to high transition a new frame search is started. This has the meaning of a general reset of the internal frame alignment unit. Synchronous state is reached only if there is one definite framing candidate. In the case of multiple candidates, the setting of the bit FMR0.FRS forces the receiver to lock onto the next available framing position. This bit is not reset automatically.

SIM… **Alarm Simulation**

Setting/resetting this bit initiates internal error simulation of: AIS (blue alarm), loss of signal (red alarm), loss of frame alignment, remote (yellow) alarm, slip, framing errors, CRC errors, code violations. The error counters FEC, CVC, CEC, EBC are incremented.

The selection of simulated alarms is done via the error simulation counter: FRS2.ESC2...0 which are incremented with each setting of bit FMR0.SIM. For complete checking of the alarm indications eight

simulation steps are necessary (FRS2.ESC2...0 = 0 after a complete simulation).

Framer Mode Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR1	CTM	SIGM	EDL	PMOD	CRC	ECM	IMOD	XAIS	(1B)

CTM… **Channel Translation Mode**

0… Channel translation mode 0

1… Channel translation mode 1

See **Table 26** on page **113** for details.

SIGM… **Select Signaling Mode**

0… Normal operation (no bit-robbing).

1… CAS Bit-robbing mode selected

Note: Bit FMR5.EIBR has also to be set, if bit-robbing mode is to be used.

EDL… **Enable DL-Bit Access via Register XDL1...3**

Only applicable in F4, F24 or F72 frame format.

0… Normal operation. The DL-bits are taken from system highway or if enabled via CCR1.EDLX from the XFIFO of the signaling controller.

1… DL-bit register access. The DL-bit information is taken from the registers XDL1...3 and overwrites the DL-bits received at the system highway (pin XDI) or the internal XFIFO of the signaling controller. However, transmitting contents of registers XDL1...3 is disabled if transparent mode is enabled (FMR4.TM).

PMOD… **PCM Mode**

For T1/J1 applications this bit must be set high. Switching into T1/J1 mode the device needs up to 10 µs to settle up to the internal clocking.

0… PCM 30 or E1 mode.

1… PCM 24 or T1/J1 mode.

CRC… **Enable CRC6**

This bit is only significant when using the ESF format.

0… CRC6 check/generation disabled. For transmit direction, all CRC bit positions are set.

1… CRC6 check/generation enabled.

ECM… **Error Counter Mode**

The function of the error counters (FEC,CEC,CVC,EBC) is determined by this bit.

0… Before reading an error counter the corresponding bit in the Disable Error Counter register (DEC) has to be set. In 8 bit access the low byte of the error counter should always be read before the high byte. The error counters are reset with the rising edge of the corresponding bits in the DEC register.

1… Every second the error counter is latched and then automatically be reset. The latched error counter state should be read within the next second. Reading the error counter during updating should be avoided (do not access an error counter within 2 µs before or after the one-second interrupt occurs).

IMOD… **System Interface Mode**

0…4.096 Mbit/s

1…2.048 Mbit/s or 1.544 Mbit/s

This bit has to be set if SIC1.SRSC or SIC1.SXSC are set.

XAIS… **Transmit AIS Towards Remote End**

Sends AIS (blue alarm) via ports: XL1, XL2 towards the remote end.

If Local Loop Mode is enabled the transmitted data is looped back to the system internal highway without any changes.

Framer Mode Register 2 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR2		MCSP	SSP	DAIS	SAIS	PLB	AXRA	EXZE	(1C)

MCSP… **Multiple Candidates Synchronization Procedure**

SSP… **Select Synchronization/Resynchronization Procedure**

Together with bit FMR2.SSP the synchronization mode of the receive framer is defined:

MCSP/SSP:

00… F12/72 format:
Specified number of errors in both FT framing and FS framing lead to loss of sync (FRS0.LFA is set). In the case of FS bit framing errors, bit FRS0.LMFA is set additionally. A complete new synchronization procedure is initiated to regain pulseframe alignment and then multiframe alignment.

F24:
normal operation: synchronization is achieved only on verification the framing pattern.

01… F12/72:
Specified number of errors in FT framing has the same effect as above. Specified number of errors in FS framing only initiates a new search for multiframe alignment without influencing pulseframe synchronous state (FRS0.LMFA is set).

F24:
Synchronous state is reached when three consecutive multiframe pattern are correctly found independent of the occurrence of CRC6 errors.

10… F24:
A one enables a synchronization mode which is able to choose multiple framing pattern candidates step by step. I.e. if in synchronous state the CRC error counter indicates that the synchronization might have been based on an alias framing pattern, setting of FMR0.FRS leads to synchronization on the next candidate available. However, only the previously assumed candidate is discarded in the internal framing pattern memory. The latter procedure can be repeated until the

framer has locked on the right pattern (no extensive CRC errors). Therefor bit FMR1.CRC must be set.

11… F24:
Synchronization is achieved on verification of the framing pattern **and** the CRC6 bits. Synchronous state is reached when framing pattern and CRC6 checksum are correctly found. For correct operation the CRC check must be enabled by setting bit FMR1.CRC6.

DAIS… Disable AIS to System Interface

0… AIS is automatically inserted into the data stream to RDO if FALC®-LH is in asynchronous state.

1… Automatic AIS insertion is disabled. Furthermore, AIS insertion can be initiated by programming bit FMR2.SAIS.

SAIS… Send AIS Towards System Interface

Sends AIS (blue alarm) via output RDO towards system interface. This function is not influenced by bit FMR2.DAIS.

PLB… Payload Loop Back

0 … Normal operation. Payload loop is disabled.

1… The payload loopback loops the data stream from the receiver section back to transmitter section. Looped data is output on pin RDO. Data received on port XDI, XSIG, SYPX and XMFS are ignored. With FMR4.TM=1 all 193 bits per frame are looped back. If FMR4.TM=0 the DL- or FS- or CRC-bits are generated internally. AIS is sent immediately on port RDO by setting the FMR2.SAIS bit. During payload loop is active the receive time slot offset (registers RC1...0) should not be changed. It is recommended to write the actual value of XC1 into this register once again, because a write access to register XC1 sets the read/write pointer of the transmit elastic buffer into its optimal position to ensure a maximum wander compensation (the write operation forces a slip).

AXRA… Automatic Transmit Remote Alarm

0 … Normal operation

1… The remote alarm (yellow alarm) bit is set automatically in the outgoing data stream if the receiver is in asynchronous state (FRS0.LFA bit is set). In synchronous state the remote alarm bit is reset.

EXZE… **Excessive Zeros Detection Enable**

Selects error detection mode in the bipolar receive bit stream.

0… Only bipolar violations are detected.

1… Bipolar violations and zero strings of 8 or more contiguous zeros in B8ZS code or more than 15 contiguous zeros in AMI code are detected additionally and counted in the code violation counter CVC.

Channel Loop Back Register (Read/Write)

Value after RESET: 00_H

	7							0	
LOOP	SPN	RTM	ECLB	CLA4	CLA3	CLA2	CLA1	CLA0	(1D)

SPN… **Select Additional Optical Pin Functions**

Together with bit LIM3.ESY the functionality of pin 80 is defined:

Programming of LOOP.SPN and LIM3.ESY and the corresponding pin function is shown below.

SPN/ESY:

00… function of pin 80 XSIG: If SIC3.TTRF = 1, transmit data from the system interface. Internal multiplexing with the XDI data stream is controlled by XSIGM. No input function defined for SIC3.TTRF = 0.

01… function of pin 80 SYNC2: external synchronization input for the DCO-X circuitry

10… function of pin 80 ROID: Receive Optical Interface Data (Input) and Pin 68: XMFB/**XOID** Transmit Optical Interface Data (Output). At the same time data received on pin 2 are ignored, data on pin XOID (pin 15) are undefined. Transmit data is clocked off with the positive transition of XCLK. After Reset the transmit multiframe begin marker is output on pin 68.

11… function of pin 80 XSIG: The signaling information from the transmit system interface is received on pin XSIG. Bit FMR5.EIBR should be cleared to disable internal signaling access from registers XS1...12. The signaling information from the line interface is transmitted on pin RSIG.

RTM… **Receive Transparent Mode**

Setting this bit disconnects control of the internal elastic store from the receiver. The elastic store is now in a “free running” mode without any possibility to update the time slot assignment to a new frame position in case of re-synchronization of the receiver. This function can be used in conjunction with the “disable AIS to system interface” feature (FMR2.DAIS) to realize undisturbed transparent reception.
This bit should be enabled in case of unframed data reception mode. After resetting RTM to 0, the elastic buffer is adjusted after the next resynchronization.

ECLB… **Enable Channel Loop Back**

0… Disables the channel loop back.

1… Enables the channel loop back selected by this register.

CLA4…0… **Channel Address For Loop Back**

CLA = 1…24 selects the channel.

During loop back, the contents of the associated outgoing channel on ports XL1/XDOP/XOID and XL2/XDON is equal to the idle channel code programmed in register IDLE.

Framer Mode Register 4 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR4	AIS3	TM	XRA	SSC1	SSC0	AUTO	FM1	FM0	(1E)

AIS3… **Select AIS Condition**

0… AIS (blue alarm) is indicated (FRS0.AIS) when two or less zeros in the received bit stream are detected in a time interval of 12 frames (F4, F12, F72) or 24 frames (ESF).

1… AIS (blue alarm) detection is only enabled when FALC®-LH is in asynchronous state. The alarm is indicated (FRS0.AIS) when

– three or less zeros within a time interval of 12 frames (F4, F12, F72), or

– five or less zeros within a time interval of 24 frames (ESF) are detected in the received bit stream.

TM… **Transparent Mode**

Setting this bit enables the transparent mode:

In transmit direction bit 8 of every FS/DL time slot from the system internal highway (XDI) is inserted in the F-bit position of the outgoing frame. Internal framing generation, insertion of CRC and DL data is disabled.

In receive direction the framing bit is also forwarded to RDO and inserted into the FS/DL time slot. Bit RDCF (bit 1 of FS/DL time slot) indicates a DL bit.

XRA… **Transmit Remote Alarm (Yellow Alarm)**

If high, remote alarm is sent via PCM route. Clearing the bit removes the remote alarm pattern. Remote alarm indication depends on the multiframe structure as follows:

F4: bit2 = 0 in every speech channel
F12: FMR0.SRAF = 0: bit2 = 0 in every speech channel
FMR0.SRAF = 1: FS-bit of frame 12 is forced to ‘1’
ESF: FMR0.SRAF = 0:
pattern ‘1111111100000000 11111111000…’
in data link channel
FMR0.SRAF = 1: bit2 = 0 in every speech channel
F72: bit2 = 0 in every speech channel

SSC1...0… **Select Sync Conditions**

Loss of Frame Alignment (FRS0.LFA or opt. FRS0.LMFA) is declared if
00 = 2 out of 4 framing bits
01 = 2 out of 5 framing bits
10 = 2 out of 6 framing bits in F4/12/72 format
10 = 2 out of 6 framing bits per multiframe period in ESF format
11 = 4 consecutive multiframe pattern in ESF format
are incorrect. It depends on the selected multiframe format and optionally on bit FMR2.SSP which framing bits are observed:

F4: FT bits → FRS0.LFA
F12, F72: SSP = 0: FT bits → FRS0.LFA: FS bits → FRS0.LFA
and FRS0.LMFA SSP = 1:FT → FRS0.LFA
FS → FRS0.LMFA
ESF: ESF framing bits → FRS0.LFA

AUTO… **Enable Auto Resynchronization**

0… The receiver does not resynchronize automatically. Starting a new synchronization procedure is possible via the bits: FMR0.EXLS or FMR0.FRS.

1… Auto-resynchronization is enabled.

FM1…0… **Select Frame Mode**

FM = 0: 12-frame multiframe format (F12, D3/4)
FM = 1: 4-frame multiframe format (F4)
FM = 2: 24-frame multiframe format (ESF)
FM = 3: 72-frame multiframe format (F72, remote switch mode)

Framer Mode Register 5 (Read/Write)

Value after RESET: 00_H

	7							0	
FMR5	SRS	EIBR	XLD	XLU	SRO	XTM	RTF		(1F)

SRS… **Signaling Register SIze**

Valid in F12/F72 frame format only

0… Signaling access is done via registers RS/XS1...6

1… Signaling access is done via increased register bank RS/XS1...12

EIBR… **Enable Internal Bit-Robbing Access**

0… Normal operation (no bit-robbing).

1… CAS Bit-robbing mode selected

Note: Bit FMR1.SIGM has also to be set, if bit-robbing mode is to be used.

XLD… **Transmit Line Loopback (LLB) Down Code**

0… Normal operation.

1… A one in this bit position causes the transmitter to replace normal transmit data with the LLB down (deactivate) code continuously until this bit is reset. The LLB down code is optionally overwritten by the framing/DL/CRC bits. For correct operation bit FMR5.XLU must be cleared

XLU… **Transmit LLB UP Code**

0… Normal operation.

1… A one in this bit position causes the transmitter to replace normal transmit data with the LLB UP (activate) Code continuously until this bit is reset. The LLB UP Code is optionally overwritten by the framing/DL/CRC bits. For correct operation bit FMR5.XLD must be cleared.

SRO… **Signaling Register Organization**

Valid in F12/F72 and ESF frame format only

0… Signaling access via registers RS/XS1...12 is done without reordering of ABCD bits.

1… Signaling access via registers RS/XS1...12 is done with reordering of ABCD bits.

For details see description of registers XS1...12 on page **305** and RS1...12 on page **333**

XTM… **Transmit Transparent Mode**

Valid if loop-timed mode is enabled (LIM2.ELT = 1).

0…Ports $\overline{\text{SYPX}}$/XMFS define the frame/multiframe begin on the transmit system highway. The transmitter is usually synchronized on this externally sourced frame boundary and generates the FAS bits according to this framing. Any change of the transmit time slot assignment or a transmit slip subsequently produces a change of the FAS bit positions.

1… Disconnects the control of the transmit system interface from the transmitter. The transmitter is now in a free running mode without any possibility to update the multiframe position. The framing (FAS bits) generated by the transmitter is not disturbed (in case of changing the transmit time slot assignment or transmit slip) by the transmit system highway unless register XC1 is written. Useful in loop-timed applications. For correct operation the transmit elastic buffer (2 frames, SIC1.XBS1/0= 10) has to be enabled

RTF… **Receive Transparent Forwarding**

Setting this bit all 193 bits per frame of the incoming multiframe are forwarded to pin RDO transparently. In asynchronous state the received data may be transparently switched through if bit FMR2.DAIS is set.

Transmit Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
XC0	BRM	MFBS		SFRZ		XCO2	XCO1	XCO0	(20)

BRM… **Enable Bit-Robbing Marker**

A one in this bit marks the robbed bit positions on the system highway. RSIGM marks the receive and XSIGM marks the transmit robbed bits. For correct operation bit FMR1.SIGM must be set.

MFBS… **Enable pure Multiframe Begin Signals**

Valid only if ESF or F72 format is selected.

If set, signals RMFB and XMFB indicate only the multiframe begin. Additional pulses (every 12 frames) are disabled.

SFRZ… **Select Freeze Output**

0… Signal $\overline{\text{RFSP}}$ is output on port $\overline{\text{RFSP}}$/FREEZS

1… Freeze status signal is output on port $\overline{\text{RFSP}}$/FREEZS

XCO2…XCO0… **Transmit Clock Slot Offset**

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse on port $\overline{\text{SYPX}}$ is active. Setting of SIC1.SXSC enforces programming the offset values in the range of 0 to 192 bits with XCO0 always cleared.

Transmit Control 1 (Read/Write)

Value after RESET: 00_H

	7							0	
XC1	XCOS		XTO5	XTO4	XTO3	XTO2	XTO1	XTO0	(21)

A write access to this address resets the transmit elastic buffer to its basic starting position. Therefore, updating of the value should only be done when the FALC®-LH is initialized or when the buffer should be centered. As a consequence a transmit slip occurs.

XCOS… Transmit Clock Offset Shift

Valid only if SIC1.SXSC = 0

0… The delay T between the beginning of time slot 0 and the initial edge of SCLKX (after $\overline{\text{SYPX}}$ goes active) is an even number in the range of 0 to 1022 SCLKX cycles.

1… The delay T is an odd number in the range of 1 to 1023 SCLKX cycles.

XTO5…XTO0… Transmit Time Slot Offset

Initial value loaded into the transmit bit counter at the trigger edge of SCLKX when the synchronous pulse on port $\overline{\text{SYPX}}$ is active. Setting of SIC1.SXSC enforces programming the offset values in the range of 0 to 192 bits.

Receive Control 0 (Read/Write)

Value after RESET: 00_H

	7							0	
RC0	RCOS	SICS	CRCI	XCRCI	RDIS	RCO2	RCO1	RCO0	(22)

RCOS… Receive Clock Offset

Valid only if SIC1.SXSC = 0

0… The delay T between the beginning of time slot 0 and the initial edge of SCLKR (after $\overline{\text{SYPX}}$ goes active) is an even number in the range of 0 to 1022 SCLKX cycles.

1… The delay T is an odd number in the range of 1 to 1023 SCLKX cycles.

SICS… **System Interface Channel Select**

Applicable only if bit FMR1.IMOD (4-MHz system interface) is cleared.

0… Received data is output on port RDO in the first channel phase. Data in the second channel phase is tristated.

Data on pin XDI is sampled in the first channel phase only. Data in the second channel phase is ignored.

1… Received data is output on port RDO in the second channel phase. Data in the first channel phase is tristated.

Data on pin XDI is sampled in the second channel phase only. Data in the first channel phase is ignored.

CRCI… **Automatic CRC6 Bit Inversion**

If set, all CRC bits of one outgoing extended multiframe are inverted in case a CRC error is flagged for the previous received multiframe. This function is logically ORed with RC0.XCRCI.

XCRCI… **Transmit CRC6 Bit Inversion**

If set, the CRC bits in the outgoing data stream are inverted before transmission. This function is logically ORed with RC0.CRCI.

RDIS… **Receive Data Input Sense**

Only applicable for dual rail mode (LIM1.DRS = 1).

0… Inputs: RDIP, RDIN active low, input ROID is active high

1… Inputs: RDIP, RDIN active high, input ROID is active low

RCO2…RCO0… **Receive Offset/Receive Frame Marker Offset**

Depending on bit SIC2.SRFSO this bit enables different functions:

Receive Clock-Slot Offset (SIC2.SRFSO = 0)
Initial value loaded into the receive bit counter at the trigger edge of SCLKR when the synchronous pulse on port $\overline{\text{SYPR}}$ is active. Setting of SIC1.SRSC enforces programming the offset values in a range of 0 to 192 bits with RCO0 always cleared.

Receive Frame Marker Offset (SIC2.SRFSO = 1)

Offset programming of the receive frame marker which is output on port $\overline{\text{SYPR}}$. The receive frame marker could be activated during any bit position of the current frame.

Calculation of the value X of the “Receive Counter Offset” register RC1/0 depends on the bit position BP which should be marked and SCLKR: **X = (2BP) mod 386**, for SCLKR = 1.544 MHz

Receive Control 1 (Read/Write)

Value after RESET: 00_H

	7							0	
RC1	SJR	RRAM	RTO5	RTO4	RTO3	RTO2	RTO1	RTO0	(23)

SJR… **Select Japanese ITU-T Requirements for ESF format**

0… Alarm handling and CRC6 generation/checking is done according ITU-T G. 704+706

1… Alarm handling and CRC6 generation/checking is done according ITU-T JG. 704 + 706

See **Table 48 "Framer Initialization (T1/J1)" on page 166** for more details.

RRAM… **Receive Remote Alarm Mode**

The conditions for remote (yellow) alarm (FRS0.RRA) detection can be selected via this bit to allow detection even in the presence of BER 10**-3:

RRAM = 0

Detection

F4: bit2 = 0 in every speech channel per frame.

F12: FMR0.SRAF = 0: bit2 = 0 in every speech channel per frame.
FMR0.SRAF = 1: S-bit of frame 12 is forced to ‘1’

ESF: FMR0.SRAF = 0: pattern ‘1111 1111 0000 0000…’ in data link channel
FMR0.SRAF = 1: bit2 = 0 in every speech channel

F72: bit2 = 0 in every speech channel per frame.

Release

The alarm is reset when above conditions are no longer detected.

RRAM = 1

Detection

F4: bit2 = 0 in 255 consecutive speech channels.

F12: FMR0.SRAF = 0: bit 2 = 0 in 255 consecutive speech channels.
FMR0.SRAF = 1: S-bit of frame 12 is forced to ‘1’

ESF: FMR0.SRAF = 0: pattern ‘1111 1111 0000 0000…’ in data link channel
FMR0.SRAF = 1: bit 2 = 0 in 255 consecutive speech channels

F72: bit 2 = 0 in 255 consecutive speech channels.

Release:
Depending on the selected multiframe format the alarm is reset when FALC-LH does not detect

- the ‘bit 2 = 0’ condition for three consecutive pulse frames (all formats if selected),
- the ‘FS bit’ condition for three consecutive multiframes (F12),
- the ‘DL pattern’ for three times in a row (ESF).

RTO5…RTO0… **Receive Time-Slot Offset/Receive Frame Marker Offset**

Depending on bit SIC2.SRFSO this bit enables different functions:

Receive Time-Slot Offset (SIC2.SRFSO = 0)
Initial value which is loaded into the receive time-slot counter at the trigger edge of SCLKR when the synchronous pulse on port $\overline{\text{SYPR}}$ is active. Setting of SIC1.SRSC enforces programming the offset values in a range of 0 to 192 bits.

Receive Frame Marker Offset (SIC2.SRFSO = 1)

Offset programming of the receive frame marker which is output on port $\overline{\text{SYPR}}$. The receive frame marker could be activated during any bit position of the current frame.

Calculation of the value X of the “Receive Counter Offset” register RC1/0 depends on the bit position BP which should be marked and SCLKR:
X = (2BP) mod 386, for SCLKR = 1.544 MHz

Transmit Pulse-Mask 2…0 (Read/Write)

Value after RESET: $9C_H$, 03_H, 00_H

	7							0	
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00	(24)
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13	(25)
XPM2	XLHP	XLT	DAXLT		XP34	XP33	XP32	XP31	(26)

The transmit pulse shape which is defined in ANSI T1. 102 is output on pins XL1 and XL2. The level of the pulse shape can be programmed via registers XPM2...0 to create a custom waveform. In order to get an optimized pulse shape for the external transformers each pulse shape is divided internally into four sub pulse shapes. In each sub pulse shape a programmed 5 bit value defines the level of the analog voltage on pins XL1/2. Together four 5 bit values have to be programmed to form one complete transmit pulse shape.The four 5 bit values are sent in the following sequence:

XP04-00: First pulse shape level
XP14-10: Second pulse shape level
XP24-20: Third pulse shape level
XP34-30: Fourth pulse shape level

Changing the LSB of each subpulse in registers XPM2...0 changes the amplitude of the differential voltage on XL1/2 by approximately 110 mV.
The XPM-values in the following table are based on simulations. They are valid for the following external circuitry: transformer ratio: 1: $\sqrt{2}$; cable: PULB 22AWG (100 Ω); serial resistors: 5 Ω. Adjustment of these coefficients may be necessary for other external conditions.

Table 54 Pulse Shaper Programming (T1/J1)

Range in m	Range in ft.	XPM0	XPM1	XPM2	XP04-XP00	XP14-XP10	XP24-XP20	XP34-XP30
		hexadecimal			decimal			
0...40	0...133	19	9B	01	25	24	6	3
40...81	133...266	5B	9F	01	27	26	7	3
81...122	266...399	7D	AB	01	29	27	10	3
122...162	399...533	7F	B7	01	31	27	13	3
162...200	533...655	5F	BB	01	31	26	14	3

XLHP… **Transmit Line High Power**

With this bit the output current capability of transmit lines XL1/XL2 is increased. According to the DC characteristics, this bit has to be set, if an output current of more than 60 mA is required.

0… Output current low

1… output current high

For absolute values see DC Characteristics.

XLT... **Transmit Line Tristate**

0 … Normal operation

1 … Transmit line XL1/XL2 or XDOP/XDON are switched into high impedance state. If this bit is set the transmit line monitor status information is frozen.

DAXLT... **Disable Automatic Tristating of XL1/2**

0... Normal operation. If a short is detected on pins XL1/2 the transmit line monitor sets the XL1/2 outputs into a high impedance state.

1... If a short is detected on pins XL1/2 an automatic setting these pins into a high impedance state (by the XL-monitor) is disabled.

Idle Channel Code Register (Read/Write)

Value after RESET: 00_H

	7						0	
IDLE	IDL7						IDL0	(29)

IDL7…IDL0… **Idle Channel Code**

If channel loop back is enabled by programming the register LOOP.ECLB = 1, the contents of the assigned outgoing channel on ports XL1/XL2 respective XDOP/XDON is set equal to the idle channel code selected by this register.

Additionally, the specified pattern overwrites the contents of all channels of the outgoing PCM frame selected via the idle channel registers ICB1…ICB3. IDL7 is transmitted first.

Transmit DL-Bit Register 1...3 (Read/Write)

Value after RESET: 00_H, 00_H, 00_H

	7							0	
XDL1	XDL17	XDL16	XDL15	XDL14	XDL13	XDL12	XDL11	XDL10	(2A)
XDL2	XDL27	XDL26	XDL25	XDL24	XDL23	XDL22	XDL21	XDL20	(2B)
XDL3	XDL37	XDL36	XDL35	XDL34	XDL33	XDL32	XDL31	XDL30	(2C)

XDL1…XDL3… **Transmit FS/DL-Bit Data**

The DL-bit register access is enabled by setting bits FMR1.EDL = 1. With the transmit multiframe begin an interrupt ISR1.XMB is generated and the contents of these registers XDL1...3 is copied into a shadow register. The contents is sent out subsequently in the data stream of the next outgoing multiframe if no transparent mode is enabled. XDL10 is sent out first.
In F4 frame format only XDL10...11 are transmitted. In F24 frame format XDL10...23 are shifted out. In F72 frame format XDL10...37 are transmitted.
The transmit multiframe begin interrupt (XMB) requests that these registers should be serviced. If requests for new information are ignored, current contents is repeated.

Clear Channel Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H

	7							0	
CCB1	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	(2D)
CCB2	CH9	CH10	CH11	CH12	CH13	CH14	CH15	CH16	(2E)
CCB3	CH17	CH18	CH19	CH20	CH21	CH22	CH23	CH24	(2F)

CH1…CH24… **Channel Selection Bits**

0… Normal operation. Bit-robbing information and Zero Code Suppression (ZCS, B7 stuffing) may change contents of the selected speech/data channel if assigned modes are enabled via bits FMR5.EIBR and FMR0.XC1/0.

1… Clear channel mode. Contents of selected speech/data channel is not overwritten by internal or external bit-robbing and

ZCS information. Transmission of channel assigned signaling and control of pulse density is applied by the user.

Idle Channel Register (Read/Write)

Value after RESET: 00_H, 00_H, 00_H, 00_H

	7							0	
ICB1	IC1	IC2	IC3	IC4	IC5	IC6	IC7	IC8	(30)
ICB2	IC9	IC10	IC11	IC12	IC13	IC14	IC15	IC16	(31)
ICB3	IC17	IC18	IC19	IC20	IC21	IC22	IC23	IC24	(32)

IC1…IC24… **Idle Channel Selection Bits**

These bits define the channels (time slots) of the outgoing PCM frame to be altered.

0… Normal operation.

1… Idle channel mode. The contents of the selected channel is overwritten by the idle channel code defined via register IDLE.

Line Interface Mode 0 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM0	XFB	XDOS	SCL1	SCL0	EQON	ELOS	LL	MAS	(34)

XFB… **Transmit Full Bauded Mode**

Only applicable for dual rail mode (bit LIM1.DRS = 1).

0…Output signals XDOP/XDON are half bauded (normal operation).

1…Output signals XDOP/XDON are full bauded.

XDOS… **Transmit Data Out Sense**

Only applicable for dual rail mode (bit LIM1.DRS = 1)

0… Output signals XDOP/XDON are active low. Output XOID is active high (normal operation).

1… Output signals XDOP/XDON are active high. Output XOID is active low.

SCL1...0… **Select Clock Output**

00… Output frequency on pin CLKX is 2048 kHz active high.

01… Output frequency on pin CLKX is 2048 kHz active low.

10… Output frequency on pin CLKX is 4096 kHz active high.

11… Output frequency on pin CLKX is 4096 kHz active low.

EQON… **Receive Equalizer On**

0… -10 dB Receiver: short haul mode

1… -36 dB Receiver: long haul mode

ELOS… **Enable Loss of Signal**

0… Normal operation, the extracted receive clock is output on pin RCLK

1… During of loss of signal (FRS0.LOS = 1) output RCLK is set high.

LL… **Local Loop**

0 … Normal operation

1 … Local loop active. The local loopback mode disconnects the receive lines RL1/RL2 (RDIP/RDIN, respectively) from the receiver. Data provided by system interface is routed back to the system interface. The transmitted data is not affected. Receiver and transmitter coding must be identical. Operates in analog and digital line interface mode. In analog line interface mode data is looped through the complete analog receiver.

MAS… **Master Mode**

0 … Slave mode

1 … Master mode on. If this bit is set and the SYNC pin is connected to V_{SS} the FALC-LH works as a master for the system. The internal DCO's of the jitter attenuator are centered and the system clocks which are output via CLK8M/CLKX are stable (divided from the DCO frequencies). If a clock (1.544 MHz or 2.048 MHz) is detected at the SYNC pin the FALC-LH synchronizes automatically to this clock. The production tolerance is approximately ± 30 ppm of the crystal frequency if C_{Load} = 15 pF.

Line Interface Mode 1 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM1	EFSC	RIL2	RIL1	RIL0	DCOC	JATT	RL	DRS	(35)

EFSC… **Enable Frame Synchronization Pulse**

0… The transmit clock is output on pin XCLK

1… Pin XCLK provides an 8 kHz frame synchronization pulse which is active for one 2.048-MHz cycle (488 ns)

RIL2…RIL0… **Receive Input Threshold**

Only valid if analog line interface and short haul mode is selected (LIM1.DRS=0 and LIM1.EQON = 0).

No signal is declared if the voltage between pins RL1 and RL2 drops below the limits programmed via bits RIL2...0 and the received data stream has no transition for a period defined in the PCD register.

The threshold where no signal is declared is programmable via the RIL2...0 bits. See **Table 58 "DC Parameters" on page 336** for details.

Note: LIM1.RIL(2:0) must be programmed before LIM0.EQON = 1 is set.

DCOC … **DCO-R and DCO-X Control**

0… 1.544-MHz reference clock for the DCO-R/DCO-X circuitry provided on pin SYNC/SYNC2.

1… 2.048-MHz reference clock for the DCO-R/DCO-X circuitry provided on pin SYNC/SYNC2.

JATT…RL... **Transmit Jitter Attenuator/Remote Loop**

00 = Normal operation. The transmit jitter attenuator is disabled. Transmit data bypasses the buffer.

01 = Remote Loop active without transmit jitter attenuator enabled. Transmit data bypasses the buffer.

10 = not assigned

11 = Remote Loop and jitter attenuator active. Received data from pins RL1/2 or RDIP/N or ROID is sent 'jitter free' on ports XL1/2 or XDOP/N or XOID. The dejittered clock is generated by the DCO-X circuitry.

DRS… **Dual Rail Select**

0 = The ternary interface is selected. Multifunction ports RL1/2 and XL1/2 become analog in/outputs.

1 = The digital dual rail interface is selected. Received data is latched on multifunction ports RDIP/RDIN while transmit data is output on pins XDOP/XDON.

Pulse Count Detection Register (Read/Write)

Value after RESET: 00_H

	7		0	
PCD	PCD7		PCD0	(36)

PCD7…PCD0… **Pulse Count Detection**

A LOS alarm (red alarm) is detected if the incoming data stream has no transitions for a programmable number T consecutive pulse positions. The number T is programmable via the PCD register and can be calculated as follows:
$T = 16(N+1)$; with $0 \leq N \leq 255$.

The maximum time is: $256 \times 16 \times 648$ ns = 2.65 ms. Every detected pulse resets the internal pulse counter. The counter is clocked with the receive clock RCLK.

Pulse Count Recovery (Read/Write)

Value after RESET: 00_H

	7							0	
PCR	PCR7							PCR0	(37)

PCR7…PCR0… Pulse Count Recovery

A LOS alarm (red alarm) is cleared if a pulse density is detected in the received bit stream.The number of pulses M which must occur in the predefined PCD time interval is programmable via the PCR register and can be calculated as follows:

M = N+1 ; with $0 \leq N \leq 255$.

The time interval starts with the first detected pulse transition. With every received pulse a counter is incremented and the actual counter is compared with the contents of PCR register. If the pulse number is ≥ the PCR value the LOS alarm is reset otherwise the alarm stays active. In this case the next detected pulse transition starts a new time interval. An additional Loss of Signal recovery condition may be selected by register LIM2.LOS2...1.

Line Interface Mode 2 (Read/Write)

Value after RESET: 00_H

	7							0	
LIM2	LBO2	LBO1	DJA2	DJA1	SCF	ELT	LOS2	LOS1	(38)

LBO2...LBO1… Line Build-Out

In long haul applications LIM0.EQON = 1 a transmit filter can be optionally placed on the transmit path to attenuate the data on pins XL1/2. Selecting the transmitter attenuation is possible in steps of 7.5 dB @772kHz which is according to FCC 68 or ANSI T1. 403.

To meet the line build-out defined by ANSI T1.403 registers XPM2...0 should be programmed as follows:

00… 0 dB

01… -7.5 dB --> XPM2...0 = 20_H, 02_H, 11_H

10… -15 dB --> XPM2...0 = 20_H, 01_H, $8E_H$

11… -22.5 dB --> XPM2...0 = 20_H, 01_H, 09_H

DJA2… **Digital Jitter Attenuation DCO-X**

0… Jitter attenuation of the transmit clock is done using an external pullable crystal between pins XTAL3/4

1… Jitter attenuation of the transmit clock is done **without** using an external pullable crystal between pins XTAL3/4. Only a free running 12.352-MHz clock has top be provided at XTAL3 (+/- 50 ppm).

DJA1… **Digital Jitter Attenuation DCO-R**

0… Jitter attenuation of the system/transmit clock is done using an external pullable crystal between pins XTAL1/2

1… Jitter attenuation of the system/transmit clock is done **without** using an external pullable crystal between pins XTAL1/2. Only a free running 16.384-MHz clock has top be provided at XTAL1.

SCF… **Select Corner Frequency of DCO-R**

Setting this bit reduces the corner frequency of the DCO-R circuit by the factor of ten to 0.6 Hz.

Reducing the corner frequency of the DCO-R circuitry increases the synchronization time before the frequencies are synchronized.

ELT… **Enable Loop-Timed**

0… normal operation

1… Transmit clock is generated from the clock supplied by XTAL3 which is synchronized with the extracted receive route clock. In this configuration the transmit elastic buffer has to be enabled. Refer to register FMR5.XTM. For correct operation of loop timed the remote loop (bit LIM1.RL = 0) must be inactive.

LOS2...1… **Loss of Signal Recovery condition**

00… The LOS alarm is cleared if the predefined pulse density (register PCR) is detected during the time interval which is defined by register PCD.

01… Additionally to the recovery condition described above a LOS alarm is only cleared if the pulse density is fulfilled and no more than 15 contiguous zeros are detected during the recovery interval. (according to TR-NWT 499).

10… Clearing of a LOS alarm is done if the pulse density is fulfilled and no more than 99 contiguous zeroes are detected during the recovery interval (according to TR-NWT 820).

11… not assigned

Loop Code Register 1 (Read/Write)

Value after RESET: 00_H

	7							0	
LCR1	EPRM	XPRBS	LDC1	LDC0	LAC1	LAC0	FLLB	LLBP	(39)

EPRM… **Enable Pseudo Random Bit Sequence Monitor**

0… Pseudo random bit sequence (PRBS) monitor is disabled.

1… PRBS monitor is enabled. Setting this bit enables incrementing the CEC2 error counter with each detected PRBS bit error. With any change of state of the PRBS internal synchronization status an interrupt ISR1.LLBSC is generated. The current status of the PRBS synchronizer is indicated by bit FRS1.LLBAD. The expected PRBS sequence has to be selected by bit LCR1.LLBP.

The PRBS status signal is output on pin $\overline{\text{RFSP}}$, if XC0.SFRZ=1 and LCR1.EPRM=1. It is set high, if the PRBS monitor is in synchronous state.

XPRBS… **Transmit Pseudo Random Bit Sequence**

A one in this bit position enables transmitting of a pseudo random bit sequence to the remote end. Depending on pit LLBP the PRBS is generated according to 2^{15} -1 or 2^{20}-1 (ITU-T O. 151).

LDC1…0... **Length Deactivate (Down) Code**

These bits defines the length of the LLB deactivate code which is programmable in register LCR2.

00… length: 5 bit

01… length: 6 bit

10… length: 7 bit

11… length: 8 bit

If a shorter pattern length is required, select a multiple of the required length and repeat the pattern in LCR2.

LAC1…0... **Length Activate (Up) Code**

These bits defines the length of the LLB activate code which is programmable in register LCR3.

00… length: 5 bit

01… length: 6 bit

10… length: 7 bit

11… length: 8 bit

If a shorter pattern length is required, select a multiple of the required length and repeat the pattern in LCR3.

FLLB… **Framed Line Loopback/Invert PRBS**

Depending on bit LCR1.XPRBS this bit enables different functions:

LCR1.XPRBS=0:

0… The line loopback code is transmitted including framing bits. LLB code overwrites the FS/DL bits.

1… The line loopback code is transmitted unframed. LLB code does not overwrite the FS/DL bits.

Invert PRBS

LCR1.XPRBS=1:

0… The generated PRBS is transmitted not inverted.

1… The PRBS is transmitted inverted.

LLBP… **Line Loopback Pattern**

LCR1.XPRBS=0

0… Fixed line loopback code according to ANSI T1. 403 (001 = loop down or 00001 = loop up).

1… Enable user programmable line loopback code via register LCR2/3.

LCR1.XPRBS=1 or LCR1.EPRM = 1

0… 2^{15} -1

1… 2^{20} -1

Loop Code Register 2 (Read/Write)

Value after RESET: 00_H

	7						0	
LCR2	LDC7						LDC0	(3A)

LDC7…LDC0… **Line Loopback Deactivate Code**

If enabled by bit FMR5.XLD the LLB deactivate code is repeated automatically until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LDC0 is transmitted last. If the selected code length is less than 8 bit, the leftmost bits of LCR2 are ignored. For correct operations bit LCR1.XPRBS has to be cleared.

Loop Code Register 3 (Read/Write)

Value after RESET: 00_H

	7						0	
LCR3	LAC7						LAC0	(3B)

LAC7…LAC0… **Line Loopback Activate Code**

If enabled by bit FMR5.XLU the LLB activate code is repeated automatically until the LLB generator is stopped. Transmit data is overwritten by the LLB code. LAC0 is transmitted last. If the selected code length is less than 8 bit, the leftmost bits of LCR3 are ignored. For correct operations bit LCR1.XPRBS has to be cleared.

System Interface Control 1 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC1	SRSC		RBS1	RBS0	SXSC		XBS1	XBS0	(3C)

SRSC… **Select Receive System Clock**

0… Input frequency on pin SCLKR: 8.192 MHz
Calculation of delay time T (SCLKR cycles) depends on the value X of the “Receive Counter Offset” register RC1/0 and of the programming of RC0.RCOS.

Delay T is an even number in the range of 0 to 1022:

RCOS = 0: $X = 5 – T/2$ if $0 \le T \le 10$

$X = 517 – T/2$ if $12 \le T \le 1022$

Delay T is an odd number in the range of 1 to 1023:

RCOS = 1: $X = 5 – (T – 1)/2$ if $1 \le T \le 11$

$X = 517 – (T – 1)/2$ if $13 \le T \le 1023$

1… Input frequency on pin SCLKR: 1.544 MHz
Calculation of delay time T (SCLKR cycles) depends on the value X of the “Receive Counter Offset” register RC1/0:
T = (196 - x/2) mod 193

Delay time T = time between beginning of time-slot 0 at RDO and the initial edge of SCLKR after $\overline{\text{SYPR}}$ goes active.
If this bit is set FMR1.IMOD must be set also and bit RC0.0 should be cleared.

RBS1…0… **Receive Buffer Size**

00… Buffer size: 2 frames

01… Buffer size: 1 frame

10… Buffer size: 92 bits

11… Bypass of receive elastic store

SXSC… **Select Transmit System Clock**

0… Input frequency on pin SCLKX: 8.192 MHz
Calculation of delay time T (SCLKX cycles) depends on the value X of the “Transmit Counter Offset” register XC1/0 and of the programming of XC1.XCOS:

Delay T is an even number in the range of 0 to 1022:

XCOS = 0: X = 498 -T/2 if $0 \leq T \leq 996$

X = 1010 - T/2 if $998 \leq T \leq 1022$

Delay T is an odd number in the range of 1 to 1023:

XCOS = 1: X = 498-(T-1)/2 if $1 \leq T \leq 997$

X = 1010 - (T-1)/2 if $999 \leq T \leq 1023$

1… input frequency on pin SCLKX: 1.544 MHz
Calculation of delay time T (SCLKX cycles) depends on the value X of the “Transmit Counter Offset” register XC1/0:
T = (380 – x/2) mod 193

Delay time T = time between beginning of time-slot 0 at XDI and the initial edge of SCLKX after $\overline{SYPX}$ goes active.
If this bit is set FMR1.IMOD must be set also and bit XC0.0 should be cleared.

XBS1…0… **Transmit Buffer Size**

00… By-pass of transmit elastic store (SCLKX=1.544 MHz) or 1 frame (SCLKX = 8.192MHz)

01… Buffer size: 1 frame

10… Buffer size: 2 frames

11… Buffer size: 92 bits

System Interface Control 2 (Read/Write)

Value after RESET: 00_H

	7							0	
SIC2	FFS	SSF						SRFSO	(3D)

FFS… **Force Freeze Signaling**

Setting this bit disables updating of the receive signaling buffer and current signaling information is frozen. After resetting this bit and receiving a complete superframe updating of the signaling buffer is

started again. The freeze signaling status could be also automatically generated by detecting the Loss of Signal alarm or a Loss of Frame Alignment or a receive slip (only if external register access via RSIG is enabled). This automatic freeze signaling function is logically ored with this bit.
The current internal freeze signaling status is available in register SIS.SFS.

SSF… **Serial Signaling Format**

Only applicable if pin function R/XSIG is selected.

0… Bits 1...4 in all time-slots except time-slot 0 + 16 are cleared.

1… Bits 1...4 in all time-slots except time-slot 0 + 16 are set high.

SRFSO… **Select Receive Frame Sync Output**

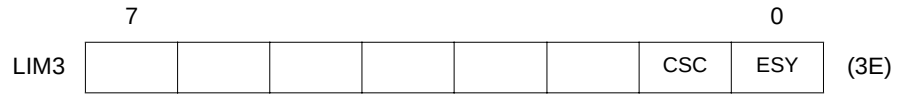
0… Pin $\overline{\text{SYPR}}$: Input

1… Pin $\overline{\text{SYPR}}$: Output

Setting this bit disables the timeslot assigner. With register RC1/0 the receive frame marker could be activated during any bit position of the current frame. This marker is active high for one 1.544-MHz cycle and is clocked off with the falling edge of SCLKR or RCLK if the receive elastic store is bypassed. If no SYPR has been activated since RESET or software reset CMDR.RES the outputs of the receive system interface assumes an arbitrary alignment.
Calculation of the value X of the “Receive Counter Offset” register RC1/0 depends on SCLKR and on the bit position BP which should be marked:
X = (2BP) mod 386, for SCLKR = 1.544 MHz

Line Interface Mode 3 (Read/Write)

Value after RESET: 00_H



CSC… **Configure System Clock CLK16M/CLK12M**

0… Dejittered XTAL1 or XTAL3 clock is output on CLK16M/ CLK12M.

1… Buffered XTAL1 or XTAL3 clock is output on CLK16M/ CLK12M.

ESY… **External Synchronization of DCO2**

Together with bit LOOP.SPN the functionality of pin 80 is defined:

Programming of LOOP.SPN and LIM3.ESY and the corresponding pin function is shown below.

SPN/ESY:

00… function of pin 80 XSIG: If SIC3.TTRF = 1, transmit data from the system interface. No input function defined for SIC3.TTRF = 0.

01… function of pin 80 SYNC2: external synchronization input for the DCO-X circuitry.

10… function of pin 80 ROID: Receive Optical Interface Data.

11… function of pin 80 XSIG: Transmit signaling input from the transmit system interface.

System Interface Control 3(Read/Write)

Value after RESET: 00_H

	7							0	
SIC3							TTRF	DAF	(40)

TTRF… **TTR Register Function**

Setting this bit the function of the TTR1...4 registers are changed. A one in each TTR register forces the XSIGM marker high for the respective time slot and controls sampling of the time slots provided by pin XSIG. XSIG is selected by LOOP.SPN = 0 and LIM3.ESY = 0.

DAF… **Disable Automatic Freeze**

Significant only if the serial signaling access is enabled.

0… Signaling is automatically frozen if one of the following alarms occurred: Loss of Signal (FRS0.LOS), Loss of Frame Alignment (FRS0.LFA), or receive slips (ISR3.RSP/N).

1… Automatic freezing of signaling data is disabled. Updating of the signaling buffer is also done if one of the above described alarm conditions is active. However, updating of the signaling buffer is stopped if SIC2.FFS is set.

Disable Error Counter (Write)

Value after RESET: 00_H

	7							0	
DEC				DBEC	DCEC	DEBC	DCVC	DFEC	(60)

DBEC… **Disable PRBS Bit Error Counter**

Only valid if LCR1.EPRM=1 and FMR1.ECM are reset.

DCEC… **Disable CRC Error Counter**

DEBC… **Disable Errored Block Counter**

DCVC… **Disable Code Violation Counter**

DFEC… **Disable Framing Error Counter**

These bits are only valid if FMR1.ECM is cleared. They have to be set before reading the error counters. They are reset automatically if the corresponding error counter high byte has been read. With the rising edge of these bits the error counters are latched and then cleared.

Transmit Signaling Registers (Write)

Value after RESET: not defined

FMR5.SRO = 0, FMR5.SRS = 1

	7							0	
XS1	A8	A7	A6	A5	A4	A3	A2	A1	(70)
XS2	A16	A15	A14	A13	A12	A11	A10	A9	(71)
XS3	A24	A23	A22	A21	A20	A19	A18	A17	(72)
XS4	B8	B7	B6	B5	B4	B3	B2	B1	(73)
XS5	B16	B15	B14	B13	B12	B11	B10	B9	(74)
XS6	B24	B23	B22	B21	B20	B19	B18	B17	(75)
XS7	A/C8	A/C7	A/C6	A/C5	A/C4	A/C3	A/C2	A/C1	(76)
XS8	A/C16	A/C15	A/C14	A/C13	A/C12	A/C11	A/C10	A/C9	(77)
XS9	A/C24	A/C23	A/C22	A/C21	A/C20	A/C19	A/C18	A/C17	(78)
XS10	B/D8	B/D7	B/D6	B/D5	B/D4	B/D3	B/D2	B/D1	(79)
XS11	B/D16	B/D15	B/D14	B/D13	B/D12	B/D11	B/D10	B/D9	(7A)
XS12	B/D24	B/D23	B/D22	B/D21	B/D20	B/D19	B/D18	B/D17	(7B)

FMR5.SRO = 1, FMR5.SRS = 1

	7							0	
XS1	A1	B1	C1/A2	D1/B2	A2/A3	B2/B3	C2/A4	D2/B4	(70)
XS2	A3/A5	B3/B5	C3/A6	D3/B6	A4/A7	B4/B7	C4/A8	D4/B8	(71)
XS3	A5/A9	B5/B9	C5/A10	D5/B10	A6/A11	B6/B11	C6/A12	D6/B12	(72)
XS4	A7/A13	B7/B13	C7/A14	D7/B14	A8/A15	B8/B15	C8/A16	D8/B16	(73)
XS5	A9/A17	B9/B17	C9/A18	D9/B18	A10/A19	B10/B19	C10/A20	D10/B20	(74)
XS6	A11/A21	B11/B21	C11/A22	D11/B22	A12/A23	B12/B23	C12/A24	D12/B24	(75)
XS7	A13/A1	B13/B1	C13/A2	D13/B2	A14/A3	B14/B3	C14/A4	D14/B4	(76)
XS8	A15/A5	B15/B5	C15/A6	D15/B6	A16/A7	B16/B7	C16/A8	D16/B8	(77)
XS9	A17/A9	B17/B9	C17/A10	D17/B10	A18/A11	B18/B11	C18/A12	D18/B12	(78)
XS10	A19/A13	B19/B13	C19/A14	D19/B14	A20/A15	B20/B15	C20/A16	D20/B16	(79)
XS11	A21/A17	B21/B17	C21/A18	D21/B18	A22/A19	B22/B19	C22/A20	D22/B20	(7A)
XS12	A23/A21	B23/B21	C23/A22	D23/B22	A24/A23	B24/B23	C24/A24	D24/B24	(7B)

Transmit Signaling Register 1...12

The transmit signaling register access is enabled by setting bit FMR5.EIBR = 1. Each register contains the bit-robbing information for 8 DS0 channels.

Starting with XMB (transmit multiframe begin), the contents of these registers is copied into a shadow register bank. Upon completion, CAS empty interrupt ISR1.CASE is set.

The contents of the shadow registers is sent out subsequently in the corresponding bit positions of the next outgoing multiframe. The transmit CAS empty interrupt ISR1.CASE requests that these registers should be serviced within the next 3 ms before the next multiframe begin. If requests for new information are ignored, current contents is repeated.
If access to XS1...12 registers is done without control of the interrupt ISR1.CASE and the write access to these registers is done exact in that moment when this interrupt is generated, data may be lost.

Note: A software reset (CMDR.XRES) resets these registers.

10.3 T1/J1 Status Register Addresses

Table 55 T1/J1 Status Register Address Arrangement

Address	Register	Type	Comment	Page
00	RFIFO	R	Receive FIFO	309
01	RFIFO	R	Receive FIFO	309
4B	RES	R	Receive Equalizer Status	309
4C	FRS0	R	Framer Receive Status 0	310
4D	FRS1	R	Framer Receive Status 1	312
4E	FRS2	R	Framer Receive Status 2	314
4F	FRS3	R	Framer Receive Status 3	315
50	FECL	R	Framing Error Counter Low	316
51	FECH	R	Framing Error Counter High	316
52	CVCL	R	Code Violation Counter Low	317
53	CVCH	R	Code Violation Counter High	317
54	CECL	R	CRC Error Counter Low	318
55	CECH	R	CRC Error Counter High	318
56	EBCL	R	Errored Block Counter Low	319
57	EBCH	R	Errored Block Counter High	319
58	BECL	R	Bit Error Counter Low	320
59	BECH	R	Bit Error Counter High	320
5C	RDL1	R	Receive DL-Bit Register 1	321
5D	RDL2	R	Receive DL-Bit Register 2	321
5E	RDL3	R	Receive DL-Bit Register 3	321
64	SIS	R	Signaling Status Register	322
65	RSIS	R	Receive Signaling Status Register	323
66	RBCL	R	Receive Byte Control Low	325
67	RBCH	R	Receive Byte Control High	325
68	ISR0	R	Interrupt Status Register 0	325
69	ISR1	R	Interrupt Status Register 1	327
6A	ISR2	R	Interrupt Status Register 2	328
6B	ISR3	R	Interrupt Status Register 3	330
6C	ISR5	R	Interrupt Status Register 5	331

Table 55 T1/J1 Status Register Address Arrangement (cont'd)

Address	Register	Type	Comment	Page
6E	GIS	R	Global Interrupt Status	332
6F	VSTR	R	Version Status	332
70	RS1	R	Receive Signaling Register 1	333
71	RS2	R	Receive Signaling Register 2	333
72	RS3	R	Receive Signaling Register 3	333
73	RS4	R	Receive Signaling Register 4	333
74	RS5	R	Receive Signaling Register 5	333
75	RS6	R	Receive Signaling Register 6	333
76	RS7	R	Receive Signaling Register 7	333
77	RS8	R	Receive Signaling Register 8	333
78	RS9	R	Receive Signaling Register 9	333
79	RS10	R	Receive Signaling Register 10	333
7A	RS11	R	Receive Signaling Register 11	333
7B	RS12	R	Receive Signaling Register 12	333

10.4 Detailed Description of T1/J1 Status Registers

Receive FIFO (Read)

	7							0	
RFIFO	RF7							RF0	(00/01)

Reading data from RFIFO can be done in an 8-bit (byte) or 16-bit (word) access depending on the selected bus interface mode. The LSB is received first from the serial interface.

The size of the accessible part of RFIFO is determined by programming the bits CCR1.RFT1…0 (RFIFO threshold level). It can be reduced from 32 bytes (RESET value) down to 2 bytes (four values: 32, 16, 4, 2 bytes).

Data Transfer

Up to 32 bytes/16 words of received data can be read from the RFIFO following a RPF or a RME interrupt.

RPF Interrupt: A fixed number of bytes/words to be read (32, 16, 4, 2 bytes). The message is not yet complete.

RME Interrupt: The message is completely received. The number of valid bytes is determined by reading the RBCL, RBCH registers.

RFIFO is released by issuing the “Receive Message Complete” command (RMC).

Receive Equalizer Status (Read)

	7							0	
RES	EV1	EV0		RES4	RES3	RES2	RES1	RES0	(4B)

EV1…0... **Equalizer Status Valid**

These bits informs the user about the current state of the receive equalization network. Only valid if LIM1.EQON is set.

00… equalizer status not valid, still adapting

01… equalizer status valid

10… equalizer status not valid

11… equalizer status valid but high noise floor

RES4…0... **Receive Equalizer Status**

The current line attenuation status in steps of about 1.4 dB are displayed in these bits. Only valid if bits EV1/0 = 01 and LIM1.EQON=1.
Accuracy: +/- 2 digit, based on temperature influence and noise amplitude variations.

00000… attenuation: 0 dB
...
11001… max. attenuation: -36 dB

Framer Receive Status Register 0 (Read)

	7							0	
FRS0	LOS	AIS	LFA	RRA			LMFA	FSRF	(4C)

LOS… **Loss of Signal (Red Alarm)**

Detection:
This bit is set when the incoming signal has „no transitions“ (analog interface) or logical zeros (dig. interface) in a time interval of T consecutive pulses, where T is programmable via PCD register:
Total account of consecutive pulses: 16 < T < 4096.

Analog interface: The receive signal level where “no transition” is declared is defined by the programmed value of LIM1.RIL2...0.

Recovery:
Analog interface: The bit is reset in short haul mode when the incoming signal has transitions with signal levels greater than the programmed receive input level (LIM1.RIL2...0) for at least M pulse periods defined by register PCR in the PCD time interval. In long haul mode additionally bit RES.6 must be set for at least 250µsec.
Digital interface: The bit is reset when the incoming data stream contains at least M ones defined by register PCR in the PCD time interval.

With the rising edge of this bit an interrupt status bit (ISR2.LOS) is set. For additionally recovery conditions refer also to register LIM2.LOS1. The bit is set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 6,7 and no alarm condition exists.

AIS… **Alarm Indication Signal (Blue Alarm)**

This bit is set when the conditions defined by bit FMR4.AIS3 are detected. The flag stays active for at least one multiframe.

With the rising edge of this bit an interrupt status bit (ISR2.AIS) is set. It is reset with the beginning of the next following multiframe if no alarm condition is detected.

The bit is set during alarm simulation and reset if FRS2.ESC = 0, 3, 4, 7 and no alarm condition exists.

LFA… **Loss of Frame Alignment**

The flag is set if pulseframe synchronization has been lost. The conditions are specified via bit FMR4.SSC1/0. Setting this bit causes an interrupt (ISR2.LFA).

The flag is cleared when synchronization has been regained. Additionally interrupt status ISR2.FAR is set with clearing this bit.

RRA… **Receive Remote Alarm (Yellow Alarm)**

The flag is set after detecting remote alarm (yellow alarm). Conditions for setting/resetting are defined by bit RC0.RRAM.

With the rising edge of this bit an interrupt status bit ISR2.RA is set.

With the falling edge of this bit an interrupt status bit ISR2.RAR is set.

The bit is set during alarm simulation and reset if FRS2.ESC = 0, 3, 4,5,7 and no alarm condition exists.

LMFA… **Loss of Multiframe Alignment**

Set in F12 or F72 format when 2 out of 4-(or 5 or 6) multiframe alignment patterns are incorrect or if LFA (loss of basic frame alignment) is detected.

Additionally the interrupt status bit ISR2.LMFA is set.

Cleared after multiframe synchronization has been regained. With the falling edge of this bit an interrupt status bit ISR2.MFAR is generated.

FSRF… **Frame Search Restart Flag**

Toggles when no framing candidate (pulse framing or multiframing) is found and a new frame search is started.

Framer Receive Status Register 1 (Read)

	7							0	
FRS1	EXZD	PDEN		LLBDD	LLBAD		XLS	XLO	(4D)

EXZD… **Excessive Zeros Detected**

Significant only if excessive zeros detection is enabled (FMR2.EXZE=1).

Set after detecting of more than 7 (B8ZS code) or more than 15 (AMI code) contiguous zeros in the received bit stream. This bit is cleared when read.

PDEN… **Pulse Density Violation Detected**

The pulse density of the received data stream is below the requirement defined by ANSI T1. 403 or more than 15 consecutive zeros are detected. With the violation of the pulse density this bit is set and remains active until the pulse density requirement is fulfilled for 23 consecutive ’1’ pulses.
Additionally an interrupt status ISR0.PDEN is generated with the rising edge of PDEN.

LLBDD… **Line Loop Back Deactivation Signal Detected**

This bit is set in case the LLB deactivate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.

Any change of this bit causes a LLBSC interrupt.

LLBAD… **Line Loopback Activation Signal Detected/PRBS Status**

Depending on bit LCR1.EPRM the source of this status bit changed.

LCR1.EPRM=0: This bit is set in case the LLB activate signal is detected and then received over a period of more than 33,16 ms with a bit error rate less than 1/100. The bit remains set as long as the bit error rate does not exceed 1/100.

If framing is aligned, the first bit position of any frame is not taken into account for the error rate calculation.

Any change of this bit causes a LLBSC interrupt.

PRBS Status

LCR1.EPRM=1: The current status of the PRBS synchronizer is indicated in this bit. It is set high if the synchronous state is reached even in the presence of a BER 1/10. A data stream containing all zeros with/without framing bits is also a valid pseudo random bit sequence. The same applies to an all ones data stream, if PRBS data inversion is selected.

XLS… **Transmit Line Short**

Significant only if the ternary line interface is selected by LIM1.DRS=0.

0… Normal operation. No short is detected.

1… The XL1 and XL2 are shortened for at least 32 pulses. As a reaction of the short the pins XL1 and XL2 are automatically forced into a high impedance state if bit XPM2.DAXLT is reset. After 32 consecutive pulse periods the outputs XL1/2 are activated again and the internal transmit current limiter is checked. If a short between XL1/2 is still further active the outputs XL1/2 are in high impedance state again. When the short disappears pins XL1/2 are activated automatically and this bit is reset. With any change of this bit an interrupt ISR1.XLSC is generated. In case of XPM2.XLT is set this bit is frozen.
Pins XL1M and XL2M have to be connected to XL1 and XL2, respectively.

XLO… **Transmit Line Open**

0… Normal operation

1… This bit is set if at least 32 consecutive zeros were sent via pins XL1/XL2 respective XDOP/XDON. This bit is reset with the first transmitted pulse. With the rising edge of this bit an interrupt ISR1.XLSC is set. In case of XPM2.XLT is set this bit is frozen.

Framer Receive Status Register 2 (Read)

	7							0	
FRS2	ESC2	ESC1	ESC0						(4E)

ESC2…ESC0… Error Simulation Counter

This three-bit counter is incremented by setting bit FMR0.SIM. The state of the counter determines the function to be tested:

For complete checking of the alarm indications, eight simulation steps are necessary (FRS2.ESC = 0 after a complete simulation).

Tested Alarms ESC2 … 0 =	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
LFA			x				x	
LMFA			x				x	
RRA (bit2 =0)		x						
RRA (S-bit frame 12)			x					
RRA (DL-pattern)							x	
LOS		x	x			x		
EBC (F12,F72)			x				x	
EBC (only ESF)		x	x			x	x	
AIS		x	x			x	x	
FEC			x				x	
CVC		x	x			x		
CEC (only ESF)		x	x			x	x	
SLPP		x						
SLPN						x		
XSLP		x	x			x	x	

Some of these alarm indications are simulated only if the FALC®-LH is configured in the appropriate mode. At simulation steps 0, 3, 4, and 7 pending status flags are reset automatically and clearing of the error counters and interrupt status registers ISR0...3 should be done. Incrementing the simulation counter should not be done at time intervals shorter than 1.5 ms (F4, F12, F72) or 3 ms (ESF). Otherwise, reactions of initiated simulations may occur at later steps.

Framer Receive Status Register 3 (Read)

	7							0	
FRS3			FEH5	FEH4	FEH3	FEH2	FEH1	FEH0	(4F)

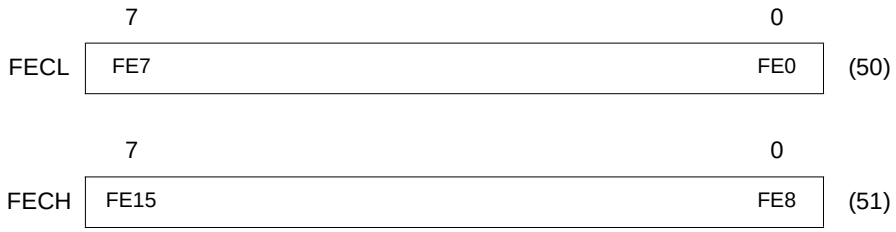
FEH5…0… **F-Bit Error History**

The bits are set if errors occur in the corresponding framing bit locations. They are updated once per superframe (ESF format) or every six frames (other framing formats).
Organization:

ESF	Others
FEH5:FAS(24)	FT (6 or 12)
FEH4:FAS(20)	FT (5 or 11)
FEH3:FAS(16)	FT (4 or 10)
FEH2:FAS(12)	FT (3 or 9)
FEH1:FAS(8)	FT (2 or 8)
FEH0:FAS(4)	FT (1 or 7)

Note:All error history bits corresponding to FS bits substituted by data link information are fixed to ‘0’.

Framing Error Counter (Read)



FE15…0… **Framing Errors**

This 16-bit counter is incremented when incorrect FT and FS bits in F4, F12 and F72 format or incorrect FAS bits in ESF format are received.
Framing errors are counted during basic frame synchronous state only (but even if multiframe synchronous state is not reached yet). The error counter doesn't roll over. During alarm simulation, the counter is incremented twice.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DFEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DFEC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Code Violation Counter (Read)

	7						0	
CVCL	CV7						CV0	(52)

	7						0	
CVCH	CV15						CV8	(53)

CV15…0… **Code Violations**

No function if NRZ code has been enabled.

If the B8ZS code (bit FMR0.RC1/0 = 11) is selected, the 16-bit counter is incremented by detecting violations which are not due to zero substitution. If FMR2.EXZE is set, additionally excessive zero strings (more than 7 contiguous zeros) are detected and counted.

If simple AMI coding is enabled (FMR0.RC0/1 = 10) all bipolar violations are counted. If FMR2.EXZE is set, additionally excessive zero strings (more than 15 contiguous zeros) are detected and counted. The error counter doesn't roll over.

During alarm simulation, the counter is incremented continuously with every second received bit.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCVC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCVC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

CRC Error Counter (Read)

	7			0	
CECL	CR7			CR0	(54)

	7			0	
CECH	CR15			CR8	(55)

CR15…0… **CRC Errors**

No function if CRC6 procedure or ESF format are disabled.

In ESF mode, the 16-bit counter is incremented when a multiframe has been received with a CRC error. CRC errors are not counted during asynchronous state. The error counter doesn't roll over.
During alarm simulation, the counter is incremented once per multiframe.

Clearing and updating the counter is done according to bit FMR1.ECM.
If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DCEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DCEC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Errored Block Counter (Read)

	7			0	
EBCL	EBC7			EBC0	(56)
	7			0	
EBCH	EBC15			EBC8	(57)

EBC15…0… **Errored Block Counter**

In ESF format this 16-bit counter is incremented once per multiframe if a multiframe has been received with a CRC error or an errored frame alignment has been detected. CRC and framing errors are not counted during asynchronous state. The error counter doesn't roll over.

In F4/12/72 format an errored block contain 4/12 or 72 frames. Incrementing is done once per multiframe if framing errors has been detected.
During alarm simulation, the counter is incremented in ESF format once per multiframe and in F4/12/72 format only one time.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the error counter bit DEC.DEBC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DEBC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Bit Error Counter (Read)

	7						0	
BECL	BEC7						BEC0	(58)

	7						0	
BECH	BEC15						BEC8	(59)

BEC15…0… **Bit Error Counter**

If the PRBS monitor is enabled by LCR1.EPRM= 1 this 16-bit counter is incremented with every received PRBS bit error in the PRBS synchronous state FRS1.LLBAD=1. The error counter doesn't roll over.

During alarm simulation, the counter is incremented continuously with every second received bit.

Clearing and updating the counter is done according to bit FMR1.ECM.

If this bit is reset the error counter is permanently updated in the buffer. For correct read access of the PRBS bit error counter bit DEC.DBEC has to be set. With the rising edge of this bit updating the buffer is stopped and the error counter is reset. Bit DEC.DBEC is reset automatically with reading the error counter high byte.

If FMR1.ECM is set every second (interrupt ISR3.SEC) the error counter is latched and then automatically reset. The latched error counter state should be read within the next second.

Receive DL-Bit Register 1 (Read)

	7							0	
RDL1	RDL17	RDL16	RDL15	RDL14	RDL13	RDL12	RDL11	RDL10	(5C)

RDL17…10… **Receive DL-Bit**

Only valid if F12, F24 or F72 format is enabled.
The received FS/DL-Bits are shifted into this register. RDL10 is received in frame 1 and RDL17 in frame 15, if F24 format is enabled. RDL10 is received in frame 26 and RDL17 in frame 40, if F72 format is enabled.
In F12 format the FS-Bits of a complete multiframe is stored in this register. RDL10 is received in frame 2 and RDL15 in frame 12.
This register is updated with every receive multiframe begin interrupt ISR0.RMB.

Receive DL-Bit Register 2 (Read)

	7							0	
RDL2	RDL27	RDL26	RDL25	RDL24	RDL23	RDL22	RDL21	RDL20	(5D)

RDL27…20… **Receive DL-Bit**

Only valid if F24 or F72 format is enabled.
The received DL-Bits are shifted into this register. RDL20 is received in frame 17 and RDL23 in frame 23, if F24 format is enabled. RDL20 is received in frame 42 and RDL27 in frame 56, if F72 format is enabled.
This register is updated with every receive multiframe begin interrupt ISR0.RMB.

Receive DL-Bit Register 3 (Read)

	7							0	
RDL3	RDL37							RDL30	(5E)

RDL37…30… **Receive DL-Bit**

Only valid if F72 format is enabled.
The received DL-Bits are shifted into this register. RDL30 is received in frame 58 and RDL37 in frame 72, if F72 format is enabled.

This register is updated with every receive multiframe begin interrupt ISR0.RMB.

Signaling Status Register (Read)

	7							0	
SIS	XDOV	XFW	XREP		RLI	CEC	SFS	BOM	(64)

XDOV… **Transmit Data Overflow**

More than 32 bytes have been written to the XFIFO.
This bit is reset by:

– a transmitter reset command XRES or

– when all bytes in the accessible half of the XFIFO have been moved in the inaccessible half.

XFW… **Transmit FIFO Write Enable**

Data can be written to the XFIFO.

XREP… **Transmission Repeat**

Status indication of CMDR.XREP.

RLI… **Receive Line Inactive**

Neither FLAGs as Interframe Time Fill nor frames are received via the signaling timeslot.

CEC… **Command Executing**

0… No command is currently executed, the CMDR register can be written to.

1… A command (written previously to CMDR) is currently executed, no further command can be temporarily written in CMDR register.

Note: CEC is active at most 2.5 periods of the current system data rate.

SFS… **Status Freeze Signaling**

0… freeze signaling status inactive.

1… freeze signaling status active.

BOM… **Bit Oriented Message**

Significant only in ESF frame format and auto switching mode is enabled.

0… HDLC mode

1… BOM mode

Receive Signaling Status Register (Read)

	7							0	
RSIS	VFR	RDO	CRC16	RAB	HA1	HA0	HFR	LA	(65)

RSIS relates to the last received HDLC or BOM frame; it is copied into RFIFO when end-of-frame is recognized (last byte of each stored frame).

VFR… **Valid Frame**

Determines whether a valid frame has been received.

1… valid HDLC frame

0… invalid HDLC frame

An invalid frame is either
– a frame which is not an integer number of 8 bits (n × 8 bits) in length (e.g. 25 bits), or
– a frame which is too short taking into account the operation mode selected via MODE (MDS2...0) and the selection of receive CRC ON/OFF (CCR3.RCRC) as follows:
  • MDS2...0 = 011 (16 bit Address),
  RCRC = 0 : 4 bytes; RCRC = 1 : 3-4 bytes
  • MDS2...0 = 010 (8 bit Address),
  RCRC = 0 : 3 bytes; RCRC = 1 : 2-3 bytes

Note:Shorter frames are not reported.

RDO… **Receive Data Overflow**

A data overflow has occurred during reception of the frame.

Additionally, an interrupt can be generated
(refer to ISR1.RDO/IMR1.RDO).

CRC16… **CRC16 Compare/Check**

0… CRC check failed; received frame contains errors.

1… CRC check o.k.; received frame is error-free.

RAB… **Receive Message Aborted**

The received frame was aborted from the transmitting station. According to the HDLC protocol, this frame must be discarded by the receiver station.

HA1...0… **High Byte Address Compare**

Significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the FALC®-LH compares the high byte of a 2-byte address with the contents of two individually programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (broadcast address).

Dependent on the result of this comparison, the following bit combinations are possible (SS7 support not active):

00… RAH2 has been recognized

01… Broadcast address has been recognized

10… RAH1 has been recognized C/R = 0 (bit 1)

11… RAH1 has been recognized C/R = 1 (bit 1)

Note: If RAH1, RAH2 contain identical values, a match is indicated by '10' or '11'.

HFR … **HDLC Frame Format**

0… A BOM frame was received.

1… A HDLC frame was received.

Note: Bits RSIS.7...2 and RSIS.0 are not valid with a BOM frame. This means, if HFR=0, all other bits of RSIS have to be ignored

LA … **Low Byte Address Compare**

Significant in HDLC modes only.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two registers. (RAL1, RAL2).

0… RAL2 has been recognized
1… RAL1 has been recognized

Receive Byte Count Low (Read)

	7						0	
RBCL	RBC7						RBC0	(66)

Together with RBCH (bits RBC11...8), indicates the length of a received frame (1…4095 bytes). Bits RBC4...0 indicate the number of valid bytes currently in RFIFO. These registers must be read by the CPU following a RME interrupt.

Received Byte Count High (Read)

	7							0	
RBCH				OV	RBC11	RBC10	RBC9	RBC8	(67)

OV… **Counter Overflow**

More than 4095 bytes received.

RBC11...8… **Receive Byte Count (most significant bits)**

Together with RBCL (bits RBC7...0) indicate the length of the received frame.

Interrupt Status Register 0 (Read)

Value after RESET: 00_H

	7							0	
ISR0	RME	RFS	ISF	RMB	RSC	CRC6	PDEN	RPF	(68)

All bits are reset when ISR0 is read.

If bit IPC.VIS is set, interrupt statuses in ISR0 may be flagged although they are masked via register IMR0. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

RME… **Receive Message End**

One complete message of length less than 32 bytes, or the last part of a frame at least 32 bytes long is stored in the receive FIFO, including the status byte.

The complete message length can be determined reading the RBCH, RBCL registers, the number of bytes currently stored in RFIFO is given by RBC4...0. Additional information is available in the RSIS register.

RFS… **Receive Frame Start**

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after an address match (in operation modes providing address recognition), or after the opening flag (transparent mode 0) is detected, delayed by two bytes. After an RFS interrupt, the contents of RSIS.3...1 is valid and can be read by the CPU.

ISF… **Incorrect Sync Format**

The FALC®-LH could not detect eight consecutive one's within 32 bits in BOM mode. Only valid if BOM receiver has been activated.

RMB… **Receive Multiframe Begin**

This bit is set with the beginning of a received multiframe of the receive line timing.

RSC… **Received Signaling Information Changed**

This interrupt bit is set during each multiframe in which signaling information on at least one channel changes its value from the previous multiframe. This interrupt only occurs in the synchronous state. The registers RS1...6/RS1...12 should be read within the next 3 ms otherwise the contents may be lost.

CRC6… **Receive CRC6 Error**

0… No CRC6 error occurs.

1… The CRC6 check of a received multiframe failed.

PDEN… **Pulse Density Violation**

The pulse density violation of the received data stream defined by ANSI T1. 403 is violated. More than 15 consecutive zeros or less than N ones in each and every time window of 8×(N+1) data bits (N=23) are detected. If IPC.SCI is set high this interrupt status bit is activated with every change of state of FRS1.PDEN.

RPF… **Receive Pool Full**

32 bytes of a frame have arrived in the receive FIFO. The frame is not yet received completely.

Interrupt Status Register 1 (Read)

	7							0	
ISR1	CASE	RDO	ALLS	XDU	XMB		XLSC	XPR	(69)

All bits are reset when ISR1 is read.

If bit IPC.VIS is set, interrupt statuses in ISR1 may be flagged although they are masked via register IMR1. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

CASE… **Transmit CAS Register Empty**

In ESF format this bit is set with the beginning of a transmitted multiframe related to the internal transmitter timing.

In F12 format this bit is set with the beginning of a transmitted multiframe, if bit FMR5.SRS = 0. If FMR5.SRS = 1, this bit is set at every second multiframe begin.

In F72 format this interrupt occurs every 12/24 frames (FMR5.SRS = 0/1) to inform the user that new bit-robbing data has to be written to XS1...6 registers (see **Table 36 "72-Frame Multiframe Structure (T1/J1)" on page 146**).

RDO… **Receive Data Overflow**

This interrupt status indicates that the CPU did not respond fast enough to an RPF or RME interrupt and that data in RFIFO has been lost. Even when this interrupt status is generated, the frame continues to be received when space in the RFIFO is available again.

Note: Whereas the bit RSIS.RDO in the frame status byte indicates whether an overflow occurred when receiving the frame currently accessed in the RFIFO, the ISR1.RDO interrupt status is generated as soon as an overflow occurs and does not necessarily pertain to the frame currently accessed by the processor.

ALLS… **All Sent**

This bit is set if the last bit of the current frame has been sent out completely and XFIFO is empty.

XDU… **Transmit Data Underrun**

Transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME was issued.

Note: Transmitter and XFIFO are reset and deactivated if this condition occurs. They are re-activated not before this interrupt status register has been read. Thus, XDU should not be masked via register IMR1.

XMB… **Transmit Multiframe Begin**

This bit is set with the beginning of a transmitted multiframe related to the internal transmit line interface timing.

XLSC… **Transmit Line Status Change**

XLSC is set with the rising edge of the bit FRS1.XLO or with any change of bit FRS1.XLS.

The actual status of the transmit line monitor can be read from the FRS1.XLS and FRS1.XLO.

XPR… **Transmit Pool Ready**

A data block of up to 32 bytes can be written to the transmit FIFO. XPR enables the fastest access to XFIFO. It has to be used for transmission of long frames, back-to-back frames or frames with shared flags.

Interrupt Status Register 2 (Read)

	7							0	
ISR2	FAR	LFA	MFAR	LMFA	AIS	LOS	RAR	RA	(6A)

All bits are reset when ISR2 is read.

If bit PIC.VIS is set, interrupt statuses in ISR2 may be flagged although they are masked via register IMR2. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

FAR… **Frame Alignment Recovery**

The framer has reached synchronization. Set with the falling edge of bit FSR0.LFA.

It is set also after alarm simulation is finished and the receiver is still synchronous.

LFA... **Loss of Frame Alignment**

The framer has lost synchronization and bit FRS0.LFA is set.
It is set during alarm simulation.

MFAR... **Multiframe Alignment Recovery**

Set when the framer has reached multiframe alignment in F12 or F72 format. With the negative transition of bit FRS0.LMFA this bit is set. It is set during alarm simulation.

LMFA... **Loss of Multiframe Alignment**

Set when the framer has lost the multiframe alignment in F12 or F72 format. With the positive transition of bit FRS0.LMFA this bit is set. It is set during alarm simulation.

AIS... **Alarm Indication Signal (Blue Alarm)**

This bit is set when an alarm indication signal is detected and bit FRS0.AIS is set. If IPC.SCI is set high this interrupt status bit is activated with every change of state of FRS0.AIS.
It is set during alarm simulation.

LOS... **Loss of Signal (Red Alarm)**

This bit is set when a loss of signal alarm is detected in the received data stream and FRS0.LOS is set. If IPC.SCI is set high this interrupt status bit is activated with every change of state of FRS0.LOS.
It is set during alarm simulation.

RAR... **Remote Alarm Recovery**

Set if a remote alarm (yellow alarm) is cleared and bit FRS0.RRA is reset. It is set also after alarm simulation is finished and no remote alarm is detected.

RA... **Remote Alarm**

A remote alarm (yellow alarm) is detected. Set with the rising edge of bit FRS0.RRA. It is set during alarm simulation.

Interrupt Status Register 3 (Read)

	7							0	
ISR3	ES	SEC	XSLP		LLBSC		RSN	RSP	(6B)

All bits are reset when ISR3 is read.

If bit IPC.VIS is set, interrupt statuses in ISR3 may be flagged although they are masked via register IMR3. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

ES… **Errored Second**

This bit is set if at least one enabled interrupt source via ESM is set during the time interval of one second. Interrupt sources of ESM register:

LFA = Loss of frame alignment detected
FER = Framing error received
CER = CRC error received
AIS = Alarm indication signal (blue alarm)
LOS = Loss of signal (red alarm)
CVE = Code violation detected
SLIP= Transmit Slip or Receive Slip positive/negative detected

SEC… **Second Timer**

The internal one second timer has expired. The timer is derived from clock RCLK.

XSLP… **Transmit Slip Indication**

Only valid if register SIC1.XBS1/0 = 01.

A one in this bit position indicates that there is an error in the host clock system. If the wander of the transmit route clock, which normally is phase locked to a common submultiple of the system clock (SCLKX), is too great, data transmission errors occur. In that case, the transmit speech memory has to be reset to its start position by writing the initial value to the transmit time-slot counter XC1.XTO.

LLBSC… **Line Loop Back Status Change/PRBS Status Change**

Depending on bit LCR1.EPRM the source of this interrupt status changed:

LCR1.EPRM=0: This bit is set, if the LLB activate signal or the LLB deactivate signal respective is detected over a period of 33,16 ms with a bit error rate less than 1/100.

The LLBSC bit is also set, if the current detection status is left, i.e., if the bit error rate exceeds 1/100.

The actual detection status can be read from the FRS1.LLBAD and FRS1.LLBDD, respectively.

PRBS Status Change

LCR1.EPRM=1: With any change of state of the PRBS synchronizer this bit is set. The current status of the PRBS synchronizer is indicated in FRS1.LLBAD.

RSN… **Receive Slip Negative**

The frequency of the receive route clock is greater than the frequency of the receive system interface working clock based on 1.544 MHz. It is set during alarm simulation.

In 2-frame buffer mode a frame is skipped.

RSP… **Receive Slip Positive**

The frequency of the receive route clock is less than the frequency of the receive system interface working clock based on 1.544 MHz. It is set during alarm simulation.

In 2-frame buffer mode a frame is repeated.

Interrupt Status Register 4 (Read)

	7							0	
ISR5	XSP	XSN							(6C)

All bits are reset when ISR5 is read.

If bit IPC.VIS is set, interrupt statuses in ISR5 may be flagged although they are masked via register IMR5. However, these masked interrupt statuses neither generate a signal on INT, nor are visible in register GIS.

XSP… **Transmit Slip Positive**

The frequency of the transmit clock is less than the frequency of the transmit system interface working clock based on 1.544 MHz. After a slip has performed writing of register XC1 is not necessary.

In 2-frame buffer mode a frame is repeated.

XSN… **Transmit Slip Negative**

The frequency of the transmit clock is greater than the frequency of the transmit system interface working clock based on 1.544 MHz. After a slip has performed writing of register XC1 is not necessary.

In 2-frame buffer mode a frame is skipped.

Global Interrupt Status Register (Read)

Value after RESET: 00_H

	7							0	
GIS				ISR5	ISR3	ISR2	ISR1	ISR0	(6E)

This status register points to pending interrupts sourced by ISR5, 3...0.

Version Status Register (Read)

	7							0	
VSTR	VN7							VN0	(6F)

VN7...0… **Version Number of Chip**

10_H…Version 1.1

13_H…Version 1.3

Receive Signaling Registers (Read)

Value after RESET: not defined

FMR5.SRO = 0

	7							0	
RS1	A8	A7	A6	A5	A4	A3	A2	A1	(70)
RS2	A16	A15	A14	A13	A12	A11	A10	A9	(71)
RS3	A24	A23	A22	A21	A20	A19	A18	A17	(72)
RS4	B8	B7	B6	B5	B4	B3	B2	B1	(73)
RS5	B16	B15	B14	B13	B12	B11	B10	B9	(74)
RS6	B24	B23	B22	B21	B20	B19	B18	B17	(75)
RS7	A/C8	A/C7	A/C6	A/C5	A/C4	A/C3	A/C2	A/C1	(76)
RS8	A/C16	A/C15	A/C14	A/C13	A/C12	A/C11	A/C10	A/C9	(77)
RS9	A/C24	A/C23	A/C22	A/C21	A/C20	A/C19	A/C18	A/C17	(78)
RS10	B/D8	B/D7	B/D6	B/D5	B/D4	B/D3	B/D2	B/D1	(79)
RS11	B/D16	B/D15	B/D14	B/D13	B/D12	B/D11	B/D10	B/D9	(7A)
RS12	B/D24	B/D23	B/D22	B/D21	B/D20	B/D19	B/D18	B/D17	(7B)

FMR5.SRO = 1

	7							0	
RS1	A1	B1	C1/A2	D1/B2	A2/A3	B2/B3	C2/A4	D2/B4	(70)
RS2	A3/A5	B3/B5	C3/A6	D3/B6	A4/A7	B4/B7	C4/A8	D4/B8	(71)
RS3	A5/A9	B5/B9	C5/A10	D5/B10	A6/A11	B6/B11	C6/A12	D6/B12	(72)
RS4	A7/A13	B7/B13	C7/A14	D7/B14	A8/A15	B8/B15	C8/A16	D8/B16	(73)
RS5	A9/A17	B9/B17	C9/A18	D9/B18	A10/A19	B10/B19	C10/A20	D10/B20	(74)
RS6	A11/A21	B11/B21	C11/A22	D11/B22	A12/A23	B12/B23	C12/A24	D12/B24	(75)
RS7	A13/A1	B13/B1	C13/A2	D13/B2	A14/A3	B14/B3	C14/A4	D14/B4	(76)
RS8	A15/A5	B15/B5	C15/A6	D15/B6	A16/A7	B16/B7	C16/A8	D16/B8	(77)
RS9	A17/A9	B17/B9	C17/A10	D17/B10	A18/A11	B18/B11	C18/A12	D18/B12	(78)
RS10	A19/A13	B19/B13	C19/A14	D19/B14	A20/A15	B20/B15	C20/A16	D20/B16	(79)
RS11	A21/A17	B21/B17	C21/A18	D21/B18	A22/A19	B22/B19	C22/A20	D22/B20	(7A)
RS12	A23/A21	B23/B21	C23/A22	D23/B22	A24/A23	B24/B23	C24/A24	D24/B24	(7B)

Receive Signaling Register 1...12

Each register contains the received bit-robbing information for 8 DS0 channels. The received robbed-bit signaling information of a complete ESF multiframe is compared with the previously received one. In F12/72 frame format the received signaling information of every 24 frames are compared with the previously received 24 frames. If the contents changed a receive signaling change interrupt ISR0.RSC is generated and informs the user that a new multiframe has to be read within the next 3 ms. Received data is stored in registers RS1...12. RS1.7 is received in channel 1 frame 1 and RS12.0 in channel 24 frame 24 (ESF).

If requests for reading the RS1...12 registers is ignored the received data may be lost.

Additionally a receive signaling data change pointer indicates an update of register RS1...12. Refer also to register RSP1/2.
Access to RS1...12 registers is only valid if the serial receive signaling access on the system highway is disabled.

11 Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 56 Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	– 40 to 85	°C
Storage temperature	T_{stg}	– 65 to 150	°C
IC supply voltage (digital)	V_{DD}	– 0.4 to 6.5	V
IC supply voltage receive (analog)	V_{DDR}	– 0.4 to 6.5	V
IC supply voltage transmit (analog)	V_{DDX}	– 0.4 to 6.5	V
Voltage on any pin with respect to ground	V_S	– 0.4 to 6.5	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	1000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993.

Note: ***Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.***

11.2 Operating Range

Table 57 Power Supply Range

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Ambient temperature	T_A	-40	85	°C	
Supply voltages	V_{DD} V_{DDR} V_{DDX}	4.75	5.25	V	1)
Ground	V_{SS} V_{SSR} V_{SSX}	0	0	V	

1) Voltage ripple on analog supply less than 50 mV

Note: In the operating range, the functions given in the circuit description are fulfilled. V_{DD}, V_{DDR} and V_{DDX} have to be connected to the same voltage level, V_{SS}, V_{SSR} and V_{SSX} have to be connected to ground level.

11.3 DC Characteristics

Table 58 DC Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input low voltage	V_{IL}	– 0.4	0.8	V	1)
Input high voltage	V_{IH}	2.0	V_{DD}+ 0.4	V	1)
Output low voltage	V_{OL}		0.45	V	I_{OL} = + 2 mA 1)
Output high voltage	V_{OH1}	2.4		V	I_{OH} = - 400µA 1)
	V_{OH2}	V_{DD} - 0.5		V	I_{OH} = - 100µA 1)
Input low voltage XTAL	V_{XTALIL}	– 0.4	1.0	V	
Input high voltage XTAL	V_{XTALIH}	3.5	V_{DD}+ 0.4	V	
Average power supply current (Analog line interface)	I_{DDE1} I_{DDT1}		165 165	mA mA	E1 application2) T1 application3)
Average power supply current (Digital line interface)	I_{DD}		85	mA	
Input leakage current	I_{IL11}		1	µA	$V_{IN} = V_{DD}$ 4)
	I_{IL12}		1	µA	$V_{IN} = V_{SS}$ 4)
	I_{IL21}		1	µA	$V_{IN} = V_{DD}$ 5)
	I_{IL12}		250	µA	$V_{IN} = V_{SS}$ 5)
	I_{ILX}		15	µA	$V_{SS} < V_{IN} < V_{DD}$ XTAL measured against V_{SS}
Output leakage current	I_{OZ}		1	µA	V_{OUT} = *tristate*1) $V_{SS} < V_{meas} < V_{DD}$ measured against V_{DD} and V_{SS}
Transmitter output impedance	R_X		3	Ω	XPM2.XLT=0 (active mode) applies to XL1and XL2 6)
		6000		Ω	XPM2.XLT=1 (tristate mode) applies to XL1and XL2 6)

Table 58 DC Parameters (cont'd)

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Transmitter output current	I_{XE1}		60	mA	XL1, XL2 ;XLHP=0
	I_{XT1}		75	mA	XL1, XL2; XLHP=1
Differential peak voltage of a mark (between XL1 and XL2)	V_X	0	3.6	V	
Transmit Line Monitor Level	V_{XM}	0.5	1	V	voltage between XL1M and XL2M
Receiver differential peak voltage of a mark (between RL1 and RL2)	V_R		V_{DD} + 5%	V	RL1, RL2
Receiver input impedance	Z_R	50 (typical value)		kΩ	6)
Receiver sensitivity	S_{RSH}	0	10	dB	RL1, RL2 LIM0.EQON=0 (short haul)
Receiver sensitivity	S_{RLHE1}	0	43	dB	RL1, RL2 LIM0.EQON=1 (E1, long haul)
Receiver sensitivity	S_{RLHT1}	0	36	dB	RL1, RL2 LIM0.EQON=1 (T1, long haul)
Receiver input threshold	V_{RTH}	55 (typical value)		%	6)
Loss of signal (LOS) detection limit in short haul mode	V_{LOSSH}	1.2 1.0 0.8 0.5 0.4 0.2 not assigned not assigned (typical values)		V	RIL2-0 = 000 RIL2-0 = 001 RIL2-0 = 010 RIL2-0 = 011 RIL2-0 = 100 RIL2-0 = 101 RIL2-0 = 110 RIL2-0 = 111 7)

1) Applies to all pins except analog pins RLx, XLx, XTALx, XLMx

2) Wiring conditions and external circuit configuration according to **Figure 23** on **page 79**; values of registers XPM2-0 = BD_H, 03_H, 00_H

3) Wiring conditions and external circuit configuration according to **Figure 49** on **page 134**; values of registers XPM2-0 = $9F_H$, 27_H, 02_H

4) Applies to all pins except RCLK, SYNC, TDI, TMS, TCK, RL1, RL2, XL1, XL2

5) Applies to pins SYNC, TDI, TMS, TCK only

6) Parameter not tested in production

7) Differential input voltage between pins RL1 and RL2; depends on programming of register LIM1.RIL2-0

Note: Typical characteristics specify mean values expected over the production spread. If not specified otherwise, typical characteristics apply at T_A = 25°C and 5.0V supply voltage.

11.4 AC Characteristics

11.4.1 Recommended Oscillator Circuits

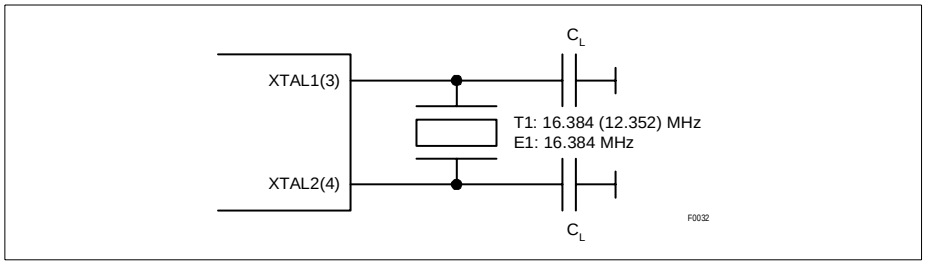


Figure 61 Crystal Oscillator Circuit (master/slave mode)

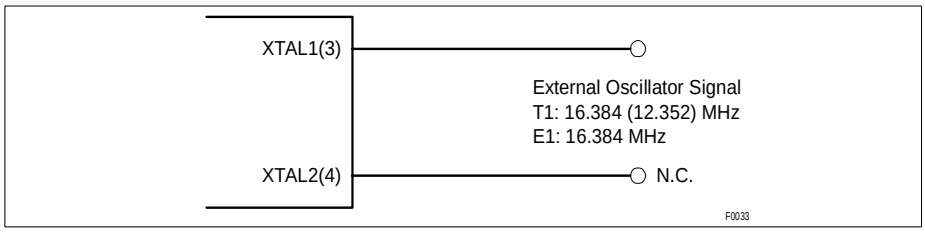


Figure 62 External Oscillator Circuit (master mode)

11.4.2 XTAL Clock Timing

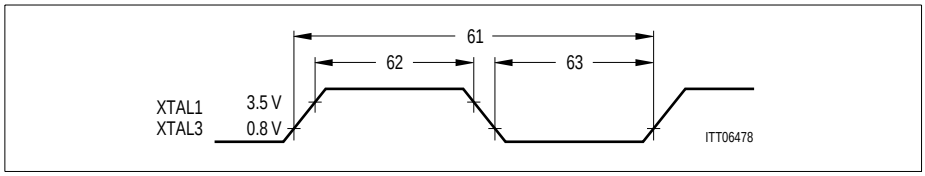


Figure 63 XTAL External Clock Timing

Table 59 XTAL Timing Parameter Values

No.	Parameter	Limit Values			Unit	Condition
		min.	typ.	max.		
61	Clock Period		61		ns	XTAL1, XTAL3
			81			XTAL3

Table 59 XTAL Timing Parameter Values (cont'd)

No.	Parameter	Limit Values			Unit	Condition
		min.	typ.	max.		
62	Clock High Phase	20			ns	XTAL1, XTAL3
		25				XTAL3
63	Clock Low Phase	20			ns	XTAL1, XTAL3
		25				XTAL3
	Clock accuracy			32[1)]	ppm	XTAL1, XTAL3
	Motional Capacitance C_1	25			fF	XTAL1, XTAL3
	Shunt Capacitance C_0			7	pF	XTAL1, XTAL3
	Load Capacitance C_L[2)]		15		pF	XTAL1, XTAL3
	Resonance Resistance R_r			40	Ω	XTAL1, XTAL3

1) to fulfill E1/T1/J1 requirements in free running mode

2) This value includes the capacitance of the external capacitor plus all parasitic capacitances. The value for the external capacitor has to be chosen depending on the printed circuit board layout. A typical value is 10 pF with 5 pF parasitic capacitance.

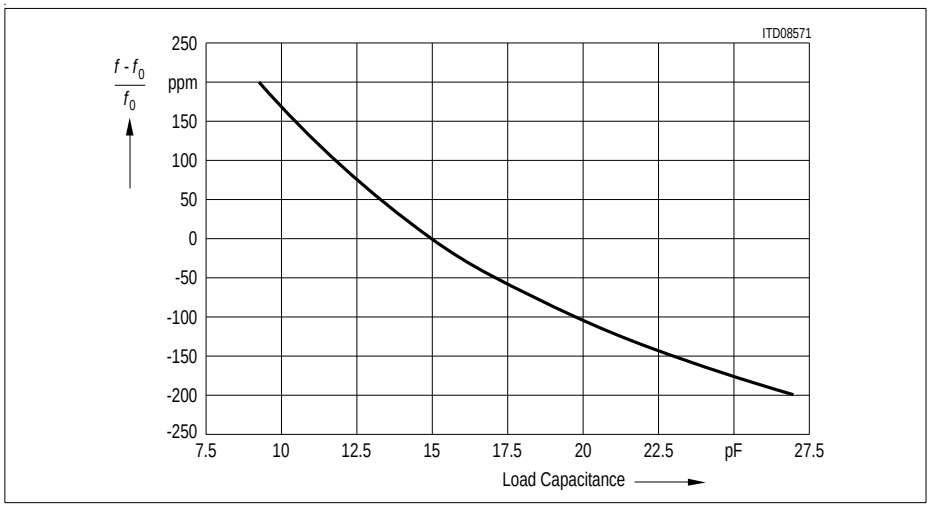


Figure 64 External Pullable Crystal Tuning Range

Note: 12.352-MHz or 16.384-MHz crystal specified for C_L=15 pF

11.4.3 JTAG Boundary Scan Interface

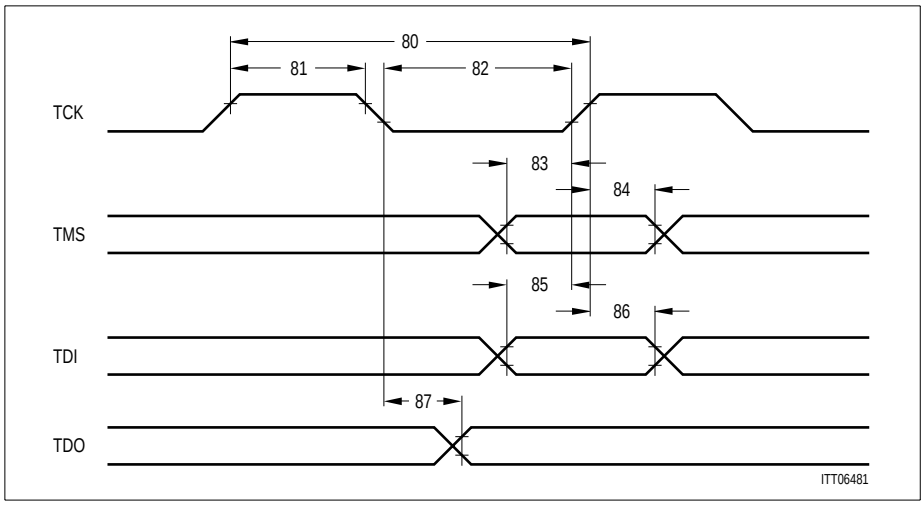


Figure 65 JTAG Boundary Scan Timing

Table 60 JTAG Boundary Scan Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
80	TCK period	250		ns
81	TCK high time	80		ns
82	TCK low time	80		ns
83	TMS setup time	40		ns
84	TMS hold time	40		ns
85	TDI setup time	40		ns
86	TDI hold time	40		ns
87	TDO valid delay		100	ns

Identification Register : 32 bit; Version: $4_{H;}$ Part Number: 42_{H}, Manufacturer: 083 $_{H}$

11.4.4 Reset

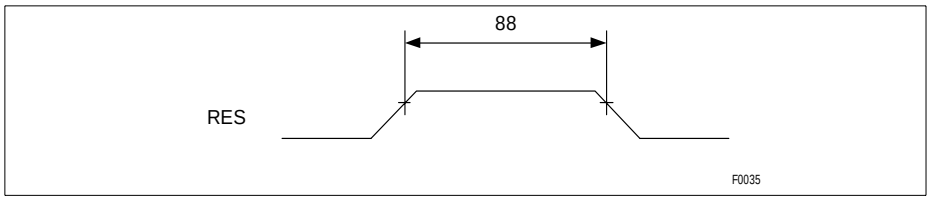


Figure 66 Reset Timing

Table 61 Reset Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
88	RES pulse width high	20[1)]		µs

1) after power supply and input clocks are stable

11.4.5 Microprocessor Interface

11.4.5.1 Intel Bus Interface Mode

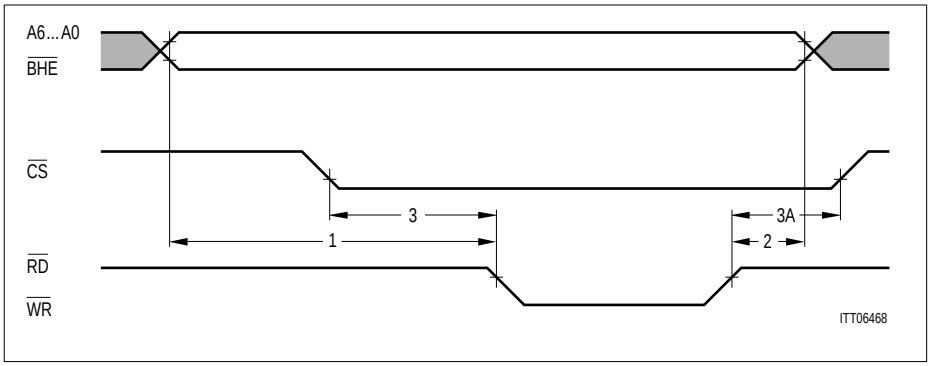


Figure 67 Intel Non-Multiplexed Address Timing

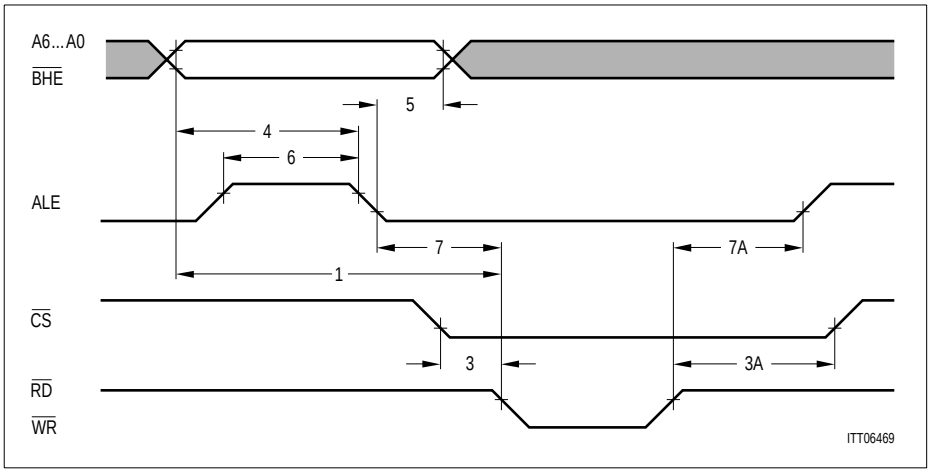


Figure 68 Intel Multiplexed Address Timing

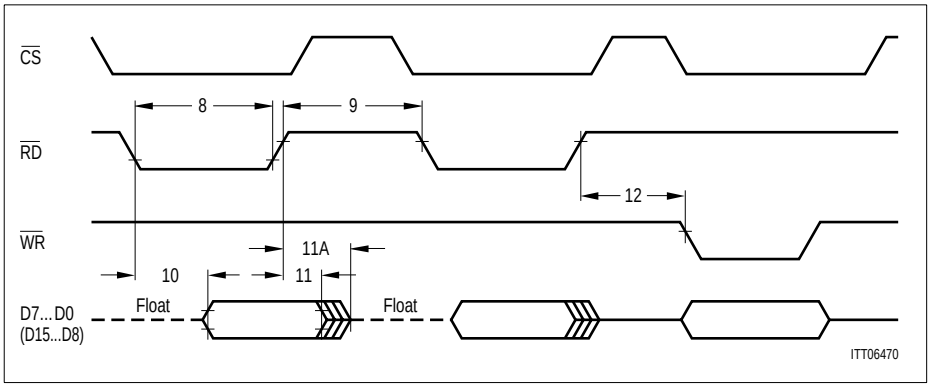


Figure 69 Intel Read Cycle Timing

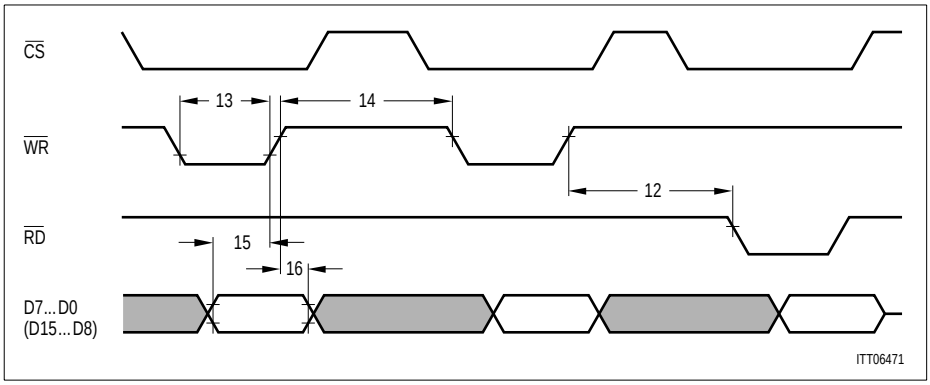


Figure 70 Intel Write Cycle Timing

Table 62 Intel Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
1	Address Ax[1], $\overline{BHE}$ setup time	15		ns
2	Address Ax[1], $\overline{BHE}$ hold time	0		ns
3	$\overline{CS}$ setup time	0		ns
3A	$\overline{CS}$ hold time	0		ns
4	Address, $\overline{BHE}$ stable before ALE inactive	20		ns
5	Address, $\overline{BHE}$ hold after ALE inactive	10		ns
6	ALE pulse width	30		ns
7	Address latch setup time before command active	0		ns
7A	ALE to command inactive delay	30		ns
8	$\overline{RD}$ pulse width	100		ns
9	$\overline{RD}$ control interval	80		ns
10	Data valid after $\overline{RD}$ active		95	ns
11	Data hold after $\overline{RD}$ inactive	10		ns
11A	$\overline{RD}$ inactive to data bus tristate[2]		30	ns
12	$\overline{WR}$ to $\overline{RD}$ or $\overline{RD}$ to $\overline{WR}$ control interval	80		ns
13	$\overline{WR}$ pulse width	60		ns
14	$\overline{WR}$ control interval	50		ns

Table 62 Intel Bus Interface Timing Parameter Values (cont'd)

No.	Parameter	Limit Values		Unit
		min.	max.	
15	Data stable before $\overline{WR}$ inactive	30		ns
16	Data hold after $\overline{WR}$ inactive	10		ns

1) Ax refers to address lines A0 to A6

2) typical value, not tested in production

11.4.5.2 Motorola Bus Interface Mode

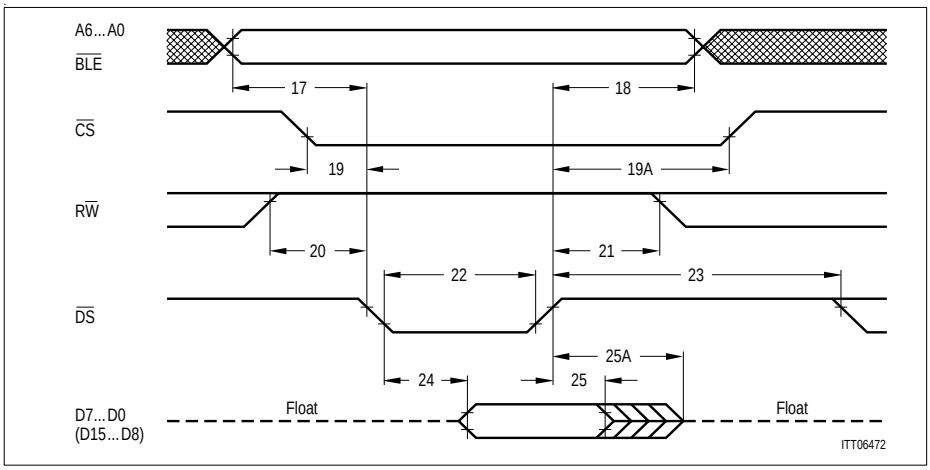


Figure 71 Motorola Read Cycle Timing

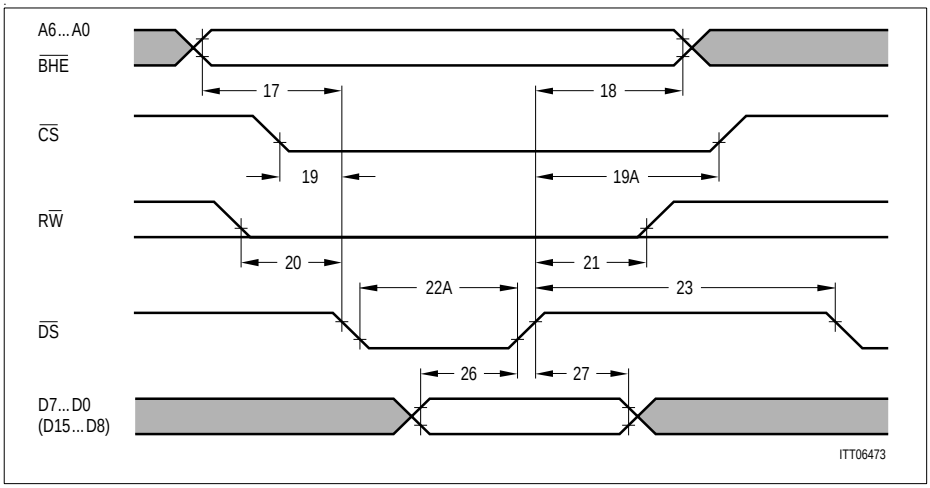


Figure 72 Motorola Write Cycle Timing

Table 63 Motorola Bus Interface Timing Parameter Values

No.	Parameter	Limit Values		Unit
		min.	max.	
17	Address, BLE, setup time before DS active	15		ns
18	Address, BLE, hold after DS inactive	0		ns
19	CS active before DS active	0		ns
19A	CS hold after DS inactive	0		ns
20	RW stable before DS active	10		ns
21	RW hold after DS inactive	0		ns
22	DS pulse width (read access)	100		ns
22A	DS pulse width (write access)	60		ns
23	DS control interval	80		ns
24	Data valid after DS active (read access)		95	ns
25	Data hold after DS inactive (read access)	10		ns
25A	DS inactive to databus tristate (read access)[1)]		30	ns
26	Data stable before DS active (write access)	30		ns
27	Data hold after DS inactive (write access)	10		ns

1) typical value, not tested in production

11.4.6 Line Interface

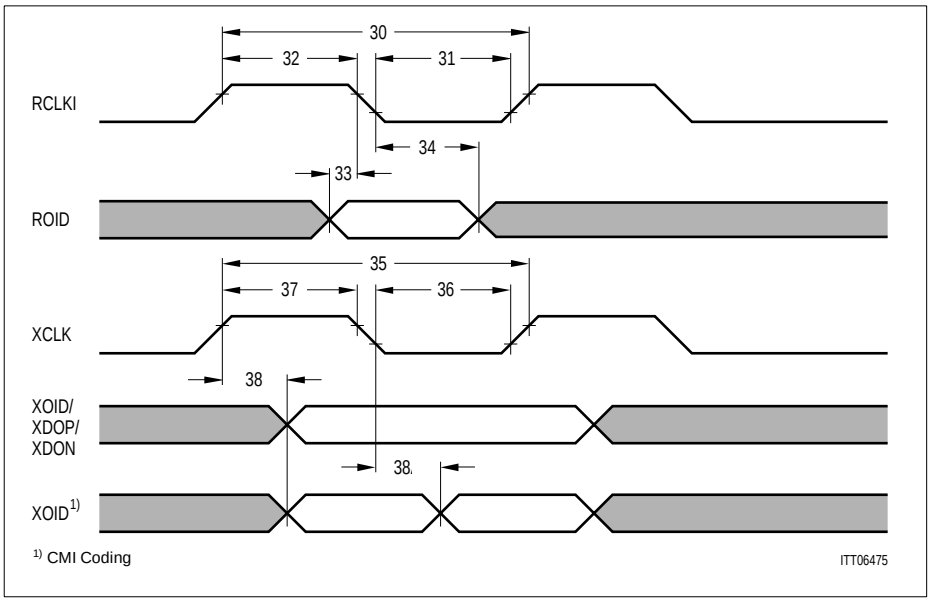


Figure 73 Timing of Dual Rail Optical Interface

Table 64 Dual Rail Optical Interface Parameter Values

No.	Parameter	Limit Values						Unit
		E1			T1			
		min.	typ.	max.	min.	typ.	max.	
30	RCLKI clock period		488			648		ns
31	RCLKI clock period low	180			240			ns
32	RCLKI clock period high	180			240			ns
33	ROID setup	50			50			ns
34	ROID hold	50			50			ns
35	XCLK clock period		488			648		ns
36	XCLK clock period low XCLK clock period low3)	190 150			230 200			ns
37	XCLK clock period high XCLK clock period high3)	190 150			230 200			ns

Table 64 Dual Rail Optical Interface Parameter Values (cont'd)

No.	Parameter	Limit Values						Unit
38	XOID delay[1)] XDOP/XDON delay[2)]			60			60	ns

[1)] NRZ coding

[2)] HDB3/AMI/B8ZS coding

[3)] depends on input RCLKI in optical interface and remote loop without transmit jitter attenuator enabled (LIM1.JATT/RL=01).

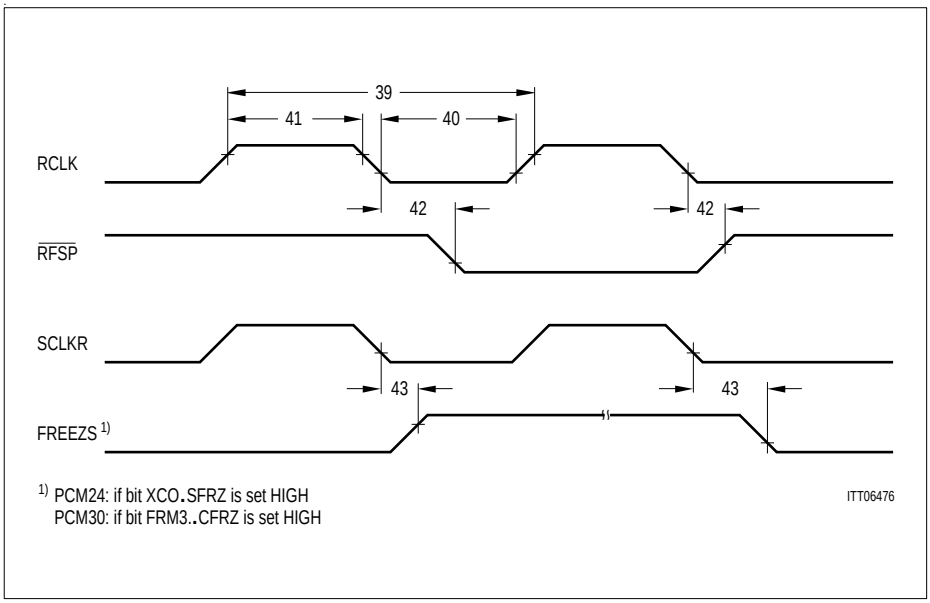


Figure 74 Receive Clock and $\overline{\text{RFSP}}$/FREEZS Timing

Table 65 Receive Clock and RFSP/FREEZS Timing Parameter Values

No.	Parameter	Limit Values						Unit
		E1			T1			
		min.	typ.	max.	min.	typ.	max.	
39	RCLK clock period		488			648		ns
40	RCLK clock low	180			240			ns
41	RCLK clock high	180			240			ns

Table 65 Receive Clock and RFSP/FREEZS Timing (cont'd)**Parameter Values**

No.	Parameter	Limit Values						Unit
		E1			T1			
		min.	typ.	max.	min.	typ.	max.	
42	$\overline{\text{RFSP}}$ delay			70			70	ns
43	FREEZS delay[1)]			95			95	ns

1) T1 using register accessed CAS and XCO.SFRZ=1 or E1/T1/J1 using serial CAS

11.4.7 System Interface

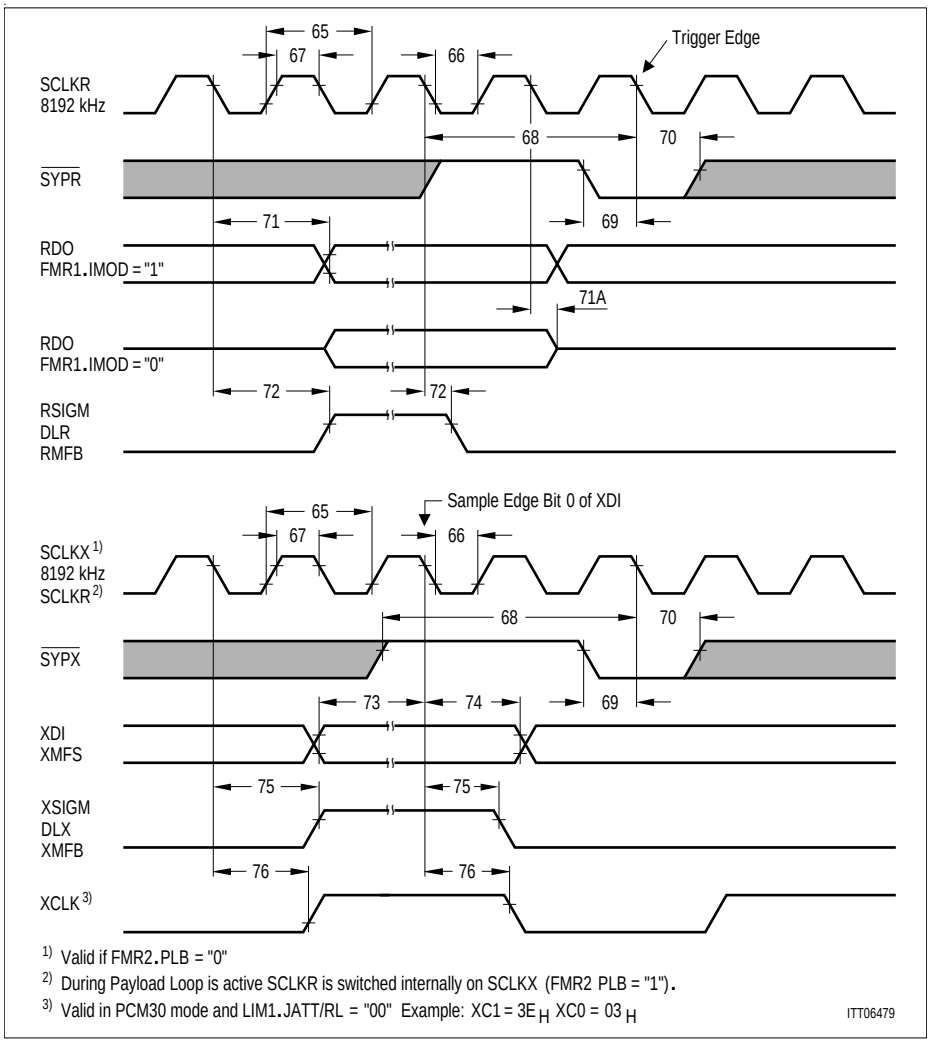


Figure 75 System Interface Timing

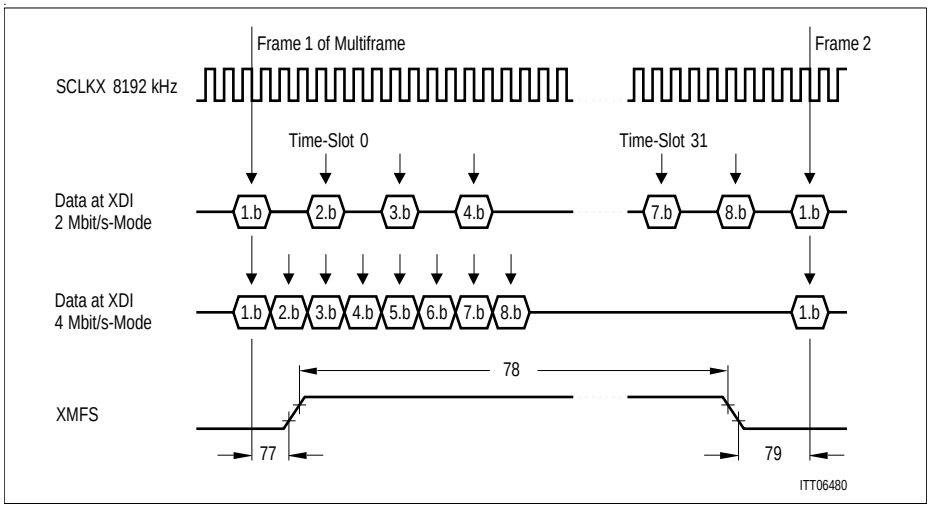


Figure 76 XMFS Timing

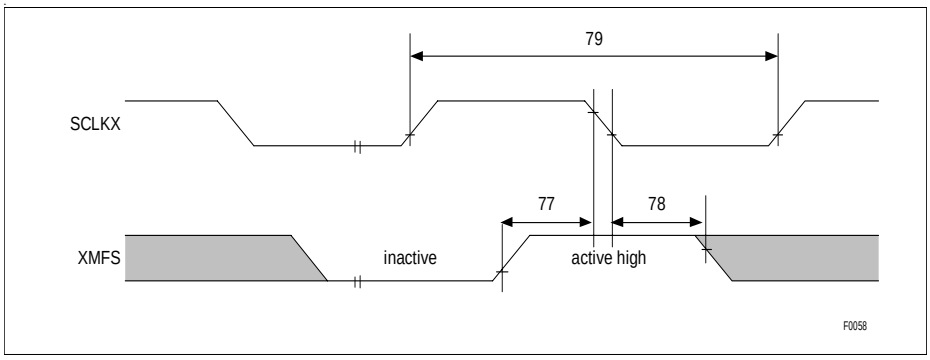


Figure 77 XMFS Timing (cont'd.)

Table 66 System Interface Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
65	SCLKX/SCLKR period		122		ns
66	SCLKX/SCLKR low (8.192 MHz)	40			ns
	SCLKX/SCLKR low (1.544/2.048 MHz)	120			ns

Table 66 System Interface Timing Parameter Values (cont'd)

No.	Parameter	Limit Values			Unit
67	SCLKX/SCLKR high (8.192 MHz)	40			ns
	SCLKX/SCLKR high (1.544/2.048 MHz)	120			ns
68	$\overline{SYPX}$/$\overline{SYPR}$ inactive setup time	$2 \times T_{65}$			ns
69	$\overline{SYPX}$/$\overline{SYPR}$ setup time	5			ns
70	$\overline{SYPX}$/$\overline{SYPR}$ hold time	50			ns
71	RDO delay[1)]	10		105	ns
71A	RDO to high impedance[1)2)]	10		105	ns
72	RSIGM, RMFB, DLR marker delay			105	ns
73	XDI setup time	5			ns
74	XDI hold time	50			ns
75	XSIGM, XMFB, DLX marker delay			105	ns
76	XCLK delay			105	ns
77	XMFS setup time	5			ns
78	XMFS hold time	50			ns
79	XMFS inactive time[1)]	$4 \times T_{65}$			ns

1) not tested in production

2) FMR1.IMOD = 0

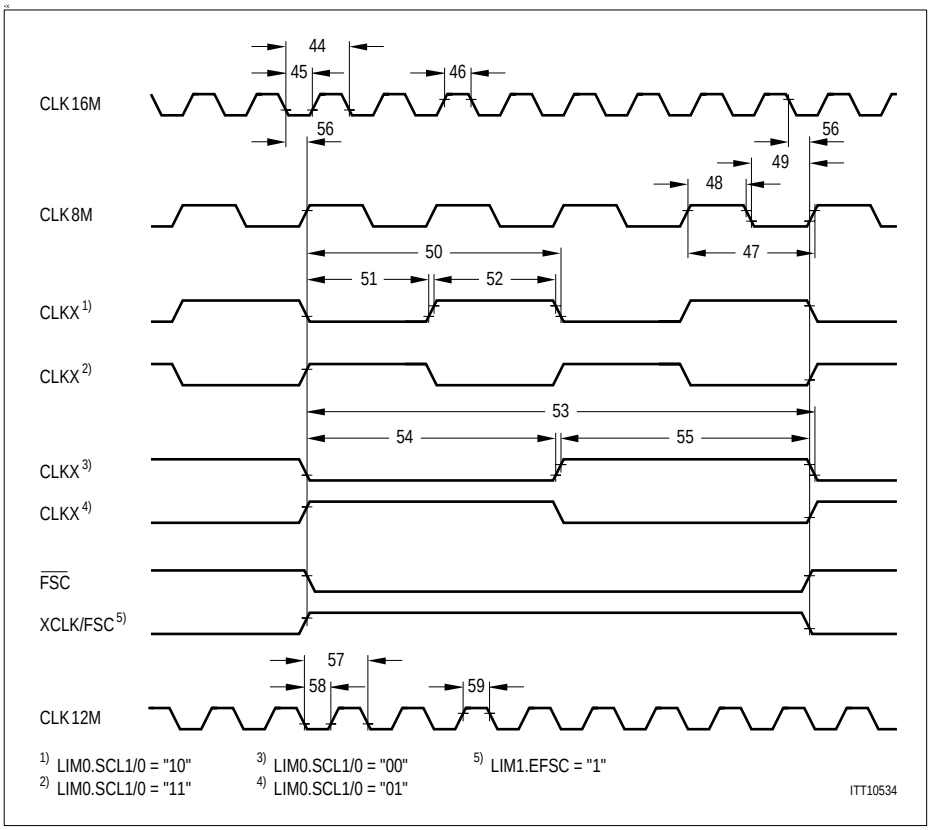


Figure 78 System Clock Timing

Table 67 System Clock Timing Parameter Values

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
44	CLK16M period		61		ns
45	CLK16M low	20			ns
46	CLK16M high	20			ns
47	CLK8M period		122		ns
48	CLK8M low	45			ns
49	CLK8M high	45			ns
50	CLKX period 4 MHz		244		ns
51	CLKX low 4 MHz	100			ns
52	CLKX high 4 MHz	100			ns
53	CLKX period 2 MHz		488		ns
54	CLKX low 2 MHz	220			ns
55	CLKX high 2 MHz	220			ns
56	FSC, $\overline{\text{FSC}}$, CLK8M, CLKX delay			50	ns
57	CLK12M period (T1/J1)		81		ns
	CLK12M period (E1)		61		ns
58	CLK12M low (T1/J1)	25			ns
	CLK12M low (E1)	20			ns
59	CLK12M high (T1/J1)	25			ns
	CLK12M high (E1)	20			ns

11.4.8 Pulse Templates - Transmitter

11.4.8.1 Pulse Template E1

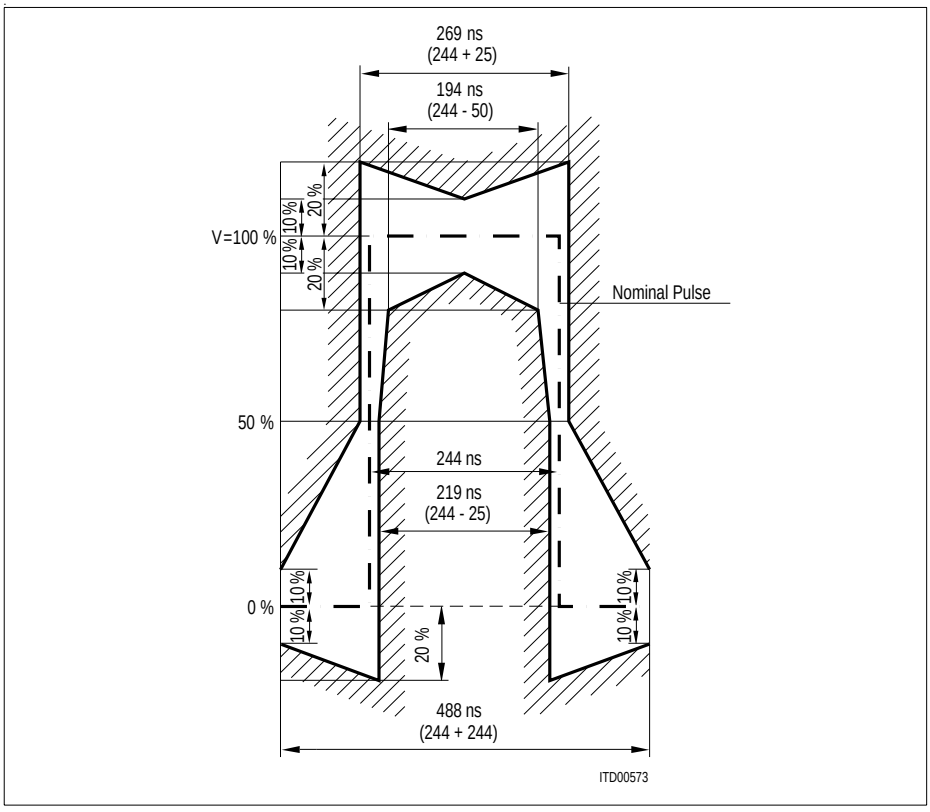


Figure 79 Pulse Shape at Transmitter Output for E1 Applications

11.4.8.2 Pulse Template T1

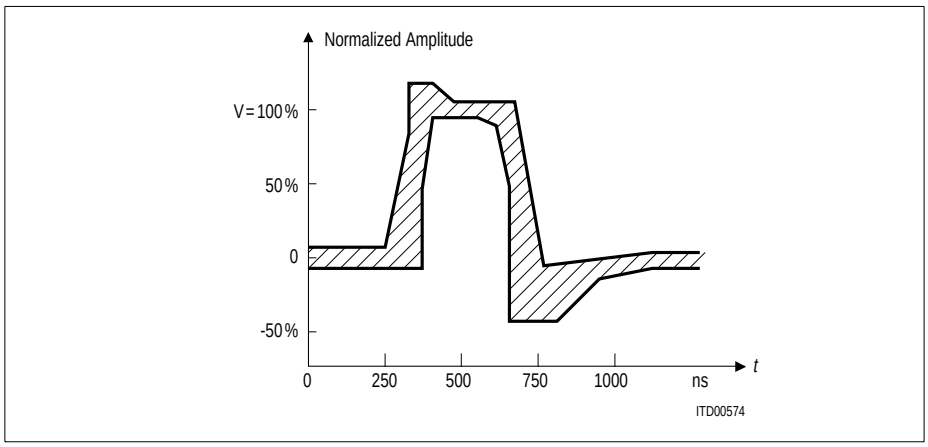


Figure 80 T1 Pulse Shape

Table 68 T1 Pulse Template (ANSI T1.102)

Maximum Curve		Minimum Curve	
Time [ns]	**Level [%][1)]**	**Time [ns]**	**Level [%]**
0	5	0	-5
250	5	350	-5
325	80	350	50
325	115	400	95
425	115	500	95
500	105	600	90
675	105	650	50
725	-7	650	-45
1100	5	800	-45
1250	5	925	-20
		1100	-5
		1250	-5

1) 100 % value must be in the range of 2.4 V and 3.6 V; tested at 0 ft. and 655 ft.

11.5 Capacitances

Table 69 Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input capacitance[1)]	C_{IN}	5	10	pF	all except XLxM, XTALx, REFR
Output capacitance[1)]	C_{OUT}	8	15	pF	all except XLx, XTALx
Output capacitance[1)]	C_{OUT}	8	20	pF	XLx
Reference voltage blocking capacitance[1)]	C_{REFR}	680[2)]	5000	pF	REFR only; including external parasitics[3)]

1) Not tested in production.

2) 680 pF are recommended value for best performance in crystal-less mode.

3) External wiring must be as short as possible.

11.6 Package Characteristics

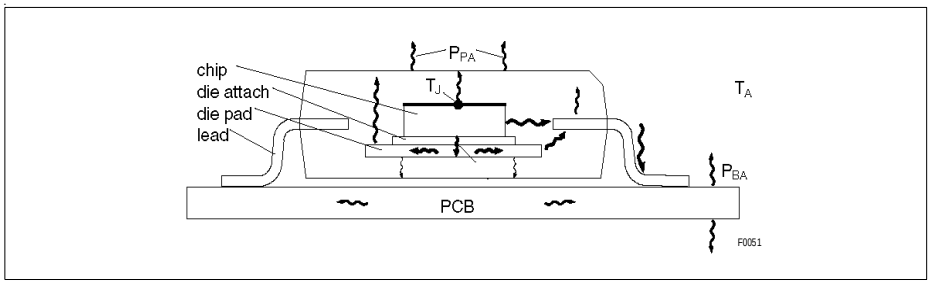


Figure 81 Thermal Behavior of Package

Table 70 Package Characteristic Values

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
Thermal Resistance	R_{thja} [1)]		47		K/W	single layer PCB, no convection
	R_{thjc} [2)]		9		K/W	
Junction Temperature	R_j			125	°C	

1) $R_{thja} = (T_{junction} - T_{ambient})/Power$
Not tested in production.

2) $R_{thjc} = (T_{junction} - T_{case})/Power$
Not tested in production.

11.7 Test Configuration

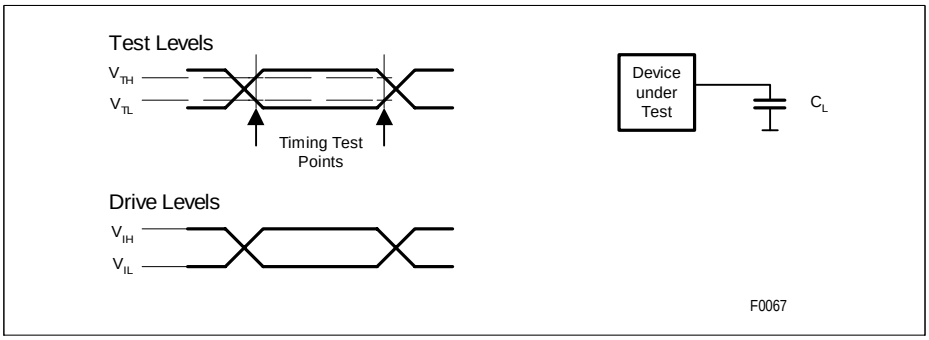


Figure 82 Input/Output Waveforms for AC Testing

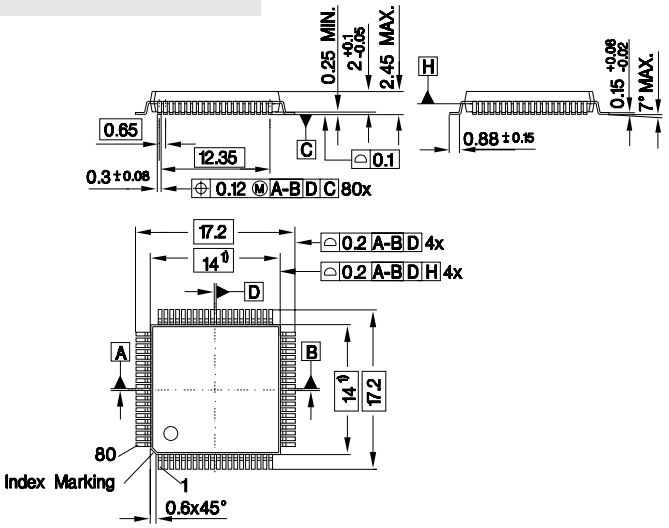
Table 71 AC Test Conditions

Parameter	Symbol	Test Values	Unit	Notes
Load Capacitance	C_L	50	pF	
Input Voltage high	V_{IH}	2.4	V	all except RLx.y
Input Voltage low	V_{IL}	0.4	V	all except RLx.y
Test Voltage high	V_{TH}	2.0	V	all except XLx.y
Test Voltage low	V_{TL}	0.8	V	all except XLx.y

Typical characteristics are mean values expected over the production spread. If not specified otherwise, typical characteristics apply at T_A = 25 °C and V_{DD} = 5.0V.

12 Package Outlines

P-MQFP-80-1
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

13 Appendix

13.1 Protection Circuitry

The design in **Figure 83** is a suggestion how to build up a generic E1/T1/J1 platform which is able to meet protection requirements according to Bellcore TR-NWT-1089, FCC Part68, UL1459. With the selection of the appropriate components the same circuitry is also able to handle the return loss and impedance to ground requirements of ETSI.

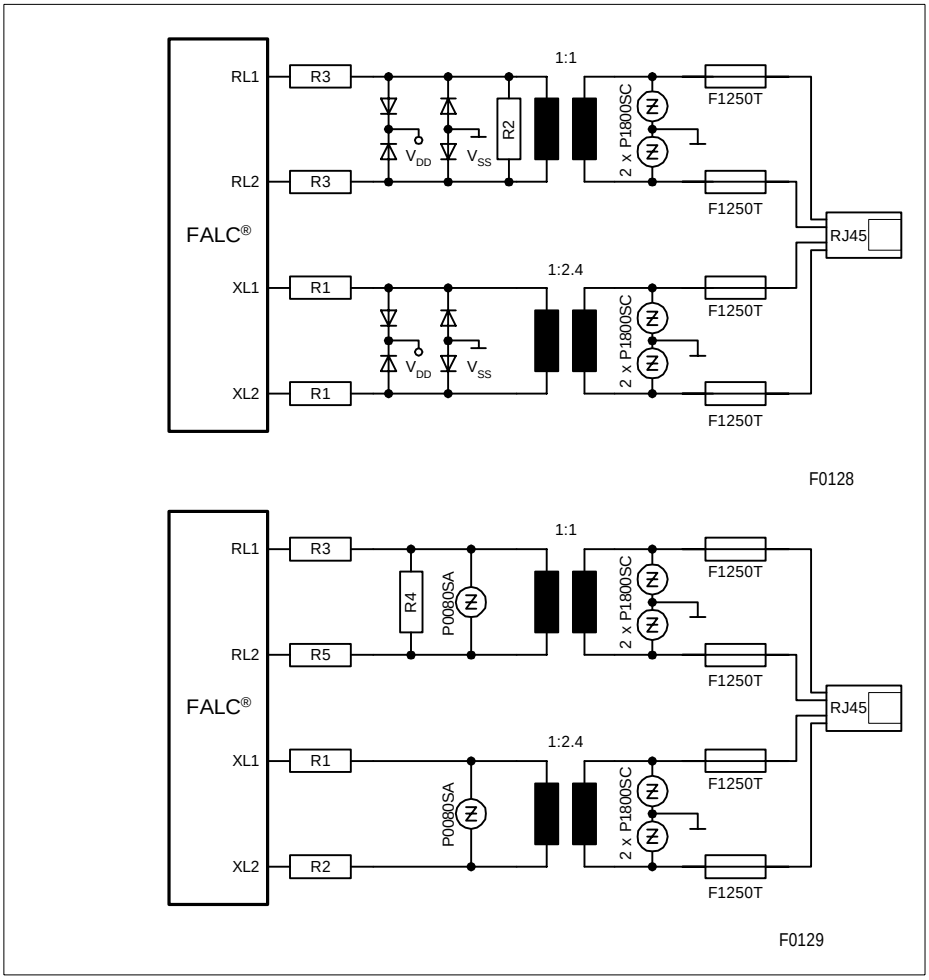


Figure 83 Protection Circuitry

13.2 Application Notes

Several application notes and technical documentation provide additional information. Online access to supporting information is available on the internet page:

http://www.infineon.com/falc

On the same page you find as well the

Boundary Scan File for FALC®-LH Version 1.3 (BSDL File)

13.3 Software Support

The following software package is provided together with the FALC®-LH Reference System EASY2255-R1:

- E1 and T1 driver functions supporting different ETSI and Bellcore requirements including HDLC and and CAS signaling
- LAPD Signaling Software
- FDL Signaling Software
- Boundary Scan File for FALC®-LH V1.3
- IBIS Model for FALC®-LH V1.3
- Gerber Files for EASY2255-R1
- External Line Front End Calculator

The 'External Line Front End Calculator' provides an easy method to optimize the external components depending on the selected application type. Calculation results are traced an can be stored in a file or printed out for documentation. The tool runs under a Win9x/NT environment.

A screenshot of the program is shown in **Figure 84** below.

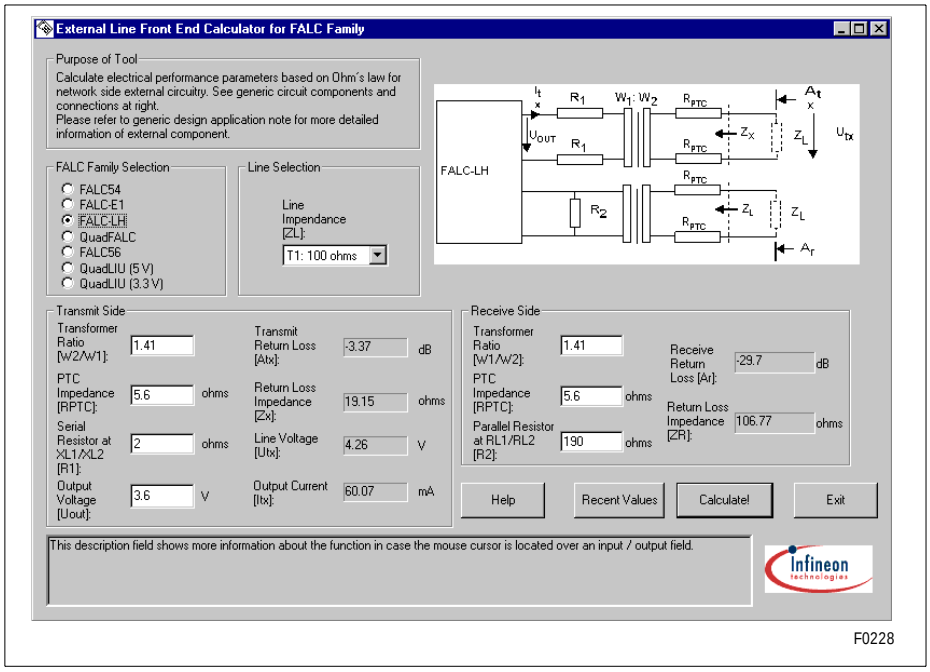


Figure 84 External Line Frontend Calculator

13.4 Differences to Version PEB 2255 V1.1

The main feature improvements are:

- Crystal-less jitter attenuation (optionally)
- Serial CAS signaling access on the PCM highway (optionally)
- Additional CAS-BR register organization (for T1)
- Additional transmit data input for fractional E1/T1/J1
- selectable receiver transparent mode
- Additional synchronization mode according to NTT requirements (for J1)
- External reference clock for DCO-X (DCO2) circuitry (SYNC2 pin)
- Optional transmit clock sourced by DCO-R (DCO1) circuitry (for E1)
- Software reset for DCO-R and DCO-X (DCO1 and DCO2)
- Enhanced loop-timed mode (optionally)
- Version register code changed from 10_H to 13_H
- Boundary Scan version register changed from 1_H to 4_H (same part number)
- Boundary Scan file changed due to additional pin functions

For a detailed description of differences to the previous version see the actual version of PEB 2255 Version 1.3/Delta Sheet.

All erratas described in ’PEB 2255 Version 1.1/Errata Sheet’ have been fixed.
Erratas described in ’PEB 2255 Version 1.3/Errata Sheet’ have not been fixed.

Due to compatibility with future products, the following naming conventions have been changed:

’DCO-1’ to ’DCO-R’ and ’DCO-2’ to ’DCO-X’

14 Glossary

A/D	Analog to digital
ADC	Analog to digital converter
AIS	Alarm indication signal (blue alarm)
AGC	Automatic gain control
ALOS	Analog loss of signal
AMI	Alternate mark inversion
ANSI	American National Standards Institute
ATM	Asynchronous transfer mode
AUXP	Auxiliary pattern
B8ZS	Line coding to avoid too long strings of consecutive ’0’
BER	Bit error rate
BFA	Basic frame alignment
BOM	Bit orientated message
Bellcore	Bell Communications Research
BPV	Bipolar violation
BSN	Backward sequence number
CAS	Channel associated signaling
CAS-BR	Channel associated signaling - bit robbing
CAS-CC	Channel associated signaling - common channel
CCS	Common channel signaling
CMI	coded mark inversion code (also known as 1T2B code)
CR	Command/Response (special bit in PPR)
CRC	Cyclic redundancy check
CSU	Channel service unit
CVC	Code violation counter
DCO	Digitally controlled oscillator
DL	Digital loop
DPLL	Digitally controlled phase locked loop
DS1	Digital signal level 1
EA	Extended address (special bit in PPR)

ESD	Electrostatic discharge
EASY	Evaluation system for FALC products
ESF	Extended superframe (F24) format
EQ	Equalizer
ETSI	European Telecommunication Standards Institute
FALC®	Framing and line interface component
FAS	Frame alignment sequence
FCC	US Federal Communication Commission
FCS	Frame check sequence (used in PPR)
FISU	Fill in signaling unit
FPS	Framing pattern sequence
FSN	Forward sequence number
HBM	Human body model for ESD classification
HDB3	High density bipolar of order 3
HDLC	High level data link control
IBIS	I/O buffer information specification (ANSI/EIA-656)
IBL	In band loop (=LLB)
ISDN	Integrated services digital network
ITU	International Telecommunications Group
JATT	Jitter attenuator
JTAG	Joined Test Action Group
LAPD	Link access procedure on D-channel
LBO	Line build out
LCV	Line code violation
LIU	Line interface unit
LFA	Loss of frame alignment
LL	Local loop
LLB	Line loop back (= IBL)
LOS	Loss of signal (red alarm)
LSB	Least significant bit
LSSU	Link status signaling unit
MF	Multiframe

MSB	Most significant bit
MSU	Message signaling unit
NRZ	Non return to zero signal
PDV	Pulse density violation
PLB	Payload loop back
PLL	Phase locked loop
PMQFP	Plastic metric quad flat pack (device package)
PPR	Periodical performance report
PRBS	Pseudo random binary sequence
PTQFP	Plastic thin metric quad flat pack (device package)
RAI	Remote alarm indication (yellow alarm)
RL	Remote loop
SAPI	Service access point identifier (special octet in PPR)
SF	Superframe
Sidactor	Overvoltage protection device for transmission lines
TAP	Test access port
TEI	Terminal endpoint identifier (special octet in PPR)
UI	Unit interval
ZCS	Zero code suppression

Index

E

F

G

H

I

J

L

M

N

O

P

R

S

T

V

W

X

Total Quality Management

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