

# SIEMENS

## PEB 3465, PEB 31665, PEB 4165

### Introduction

#### 1 Introduction

The MuSLIC, a chipset of three highly sophisticated ICs, bridges the gap between the analog and the digital signal transmission in modern telecommunication systems.

This highly integrated chip set supports to realize an extremely compact Analog Subscriber Line Interface Module. Only a few external components are required and there is no trimming or adjustment necessary to meet worldwide recommendations.

Each device is made of the best fitting technology (CMOS, BiCMOS and Smart Power Technology) and the standard SMD-packages P-MQFP and P-DSO are used.

The chipset consists of the following three ICs:

- PEB 31665 (MuPP Multichannel Processor for POTS)
- PEB 3465 (QAP Quad Analog POTS)
- PEB 4165 (AHV-SLIC Advanced High Voltage Subscriber Line Circuit)

## Multichannel Subscriber Line Interface Concept MuSLIC

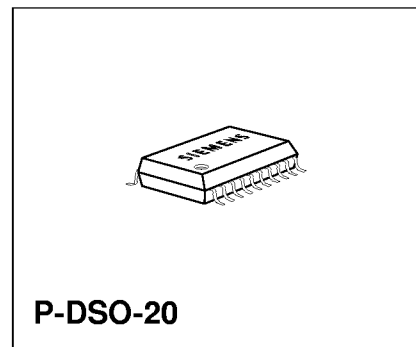
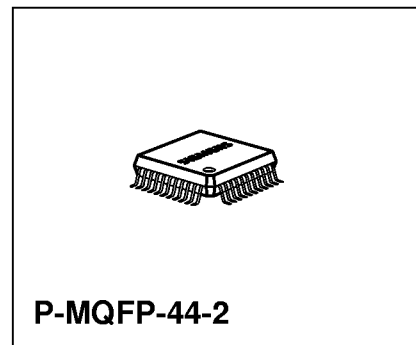
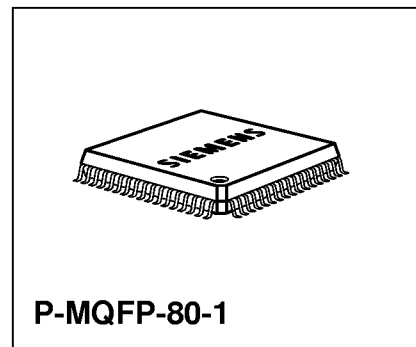
PEB 3465  
PEB 31665  
PEB 4165

Version 1.0

CMOS

### 1.1 Features

- Chip set of three well fitted chips optimized for a 16 POTS-base system
- Including all low and high voltage SLIC functions
- Only a few external components are required
- No trimming or adjustments are required
- Specification according to relevant ITU-T, LSSGR and DTAG recommendations
- Digital signal processing technique
- Advanced low power CMOS and BiCMOS<sup>1)</sup> and Smart Power technology
- PCM encoded digital voice transmission (A-Law or  $\mu$ -Law)
- Two serial IOM-2 (GCI) Interfaces with together 6 pins
- 12 Pin, 8 bits parallel microcontroller interface
- High performance AD and DA Conversion
- Programmable digital filters for
  - Impedance matching
  - Transhybrid balancing
  - Frequency response
  - Gain
- Advanced test capabilities
  - Integrated line and circuit tests
  - Two programmable tone generators



<sup>1)</sup> Abbreviations see chapter 10.3

Type	Ordering Code	Package
PEB 3465 V1.0	on request	P-MQFP-80-1
PEB 31665 V1.0	on request	P-MQFP-44-2
PEB 4165 V1.0	on request	P-DSO-20

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**Introduction**

- Fully digital programmable DC-Characteristic
  - Programmable Constant Current from 0 to 50 mA
  - Programmable Resistive Values from 0 to  $2 \times 500 \Omega$
  - Programmable Constant Voltage
- Programmable Integrated Teletax Injection and Filtering during Active in Onhook and Offhook
  - Programmable up to 10 Vrms at Ring/Tip-wire of the AHV-SLIC
  - Programmable frequency (12/16 kHz)
- Polarity reversal (programmable soft or hard)
- Integrated (balanced) Ringing Generation with zero crossing injection
  - Programmable frequency between 16.6 and 70 Hz
  - Programmable amplitude up to 85 Vrms at Ring/Tip-wire of the AHV-SLIC
- Three operating modes: Power Down, Active and Ringing
- Offhook detection with programmable thresholds for all operating modes
- Integrated Ring Trip Detection with zero crossing turn off function
- Ground Start and Loop Start possible
- Integrated checksum calculation for CRAM (AC and DC separated)
- Linecard Identification
- Sensing of transversal and longitudinal line current
- Battery voltage – 24 V ... – 80 V; Auxiliary voltage + 5 V... + 85 V
- Boosted battery mode with up to 150 V supply for long telephone lines and up to 85 Vrms balanced ringing
- Reliable 170 V Smart Power Technology
- Standard SMD packages: P-MQFP-44 and P-MQFP-80 for the low voltage parts and small power package P-DSO-20 for the high voltage device

1.2 Logic Symbol (PEB 3465)

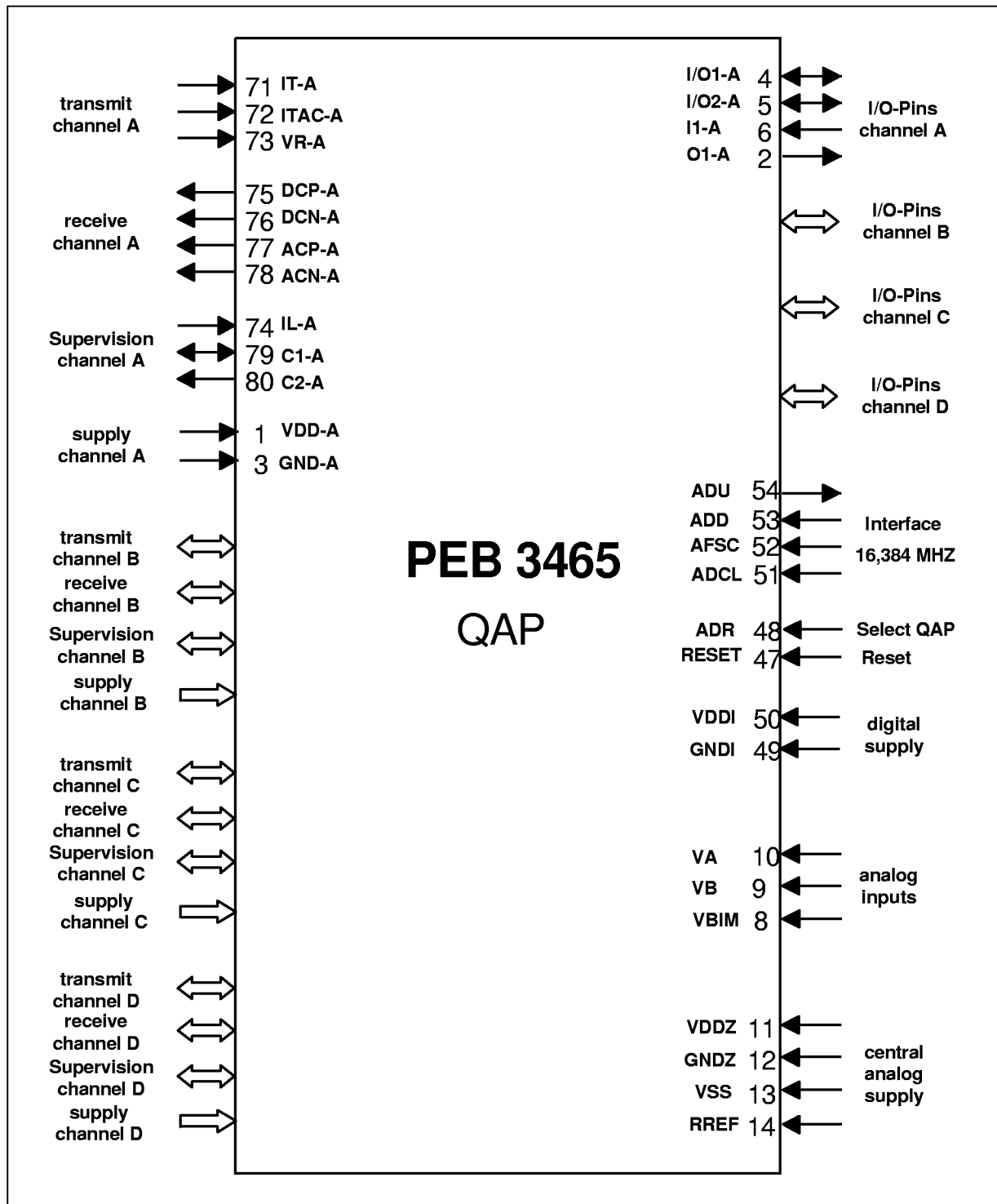


Figure 1

1.2.1 Pin Configuration (PEB 3465)

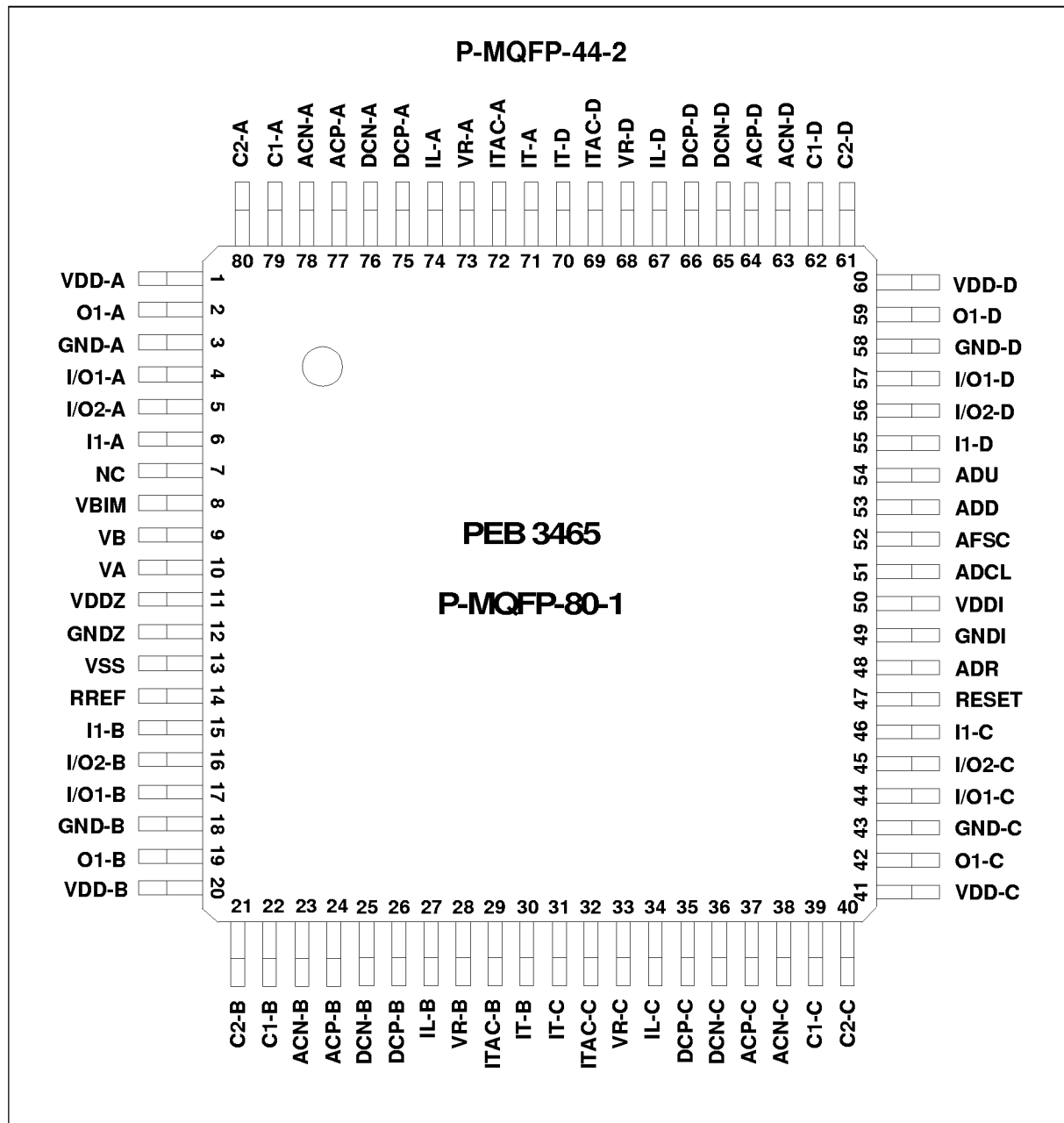


Figure 2

**Introduction**

**1.2.2 Pin Definition and Functions (PEB 3465)**

The following tables group the pins according to their functions. They include pin number, pin name, type, a brief description of the function, and cross-references referring to the sections in which the pin functions are discussed.

**Table 1 Pin Definition and Functions (PEB 3465)**

Pin No.	Name	Type	Function	Reference
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**Power Supply Pins**

1	VDD-A	–	+ 5 V Analog Supply Voltage (channel A)	
20	VDD-B	–	+ 5 V Analog Supply Voltage (channel B)	
41	VDD-C	–	+ 5 V Analog Supply Voltage (channel C)	
60	VDD-D	–	+ 5 V Analog Supply Voltage (channel D)	
3	GND-A	–	Analog Ground (channel A)	
18	GND-B	–	Analog Ground (channel B)	
43	GND-C	–	Analog Ground (channel C)	
58	GND-D	–	Analog Ground (channel D)	
11	VDDZ	–	+ 5 V Analog Supply Voltage (bias)	
12	GNDZ	–	Analog Ground (bias)	
13	VSS	–	– 5 V Analog Supply Voltage	
50	VDDI	–	+ 5 V Digital Supply Voltage	
49	GNDI	–	Digital Ground	

**Interface Pins to MuPP (PEB 31665)**

54	ADU	O	Analog Data Upstream	
53	ADD	I	Analog Data Downstream	
51	ADCL	I	Analog Data-Clock	
52	AFSC	I	Analog Frame-Sync.	
48	ADR	I	Select odd or even port nr.	
47	RESET	I	Interface-Reset	

**Table 1 Pin Definition and Functions (PEB 3465) (cont'd)**

Pin No.	Name	Type	Function	Reference
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**Interface to AHV-SLIC (PEB 4165)**

71	IT-A	I	Transversal Current Input (AC+DC), chan. A	
72	ITAC-A	I	Transversal Current Input (AC), chan. A	
73	VR-A	I	Reference Input, chan. A	
74	IL-A	I	Longitudinal Current Input, chan. A	
77	ACP-A	O	Two Wire Output Voltage (ACP), chan. A	
78	ACN-A	O	Two Wire Output Voltage (ACN), chan. A	
75	DCP-A	O	Two Wire Output Voltage (DCP), chan. A	
76	DCN-A	O	Two Wire Output Voltage (DCN), chan. A	
79	C1-A	I/O	Digital Interface to HV-SLIC, chan. A	
80	C2-A	O	Digital Interface to HV-SLIC, chan. A	
30	IT-B	I	Transversal Current Input (AC+DC), chan. B	
29	ITAC-B	I	Transversal Current Input (AC), chan. B	
28	VR-B	I	Reference Input, chan. B	
27	IL-B	I	Longitudinal Current Input, chan. B	
24	ACP-B	O	Two Wire Output Voltage (ACP), chan. B	
23	ACN-B	O	Two Wire Output Voltage (ACN), chan. B	
26	DCP-B	O	Two Wire Output Voltage (DCP), chan. B	
25	DCN-B	O	Two Wire Output Voltage (DCN), chan. B	
22	C1-B	I/O	Digital Interface to HV-SLIC, chan. B	
21	C2-B	O	Digital Interface to HV-SLIC, chan. B	
31	IT-C	I	Transversal Current Input (AC+DC), chan. C	
32	ITAC-C	I	Transversal Current Input (AC), chan. C	
33	VR-C	I	Reference Input, chan. C	
34	IL-C	I	Longitudinal Current Input, chan. C	
37	ACP-C	O	Two Wire Output Voltage (ACP), chan. C	
38	ACN-C	O	Two Wire Output Voltage (ACN), chan. C	
35	DCP-C	O	Two Wire Output Voltage (DCP), chan. C	
36	DCN-C	O	Two Wire Output Voltage (DCN), chan. C	

**Table 1 Pin Definition and Functions (PEB 3465) (cont'd)**

<b>Pin No.</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>	<b>Reference</b>
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**Interface to AHV-SLIC (PEB 4165) (cont'd)**

39	C1-C	I/O	Digital Interface to HV-SLIC, chan. C	
40	C2-C	O	Digital Interface to HV-SLIC, chan. C	
70	IT-D	I	Transversal Current Input (AC+DC), chan. D	
69	ITAC-D	I	Transversal Current Input (AC), chan. D	
68	VR-D	I	Reference Input, chan. D	
67	IL-D	I	Longitudinal Current Input, chan. D	
64	ACP-D	O	Two Wire Output Voltage (ACP), chan. D	
63	ACN-D	O	Two Wire Output Voltage (ACN), chan. D	
66	DCP-D	O	Two Wire Output Voltage (DCP), chan. D	
65	DCN-D	O	Two Wire Output Voltage (DCN), chan. D	
62	C1-D	I/O	Digital Interface to HV-SLIC, chan. D	
61	C2-D	O	Digital Interface to HV-SLIC, chan. D	



### Introduction

**Table 1 Pin Definition and Functions (PEB 3465) (cont'd)**

Pin No.	Name	Type	Function	Reference
---------	------	------	----------	-----------

#### IO Pins

4	IO1-A	I/O	User-Programmable I/O Pin, chan. A	
5	IO2-A	I/O	User-Programmable I/O Pin, chan. A	
6	I1-A	I	Fixed Input Pin, chan. A	
2	O1-A	O	Fixed Output Pin, chan. A	
17	IO1-B	I/O	User-Programmable I/O Pin, chan. B	
16	IO2-B	I/O	User-Programmable I/O Pin, chan. B	
15	I1-B	I	Fixed Input Pin, chan. B	
19	O1-B	O	Fixed Output Pin, chan. B	
44	IO1-C	I/O	User-Programmable I/O Pin, chan. C	
45	IO2-C	I/O	User-Programmable I/O Pin, chan. C	
46	I1-C	I	Fixed Input Pin, chan. C	
42	O1-C	O	Fixed Output Pin, chan. C	
57	IO1-D	I/O	User-Programmable I/O Pin, chan. D	
56	IO2-D	I/O	User-Programmable I/O Pin, chan. D	
55	I1-D	I	Fixed Input Pin, chan. D	
59	O1-D	O	Fixed Output Pin, chan. D	

#### Miscellaneous Function Pins

14	RREF	I	External resistor to GNDZ	
10	VA	I	Voltage sense a	
9	VB	I	Voltage sense b	
8	VBIM	I	Battery image sense input	

#### Pins not Used

7	N.C.	–	Not connected (not used)	
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1.2.3 Functional Block Diagram (PEB 3465)

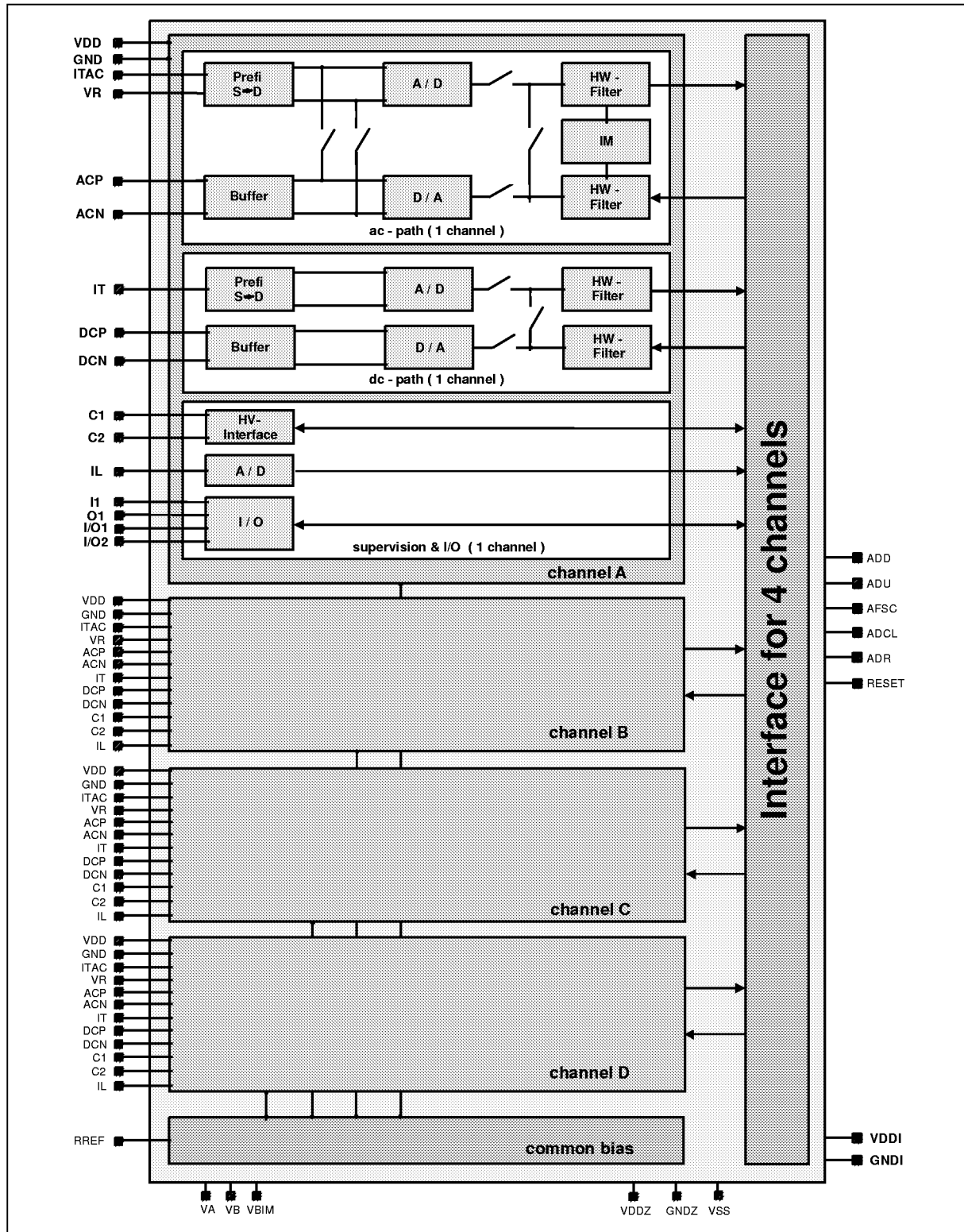


Figure 3

1.3 Logic Symbol (PEB 31665)

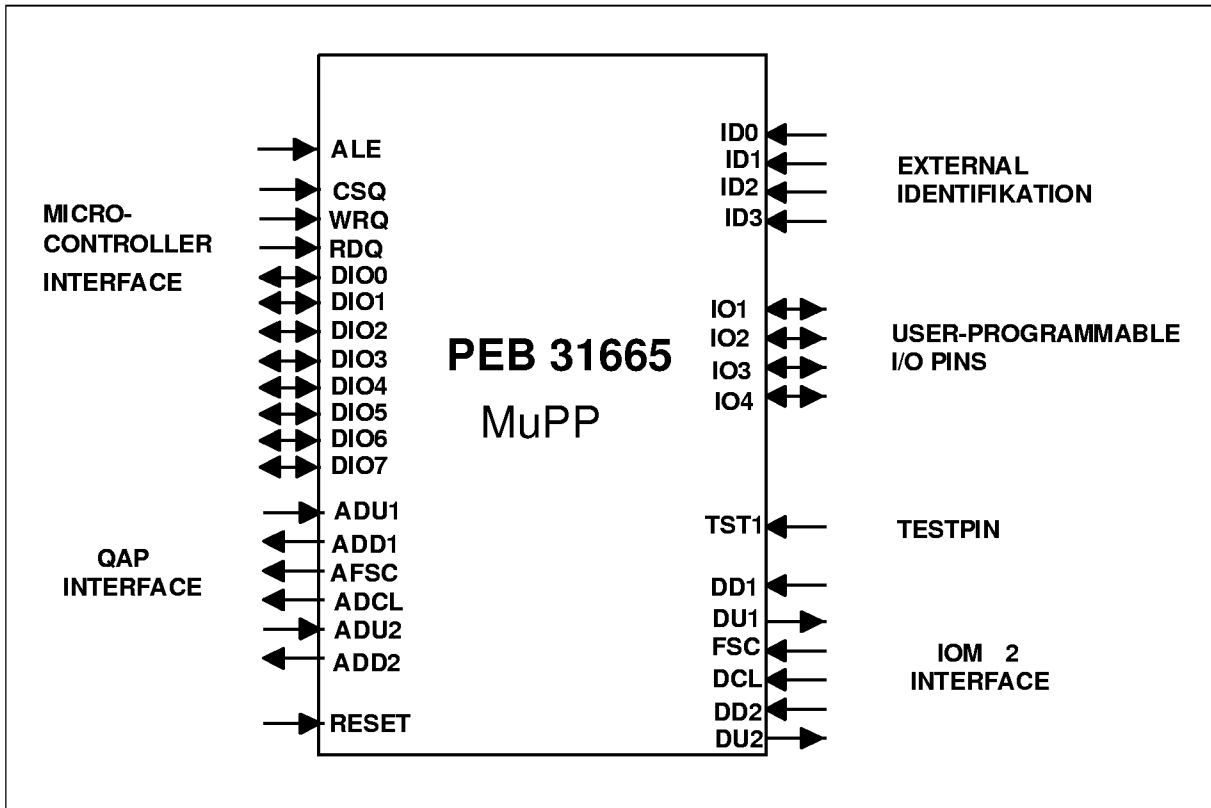


Figure 4

1.3.1 Pin Configuration (PEB 31665)

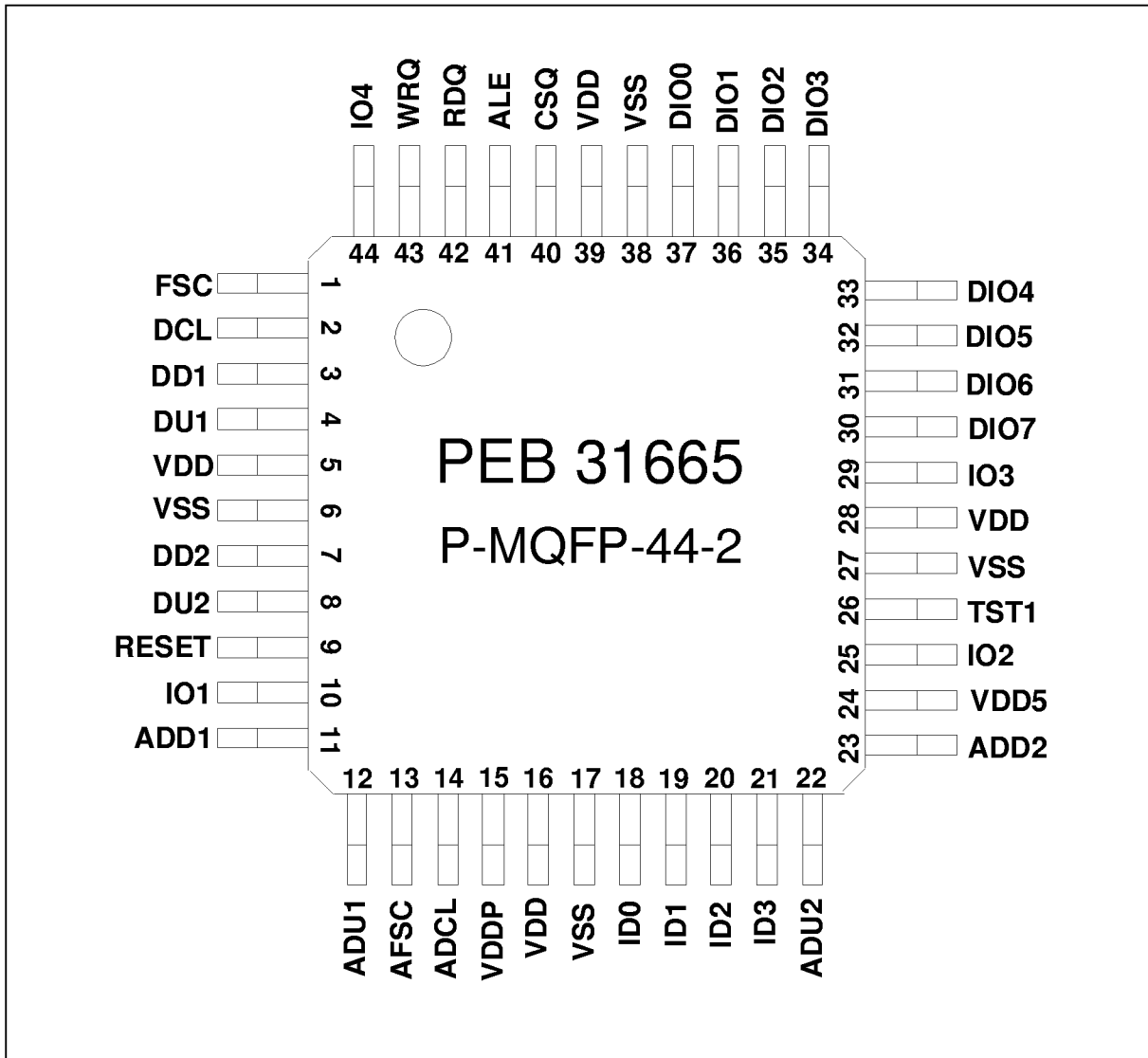


Figure 5

**Introduction**

**1.3.2 Pin Definitions and Functions (PEB 31665)**

The following tables group the pins according to their functions. They include pin number, pin name, type, a brief description of the function, and cross-references referring to the sections in which the pin functions are discussed.

**Table 2 Pin Definitions and Functions (PEB 31665)**

Pin No.	Name	Type	Function	Reference
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**Power Supply Pins**

6	VSS	–	Digital Ground	
17	VSS	–	Digital Ground	
27	VSS	–	Digital Ground	
38	VSS	–	Digital Ground	
5	VDD	–	+ 3.3 V Digital Supply Voltage	
15	VDDP	–	+ 3.3 V Digital Supply Voltage for PLL	
16	VDD	–	+ 3.3 V Digital Supply Voltage	
28	VDD	–	+ 3.3 V Digital Supply Voltage	
39	VDD	–	+ 3.3 V Digital Supply Voltage	
24	VDD5	–	+ 5 V Digital Supply Voltage	

**IOM<sup>®</sup>-2 Pins**

4	DU1	O	1'st IOM-2 Data Upstream (open drain)	
3	DD1	I	1'st IOM-2 Data Downstream	
2	DCL	I	IOM-2 Data-Clock	
1	FSC	I	IOM-2 Frame-Sync.	
8	DU2	O	2'nd IOM-2 Data Upstream (open drain)	
7	DD2	I	2'nd IOM-2 Data Downstream	

**Table 2 Pin Definitions and Functions (PEB 31665) (cont'd)**

Pin No.	Name	Type	Function	Reference
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#### MuPP/QAP Interface

11	ADD1	O	1'st QAP	Data Downstream	
12	ADU1	I	1'st QAP	Data Upstream	
13	AFSC	O	QAP	Frame-Sync	
14	ADCL	O	QAP	Data-Clock	
23	ADD2	O	2'nd QAP	Data Downstream	
22	ADU2	I	2'nd QAP	Data Upstream	

#### Microcontroller Interface

40	CSQ	I	μC Chip select		
41	ALE	I	μC Address latch enable		
42	RDQ	I	μC Data-Clock read		
43	WRQ	I	μC Data-Clock write		
37	DIO0	I/O	μC Data / Address		
36	DIO1	I/O	μC Data / Address		
35	DIO2	I/O	μC Data / Address		
34	DIO3	I/O	μC Data / Address		
33	DIO4	I/O	μC Data / Address		
32	DIO5	I/O	μC Data / Address		
31	DIO6	I/O	μC Data / Address		
30	DIO7	I/O	μC Data / Address		

#### IO Pins

10	IO1	I/O	User-Programmable I/O Pin		
25	IO2	I/O	User-Programmable I/O Pin		
29	IO3	I/O	User-Programmable I/O Pin		
44	IO4	I/O	User-Programmable I/O Pin		

**Table 2 Pin Definitions and Functions (PEB 31665) (cont'd)**

<b>Pin No.</b>	<b>Name</b>	<b>Type</b>	<b>Function</b>	<b>Reference</b>
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**Miscellaneous Function Pins**

9	RESET	I	Reset	
18	ID0	I	External Identification	
19	ID1	I	External Identification	
20	ID2	I	External Identification	
21	ID3	I	External Identification	
26	TST1	I	Test Pin (must be connected to VSS)	

1.3.3 Functional Block Diagram (PEB 31665)

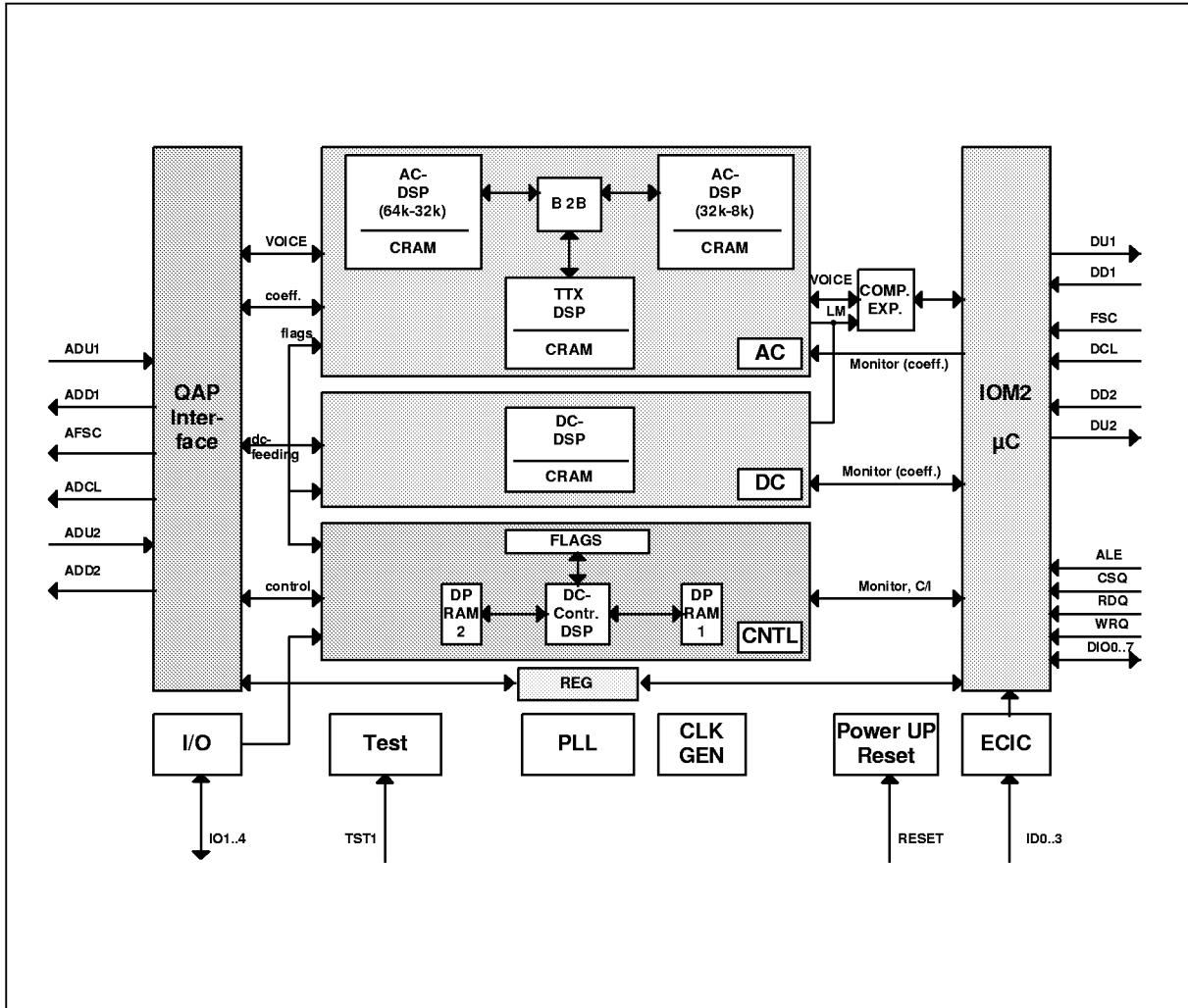


Figure 6



1.4 Logic Symbol (PEB 4165)

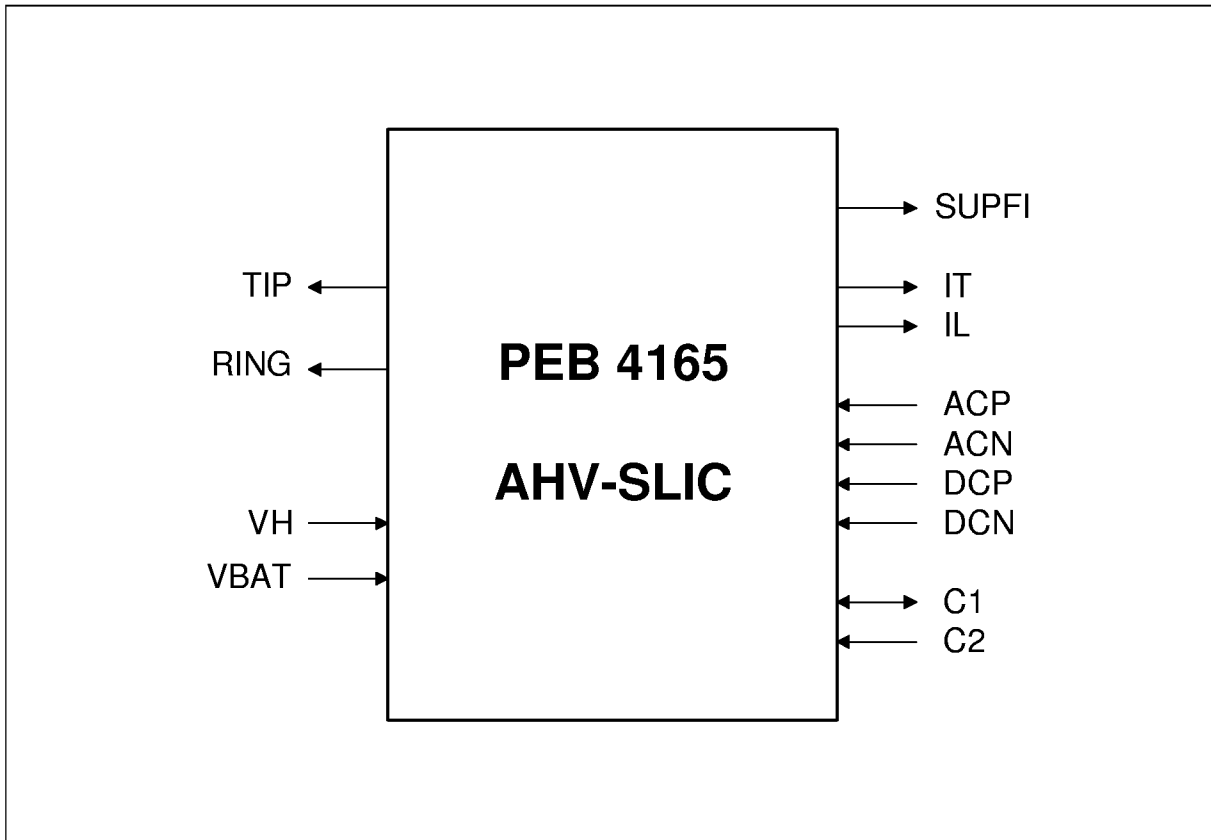
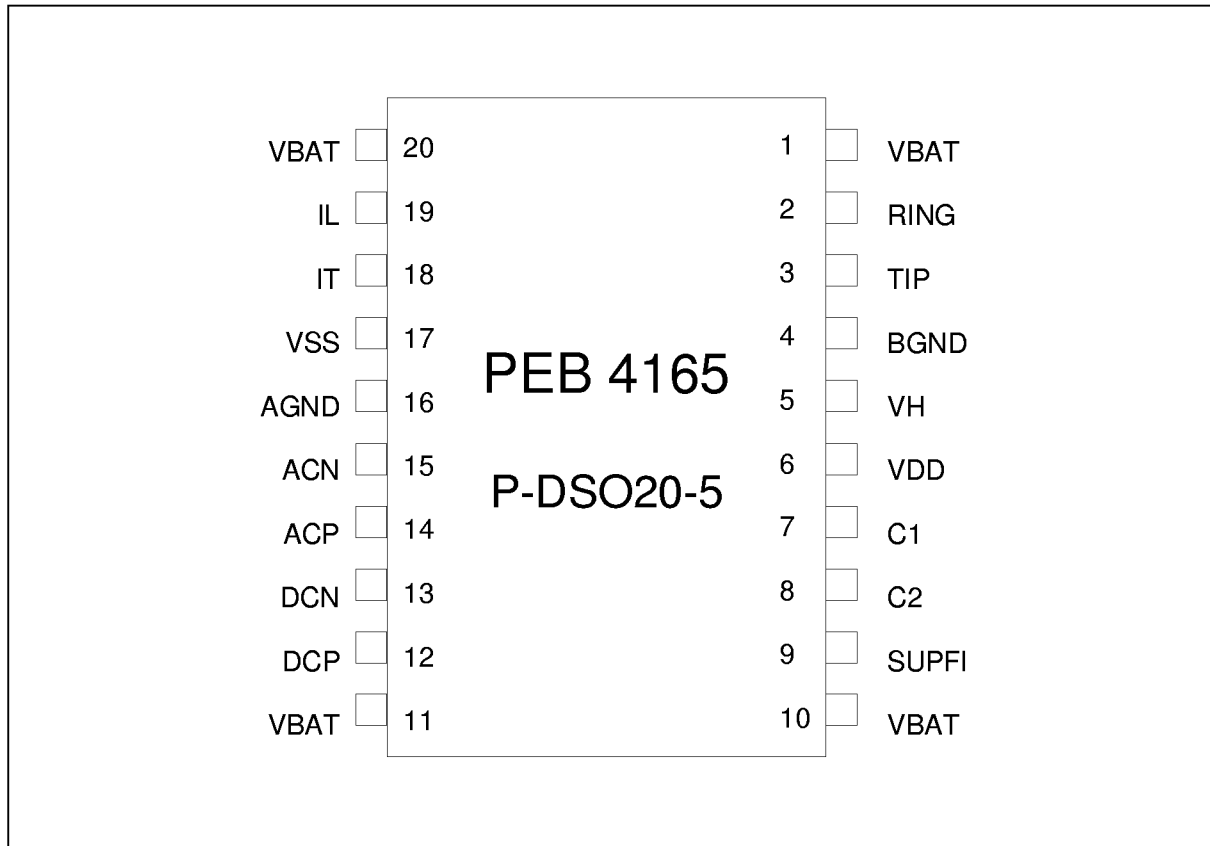


Figure 7

**1.4.1 Pin Configuration (PEB 4165)****Figure 8**

**Introduction**
**1.4.2 Pin Definitions and Functions (PEB 4165)**

Pin No.	Symbol	Type	Description
1,10,11,20	VBAT	Supply	Negative battery supply voltage (– 24 ... – 80 V), referred to BGND
2	RING	O	Subscriber loop connection RING
3	TIP	O	Subscriber loop connection TIP
4	BGND	Supply	Battery ground: TIP, RING, VBAT and VH refer to this pin
5	VH	Supply	Auxiliary positive battery supply voltage (+ 5 ... + 85 V) used in ringing mode
9	SUPFI	O	External capacitance for supply voltage filtering (internal resistance of about 30 kΩ)
6	VDD	Supply	Positive supply voltage (+ 5 V), referred to AGND
7	C1	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload this pin sinks a current of typ. 150 μA
8	C2	I	Ternary logic input, controlling the operation mode
12,13	DCP,DCN	I	Differential two wire DC-input voltage; multiplied by – 25 and related to $(VH - VBAT) / 2$ , DCN appears at TIP and DCP at RING output, respectively
14,15	ACP,ACN	I	Differential two wire AC-input voltage; multiplied by – 3.125, ACN appears at TIP and ACP at RING output, respectively
16	AGND	Supply	Analog ground: VDD, VSS and all signal and control pins with the exception of TIP and RING refer to AGND
17	VSS	Supply	Negative supply voltage (– 5 V), referred to AGND
18	IT	O	Current output representing the transversal current scaled down by a factor of 50.
19	IL	O	Current output: longitudinal line current scaled down by a factor of 50.

1.4.3 Functional Block Diagram (PEB 4165)

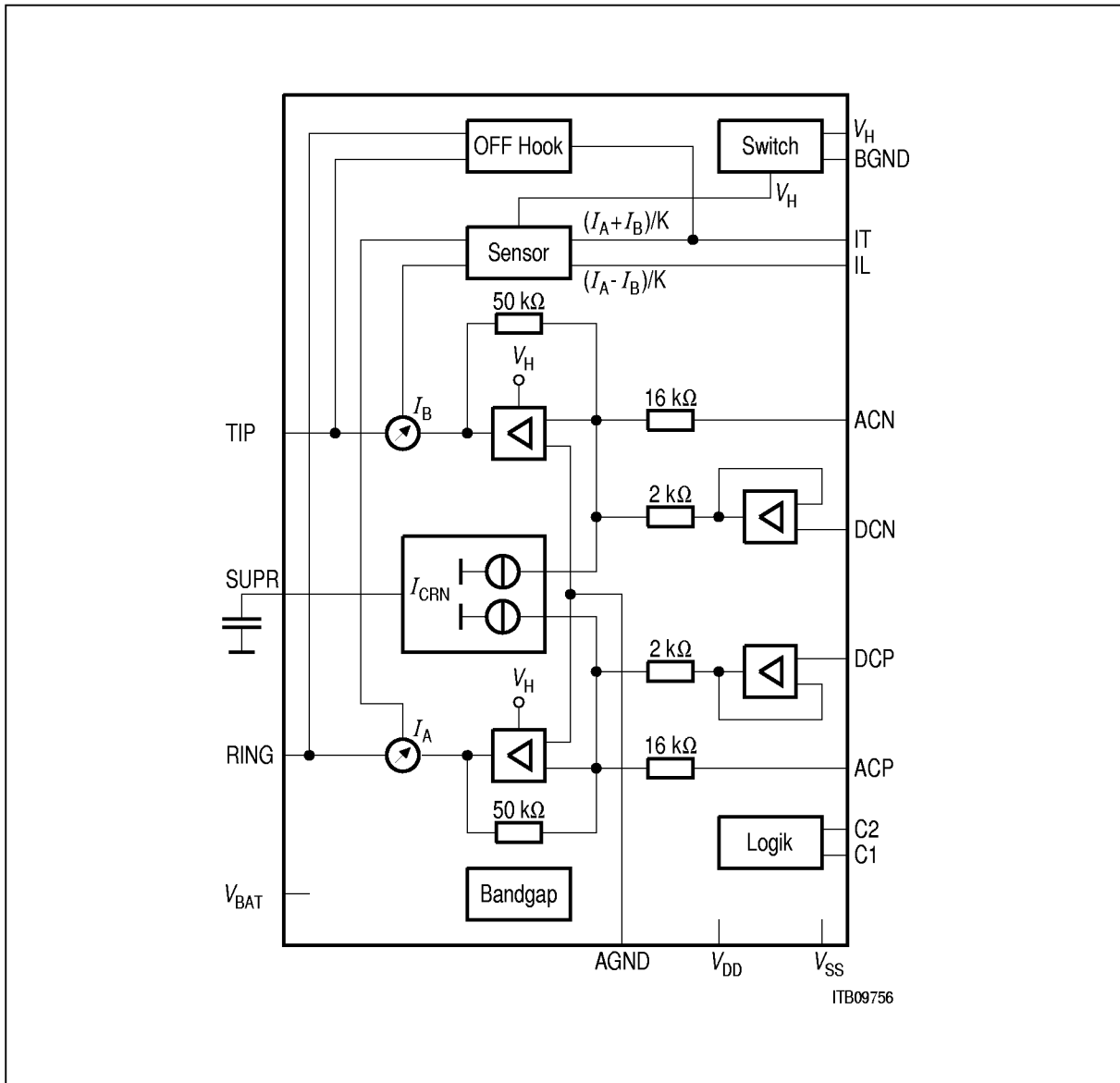
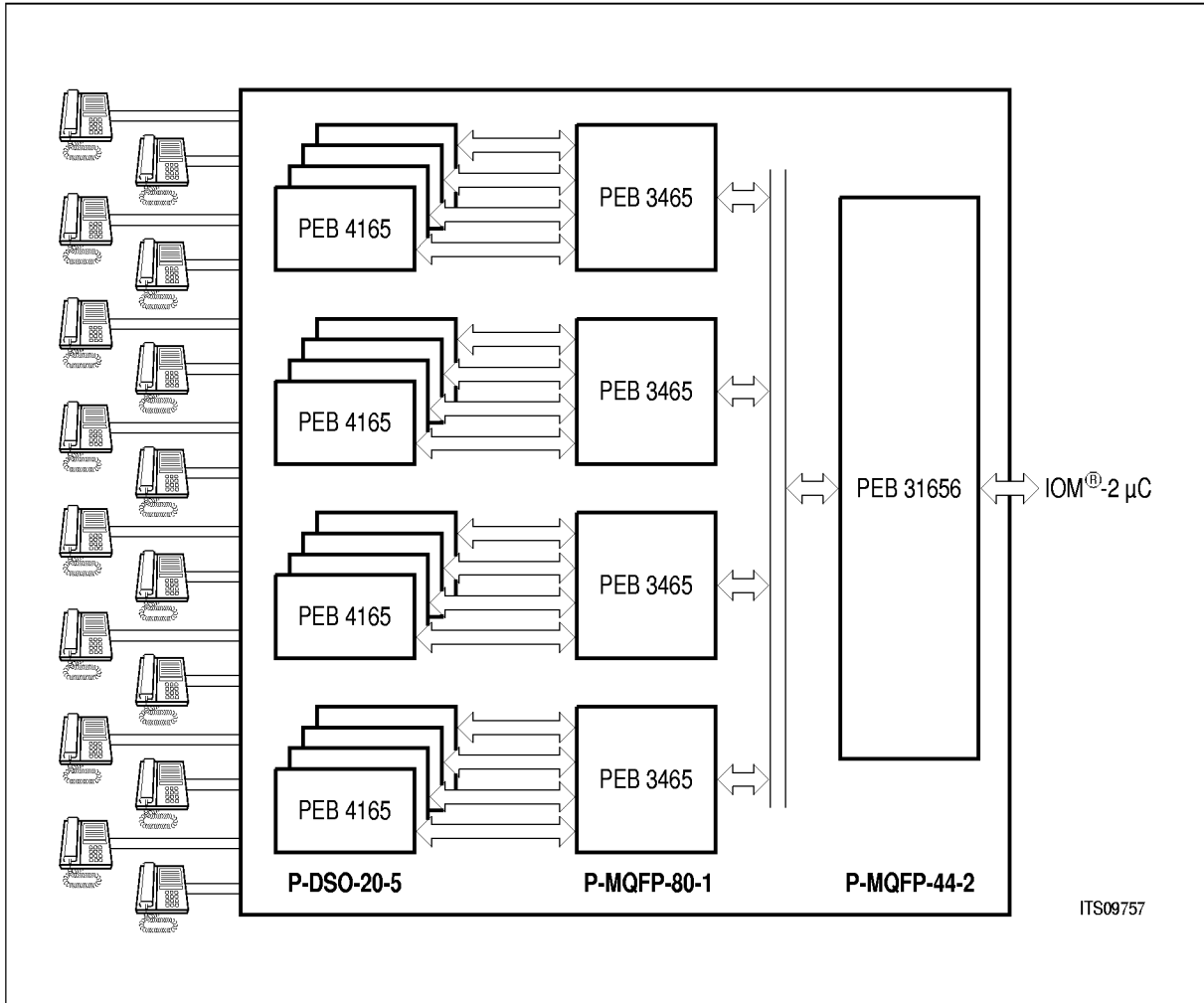


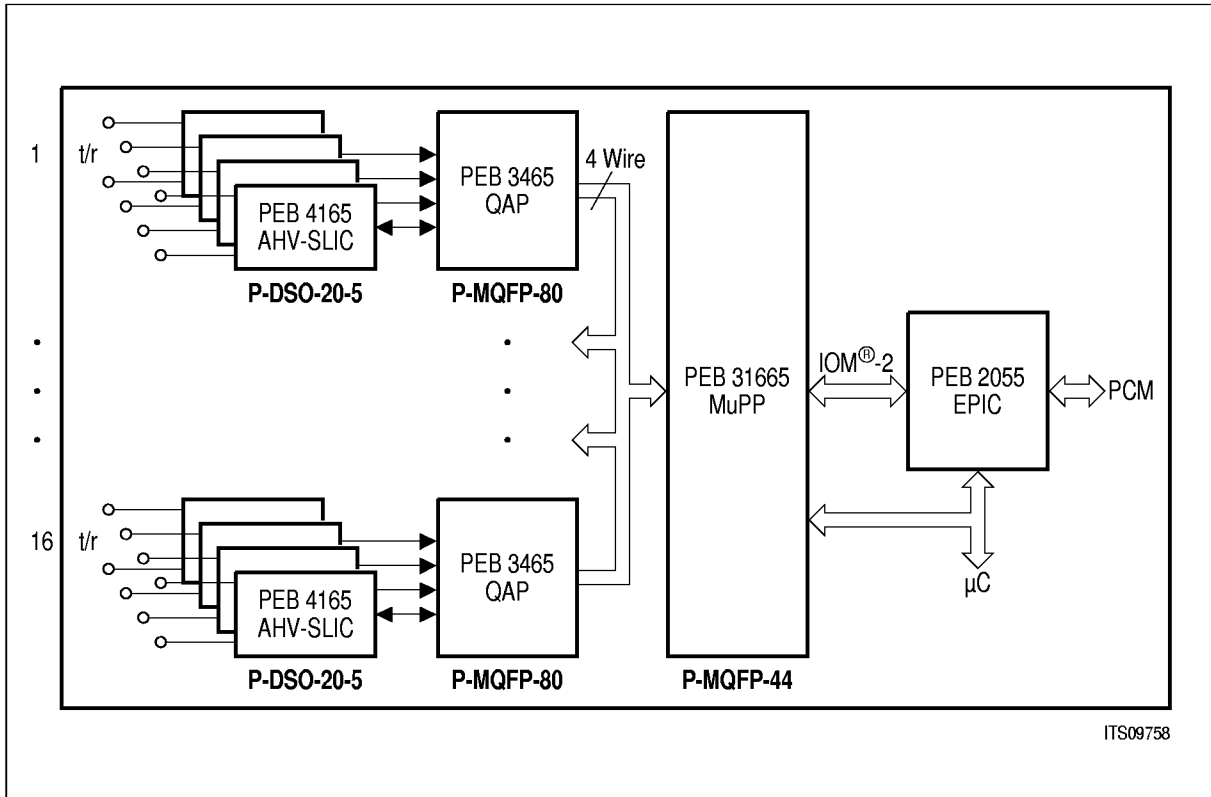
Figure 9

**1.5 System Integration**

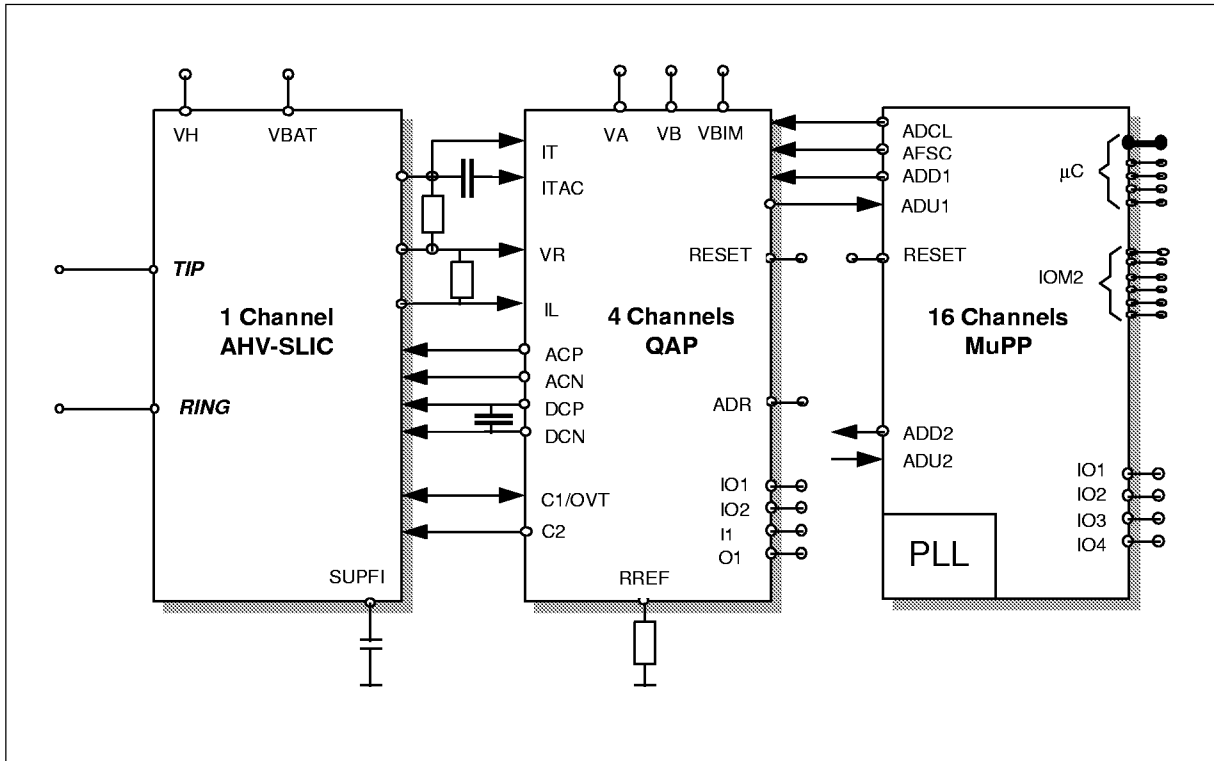


**Figure 10 Block Figure of an Analog Linecard for 16 Subscribers Using MuSLIC**

**Introduction**



**Figure 11 Application Example of a Central Office Analog Linecard for 16 Subscribers**



**Figure 12 Overview of the Connection of MuPP, QAP and AHV-SLIC for One Subscriber**

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**Functional Description****2 Functional Description**

The Multichannel Signal Processing Subscriber Line Interface Codec Filter Chipset, MuSLIC, is a logic continuation of the well established family of the SIEMENS PCM-Codec-Filter-ICs with the integration of all DC-feeding, Supervision and Meterpulse Injection features on chip as well. Fabricated in advanced CMOS, BiCMOS and High Voltage Technology SPT170 the MuSLIC is tailored for very flexible solutions in analog/digital communication systems.

The chip set consists of the digital signal processor for 16 channels (MuPP, multichannel processor for POTS), the analog/digital and digital/analog converter for 4 channels (QAP, quad analog POTS) and the high voltage interface chip for 1 channel (AHV-SLIC, advanced high voltage subscriber line interface circuit).

The MuPP uses the benefits of a DSP not only for the voice channel but even for line feeding and supervision which leads to a very high flexibility without the need of external components. Based on an advanced digital filter concept, the PEB 31665 (MuPP) and the PEB 3465 (QAP) provides excellent transmission performance. The new filter concept leads to a maximum of independence between the different filter blocks. Each filter block can be seen as a one to one representative of the corresponding network element. Together with the software package MuSLICOS, filter optimizing to different applications can be done in a clear and straight forward procedure. The AC frequency behavior is mainly determined by the digital filters. Using the oversampling 1 bit  $\Sigma\Delta$ -AD/DA converters, linearity is only limited by second order parasitic effects.

The digital solution of line feeding offers free programmability of feeding current and voltage as well as very fast settling of the dc-operating point after transitions. A 0.3 Hz lowpass filter in the DC-loop is mainly responsible for the system stability.

Additionally teletax generation and filtering is implemented as well as free programmable balanced ring generation with zero-crossing injection. Offhook detection with programmable thresholds is possible in all operating modes. To reduce overall power consumption of the linecard, the MuPP, the QAP and the AHV-SLIC provide a Power Down mode.

To program the MuSLIC or to get status information about the chipset or the system 2 user interfaces are available: the IOM-2 interface and a 8-bit-parallel simple microcontroller interface.

The PEB 4165 (AHV-SLIC) provides battery feeding between – 24 V and – 80 V and ringing injection with a differential ring voltage up to 85 Vrms. In order to achieve these high amplitudes, an auxiliary positive battery voltage is used during ringing. This voltage can also be applied to drive very long telephone lines.

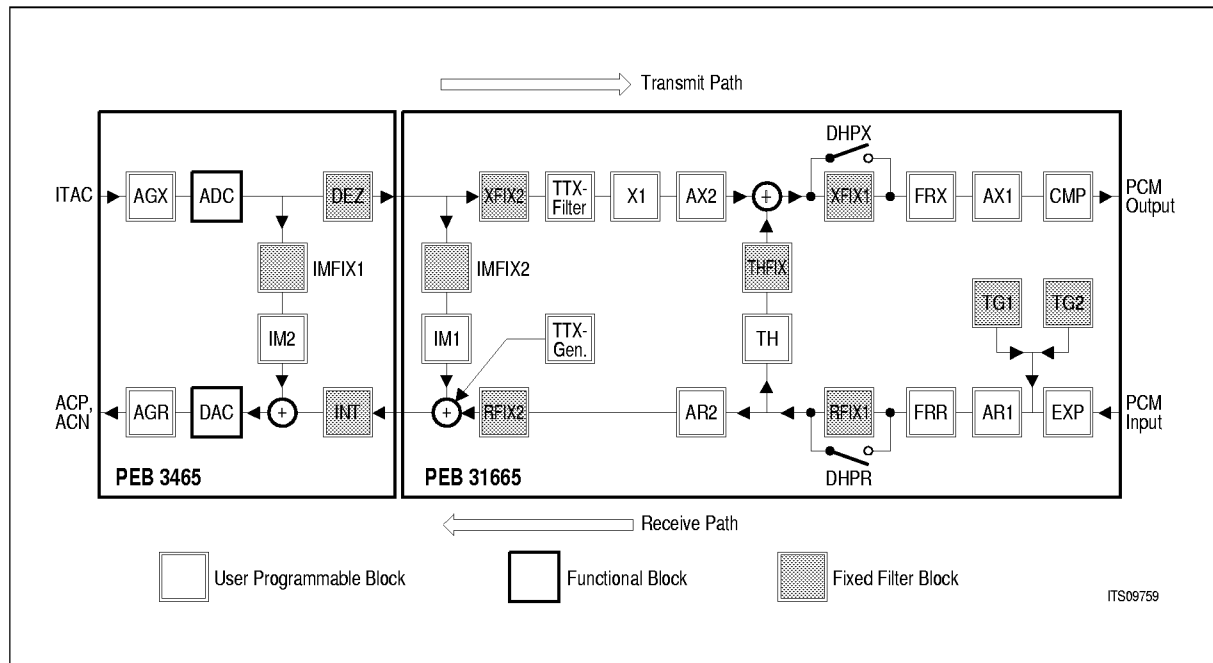
The AHV-SLIC is designed for a voltage feeding - current sensing line interface concept and provides sensing of transversal and longitudinal currents on both wires. In Power Down mode the AHV-SLIC is switched off turning the line outputs to a high impedance state. Off-hook supervision is provided by activating a simple line current sensor.



**Functional Description**

**2.1 Principles**

**2.1.1 Signal Flow Graph: AC**



**Figure 13**

**Transmit Path**

The analog input signal has to be connected to pin ITAC of the PEB 3465 by an external capacitor (470 nF) for AC/DC separation. After passing a programmable gain stage (AGX = 0 or 6 dB) and a simple antialiasing prefilter the voice signal is converted to a 1-bit digital data stream in the  $\Sigma\Delta$ -converter. The first down sampling steps are done in fast running digital hardware filters on the PEB 3465. This down sampled AC-signal (64 kHz sampling rate) is sent to the PEB 31665 via the MuPP/QAP-Interface in the ADU-channel. The following signal processing is done in the DSP-machine of the PEB 31665. The benefits of this are the programmability of frequency and gain behavior. At the end the fully processed signal is transferred to the IOM-2 Interface in a PCM-compressed (A-law /  $\mu$ -law) signal representation.

Functional Description

Receive Path

The digital input signal is received via the IOM-2 Interface of the PEB 31665. Expansion, PCM-lowpass-filtering, gain correction and frequency response correction are the next steps which are done by the DSP-machine. This 64 kHz AC signal is sent from the QAP to the MuPP via the MuPP/QAP-Interface in the ADD-channel. The up sampling interpolation steps are processed by fast hardware structures in the PEB 3465 to reduce the DSP-workload. The 1-bit data stream is then converted to an analog equivalent. A subsequent programmable gain stage (AGR = 0 or 6 dB) and smoothing filter provides the AC output signal at the Pins ACP and ACN of the PEB 3465 for direct connection to the AHV-SLIC PEB 4165.

Loops

There are two different loops implemented: The Impedance Matching (IM) loop which is divided into 2 separate loops to guarantee very high flexibility to various impedances, and the Transhybrid Balancing (TH) loop.

For test purposes it is possible to close a loop behind the  $\Sigma\Delta$ -converter to check either the analog of the digital part of the PEB 3465 and the PEB 31665 respectively.

2.1.2 Signal Flow Graph: DC

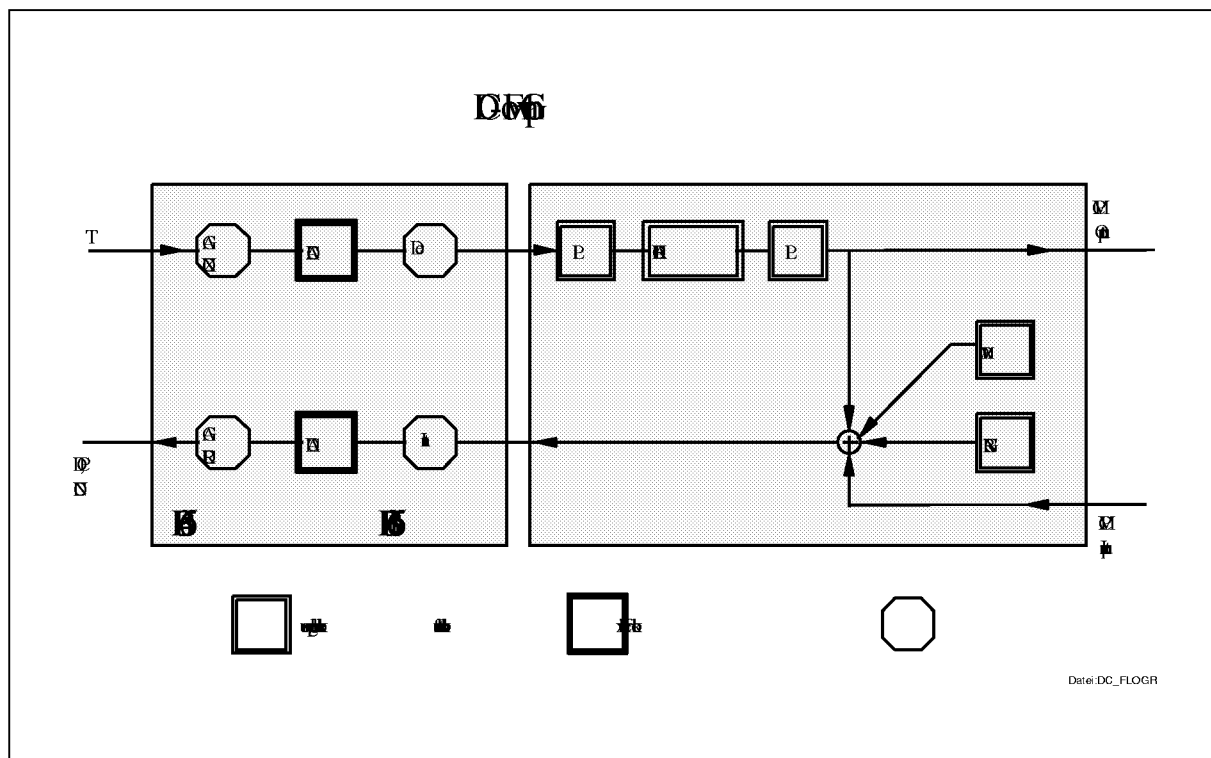


Figure 14

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## Functional Description

### DC Characteristic

The incoming information (transmit direction) at pin IT (scaled transversal AC + DC-current, transferred to a voltage via an external 1.5 k $\Omega$  resistor at IT) passes first an antialiasing filter and is then converted to a 1-bit digital data stream in the  $\Sigma\Delta$ -converter. Down sampling is done in hardware filters of the PEB 3465. This DC-information (2 kHz sampling rate) is then fed to the PEB 31665 where it is first lowpass filtered (0.3 Hz corner frequency) for stability and noise reasons. The following DC-characteristic consists of three branches which represents different kinds of feeding behavior. In typical applications it acts as a programmable constant current source ( $R_{in} > 30$  k $\Omega$ ). If the desired value cannot be held feeding switches automatically and smoothly to the resistive branch ( $R_{in}$  programmable between 0 ... 1 k $\Omega$ ). The third branch is used for feeding long lines - the DC-characteristic switches to a constant voltage behavior. For superimposing voice as well as Teletax pulses the necessary drop at the line can be calculated and taken into account as well. The outgoing bit stream (2 kHz sampling rate), representing the DC-feeding value is then sent back to the PEB 3465 where a 1-bit  $\Sigma\Delta$ -converter and a following smoothing filter (using an external 33 nF capacitor) establish the desired values at the Pins DCP and DCN, respectively. Depending on the operating mode (Active, Ringing, Active with Boosted Battery) a gain of 0 or 4 dB is inserted.

For test purposes it is possible to close a loop to test either the analog part or the digital part of the DC path.

### Supervision

The HOOK-information is the most important one and is provided via the IOM-2 Interface (CIDU-4: HOOK; see **chapter 4.2**), in all operating modes:

- **Power Down:** In this state the transversal line current is sensed by the PEB 4165 and fed to the PEB 3465 via Pin IT. Offhook is detected if the voltage at IT exceeds a programmed value.
- **Active:** Offhook is detected if the incoming voltage at IT exceeds a programmed value. To avoid instable information, lowpass filtering and a hysteresis is provided.
- **Ringing:** Offhook is detected if the DC-value at IT exceeds the programmed Ring Trip threshold. The AC-value is filtered automatically. Ring Trip detection is reported within 2 cycles of the ring period and then the internal ring generator is switched off within 2 cycles at zero crossing of the ring voltage.

For Ground Key information the PEB 4165 provides the longitudinal current information at the Pin IL. The PEB 3465 uses a  $\Sigma\Delta$ -converter - similar to the DC-transmit path - to convert this signal to its digital representation. The accuracy is  $\pm 10\%$  compared to  $\pm 5\%$  of the DC-path. The 1-bit digital data stream is also down sampled and sent to the

**Functional Description**

PEB 31665 via the ADU-channel of the MuPP/QAP-Interface. Generation of the Ground Key bit is done in the PEB 31665 (CIDU-3: GNK; see **chapter 4.2**)

**Additional Features**

The PEB 3465 provides three general purpose input Pins (VA, VB, VBIM) for measuring. Via the MuPP/QAP-Interface it is possible to select one of these inputs for the measurement. The DC-signal at the selected input is converted to digital using the same  $\Sigma\Delta$ -converter as for Ground Key information (accuracy of  $\pm 10\%$ ) and sent to the PEB 31665. The input range is between  $-2.4\text{ V} \dots +2.4\text{ V}$ . As a further selection it is also possible to measure the internal VDDZ-voltage of the PEB 3465.

**2.1.3 AHV-SLIC**

The Advanced High Voltage Subscriber Line IC (AHV-SLIC) PEB 4165 is a reliable interface between the telephone line and the PEB 3465/PEB 31665.

The PEB 4165 supports AC and DC control loops based on feeding a voltage  $V_{RT}$  to the line and sensing the transversal line current  $I_{RT}$  (**figure 15**).

DC- and AC-voltages are handled separately with different gain on the AHV-SLIC. Both are applied differentially via pins DCP, DCN, and ACP, ACN, respectively. The line voltages  $V_R$  and  $V_T$  are the amplified input voltages, related to the mean supply voltage,  $V_T = VTIP = (VH' - VBAT) / 2 - 25 \times VDCN - 50/16 \times VACN$

$$V_R = VRING = (VH' - VBAT) / 2 - 25 \times VDCCP - 50/16 \times VACP.$$

Depending on the operation mode, VH' is switched either to VH or to BGND via the supply switch. The transversal line voltage  $V_{RT} = V_R - V_T$  is simply related to the input voltages

$$V_{RT} = 25 \times (VDCCP - VDCN) + 50/16 \times (VACP - VACN) = 50 \times VDCCP + 6.25 \times VACP$$

A reversed polarity of  $V_{RT}$  is easily obtained by changing the sign of  $(VDCCP - VDCN)$ .

The transversal and longitudinal currents are measured in the buffers and scaled images are provided at the IT and IL pin, respectively:

$$IT = (I_R + I_{TIP})/100 = I_{RT}/50 \qquad IL = -(I_R - I_{TIP})/100 = -I_{Long}/50$$

Functional Description

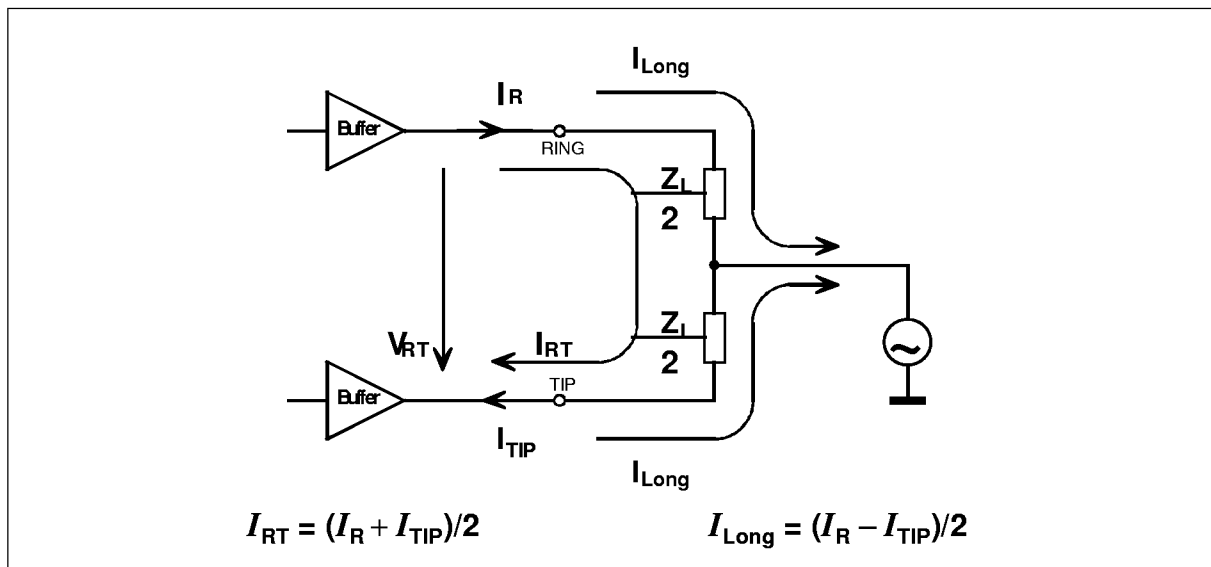


Figure 15 Definition of Output Current Directions

The PEB 4165 operates in four modes controlled by ternary logic signals at the C1 and C2 input (see table 3).

Table 3 Programming of Operating Modes

		C 2 (Pin 9)		
		VIL	VIM	VIH
C 1(Pin 8)	VIL	PDNH	PDNR	HIR
	VIM	PDNH	BB	HIT
	VIH	PDNH	ACT	HIRT

HIR ... Ring wire set to high impedance

HIT ... Tip wire set to high impedance

**High Impedance (HIR/HIT/HIRT):** In this mode each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while the current through the RING output still can be measured by IT or IL. Programming HIR switches off the RING buffer. In the mode HIRT both buffers show high impedance.

**Active (ACT):** This is the regular transmit and receive mode for voiceband and teletax. The line driving section is operated between VBAT and BGND.

**Boosted battery (BB):** In order to provide a balanced ring signal of up to 85 Vrms or to drive longer telephone lines, an auxiliary positive battery voltage VH is used, enabling a higher voltage across the line. Transmission performance remains unchanged compared with ACT mode.

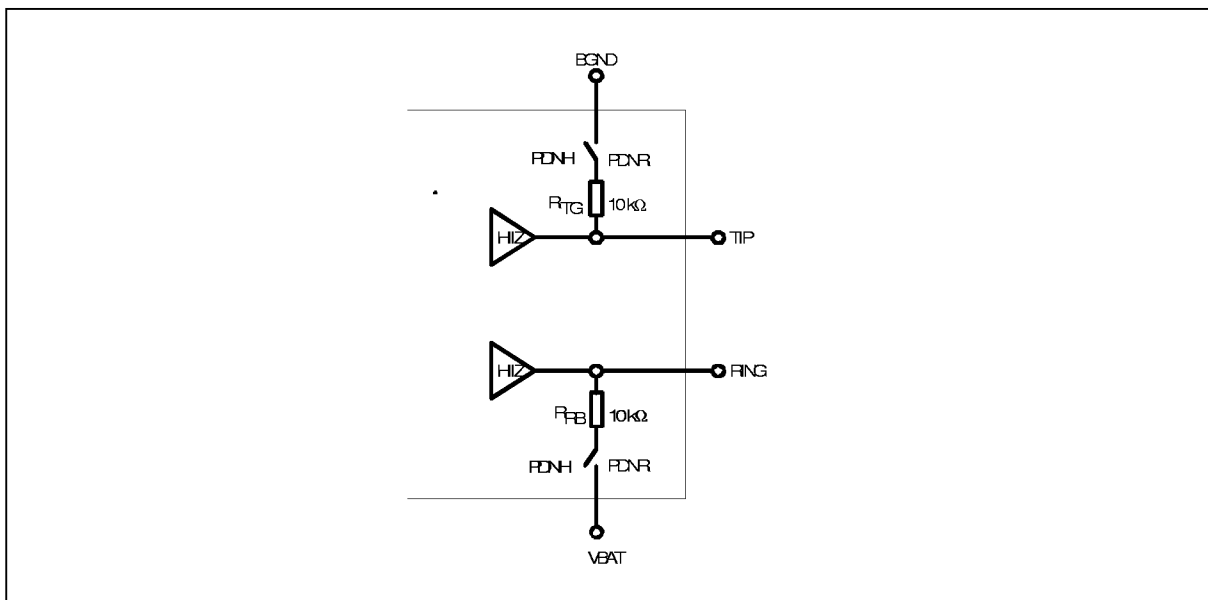
**Functional Description**

The **Power Down (PDN)** state is intended to reduce power consumption of the linecard to a minimum: the PEB 4165 is switched off completely, no operation is available.

With respect to the output impedance of TIP and RING two PDN-modes have to be distinguished:

A resistive one (PDNR) provides a connection of 10 kΩ each from TIP to BGND and RING to VBAT, respectively, while the outputs of the buffers show high impedance (**figure 16**). The current through these resistors is sensed and transferred to the IT pin to allow offhook supervision.

The other mode (PDNH) offers high impedance at TIP and RING.



**Figure 16 TIP and RING Impedance in Power Down**

**2.1.4 Test Features**

There are two different kinds of test features: Internal test loops for circuit testing and defined test loops to perform board and line tests. There are loops for testing AC and DC path. As a special feature it is possible to switch signals to and from the DC-path via the IOM-2 Interface. Additionally there is the possibility to cut off the AC-receive and transmit path (the different kinds of testmodes are described in **chapter 8**).

3 Interfaces

3.1 IOM<sup>®</sup>-2 Interface

The IOM-2 Interface consists of two data lines and two clock lines. DU (data upstream) carries data from the MuSLIC to a master device. DD (data downstream) carries data from the master device to the MuSLIC. A frame synchronization clock signal (8 kHz, FSC) as well as a data clock signal (4096 kHz, DCL) has to be supplied to the MuSLIC. The MuSLIC handles data as described in the IOM-2 specification for analog devices (see **chapter 10.1**).

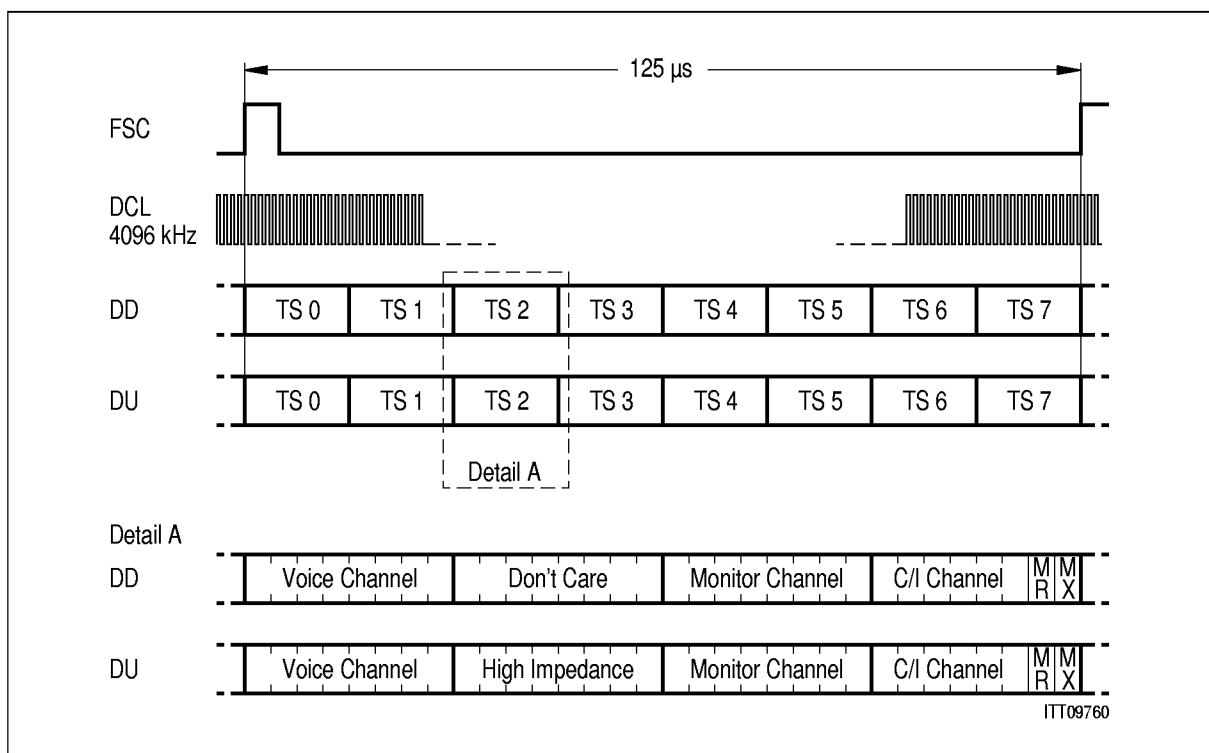
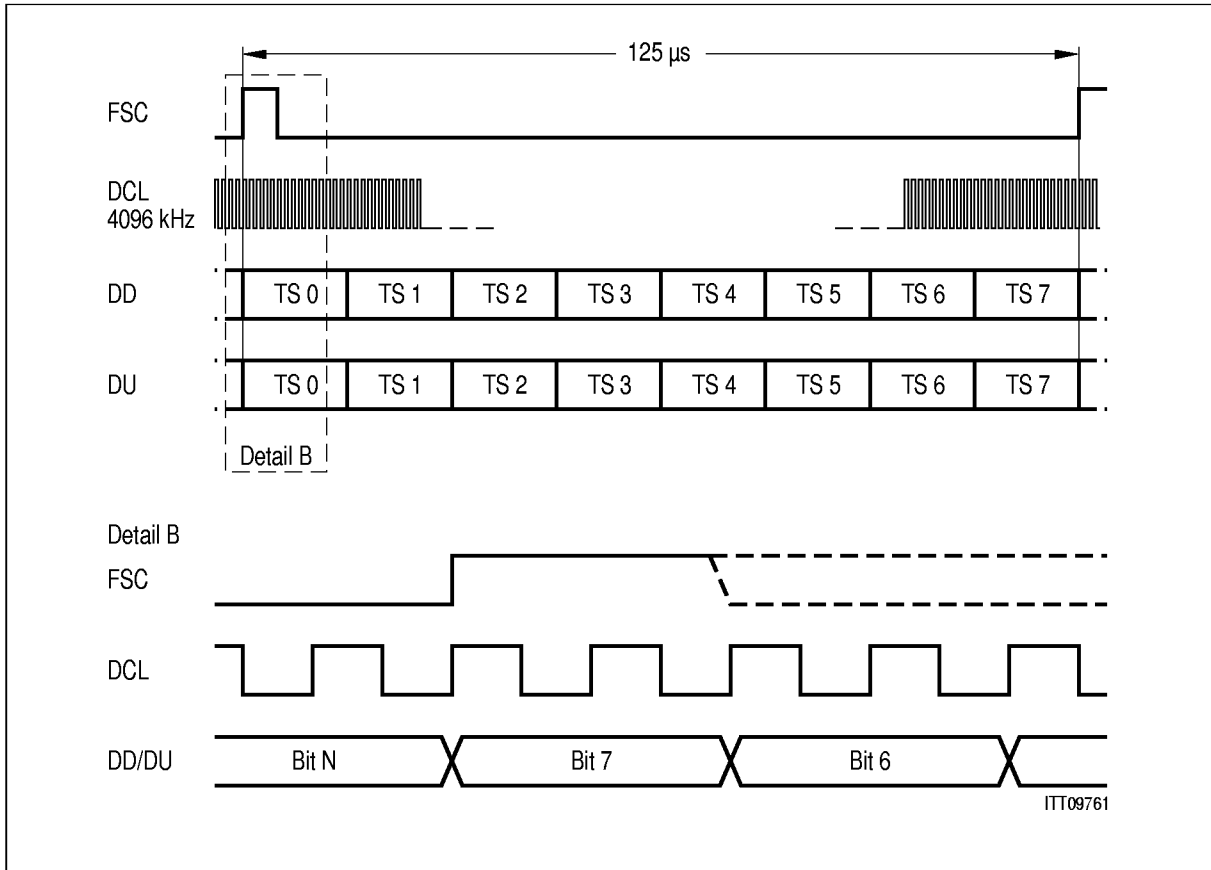


Figure 17 IOM<sup>®</sup>-2 Interface Timing for 8 Voice Channels (per 8 kHz frame)

**Interfaces**



**Figure 18 IOM<sup>®</sup>-2 Interface Timing (DCL = 4096 kHz, per 8 kHz frame)**



Interfaces

IOM<sup>®</sup>-2 Time Slot Assignment

An assignment of 16 time slots is given by the two IOM-2 interfaces of the MuPP. Each of them assigns 8 time slots synchronized with the FSC. This 8 slot structure is carried on from the MuPP to the QAP. In the QAP the assignment is partly done by pin-strapping (see figure 19).

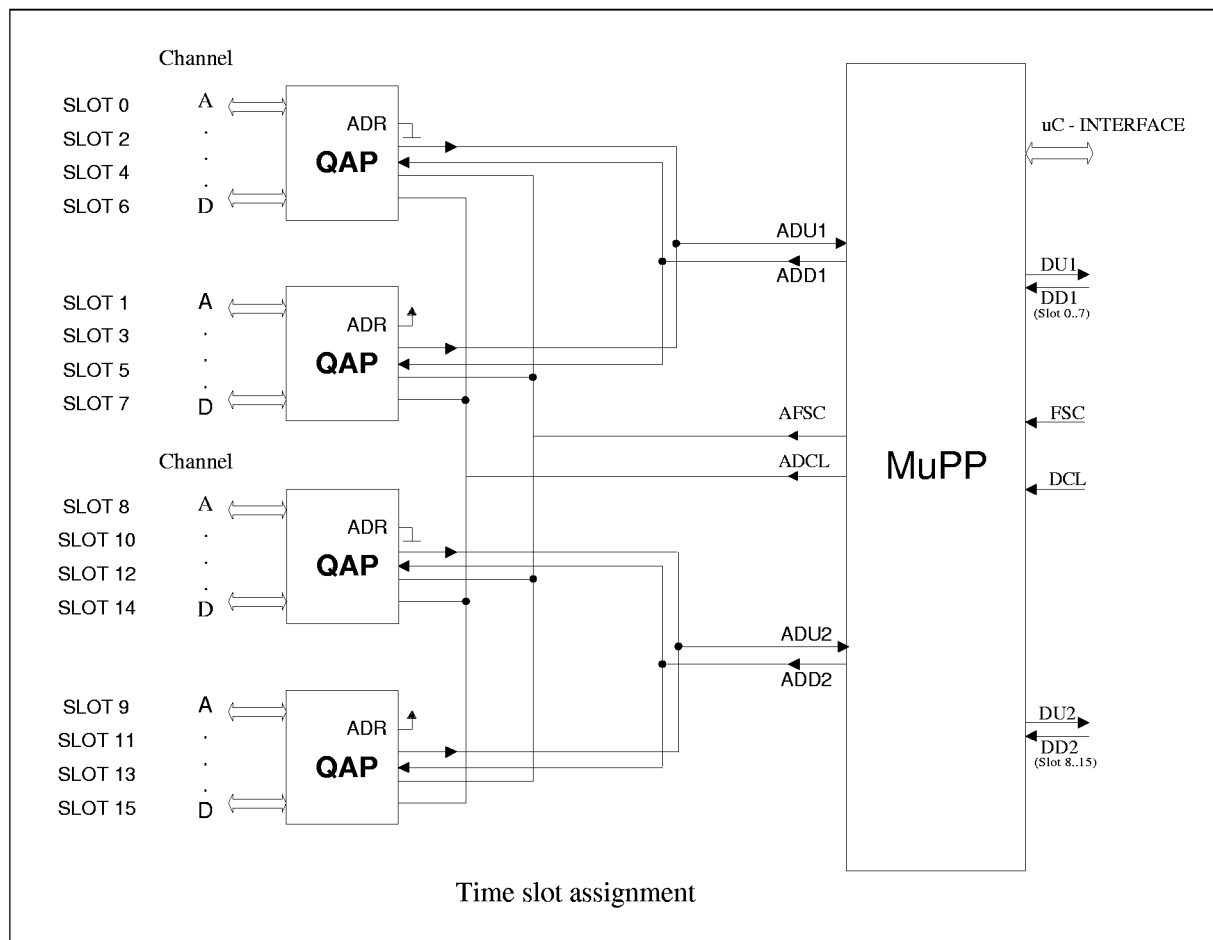


Figure 19 Time Slot Assignment

3.2  $\mu$ C Interface

The parallel  $\mu$ C-Interface is used to communicate with an external master device and consists of four control lines (ALE, CSQ, RDQ, WRQ) and 8 bidirectional data lines (DIO0 ... DIO7) and provides fast parallel data transfer to a microcontroller device as an alternative to the IOM-2 monitor channel data transfer. Only one method of transfer can be used at a time, with the  $\mu$ C-Interface having a higher priority than the IOM-2 Interface. Thus, data transfer via the  $\mu$ C-Interface interrupts a communication via the IOM-2 monitor channel. During a data transfer cycle via the  $\mu$ C-Interface, IOM-2 monitor channel data will be ignored. The C/I-channel information is still transferred via the C/I-channel of the IOM-2 interface and is not affected by the  $\mu$ C-Interface communication.

The  $\mu$ C-Interface of the MuPP has a multiplexed 8-bit address/data bus and allows direct connection to a microcontroller of the 8051- and the Siemens C16X-family without additional components.

With every falling edge of ALE-line the MuPP latches the bus data on the 8 data lines DIO0 ... DIO7 and stores it as address information. CSQ combined with RDQ or WRQ starts the data transfer cycle via the parallel  $\mu$ C-Interface. The data on DIO0 ... DIO7 are valid on the rising edge of WRQ/RDQ (if CSQ is low). Depending on the previously latched address information, these data have a different meaning; e.g. the 8 bit of a command/data byte is preceded by the address 00000001 or the subscriber/slot address for a subsequent data byte of a e.g. SOP-, TOP-, or COPI-command has the address information 00000000 (see **table 4**).

A data transfer cycle to address 00000000 and 11111111 is already finished after the transfer of the first data byte; transfer cycles to addresses 00000001 and 00000010 consists of more transfers, depending on the length information in the first byte.

As soon as the data transfer cycle via the  $\mu$ C-Interface has been completed, control information via the IOM-2 monitor channel will be accepted again (synchronized with the next FSC), until the next data transfer cycle starts with CSQ and RDQ/WRQ.

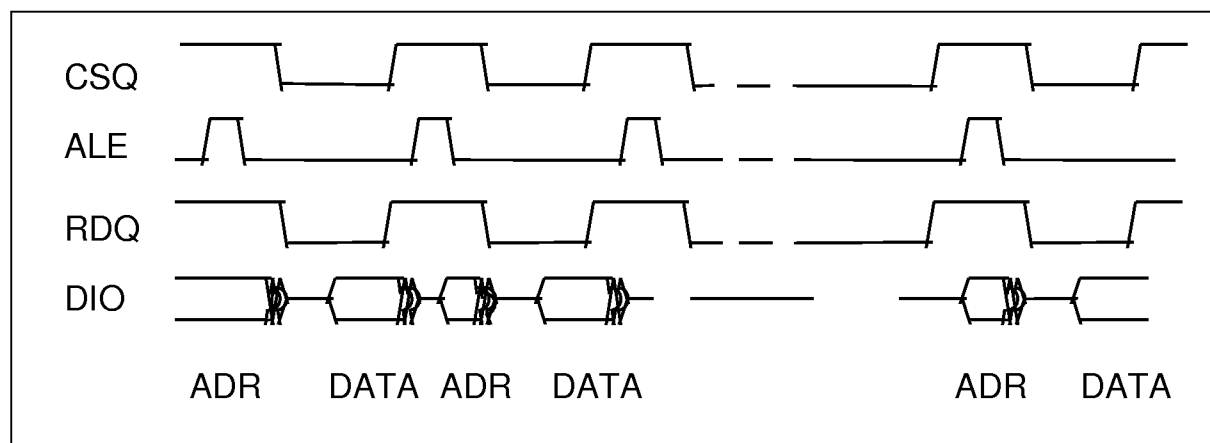
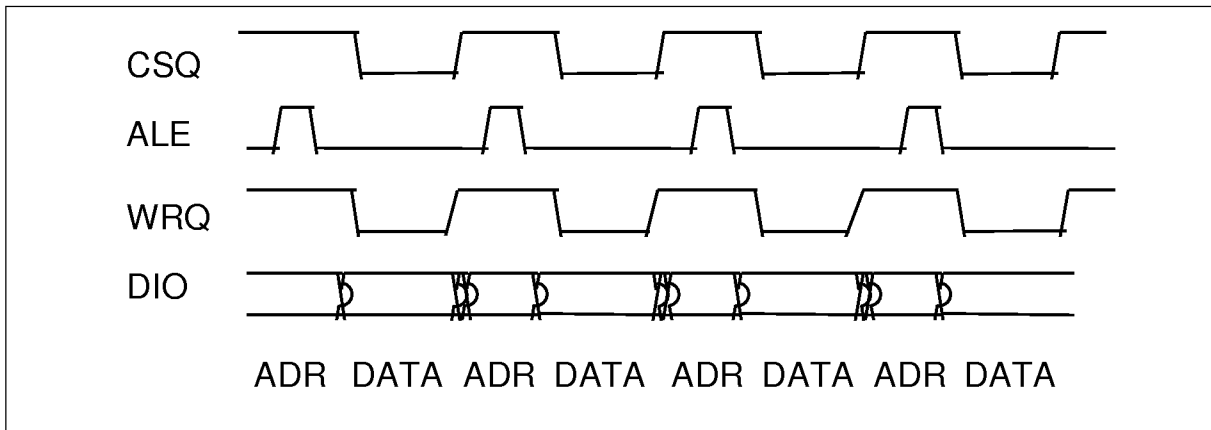


Figure 20 Example for a Read Access, with One Data Byte Transferred via DIO

**Interfaces**



**Figure 21 Example for a Write Access, With One Data Byte Transferred**

**Table 4 Possible Address Information to Identify the Following Data Nibbles**

Address	Command
00000000	address
00000001	data
00000010	status
...	reserved
11111111	reset $\mu$ C Interface

Data transfer to and from the MuSLIC is asynchron and the data will be transferred in bytes. Basically there is no difference to the IOM-2 commands, accept those which requires a slot specific address information.

### 3.3 MuPP/QAP Interface

The MuPP/QAP-Interface, the link between the MuPP and the QAP, is a serial interface based on the 6 signals AFSC (analog frame sync), ADCL (analog data clock), ADU1/ADU2 (analog data upstream) and ADD1/ADD2 (analog data downstream). ADU1 and ADD1 are common to the first group of 8 time slots (channels) and ADU2 and ADD2 to the second 8 time slots (channels). AFSC and ADCL are common to both groups of time slots (timing diagram see **chapter 7.2.6**).

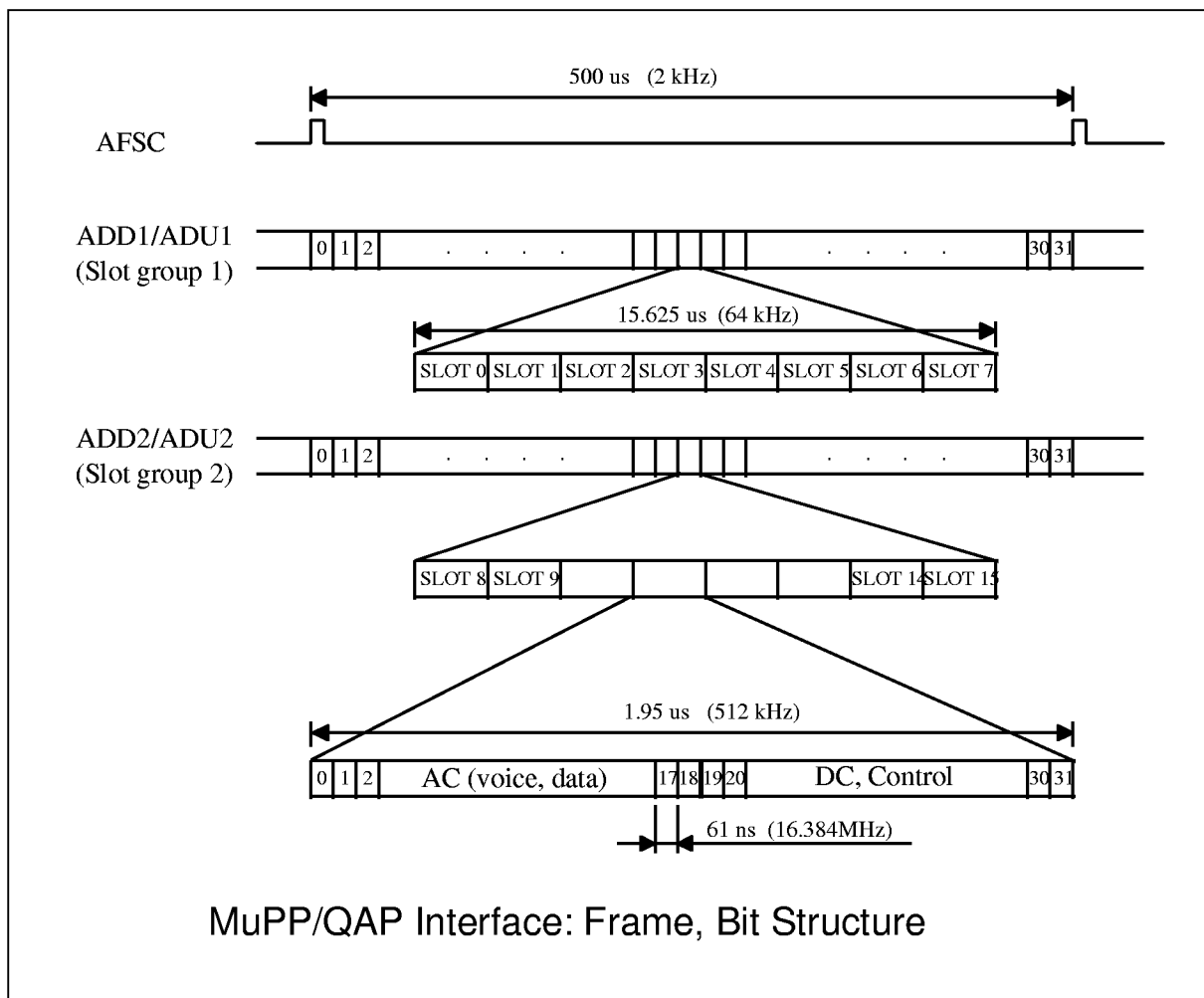


Figure 22 MuPP/QAP Interface: Frame, Bit Structure

### 3.4 QAP/AHV-SLIC Interface

#### Output Voltage AC (ACP, ACN)

The output voltage at the pins ACP and ACN represents the AC-information together with Teletax info at the receive path. The AC-information is received via the MuPP/QAP-Interface in the ADD channel. The 64-kHz Bitstream is converted to analog, passes a programmable gain stage of 0 / – 6 dB and is buffered to drive a load of  $R_L > 15 \text{ k}\Omega$  and  $C_L < 10 \text{ pF}$ , which is the input impedance of the AHV-SLIC.

#### Output Voltage DC (DCP, DCN)

The output voltage at the pins DCP and DCN represents the DC-information together with the Ring Burst at the receive path. The DC-information is received via the MuPP/QAP-Interface in the ADD channel. The 2-kHz Bitstream is converted to analog and buffered to drive an external smoothing capacitor of 33 nF. The pins are directly connected to the AHV-SLIC.

#### Transversal Current Sense AC - Input (ITAC)

The pin ITAC is the input voltage pin for the AC transversal current information from the AHV-SLIC in the transmit path. AC/DC separation is done by an external highpass filter (ext. capacitor = 470 nF). The input resistance is larger than 20 k $\Omega$ . Current/voltage conversion is done via an external resistor of 1.5 k $\Omega$  (same for pin IT). The signal passes a programmable gain stage 0 or 6 dB, is converted to digital and sent to the PEB 31665 via the MuPP/QAP-Interface in the ADU channel (64-kHz Bitstream).

#### Transversal Current Sense DC - Input (IT)

The pin IT is the input voltage pin for the DC transversal current information from the AHV-SLIC in the transmit path. The input resistance is larger than 500 k $\Omega$ . Current/voltage conversion is done via an external resistor of 1.5 k $\Omega$  (same for pin ITAC). The voltage at Pin IT is lowpass filtered and converted to digital. The bitstream (2 kHz) is sent to the PEB 31665 via the MuPP/QAP-Interface for further signal processing.

#### Longitudinal Current Sense - Input (IL)

The scaled longitudinal current information transferred from the AHV-SLIC - the current/voltage conversion is done by an external resistor of 1.5 k $\Omega$  - is converted into digital and sent to the PEB 31665 via the MuPP/QAP-Interface in the ADU channel. In the PEB 31665 the IL-information is lowpass filtered (time programmable using DUPGNK-counter) and reported via the Data Upstream C/I-channel (CIDU-3) of the IOM-2 interface if the measured value exceeds a programmed limit. In Power Down, the GNK-bit is set to "0" and the setting of the Interrupt bit (CIDU-3) caused by GNK is prohibited.

**Interfaces**

**Ternary Interface (C1, C2)**

In order to set the AHV-SLIC to the different operating modes, the information of the board-controller is passed through from the IOM-2-channel via the MuPP/ QAP-Interface to the ternary AHV-SLIC-Interface pins C1 and C2.

**Table 5**

		C2		
		VOL	VOM	VOH
C1	VOL	PDNH	PDNR	HIR
	VOM	ACT2	BB	HIT
	VOH	ACT3	ACT	HIRT

- PNDH - Power Down High Impedance
- PDNR - Power Down Resistive
- ACT - Active Mode
- ACT2 - Active Mode 2 (power save for SLIC, for future use)
- ACT3 - Active Mode 3 (power save for SLIC, for future use)
- BB - Boosted Battery
- HIR - Ring wire set to high impedance
- HIT - Tip wire set to high impedance
- HIRT - Ring and Tip wires set to high impedance

For signalling “Over temperature” the AHV-SLIC drains a current (IOT) from pin C1. This current is sensed by the PEB 3465 and transferred in the ADU channel to the PEB 31665. The PEB 31665 sends the overtemperature message via the C/I-channel (CIDU-2: SLCX and TCR0-5) of the IOM-2 Interface. This is possible in any operating states of the AHV-Interface except for Power Down.

**Programming the MuSLIC**

**4 Programming the MuSLIC**

With the appropriate commands, the MuSLIC can be programmed and verified very flexible via the IOM-2 Interface Monitor channel, and the Microcontroller Interface respectively.

**Transfer via the IOM<sup>®</sup>-2 Interface**

Data transfer to the MuSLIC starts with a MuSLIC-specific address byte (81<sub>H</sub>).

With the second byte one of 5 different types of commands (SOP, TOP, XOP, COP or COPI) is selected. Due to the extended MuSLIC feature control facilities these commands contain additional information (e.g. number of subsequent bytes) for programming (write) and verifying (read) the MuSLIC status.

A write command is followed by up to 8 bytes of data. The MuSLIC responds to a read command with its IOM-2 specific address and the requested information, that is up to 15 bytes of data.

**Attention:** Each byte of the monitor channel has to be transferred twice at least according to the IOM-2 Monitor handshake procedure. (For more information on IOM-2 specific Monitor Channel Data Structure see **chapter 3.1** and **chapter 10**).

**Transfer via the Microcontroller Interface**

Data transfer to and from the MuSLIC is asynchron and the data will be transferred in bytes. Basically there is no difference to the IOM-2 commands.

(For more information, about the  $\mu$ C Interface see **chapter 3.2**).

**4.1 Types of Monitor /  $\mu$ C Interface Bytes**

The 8-bit Monitor /  $\mu$ C Interface bytes have to be interpreted as either commands or status information stored in Configuration Registers or the Coefficient RAMs. There are 5 different types of MuSLIC commands which are selected by bit 4 and 5 (partly bit 2 and 3) as shown below.

<b>SOP</b>	<b>STATUS OPERATION:</b>				MuSLIC status setting/monitoring			
Bit	7	6	5	4	3	2	1	0
	<b>B</b>	<b>RW</b>	<b>0</b>	<b>1</b>	<b>ATR</b>	<b>LSEL2</b>	<b>LSEL1</b>	<b>LSEL0</b>

<b>XOP</b>	<b>EXTENDED OPERATION:</b>				General settings			
Bit	7	6	5	4	3	2	1	0
	<b>0</b>	<b>RW</b>	<b>1</b>	<b>0</b>	<b>ATR</b>	<b>LSEL2</b>	<b>LSEL1</b>	<b>LSEL0</b>

**Programming the MuSLIC**

<b>TOP</b>	<b>TRANSFER OPERATION:</b>			Read Certain Status / Options only				
Bit	7	6	5	4	3	2	1	0
	0	R	1	1	0	0	LSEL1	LSEL0
<b>COP</b>	<b>COEFFICIENT OPERATION:</b>			Filter coefficient setting/monitoring				
Bit	7	6	5	4	3	2	1	0
	ICRAM	RW	0	0	0	1	WCRAM1	WCRAM0
<b>COPI</b>	<b>COEFFICIENT OPERATION INITIALIZE:</b>			Coefficient set assignment				
Bit	7	6	5	4	3	2	1	0
	B	RW	0	0	1	0	LSEL1	LSEL0

**Table 6 Storage of Programming Information**

6 status configuration registers: (for each channel)	SCR0, ... SCR5 accessed by SOP command
2 test registers: (for each channel)	STCR0, STCR1 accessed by SOP command
9 extended configuration registers:	XR0 ... XR8 accessed by XOP command
18 extended test registers:	XTR0 ... XTR17 accessed by XOP command
2 Transfer configuration registers: (for each channel)	TCR0, TCR1 accessed by TOP command
AC- and DC-Coefficient RAMs:	CRAMs accessed by COP command
2 coefficient set assignment registers: (for each channel)	CAR0, CAR1 accessed by COPI command



**Programming the MuSLIC**

Overview of commands and registers via the IOM-2/ $\mu$ C Interface:

**SOP Command**

Bit	7	6	5	4	3	2	1	0
SOP for SCR/STCR	B	RW	0	1	ATR	LSEL2	LSEL1	LSEL0

**SOP Configuration Registers**

Bit	7	6	5	4	3	2	1	0
SCR0	POLNR	N/BB	LB	ETG2	ETG1	ENO	ENTE	COR
SCR1	TTXNO	TTX12	NOSL	SOREV	ACT3	ACT2	QIO2D	QIO1D
SCR2	VB/2M	ICONM	TEMPM	FAILM	MVAM	LSUPM	1	1
SCR3	AG6DB	LIN	LAW	COR8	0	0	0	0
SCR4	LOW Byte of DC-Offset Compensation							
SCR5	HIGH Byte of DC-Offset Compensation							
STCR0	FUSE3	FUSE2	FUSE1	FUSE0	0	0	0	0
STCR1	RSV5	RSV4	RSV3	RSV2	RSV1	RSV0	RSVU1	RSVU0

**XOP Command**

Bit	7	6	5	4	3	2	1	0
XOP for XR/XTR	0	RW	1	0	ATR	LSEL2	LSEL1	LSEL0

**Programming the MuSLIC**

**XOP Configuration Registers**

Bit	7	6	5	4	3	2	1	0
XR0	MIO4D	MIO3D	MIO2D	MIO1D	MIO4	MIO3	MIO2	MIO1
XR1	DUPGNK				DUP			
XR2	REXTEN	0	0	FIXC	IDR	EX-MCLK	0	0
XR3	LOW Byte of AC-CRAM checksum							
XR4	HIGH Byte of AC-CRAM checksum							
XR5	LOW Byte of AC-CRAM checksum							
XR6	HIGH Byte of AC-CRAM checksum							
XR7	ECIC1 (Byte 0 to Byte 14)							
XR8	ECIC2 (Byte 15 to Byte 29)							

**Programming the MuSLIC**

**XOP Test Register**

Bit	7	6	5	4	3	2	1	0
XTR0	HIT	HIR	ELM	SOFTON	OPIM8M	DLP03	DLP5	DISPOFI
XTR1	CAL	LMSEL1	LMSEL0	LMNOTCH	LMBP	LM2PCM	PCM2DC	ITIME
XTR2	RING-ON	DDCC	DCAD16	ERAMP	ERECT	AC-ADCPD	AC-DACPD	AFE-OFF
XTR3	DHP-X	DHP-R	TH	FRX	FRR	AX	AR	IM
XTR4	DLB-8M	DLB-64K	DLB-32K	DLB-PCM	ALB-8M	ALB-64K	ALB-8K	DCHOLD
XTR5	DC-DLB	DC-ALB	DC-ALBIT	DC-ALBIL	DC-ALBV	DCLMU2	DCLMU1	DCLMU0
XTR6	TTXL	DTTXL	NOAGC	ILITMUX	COT16	DITOFF	AXG0	ARG0
XTR7	QDETQ4	QDETQ3	QDETQ2	QDETQ1	0	0	0	0
XTR8	TQAP-FIR3	TQAP-FIR2	TQAP-FIR1	TQAP-FIR0	0	0	0	0
XTR9	Fuse QAP1				Fuse QAP2			
XTR10	Fuse QAP 3				Fuse QAP4			
XTR11	Blocktest 1							
XTR12	Blocktest 2							
XTR13	Blocktest 3							
XTR14	RSV1Q3	RSV1Q2	RSV1Q1	RSV1Q0	RSV2Q3	RSV2Q2	RSV2Q1	RSV2Q0
XTR15	RSV3Q3	RSV3Q2	RSV3Q1	RSV3Q0	RSV4Q3	RSV4Q2	RSV4Q1	RSV4Q0
XTR16	RSV5Q3	RSV5Q2	RSV5Q1	RSV5Q0	RSV6Q3	RSV6Q2	RSV6Q1	RSV6Q0
XTR17	RSVU1Q3	RSVU1Q2	RSVU1Q1	RSVU1Q0	RSVU0Q3	RSVU0Q2	RSVU0Q1	RSVU0Q0

**Programming the MuSLIC**

**TOP Command**

Bit	7	6	5	4	3	2	1	0
	0	R	1	1	0	0	LSEL1	LSEL0

**TOP Configuration Registers**

Bit	7	6	5	4	3	2	1	0
TCR0	VB/2	ICON	TEMP	FAIL	MVA	LSUP	RES	0

TCR1	NMVB/2	NMICON	NMTEMP	NMFAIL	NMMVA	NMLSUP	RLM1	RLM0
------	--------	--------	--------	--------	-------	--------	------	------

**COP Command**

Bit	7	6	5	4	3	2	1	0
	ICRAM	RW	0	0	0	1	WGRAM1	WGRAM0

	SET2	SET1	SET0	CODE4	CODE3	CODE2	CODE1	CODE0
--	------	------	------	-------	-------	-------	-------	-------

**COPI Command**

Bit	7	6	5	4	3	2	1	0
	B	RW	0	0	1	0	LSEL1	LSEL0

**CAR Coefficient set Assignment Registers**

Bit	7	6	5	4	3	2	1	0
CAR0	DC1	DC0	AC2	AC1	AC0	0	0	HLOAD

CAR1	TG1.2	TG1.1	TG1.0	TG2.2	TG2.1	TG2.0	0	0
------	-------	-------	-------	-------	-------	-------	---	---

**Programming the MuSLIC**

**4.1.1 SOP Command**

To modify or evaluate the MuSLIC status, individually for each channel, the contents of up to 6 configuration registers SCR0, ... SCR5 may be transferred to or from the MuSLIC. This is done by a SOP Command (status operation command).

With ATR = 1 and LSEL0 = 0/1 and LSEL1 = LSEL2 = 0 the registers STCR0, STCR1 can be set/read.

Bit 7	6	5	4	3	2	1	0
<b>B</b>	<b>RW</b>	<b>0</b>	<b>1</b>	<b>ATR</b>	<b>LSEL2</b>	<b>LSEL1</b>	<b>LSEL0</b>

**B** Broadcast

B = 0 Only one channel (time slot) is programmed

B = 1 All channels (up to 16) are programmed with the same information

**RW** Read/Write Information: Enables reading from the MuSLIC or writing information to the MuSLIC

RW = 0 Write to the MuSLIC

RW = 1 Read from the MuSLIC

**ATR** Access Test Register

ATR = 0 SCR0 ... SCR5 Registers are available

ATR = 1 STCR0, STCR1 Registers are read/writeable

**LSEL** Length select information

This field identifies the number of SOP Register

ATR	LSEL 2	LSEL 1	LSEL 0	
0	0	0	0	SCR0
0	0	0	1	SCR1
0	0	1	0	SCR2
0	0	1	1	SCR3
0	1	0	0	SCR4
0	1	0	1	SCR5
0	1	1	1	SCR0 to SCR5
1	0	0	0	STCR0
1	0	0	1	STCR1

**Programming the MuSLIC**

**SCR0 Configuration Register 0**

Configuration register SCR0 defines the basic feeding modes of the MuSLIC and enables/disables test features:

Bit 7	6	5	4	3	2	1	0
<b>POLNR</b>	<b>N/BB</b>	<b>LB</b>	<b>ETG2</b>	<b>ETG1</b>	<b>ENO</b>	<b>ENTE</b>	<b>COR</b>

Reset value: 00<sub>H</sub>

- POLNR** Normal or Reverse Polarity (see **chapter 5.4**)  
 POLNR = 0 sets the MuSLIC to Normal Polarity feeding  
 POLNR = 1 sets the MuSLIC to Reverse Polarity feeding
- N/BB** MuSLIC is in normal or Boosted Battery mode (see **chapter 5.4**).  
 N/BB = 0 Normal feeding  
 N/BB = 1 Changes ternary interface to AHV-SLIC which sets the AHV-SLIC to Boosted Battery mode
- LB** Handling of Loop Back functions for testing PCM loops  
 LB = 0 normal function  
 LB = 1 the desired Loop Back function is enabled
- ETG2** Enables programmable Test Tone Generator 2  
 ETG2 = 0 Test Tone Generator 2 is disabled  
 ETG2 = 1 Test Tone Generator 2 is enabled
- ETG1** Enables programmable Test Tone Generator 1  
 ETG1 = 0 Test Tone Generator 1 is disabled  
 ETG1 = 1 Test Tone Generator 1 is enabled
- ENO** Enables Offset compensation  
 ENO = 0 no DC offset compensation  
 ENO = 1 DC offset compensation
- ENTE** Enables Test  
 ENTE = 0 normal operation  
 ENTE = 1 enables the test selected by the test registers (see **chapter 8**)
- COR** Cut Off Receive Path for test reasons (see **chapter 8**)  
 COR = 0 Receive Path transmission is available  
 COR = 1 Receive Path is disabled

**Programming the MuSLIC**

**SCR1 Configuration Register 1**

Configuration register SCR1 defines the meterpulse settings and the soft/hard reversal, linear mode and IO settings.

Bit	7	6	5	4	3	2	1	0
	<b>TTXNO</b>	<b>TTX12</b>	<b>NOSL</b>	<b>SOREV</b>	<b>ACT3</b>	<b>ACT2</b>	<b>QIO2D</b>	<b>QIO1D</b>

Reset value: 00<sub>H</sub>

**TTXNO** Meterpulses are represented by teletax (TTX) with 12 or 16 kHz or with Reverse Polarity

TTXNO = 0 Meterpulses are represented with 12 kHz or 16 kHz

TTXNO = 1 Meterpulses are represented with Reverse Polarity

**TTX12** Teletax-signal with 12 kHz or 16 kHz

TTX12 = 0 16 kHz teletax-signal

TTX12 = 1 12 kHz teletax-signal

**NOSL** No slope: means that the ramping of teletax (TTX) signal is switched off

NOSL = 0 Slope of TTX-Signal is smooth

NOSL = 1 Hard switch of TTX-Signal

**SOREV** Soft Reversal Meterpulses

SOREV = 0 hard reversal

SOREV = 1 soft reversal

**ACT3** Active Mode with power save status of HV-SLIC (for future use)

ACT3 = 0 normal mode

ACT3 = 1 C1, C2 indicates the power save mode for the HV-SLIC

**ACT2** Active Mode with power save status of HV-SLIC (for future use)

ACT2 = 0 normal mode

ACT2 = 1 C1, C2 indicates the power save mode for the HV-SLIC

**QIO1D** Direction for programmable IO - Pin of the QAP IO1

QIO1D = 0 sets the pin IO1 as an input

QIO1D = 1 sets the pin IO1 as an output

**QIO2D** Direction for programmable IO - Pin of the QAP IO2

QIO2D = 0 sets the pin IO2 as an input

QIO2D = 1 sets the pin IO2 as an output

**Programming the MuSLIC**

**SCR2 Configuration Register 2**

Configuration register SCR2 is the Mask register. Each bit of TCR0 (Signalling register) can be masked (except the RES bit); that means changes of such a 'masked bit' are not causing a change of the SLCX - bit (Data Upstream C/I-channel byte).

Bit 7	6	5	4	3	2	1	0
<b>VB/2M</b>	<b>ICONM</b>	<b>TEMPM</b>	<b>FAILM</b>	<b>MVAM</b>	<b>LSUPM</b>	1	1

Reset value: FF<sub>H</sub>

**VB/2M** Mask bit for half battery information  
 VB/2M = 0 each change of the VB/2 bit leads to an interrupt (SLCX-bit)  
 VB/2M = 1 changes of VB/2 bit are neglected

**ICONM** Mask bit for constant current information  
 ICONM = 0 each change of the ICON bit leads to an interrupt (SLCX-bit)  
 ICONM = 1 changes of ICON bit are neglected

**TEMPM** Mask bit for over temperature information  
 TEMPM = 0 each change of the TEMP bit leads to an interrupt (SLCX-bit)  
 TEMPM = 1 changes of TEMP bit are neglected

**FAILM** Mask bit for clock fail information  
 FAILM = 0 each change of the FAIL bit leads to an interrupt (SLCX-bit)  
 FAILM = 1 changes of FAIL bit are neglected

**MVAM** Mask bit for internal measurement results  
 MVAM = 0 each change of the MVA bit leads to an interrupt (SLCX-bit)  
 MVAM = 1 changes of the MVA bit are neglected

**LSUPM** Mask bit for line supervision  
 LSUPM = 0 each change of the LSUP bit leads to an interrupt (SLCX-bit)  
 LSUPM = 1 changes of the LSUP bit are neglected

Information about changing half battery- and constant current- information will be neglected on both of the Power Down and the Ringing state.



**Programming the MuSLIC**

**SCR3 Configuration Register**

Bit	7	6	5	4	3	2	1	0
	AG6DB	LIN	LAW	COR8	0	0	0	0

Reset value: 00<sub>H</sub>

**AG6DB** Fixed gain in the transmit path.

AG6DB = 0 0 dB gain

AG6DB = 1 + 6 dB gain

**LIN** Linear mode selection (16 bit linear information in voice channel A (upper byte) and B (lower byte))

LIN = 0 PCM-mode is selected

LIN = 1 linear mode is selected

**LAW** PCM-law selection

LAW = 0 A-Law is selected

LAW = 1  $\mu$ -Law is selected ( $\mu$ 255 PCM)

**COR8** Cut off receive (voice only)

COR8 = 0 normal operation

COR8 = 1 cut off receive is enabled

**SCR4 and SCR5 Configuration Register**

These two registers content the DC offset bytes. They can be used one by one. Activation is controlled by the ENO bit (SCR0-2)

**SCR4**

Bit	7	6	5	4	3	2	1	0
	LOW Byte of DC-Offset Compensation							

Reset value: 00<sub>H</sub>

**SCR5**

Bit	7	6	5	4	3	2	1	0
	HIGH Byte of DC-Offset Compensation							

Reset value: 00<sub>H</sub>

**Programming the MuSLIC****STCR0 Test Configuration Register 0**

The Test Configuration register STCR0 is used for fuse operation and test only.

Bit 7	6	5	4	3	2	1	0
<b>FUSE3</b>	<b>FUSE2</b>	<b>FUSE1</b>	<b>FUSE0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>

Reset value: 00<sub>H</sub>

**FUSE0 to FUSE3** Information for fuse operation

**STCR1 Test Configuration Register 1**

The Test Configuration register STCR1 is used for reserved operations of the PEB 3465 (QAP).

Bit 7	6	5	4	3	2	1	0
<b>RSV5</b>	<b>RSV4</b>	<b>RSV3</b>	<b>RSV2</b>	<b>RSV1</b>	<b>RSV0</b>	<b>RSVU1</b>	<b>RSVU2</b>

Reset value: 00<sub>H</sub>

**RSV0 to RSV5** from PEB 31665 to PEB 3465

**RSVU0 to RSVU1** from PEB 3465 to PEB 31665

**Programming the MuSLIC**

**4.1.2 XOP Command**

To modify or evaluate test configurations, to select special functions, to control the coefficient RAMs, to get information for fusing and ECIC and other common functions up to 15 Bytes maybe transferred to or from the MuSLIC, using the XOP Command (extended operation command).

Bit 7	6	5	4	3	2	1	0
0	RW	1	0	ATR	LSEL2	LSEL1	LSEL0

**RW** Read/Write Information: Enables reading from the MuSLIC or writing information to the MuSLIC  
 RW = 0 Write to the MuSLIC  
 RW = 1 Read from the MuSLIC

**LSEL** Length select information.  
 This field identifies the subsequent data bytes.

ATR	LSEL 2	LSEL 1	LSEL 0	
0	0	0	0	XR0
0	0	0	1	XR1
0	0	1	0	XR2
0	0	1	1	AC-RAM + DC-RAM Checksum
0	1	0	0	AC-RAM Checksum
0	1	0	1	DC-RAM Checksum
0	1	1	0	ECIC1 (0 to 14)
0	1	1	1	ECIC2 (15 to 29)
1	0	0	0	XTR0
1	0	0	1	XTR1 and XTR2
1	0	1	0	XTR0 to XTR8
1	0	1	1	Fuse register 0 to Fuse register 1
1	1	0	0	Blocktest 1 to Blocktest 3
1	1	0	1	XTR14 to XTR17
1	1	1	0	RESERVED
1	1	1	1	RESERVED

**Programming the MuSLIC**

**XR0 Extended Operation Register 0**

Extended Operation Register 0 defines the four IO-pins of the MuPP.

Bit 7	6	5	4	3	2	1	0
<b>MIO4D</b>	<b>MIO3D</b>	<b>MIO2D</b>	<b>MIO1D</b>	<b>MIO4</b>	<b>MIO3</b>	<b>MIO2</b>	<b>MIO1</b>

Reset value: 00<sub>H</sub>

**MIOiD** Direction for programmable IO - Pins of the MuPP IO1 to IO4  
 MIOiD = 0 sets the pin IOi as an input  
 MIOiD = 1 sets the pin IOi as an output

**MIOi** Value of programmable IO - Pins of the MuPP IO1 to IO4  
 MIOi = 0 sets the pin IOi to LOW or if it is read it is LOW  
 MIOi = 1 sets the pin IOi to HIGH or if it is read it is HIGH

If the bit REXTEN (XR2-7) is set to 1 (Unbalanced Ringing) the MIO1 pin is switched to the ring pulse control function. Thus a zero-crossing signal connected to the MIO1 (combined with the Ringing Mode, burst on/off) generates a correct switching signal for the ringer relay sent on QIO1 of the selected subscriber line (see **chapter 4.2** and **chapter 5.5**).

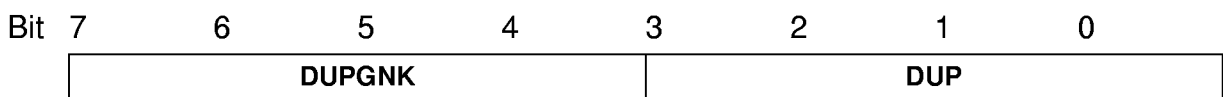
If the bit EX-MCLK (XR2-2) and TST1 pin (No.26) are set to 1 and the MIO2 pin is set as an input the MuPP is ready for external clocking (32 MHz) (the internal PLL is shut down).

If the TST1 pin (No.26) and the bit EX-MCLK (XR-2) is set to 1 and the MIO2 pin is set as an output the 32 MHz clock (output of the internal PLL) is on the MIO2 pin.

**Programming the MuSLIC**

**XR1 Extended Operation Register 1**

Extended Operation Register 1 defines the Data Upstream Persistency Counters.



Reset value: 5A<sub>H</sub>

**DUPGNK** To restrict the rate of upstream C/I-bit changes, deglitching (persistence checking) of the status information from the MuSLIC may be applied. New status information will be transmitted upstream, after it has been stable for N milliseconds. N is binary programmable in the range of 4 to 60 ms in steps of 4 ms, with DUPGNK = 0<sub>H</sub> the deglitching is disabled.

Reset value is 20 ms.

The HOOK bit (for external indication) and the GNK bit are influenced.

(Detailed info see **chapter 4.2**, and **figure 23**.)

**DUP** To restrict the rate of upstream C/I-bit changes, deglitching (persistence checking) of the status information from the MuSLIC may be applied. New status information will be transmitted upstream, after it has been stable for N milliseconds. N is binary programmable in the range of 1 to 15 ms in steps of 1 ms; with DUP = 0<sub>h</sub> the deglitching is disabled.

Reset value is 10 ms.

The HOOK, SLCX and the QI1-bits are influenced (different counters but same programming).

(Detailed info see **chapter 4.2**, and **figure 23**.)

**Programming the MuSLIC**

**XR2 Extended Operation Register 2**

Extended Operation Register 2 defines basic operations for all channels.

Bit 7	6	5	4	3	2	1	0
<b>REXTEN</b>	0	0	<b>FIXC</b>	<b>IDR</b>	<b>EX-MCLK</b>	0	0

Reset value: 10<sub>H</sub>

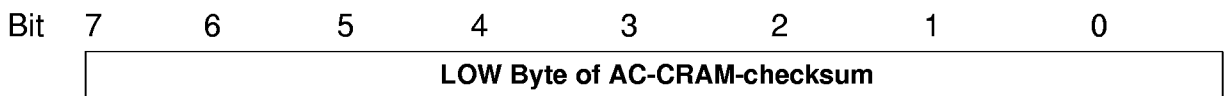
- REXTEN** External Ringing Mode Enabled (see **chapter 5.5**)  
 REXTEN = 0 use internal ringing mode  
 REXTEN = 1 use external ringing mode
- FIXC** The MuSLIC uses either fixed coefficients or the programmed ones.  
 FIXC = 0 programmed coefficients used  
 FIXC = 1 fixed coefficients used
- IDR** Initializes Data RAM  
 IDR = 0 normal operation is selected  
 IDR = 1 content of Data RAM is set to 0 (for test purposes)
- EX-MCLK** Possibility to provide the MuSLIC with an external clock (see XR0)  
 EX-MCLK = 0 normal operation is selected  
 EX-MCLK = 1 internal PLL is shut down or internal clock is connected to the pin MIO2, respectively (see XR0)

**Programming the MuSLIC**

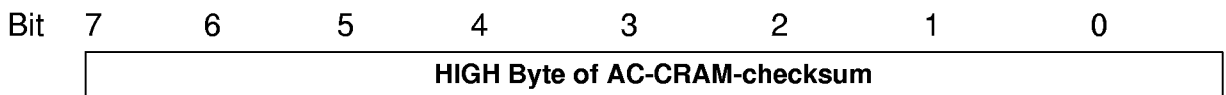
**XR3 TO XR6 Extended Operation Registers 3 to 6**

XR3 to XR6 are the checksums of all the Coefficient bytes written into the Coefficient RAM (CRAM) of the MuPP by the COP-Command. Reading these bytes starts the sum generation. There are two identical blocks of CRAMs (time slot 0 to 7 and 8 to 15). Each reading alternates the block access.

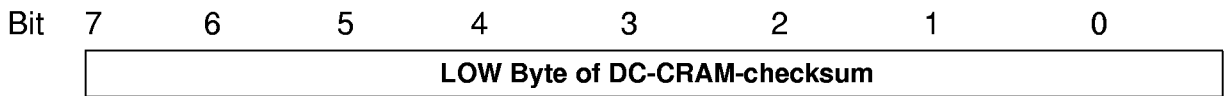
**XR3**



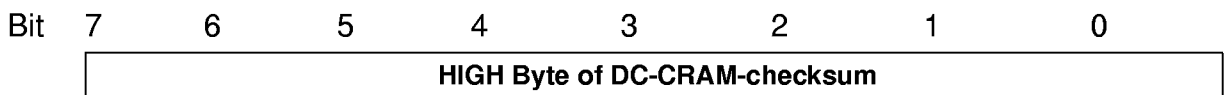
**XR4**



**XR5**



**XR6**



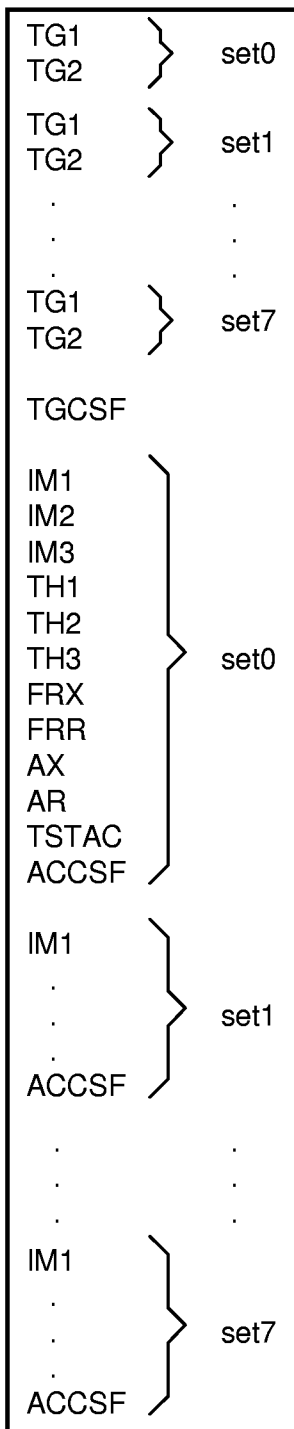
(Algorithm of defining the checksum:  $x^{16} + x^{10} + x^7 + x + 1$ )  
 (With that algorithm you can reach a fault coverage of:  $1-2^{-15}$ )

**Programming the MuSLIC**

Sum generation is done in the following manner (see **chapter 4.1.4**)

**AC-CRAM-Checksum**

The sequence of the coefficients is:

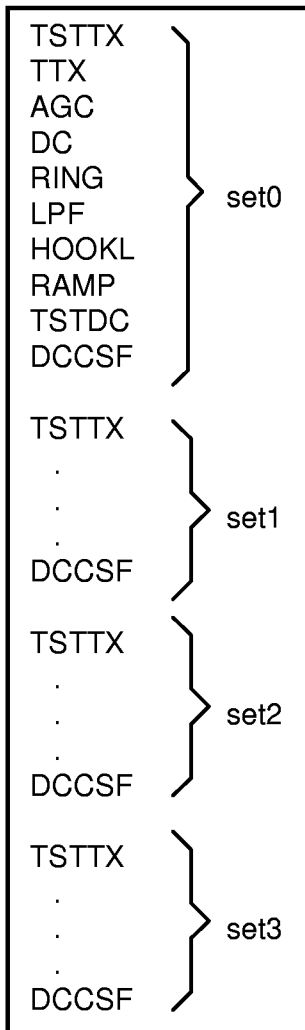




**Programming the MuSLIC**

**DC-RAM-Checksum**

The sequence of the coefficients is:



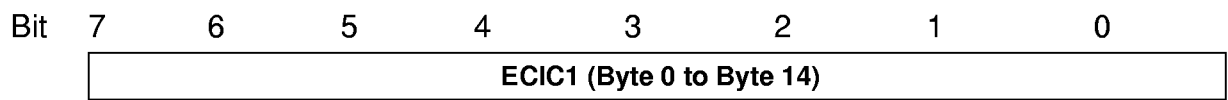
Using the “checksum fill” Bytes (TGCSF, ACCSF, DCCSF) it is possible to create a fixed set-checksum independent of changed coefficients.

**Programming the MuSLIC**

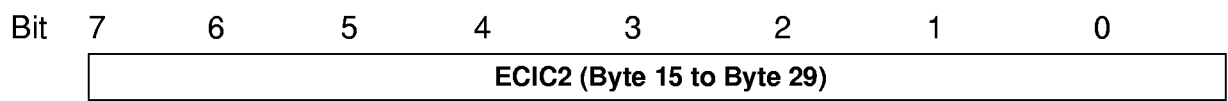
**XR7 and XR8 Extended Operation Register 7 to 8**

Each of these two registers feasible to read 15 bytes of design/status information generated by an external ASIC. More details about the extended IOM-2 Channel Identification see **chapter 10**.

**XR7**



**XR8**

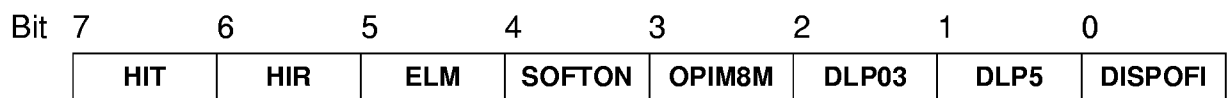


XR7 and XR8 shows the data stream of the input pin ID0. If the input pins ID1, ID2 and ID3 = 1, ID0 works as a serial input controlled by FSC and DCL (see **chapter 10**).

Reading XR7 or XR8 15 bytes each will be transferred from ID0 to IOM-2 Interface Monitor channel.

**XTR0 Extended Operation Test Register 0**

Extended Operation Test Register XTR0 defines testing features.



Reset value: 00<sub>H</sub>

**HIT** for AHV-SLIC test functions  
 HIT = 0 normal operation  
 HIT = 1 changes HV-interface (C1,C2) which set the TIP wire to high impedance

**HIR** for AHV-SLIC test functions  
 HIR = 0 normal operation  
 HIR = 1 changes HV-interface (C1,C2) which set the RING wire to high impedance

---

**Programming the MuSLIC**

<b>ELM</b>	Enable level meter
ELM = 0	normal operation if LM2PCM = 1 the input to the Levelmeter is switched to PCM Voice-Channel
ELM = 1	level meter function is enabled if LM2PCM = 1 the output of the Levelmeter is switched to PCM Voice-Channel
<b>SOFTON</b>	SW-fuses are activated in the PEB 3465
SOFTON = 0	HW-fuses are activated
SOFTON = 1	SW-fuses are activated
<b>OPIM8M</b>	Open fast digital Impedance Matching Loop (IM8M)
OPIM8M = 0	normal operation
OPIM8M = 1	opens fast digital IM-Loop ( $H_{IM8M} = 0$ )
<b>DLP03</b>	Disable LP03-lowpass
DLP03 = 0	normal operation
DLP03 = 1	disables programmable lowpass ( $H_{LP03} = 1$ )
<b>DLP5</b>	Disable LP5-lowpass
DLP5 = 0	normal operation
DLP5 = 1	disables programmable lowpass ( $H_{LP5} = 1$ )
<b>DISPOFI</b>	Disable Postfilter (DC path)
DISPOFI = 0	normal operation
DISPOFI = 1	disables postfilter

**Programming the MuSLIC**

**XTR1 Extended Operation Test Register 1**

XTR1 controls the level meter functions

Bit 7	6	5	4	3	2	1	0
<b>CAL</b>	<b>LMSEL1</b>	<b>LMSEL0</b>	<b>LMNOTCH</b>	<b>LMBP</b>	<b>LM2PCM</b>	<b>PCM2DC</b>	<b>ITIME</b>

Reset value: 00<sub>H</sub>

**CAL** Enable level meter result register  
 CAL = 0 normal operation (offset register - SCR4/SCR5 - is read)  
 CAL = 1 levelmeter result register is read

**LMSEL** selects Levelmeter and Thresholdpairs

LMSEL1	LMSEL0	
0	0	DC-Levelmeter Thresholdpair 0
0	1	DC-Levelmeter Thresholdpair 1
1	0	AC-Levelmeter
1	1	TTX-Levelmeter

**LMNOTCH** Bandpass or Notchfilter Function for Levelmetering AC  
 LMNOTCH = 0 Bandpass Function  
 LMNOTCH = 1 Notchfilter Function

**LMBP** Activates the Bandpass or Notchfilter in the AC Transmit Path  
 LMBP = 0 normal operation  
 LMBP = 1 Bandpass/Notchfilter enabled

**LM2PCM** Switches the selected Levelmeter Signal to the PCM Voice-Channel  
 LM2PCM = 0 normal operation  
 LM2PCM = 1 switches the selected Levelmetersignal to the PCM Voice-Channel

**PCM2DC** switches the Receive PCM Voice-Channel to DC-Output  
 PCM2DC = 0 normal operation  
 PCM2DC = 1 switches the Receive PCM Voice-Channel to DC-Output

**ITIME** Integration time of AC and TTX Levelmeter  
 ITIME = 0 16 ms Integrationtime  
 ITIME = 1 256 ms Integrationtime

**Programming the MuSLIC**

**XTR2 Extended Operation Test Register 2**

Extended Operation Test Register XTR2 defines testing features (see **chapter 8**).

Bit 7	6	5	4	3	2	1	0
<b>RING-ON</b>	<b>DDCC</b>	<b>DCAD16</b>	<b>ERAMP</b>	<b>ERECT</b>	<b>AC-ADCPD</b>	<b>AC-DACPD</b>	<b>AFE-OFF</b>

Reset value: 00<sub>H</sub>

- RING-ON**      Interrupt DC-characteristic and enables the Ringing Offset  
                   RING-ON = 0      normal operation  
                   RING-ON = 1      Interrupts DC-loop (HDCC = 0) and enables the Ringing Offset
  
- DDCC**            Disable DC-characteristic  
                   DDCC = 0            normal operation  
                   DDCC = 1            disables DC-loop (HDCC = 1)
  
- DCAD16**        DC gain of 16 in AD direction  
                   DCAD16 = 0        normal operation  
                   DCAD16 = 1        gain of 16
  
- ERAMP**         Enable Ramping generator  
                   ERAMP = 0         ramping generator off  
                   ERAMP = 1         ramping generator on
  
- ERECT**         Enable rectifier in DC-levelmeter  
                   ERECT = 0         normal operation (HRECT = 1)  
                   ERECT = 1         enables rectifier
  
- AC-ADCPD**     ADC is set to power down (transmit path is opened)  
                   AC-ADCPD = 0     normal operation  
                   AC-ADCPD = 1     transmit path is inactive
  
- AC-DACPD**     DAC is set to power down (receive path is opened)  
                   AC-DACPD = 0     normal operation  
                   AC-DACPD = 1     receive path is inactive
  
- AFE-OFF**        Analog front end is activated or deactivated  
                   AFE-OFF = 0        normal operation  
                   AFE-OFF = 1        the analog front end is deactivated

**Programming the MuSLIC**

**XTR3 Extended Operation Test Register 3**

Extended Operation Test Register XTR3 defines the basic MuSLIC settings which enable / disable the programmable digital filters.

Bit 7	6	5	4	3	2	1	0
<b>DHP-X</b>	<b>DHP-R</b>	<b>TH</b>	<b>FRX</b>	<b>FRR</b>	<b>AX</b>	<b>AR</b>	<b>IM</b>

Reset value: 00<sub>H</sub>

- DHP-X** Disable Transmit Highpass for test reasons  
 DHP-X = 0 Transmit Highpass Filter is enabled  
 DHP-X = 1 Transmit Highpass Filter is disabled
- DHP-R** Disable Receive Highpass for test reasons  
 DHP-R = 0 Receive Highpass Filter is enabled  
 DHP-R = 1 Receive Highpass Filter is disabled
- TH** Set Transhybrid Balancing Filter - together with the bit FIXC (XR2-4).  
 For FIXC = 1: the TH-Filter is set to  $H_{TH} = \text{for } Z_{BRD}$ ;  
 For FIXC = 0:  
 TH = 0 TH-filter is disabled  
 TH = 1 TH-filter is enabled (use programmed values)
- FRX** Enable FRX- (Frequency Response Transmit) Filter  
 For FIXC = 0:  
 FRX = 0 FRX-filter is disabled ( $H_{FRX} = 1$ )  
 FRX = 1 FRX-filter is enabled (use programmed values)
- FRR** Enable FRR- (Frequency Response Receive) Filter  
 For FIXC = 0:  
 FRR = 0 FRR-filter is disabled ( $H_{FRR} = 1$ )  
 FRR = 1 FRR-filter is enabled (use programmed values)
- AX** Set AX- (Amplification/Attenuation Transmit) Filter  
 For FIXC = 0:  
 AX = 0 AX-filter is set to default value ( $H_{AX} = 10 \text{ dB}$ )  
 AX = 1 AX-filter is enabled (use programmed values)
- AR** Set AR- (Amplification/Attenuation Receive) Filter  
 For FIXC = 0:  
 AR = 0 AR-filter is set to default value ( $H_{AR} = -15.11 \text{ dB}$ )  
 AR = 1 AR-filter is enabled (use programmed values)
- IM** Activates or deactivates the 64 kHz filter  
 IM = 0 64 kHz filter is deactivated ( $H_{IM} = 0$ )  
 IM = 1 64 kHz filter is activated

**Programming the MuSLIC**

**XTR4 Extended Operation Test Register 4**

Extended Operation Test Register XTR4 defines testing features.

Bit 7	6	5	4	3	2	1	0
DLB-8M	DLB-64K	DLB-32K	DLB-PCM	ALB-8M	ALB-64K	ALB-8K	DCHOLD

Reset value: 00<sub>H</sub>

- DLB-8M** AC digital loop: 8 MHz in/output is short cut  
 DLB-8M = 0 normal operation  
 DLB-8M = 1 8 MHz in/output is short cut
  
- DLB-64K** AC digital loop: 64 kHz in/output is short cut  
 DLB-64K = 0 normal operation  
 DLB-64K = 1 64 kHz in/output is short cut
  
- DLB-32K** AC digital loop: 32 kHz in/output is short cut  
 DLB-32K = 0 normal operation  
 DLB-32K = 1 32 kHz in/output is short cut
  
- DLB-PCM** AC digital loop: PCM in/output is short cut  
 DLB-PCM = 0 normal operation  
 DLB-PCM = 1 PCM in/output is short cut
  
- ALB-8M** AC analog loop: 8 MHz in/output is short cut  
 ALB-8M = 0 normal operation  
 ALB-8M = 1 8 MHz short cut
  
- ALB-64K** AC analog loop: 64 kHz in/output is short cut  
 ALB-64K = 0 normal operation  
 ALB-64K = 1 64 kHz in/output is short cut
  
- ALB-8K** AC analog and digital loops:  
 ALB-8K = 0 normal operation  
 ALB-8K = 1 and ALB-8M = 0 8 kHz loop in the AC DSP  
 (AC digital loop)  
 ALB-8K = 1 and ALB-8M = 1 Pre-/Postfilter out/input is short cut  
 (AC analog loop)
  
- DCHOLD** Holds the current DC-Output  
 DCHOLD = 0 normal operation  
 DCHOLD = 1 DC-Output is held

**Programming the MuSLIC**

**XTR5 Extended Operation Test Register 5**

XTR5 defines testing functions

Bit 7	6	5	4	3	2	1	0
DC-DLB	DC-ALB	DC-ALBIT	DC-ALBIL	DC-ALBV	DCLMU2	DCLMU1	DCLMU0

Reset value: 00<sub>H</sub>

**DC-DLB** DC digital loop: 1 MHz in/output is short cut  
 DC-DLB = 0 normal operation  
 DC-DLB = 1 1 MHz in/output is short cut

**DC-ALB** DC analog loop:  
 DC-ALB = 0 normal operation  
 DC-ALB = 1 short cut of in/output of DC-ADC and DC-DAC

**DC-ALBIT** DC analog loop: IT is switched to DCP/DCN  
 DC\_ALBIT = 0 normal operation  
 DC\_ALBIT = 1 IT is switched to DCP/DCN

**DC-ALBIL** DC analog loop: IL is switched to DCP/DCN  
 DC\_ALBIL = 0 normal operation  
 DC\_ALBIL = 1 IL is switched to DCP/DCN

**DC-ALBV** DC analog loop: VA, VB, VBIM, VDDIM is switched to DCP/DCN  
 DC\_ALBV = 0 normal operation  
 DC\_ALBV = 1 VA, VB, VBIM, VDDIM is switched to DCP/DCN

**DCLMU** Selects the signal switched to the DC-Levelmeter

DCLMU2	DCLMU1	DCLMU0	
0	0	0	IT
0	1	0	IL
1	0	0	VA
1	0	1	VB
1	1	0	VBIM
1	1	1	VDDIM



**Programming the MuSLIC**

**XTR6 Extended Operation Test Register 6**

XTR6 defines testing functions

Bit 7	6	5	4	3	2	1	0
<b>TTXL</b>	<b>DTTXL</b>	<b>NOAGC</b>	<b>ILITMUX</b>	<b>COT16</b>	<b>DITOFF</b>	<b>AXG0</b>	<b>ARG0</b>

Reset value: 00<sub>H</sub>

- TTXL**      Enables current measurement for TTX  
               TTXL = 0      normal operation  
               TTXL = 1 and IM = 1 and OPIM8M=1 enables TTX current measurement
  
- DTTXL**    Analog testloop: input/output is shortcut  
               DTTXL = 0    normal operation  
               DTTXL = 1    input/output is shortcut t
  
- NOAGC**    disable automatic gain control for TTX  
               NOAGC = 0    normal operation  
               NOAGC = 1    disable automatic gain control
  
- ILITMUX**   IL changes to IT and vice versa  
               ILITMUX = 0   normal operation  
               ILITMUX = 1   IL changes to IT and vice versa
  
- COT16**    cut off transmit path  
               COT16 = 0    normal operation  
               COT16 = 1    cut off transmit path
  
- DITOFF**    Disables the dither for noiseshapers  
               DITOFF = 0    normal operation  
               DITOFF = 1    Dither disabled
  
- AXG0**      0 dB Gain for Transmit Path  
               AXG0 = 0      normal operation  
               AXG0 = 1      0 dB Gain for Transmit Path
  
- ARG0**      0 dB Gain for Receive Path  
               ARG0 = 0      normal operation  
               ARG0 = 1      0 dB Gain for Receive Path

### Programming the MuSLIC

#### XTR7 Extended Operation Test Register 7

XTR7 informs how many PEB 3465 are connected to the PEB 31665

Bit 7	6	5	4	3	2	1	0
QDETQ4	QDETQ3	QDETQ2	QDETQ1	0	0	0	0

Reset value: 00<sub>H</sub>

**QDETQ4** informs about PEB 3465 connection

**QDETQi = 0** there is no PEB 3465 connected to the i-th interface

**QDETQi = 1** there is a PEB 3465 connected to the i-th interface

*Note: This information is available after the first AFSC-pulse.*

**Programming the MuSLIC**

**XTR8 Extended Operation Test Register 8**

XTR8 defines testing functions

Bit 7	6	5	4	3	2	1	0
TQAP-FIR3	TQAP-FIR2	TQAP-FIR1	TQAP-FIR0	0	0	0	ENRSV

Reset value: 00<sub>H</sub>

- TQAP-FIR3** Disables Noiseshaping Function for Channel 9, 11, 13, 15  
 TQAP-FIR3 = 0 normal operation  
 TQAP-FIR3 = 1 Noiseshaping Function is disabled
- TQAP-FIR2** Disables Noiseshaping Function for Channel 8, 10, 12, 14  
 TQAP-FIR2 = 0 normal operation  
 TQAP-FIR2 = 1 Noiseshaping Function is disabled
- TQAP-FIR1** Disables Noiseshaping Function for Channel 1, 3, 5, 7  
 TQAP-FIR1 = 0 normal operation  
 TQAP-FIR1 = 1 Noiseshaping Function is disabled
- TQAP-FIR0** Disables Noiseshaping Function for Channel 0, 2, 4, 6  
 TQAP-FIR0 = 0 normal operation  
 TQAP-FIR0 = 1 Noiseshaping Function is disabled
- ENRSV** Enables Reserved Registers (STCR1, XTR14 to XTR17)  
 ENRSV = 0 normal operation  
 ENRSV = 1 reserved registers are enabled

**XTR9 to XTR10 Extended Operation Test Register 9 and 10**

These bytes are used for the fuse operation of the PEB 3465.

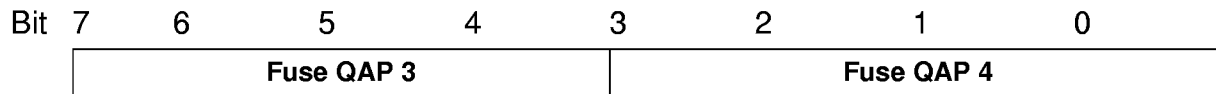
**XTR9**

Bit 7	6	5	4	3	2	1	0
Fuse QAP 1				Fuse QAP 2			

Reset value: 00<sub>H</sub>

**Programming the MuSLIC**

**XTR10**

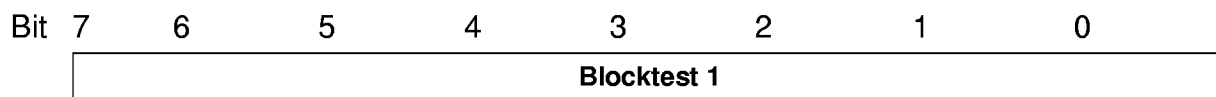


Reset value: 00<sub>H</sub>

**XTR11 to XTR13 Extended Operation Test Register 11 to 13**

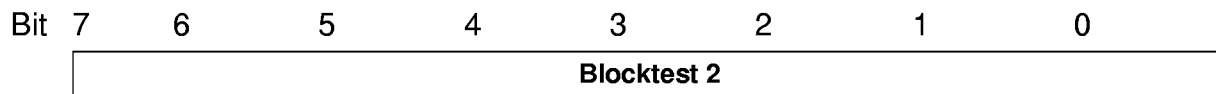
These 3 bytes show the result of the test of internal function blocks.

**XTR11**



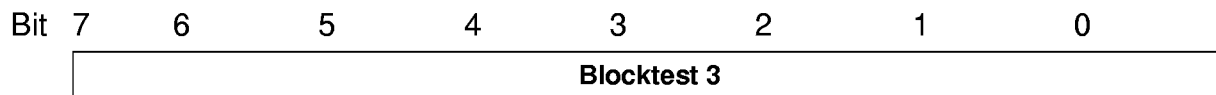
Reset value: 00<sub>H</sub>

**XTR12**



Reset value: 00<sub>H</sub>

**XTR13**



Reset value: 00<sub>H</sub>

*Note: Write XTR11 with bit 0 = 1 starts the blocktests. There are several types of tests. Selection is done by the bits 1 to 7 of XTR11 (see **chapter 8**).*

**XTR14 to XTR16 Extended Operation Test Register 14 to 16**

XTR14 to XTR16 are reserved for transfer of information from the PEB 31665 to the PEB 3465.

Reset value: 00<sub>H</sub>

**Programming the MuSLIC**

**XTR17 Extended Operation Test Register 17**

XTR17 is reserved for transfer of information from the PEB 3465 to the PEB 31665.

Reset value: 00<sub>H</sub>

**4.1.3 TOP Command**

With the TOP Command the TCR0 and TCR1 registers can be read. Each channel has its own registers addressed by the time slot or by address

Bit 7	6	5	4	3	2	1	0
0	R	1	1	0	0	LSEL1	LSEL0

**R** Read Information: Enables reading from the MuSLIC

R = 0 No operation

R = 1 Read from MuSLIC

**LSEL** Length select information

This field identifies the number of the TCR Register and the handling of interrupts too.

LSEL 1 LSEL 0

0 0 TCR0 (Reset of the interrupt)

0 1 TCR1 (Not masked interrupts are not affected)

1 1 TCR0 and TCR1 (Reset of the interrupt)

**Programming the MuSLIC**

**TCR0 Configuration Register 0**

TCR0 is the Signalling register. It indicates status information of each channel. If there is any change of one or more bits it is indicated via the SCLX bit in the C/I-channel. Each bit, except the RES bit, can be masked by the SCR2 Register (see also **figure 23**).

Bit 7	6	5	4	3	2	1	0
<b>VB/2</b>	<b>ICON</b>	<b>TEMP</b>	<b>FAIL</b>	<b>MVA</b>	<b>LSUP</b>	<b>RES</b>	<b>0</b>

Reset value: 02<sub>H</sub>

- VB/2**      Half battery voltage is detected  
 interrupt masked in Power Denial and Ringing State  
 VB/2 = 0      line voltage smaller than half battery  
 VB/2 = 1      line voltage larger than half battery
  
- ICON**      Current limitation information  
 interrupt masked in Power Denial and Ringing State  
 ICON = 0      Resistive Feeding  
 ICON = 1      Constant Current Feeding
  
- TEMP**      Temperature alarm of the AHV-SLIC which is signalled through the  
 HV-SLIC Interface (see **chapter 3.4**)  
 TEMP = 0      normal temperature  
 TEMP = 1      Temperature alarm from AHV-SLIC detected
  
- FAIL**      DCL or FSC Fail: Not the right count of clock cycles between two frame  
 syncs  
 FAIL = 0      no clock fails are detected  
 FAIL = 1      clock fails are detected  
 The FAIL bit is not influenced by the DUP-counter (each failure is reported).
  
- MVA**      Internal measurement results shown in the TCR1-0 and TCR1-1 are valid  
 or not valid (see **chapter 8**)  
 MVA = 0      the level metering results are not valid  
 MVA = 1      the level metering results are valid
  
- LSUP**      Line Supervision (of broken line)  
 LSUP = 0      the transversal current is higher than the programmed level  
 LSUP = 1      the transversal current is lower than the programmed level
  
- RES**      Reset status  
 RES = 0      no Reset has occurred  
 RES = 1      Reset has occurred via Reset-pin or via Power on Reset

**Programming the MuSLIC**

Any change of these bits (except the FAIL bit: only the positive going is reported) is signalled via the interrupt-bit (SLCX) in the C/I-DU-channel. There are two types of generating an interrupt:

- Each toggling of a non-masked TCR0-bit combined with a DUP-counter
- Toggling of the non-masked TEMP or MVA-bit and positive going FAIL bit (no filtering by the DUP-counter)

The status information is stored in the TCR0-register and an interrupt is generated but only if there isn't a not-handled interrupt.

Reading the TCR0-register gives the frozen interrupt status, clears the interrupt and enables the signalling of a further interrupt but not until after at least two 8 kHz frames.

*Note: The HOOK and the GNK signalling are directly filtered by there own DUP(GNK)-counters and they are directly put into the C/I-DU-channel (see **chapter 4.2**).*

**TCR1 Configuration Register 1**

TCR1 indicates interrupt information and level meter results of one channel.

Bit 7	6	5	4	3	2	1	0
NMVB/2	NMICON	NMTEMP	NMFAIL	NMMVA	NMLSUP	RLM1	RLM0

Reset value: 00<sub>H</sub>

**NMVB/2 to NMLSUP** Not masked signalling information. (The meaning of each bit is the same as described above.)  
Reading this register won't affect any stored information.

**RLM1 and RLM0** Result Level Metering

RLM1	RLM0	
0	0	below both levels
x	1	above level 0
1	x	above level 1

Programming the MuSLIC

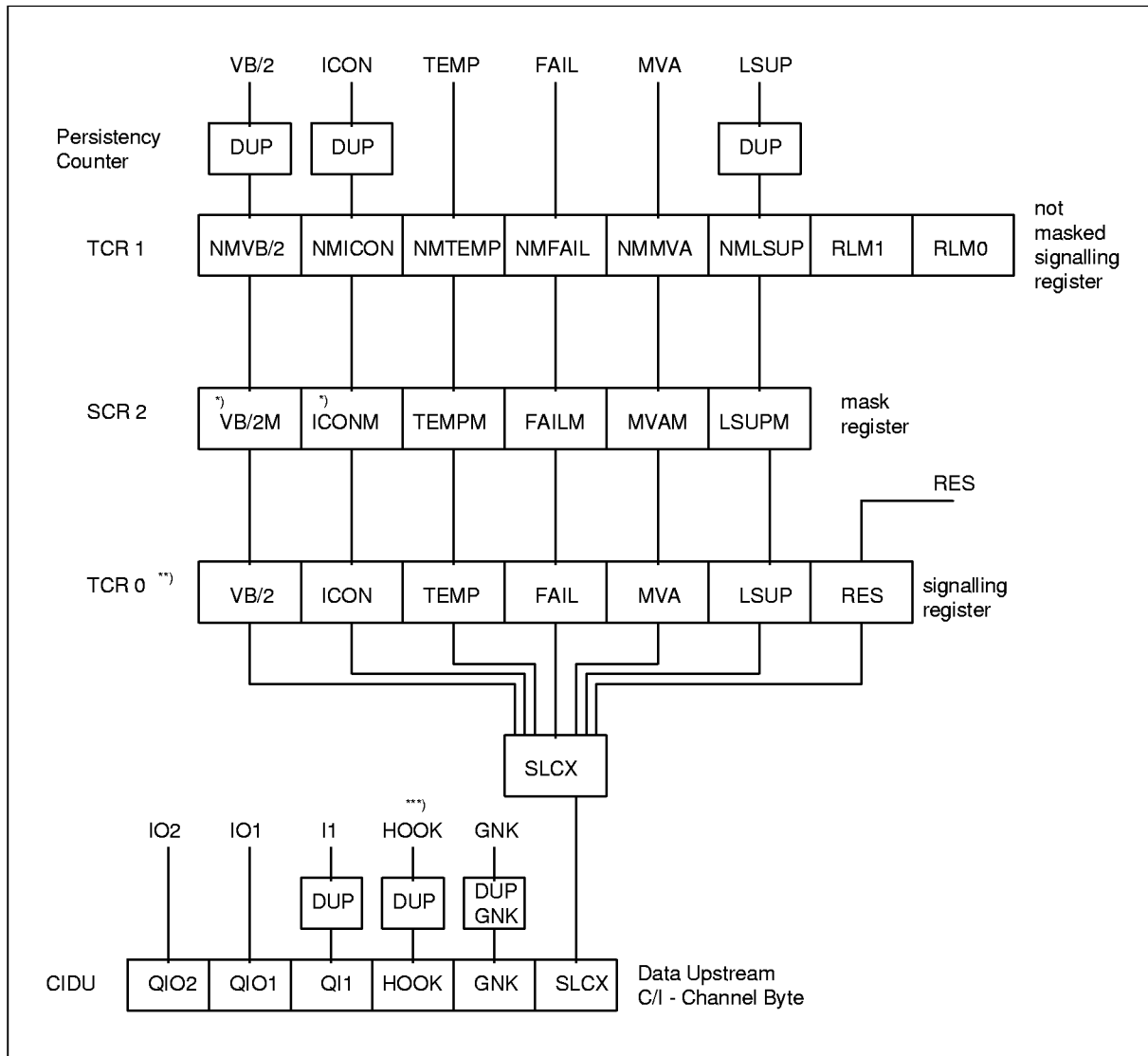


Figure 23 Interrupt Logic (block structure)

- 1) In Power Down and Ringing Mode changes of VB/2 and ICON are masked.
- 2) TCR0 is locked if one of the signals changes and is enabled after reading. Each change of TCR0 sets the interrupt bit SLCX to 1. Reading TCR0 sets SLCX to 0 but not before two 8 kHz frames. A take over of the signal FAIL from TCR1 to TCR0 clears this signal in TCR1.
- 3) In Power Down Mode the persistency counter DUPGNK is used.



**Programming the MuSLIC**

**4.1.4 COP Command**

With a COP Command coefficients for the programmable filters can be written to or read from the MuSLIC (write access is only allowed if FIXC = 1 or to an unused SET).

(Filter optimizing to different applications is supported by the software package MuSLICOS.)

The coefficients are gathered to 8 and 4 SETS respectively. So an optimum is reached between supplying each channel, handling and memory space. **Figure 24** gives an overview of the Coefficient RAM structure.

To assign a SET to a channel the COPI command is used.

Bit 7	6	5	4	3	2	1	0
<b>ICRAM</b>	<b>RW</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>WGRAM1</b>	<b>WGRAM0</b>

Bit 7	6	5	4	3	2	1	0
<b>SET2</b>	<b>SET1</b>	<b>SET0</b>	<b>CODE 4</b>	<b>CODE 3</b>	<b>CODE 2</b>	<b>CODE 1</b>	<b>CODE 0</b>

**ICRAM** Initialize CRAM  
 ICRAM = 0 Only one coefficient is programmed (destination is coded in the following byte)  
 ICRAM = 1 the whole AC- or DC-CRAM is written with the information of the following byte

**RW** Read/ Write  
 RW = 0 Subsequent data is written to the MuSLIC  
 RW = 1 Read data from the MuSLIC

**WGRAM1 and WGRAM0** Write to CRAM (only valid in combination with ICRAM=1)

WGRAM1	WGRAM0	
0	0	no write
0	1	AC-CRAM
1	0	DC-CRAM
1	1	AC-CRAM and DC-CRAM

## Programming the MuSLIC

SET	includes the number of coefficient set			
	SET2	SET1	SET0	
	0	0	0	SET 0
	0	0	1	SET 1
	0	1	0	SET 2
	0	1	1	SET 3
	1	0	0	SET 4
	1	0	1	SET 5
	1	1	0	SET 6
	1	1	1	SET 7

**SET 0 to SET 7** for the 8 sets of AC-coefficients and the 8 sets of Tone Generator 1 and 2

**SET 0 to SET 3** for the 4 sets of DC-coefficients

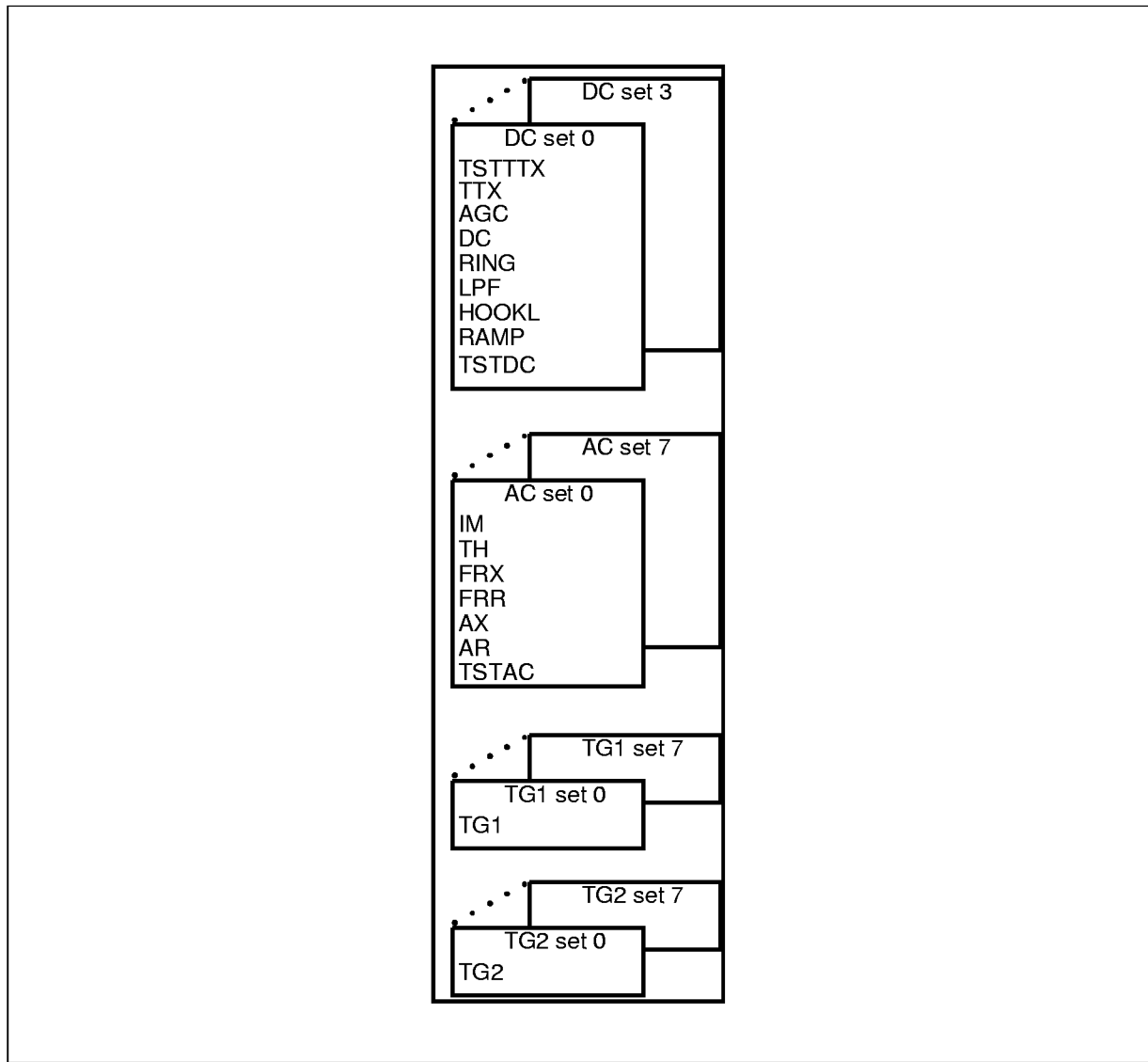
**Programming the MuSLIC**

**CODE** includes the number of following bytes and filter-addresses<sup>1)</sup>

CODE4	CODE3	CODE2	CODE1	CODE0		
0	0	0	0	0	TH-Filter coefficients (part 1)	(followed by 8 bytes of data)
0	0	0	0	1	TH-Filter coefficients (part 2)	(followed by 8 bytes of data)
0	0	0	1	0	TH-Filter coefficients (part 3)	(followed by 8 bytes of data)
0	0	0	1	1	FRX-filter coefficients	(followed by 8 bytes of data)
0	0	1	0	0	FRR-filter coefficients	(followed by 8 bytes of data)
0	0	1	0	1	AX-filter coefficients	(followed by 8 bytes of data)
0	0	1	1	0	AR-filter coefficients	(followed by 8 bytes of data)
0	0	1	1	1	TG1-filter coefficients	(followed by 8 bytes of data)
0	1	0	0	0	TG2-filter coefficients	(followed by 8 bytes of data)
0	1	0	0	1	AC test coefficients	(followed by 8 bytes of data)
0	1	0	1	0	IM-filter coefficients (part 3)	(followed by 8 bytes of data)
0	1	0	1	1	IM-filter coefficients (part 1)	(followed by 8 bytes of data)
0	1	1	0	0	IM-filter coefficients (part 2)	(followed by 8 bytes of data)
0	1	1	0	1	TG CSF (checksum fill)	(followed by 8 bytes of data)
0	1	1	1	0	AC CSF (checksum fill)	(followed by 8 bytes of data)
1	0	0	0	0	TTX test coefficients	(followed by 8 bytes of data)
1	0	0	0	1	TTX coefficients	(followed by 8 bytes of data)
1	0	0	1	0	AGC coefficients	(followed by 8 bytes of data)
1	0	0	1	1	LP-filter coefficients	(followed by 8 bytes of data)
1	0	1	0	0	Hook level coefficients	(followed by 8 bytes of data)
1	0	1	0	1	DC test coefficients	(followed by 8 bytes of data)
1	0	1	1	0	Ringing coefficients	(followed by 8 bytes of data)
1	0	1	1	1	DC-characteristic coefficients	(followed by 8 bytes of data)
1	1	0	0	0	Ramp generator, Ringer delay coefficients	(followed by 8 bytes of data)
1	1	0	0	1	DC CSF (checksum fill)	(followed by 8 bytes of data)

<sup>1)</sup> For generating a correct checksum all not used bits must be set to 0.

**Programming the MuSLIC**



**Figure 24 Overview of Sets of Coefficients**

**Programming the MuSLIC**

**4.1.5 COPI Command**

The COPI command allows to assign the sets of the Coefficient RAMs to a selected channel (given by the time slot or by address).

Bit	7	6	5	4	3	2	1	0
	<b>B</b>	<b>RW</b>	<b>0</b>	<b>0</b>	<b>1</b>	<b>0</b>	<b>LSEL1</b>	<b>LSEL0</b>

**B** Broadcast  
 B = 0 Only one channel (time slot) is programmed  
 B = 1 All channels (up to 16) are programmed with the same information

**RW** Read/ Write  
 RW = 0 Subsequent data is written to the MuSLIC  
 RW = 1 Set assignment is read

**LSEL** Length select information.  
 This field identifies the subsequent data bytes.

LSEL 1	LSEL 0	
0	0	CAR0
0	1	CAR1
1	1	CAR0 and CAR1

**Programming the MuSLIC**

**CAR0 Coefficient set Assignment Register 0**

CAR0 indicates AC and DC coefficients set assignment.

Bit 7	6	5	4	3	2	1	0
DC1	DC0	AC2	AC1	AC0	0	0	HLOAD

Reset value: 00<sub>H</sub>

**DC**

DC1	DC0	
0	0	DC coefficient set 0
0	1	DC coefficient set 1
1	0	DC coefficient set 2
1	1	DC coefficient set 3

**AC**

AC2	AC1	AC0	
0	0	0	AC coefficient set 0
0	0	1	AC coefficient set 1
0	1	0	AC coefficient set 2
0	1	1	AC coefficient set 3
1	0	0	AC coefficient set 4
1	0	1	AC coefficient set 5
1	1	0	AC coefficient set 6
1	1	1	AC coefficient set 7

**HLOAD**

Hook for Load

HLOAD = 0      normal operation

HLOAD = 1      load is activated (LP03 will be preset)

**Programming the MuSLIC**

**CAR1 Coefficient set Assignment Register 1**

CAR1 indicates Tone Generator coefficients set assignment.

Bit 7	6	5	4	3	2	1	0
TG1.2	TG1.1	TG1.0	TG2.2	TG2.1	TG2.0	0	0

Reset value: 00<sub>H</sub>

**TG1**

TG1.2	TG1.1	TG1.0	
0	0	0	Tone Generator 1 set 0
0	0	1	Tone Generator 1 set 1
0	1	0	Tone Generator 1 set 2
0	1	1	Tone Generator 1 set 3
1	0	0	Tone Generator 1 set 4
1	0	1	Tone Generator 1 set 5
1	1	0	Tone Generator 1 set 6
1	1	1	Tone Generator 1 set 7

**TG2**

TG2.2	TG2.1	TG2.0	
0	0	0	Tone Generator 2 set 0
0	0	1	Tone Generator 2 set 1
0	1	0	Tone Generator 2 set 2
0	1	1	Tone Generator 2 set 3
1	0	0	Tone Generator 2 set 4
1	0	1	Tone Generator 2 set 5
1	1	0	Tone Generator 2 set 6
1	1	1	Tone Generator 2 set 7

**Programming the MuSLIC**

**4.2 IOM<sup>®</sup>-2 Interface Command / Indication Byte**

The Command/Indication (C/I) channel is used to communicate real time status information and for fast controlling of the MuSLIC. Data on the C/I channel are continuously transmitted in each frame until new data is sent.

**Data Downstream C/I - Channel Byte (receive) - CIDD**

This Byte is used for fast controlling of the MuSLIC. Each transfer to the MuSLIC has to last for at least 2 consecutive frames (FSC-cycles) so that it is accepted internally. Changes (spikes) of less than 2 FSC cycles are neglected.

(Note that there is no address DD direction because there is only one MuPP.)

Bit	7	6	5	4	3	2
	QIO2	QIO1	QO1	M2	M1	M0

**M0, M1, M2** these bits define the actual status; see table below (for details see chapter 5)

M2	M1	M0	Description
0	0	0	Power-Down High Impedance (loop open, PDNH)
1	1	1	Power-Down Resistive (loop open, PDNR)
0	1	0	Active State
1	1	0	Active State with Meterpulses
1	0	0	Ground Start
0	0	1	Ringling State (ring pause)
1	0	1	Ringling State (ring burst on)

**QO1** Value for the fixed Output Pin O1 of the QAP.

QO1 = 0 The corresponding pin at the digital interface of the QAP is set to a logic 0.

QO1 = 1 The corresponding pin at the digital interface of the QAP is set to a logic 1.

*Note: The Output Pin O1 of the QAP is tristate after reset and will be enabled by the first SOP command.*



**Programming the MuSLIC**

- QIO1** Value for the programmable Input/Output Pin IO1 of the QAP if programmed as an output pin. If the bit REXTEN (XR2-7) is set to 1 (external ringing) the internally created Ring Burst On Signal (for an external relay driver) **chapter 5.5)**
- QIO1 = 0 The corresponding pin at the digital interface of the QAP is set to a logic 0.
- QIO1 = 1 The corresponding pin at the digital interface of the QAP is set to a logic 1.
- QIO2** Value for the programmable Input/Output Pin IO2 of the QAP if programmed as an output pin.
- QIO2 = 0 The corresponding pin at the digital interface of the QAP is set to a logic 0.
- QIO2 = 1 The corresponding pin at the digital interface of the QAP is set to a logic 1.

**Data Upstream C/I - Channel Byte (transmit) - CIDU**

This Byte is used for fast transfer of the most important and time critical informations from the MuSLIC. Each transfer from the MuSLIC lasts for at least 2 consecutive frames.

(Note that there is no address in DU direction too.)

Bit	7	6	5	4	3	2
	<b>QIO2</b>	<b>QIO1</b>	<b>QI1</b>	<b>HOOK</b>	<b>GNK</b>	<b>SLCX</b>

- SLCX** Interrupt bit: Summary output of the whole signalling register (TCR0).
- SLCX = 0 No unmasked bit in the signalling register has toggled.
- SLCX = 1 Any unmasked bit in the signalling register has toggled.
- GNK** Indication if a ground connection is detected (filtered via the DUPGNK-counter). The function is disabled in Power Down State (GNK is set to 0).
- GNK = 0 No ground connection was detected.
- GNK = 1 Ground connection was detected.
- HOOK** Indication of the loop condition (filtered via the DUP-counter or the DUPGNK-counter in Power Down State).
- HOOK = 0 Subscriber is Onhook.
- HOOK = 1 Subscriber is Offhook.
- QI1** Logical state of the Input Pin I1 of the QAP.
- QI1 = 0 The corresponding pin at the digital interface of the QAP is receiving a logic 0.
- QI1 = 1 The corresponding pin at the digital interface of the QAP is receiving a logic 1.

---

**Programming the MuSLIC**

- QIO1** Logical state of the programmable Input/Output Pin IO1 of the QAP - even if not programmed as an input pin. <sup>1)</sup>
- QIO1 = 0 The corresponding pin at the digital interface of the QAP is receiving a logic 0.
- QIO1 = 1 The corresponding pin at the digital interface of the QAP is receiving a logic 1.
- QIO2** Logical state of the programmable Input/Output Pin IO2 of the QAP - even if not programmed as an input pin.
- QIO2 = 0 The corresponding pin at the digital interface of the QAP is receiving a logic 0.
- QIO2 = 1 The corresponding pin at the digital interface of the QAP is receiving a logic 1.

<sup>1)</sup> If the Input/Output Pin is programmed as an output the corresponding bit in the CIDU is "1".

The DUP- (DUPGNK-)counters filter the status-information and the input I1. The counters count down and generate enable signals for the registers if they are zero. Then they start counting again at the programmed value. If a status information or the input signal changes the proper counter is set and continues counting down. There are DUP-counters for HOOK, VB/2, ICON, LSUP generating SLCX and the input pin I1 and one DUPGNK-counter for HOOK in Power Down mode or for GNK in all other modes. Changing the mode freezes the actual status of HOOK and sets the actual HOOK-counter.

**Operating Modes**

**5 Operating Modes**

The MuSLIC supports 3 different Operating Modes: Power Down (PDown), Active and Ringing which are controlled via the lower 3 bits of the Data Downstream C/I Channel Byte (CIDD).

**Table 7**

<b>M2 (CIDD-4)</b>	<b>M1 (CIDD-3)</b>	<b>M0 (CIDD-2)</b>	<b>Description</b>
0	0	0	Power-Down High Impedance (PDNH)
1	1	1	Power-Down Resistive (PDNR)
0	1	0	Active State
1	1	0	Active State with Meterpulses
1	0	0	Active State with Ground Start
0	0	1	Ringing State (ring pause)
1	0	1	Ringing State (ring burst on)

Operating Modes

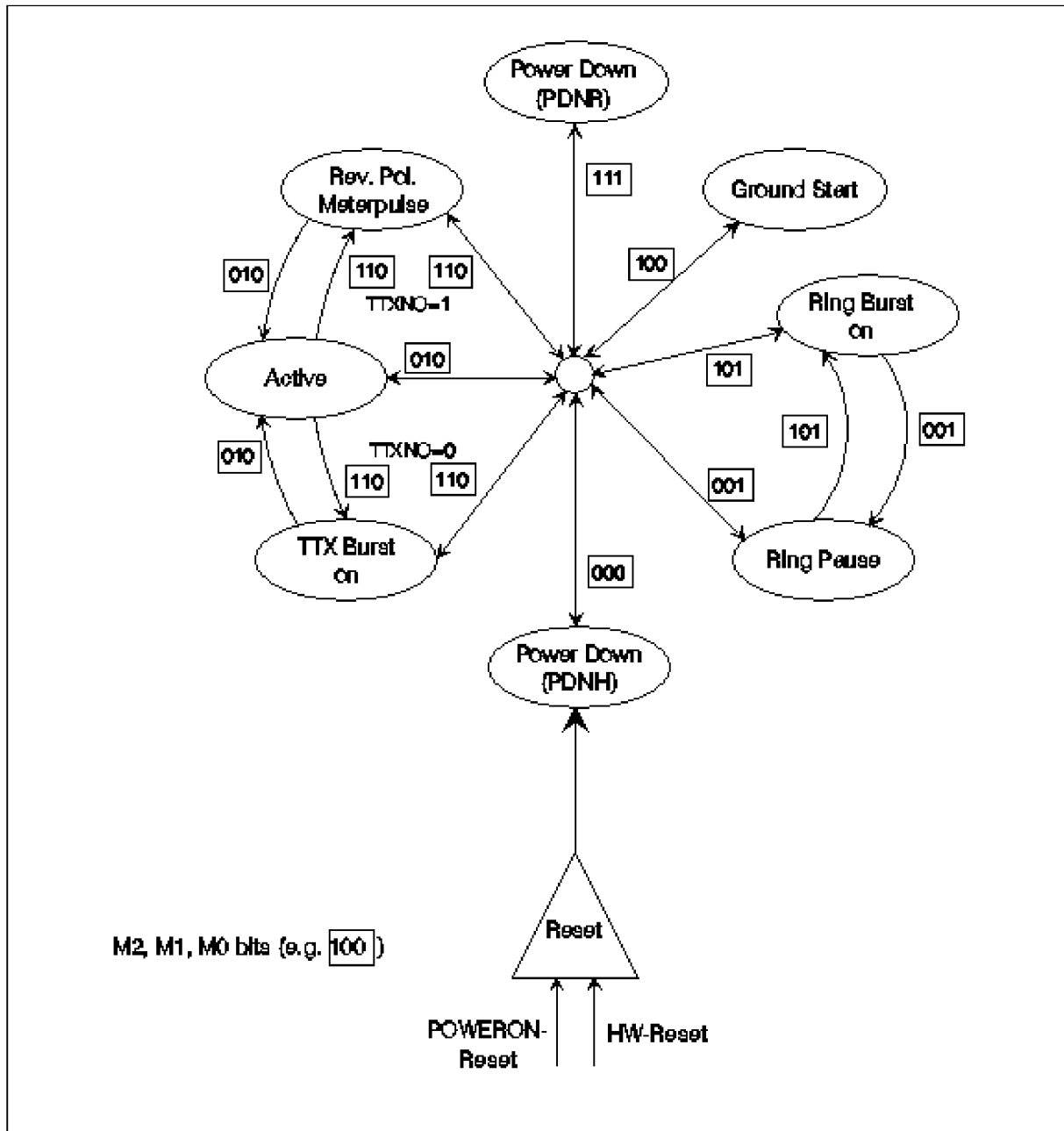


Figure 25

Operating Modes

Table 8 Operating Modes and the Ternary HV-Interface

MuPP										GAP						AHV-SLIC					
M2 (CIDD-4)	M1 (CIDD-3)	M0 (CIDD-2)	Description	BB (SCR0-6)	HIT (XTR0-7)	HIR (XTR0-6)	C1			C2			C1			C2			Description		
							VOL	VOM	VOH	VOL	VOM	VOH	VIL	VIM	VIH	VIL	VIM	VIH			
0	0	0	Power Down High Impedance (PDNH)	0	0	0	X			X					(X)	X				PDNH (also for not used combinations)	
1	1	1	Power Down Resistive (PDNR)	0	0	0	X				X						X			PDNR	
0	1	0	Active State	0	0	0			X		X				X		X			ACT	
1	1	0	Active State with Meterpulses	0	0	0			X		X				X		X			ACT	
1	0	0	Active State with Ground Start	0	0	0		X										X		HIT	
0	0	1	Ringling State (ring pause)	0	0	0		X			X						X			BB	
1	0	1	Ringling State (ring burst on)	0	0	0		X			X						X			BB	
0	1	0	Every Active State	1	0	0		X			X						X			BB	
1	1	0	For testing only; Active State with or without Meterpulses	0	1	0		X											X	HIT	
0	1	0	For testing only; Active State with or without Meterpulses	0	0	1	X													HIR	
0	1	0	For testing only; Active State with or without Meterpulses	0	1	1			X										X	HIRT	

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## Operating Modes

### 5.1 Reset Behavior

The MuSLIC has 2 different reset sources that are internally connected.

The **Reset pins**,  
which work totally asynchronously to the external clocks.

#### Power On Reset.

If internal VDD gets above typ. 2.33 V the MuPP is reset by Power On Reset.

Both sources set the MuSLIC to the basic setting modes (see below).

After a reset caused by any of the sources mentioned above, the reset bit (TCR0-1 = RES) is set to one and the SLCX-interrupt (CIDU-2) is set. Reading the TCR0 register clears the interrupt and the RES-bit.

The Reset pin (RESET) of the MuPP and the QAP has a Schmitt-Trigger input to reduce the sensitivity for spikes. In addition the pin RESET has a spike rejection. All spikes smaller than typ. 70 ns are neglected. The pin RESET can be set to 1 for an unlimited time but at least 2  $\mu$ s is recommended; during that, the DU pin is set to high impedance. The  $\mu$ C-IO pins are set as inputs.

In the MuPP a reset activates the reset routine - but only if the DCL is present - which lasts at least two 2 kHz frame (AFSC) periods for setting the default values. After this time and if an external reset is not active (RESET = 0) the MuPP starts the normal (default) operation at the beginning of the next 8 kHz frame (FSC).

In the QAP a reset works totally asynchronously and no reset routine is necessary.

The normal (default) operation of the QAP starts at the beginning of a 2 kHz frame (ASFC) if the external reset (RESET = 0) is released.

### 5.2 Basic Setting Modes

After RESET, the MuSLIC is switched automatically to its basic settings in which internal default values for all filters and settings (AC and DC) are used. The whole module works in a kind of "emergency mode" and can be handled by the C/I-Interface commands only. This means that for an (un-)determined reset (e.g. Power On Reset) the MuSLIC is reset, but can be switched to or return automatically into any operating mode presented by the C/I-channel after 2 AFSC + 2 FSC cycles. In all modes the outputs (QO<sub>i</sub>) become tristate up to the first SOP Command, the I/Os (MIO<sub>i</sub>, QIO<sub>i</sub>) become inputs, supervision and DC-feeding are still working and conversation can go on in a proper way until all filters and settings have been reloaded by SOP, XOP and COP Commands.

Actions initialized by a reset:

- All configuration registers are set to their default values (note that the Coefficient RAM is **not** reset)
- The RES-bit (TCR0-1) is set to 1 to indicate that a reset has taken place
- The IOM-2 and the  $\mu$ C-interface is reset. Running communication is stopped
- DU is in high impedance state
- AC- and DC-loop use the default values and not the programmed ones (see below)

**Operating Modes**

**Table 9**

<b>DC</b>			
Const I	24	mA	Limit for Constant Current
Const V	38	V	Limit for Constant Voltage
Vdrop	28	V	Overall voltage drop
BoostGain	1.3		Additional gain in Boosted Battery Mode
RFS	375	$\Omega$	Feeding Resistance (excluding the external Fuse resistors)
$f_{Ring}$	25	Hz	Ring Frequency
$A_{Ring}$	62	Vrms	Ring rms-value at Ring/Tip wire
DC Offset <sub>Ring</sub>	22	V	Ring offset
$f_{RingLP}$	75	Hz	Corner Frequency of Ring-Lowpass
OffhookPD	2	mA	Power-Down Current for Offhook Detection
OffhookAct	8	mA	Offhook Detection in Active with 2 mA hysteresis
OffhookRing	5	mA	DC-Current for Offhook Detection in Ringing Mode
LineSup	5	mA	Current for Line-Supervision
Levelmeter1	8	mA	First levelmeter threshold
Levelmeter2	12	mA	Second levelmeter threshold
Levelmeter3	21	mA	Third levelmeter threshold
Levelmeter4	25	mA	Fourth levelmeter threshold
GKD1	17	mA	First threshold-current for Ground-Key-Detection
GKD2	40	mA	Second threshold-current for Ground-Key-Detection
RingTip	52	V	Threshold at Ring/Tip wire
DC-Lowpass	0.3/20	Hz	DC- Lowpass set to 0.3 and 20 Hz respectively
ConstRamp	300	V/s	Slope of the ramp while testing
delay <sub>Ring</sub>	0	ms	Delay of Ring Burst
SRend1	1/128		Silent-Reversal threshold 1 (referred to the input of the rampgenerator)
SRend2	1/512		Silent-Reversal threshold 2 (referred to the input of the rampgenerator)
SRduration	ca. 80	ms	Duration of a Silent-Reversal-sequence
DUP	10	ms	Data Upstream Persistency Counter is set to 10 ms
DUPGNK	20	ms	Data Upstream Persistency Counter for GNK is set to 20 ms

- Boosted Battery is reset to normal feeding
- Reverse Polarity is reset to Normal Polarity
- All bits of the Signalling Register are masked and reset to 0 without the RES bit

**Operating Modes**

- The Data Upstream C/I channel bits are set to 0 except SLCX, it is set to 1 (the IO's are set to Input pins)
- Outputs are set tristate until the first SOP command
- C1 and C2 are set to PDNH
- A-Law is chosen

**Table 10**

<b>AC</b>			
IM-Filter	900	$\Omega$	Approximately 900 $\Omega$ Real Input Impedance
TH-Filter	TH <sub>BRD</sub>		Approximately BRD-Impedance for Balanced Network
AX	10	dB	Attenuation Transmit (this means about 0 dB)
AR	- 15.11	dB	Attenuation Receive (this means about - 7 dB)
ATTX	4	Vrms	Teletax Generator Amplitude at Ring / Tip wire at AHV-SLIC
f <sub>TTX</sub>	16	kHz	Teletax Generator frequency;
TG1	1008	Hz	Tone Generator 1 and AC -levelmeter Bandpass (- 14 dBm0)
TG2	2000	Hz	Tone Generator 2 (+ 2 dB compared to TG1)

**5.3 Power Down (PDown)**

After a Reset (including the Power On Reset) or programming the CIDD-Byte the MuSLIC is set to Power Down State. In Power Down all functions which are not necessary are disabled to minimize power consumption. This can be done for all the channels or only for the not active ones. While the interface is fully working - including programmability of the registers with SOP or XOP commands and the Coefficient RAM (COP commands) - the rest of the MuSLIC is turned off except the supervision of the line. The change of the line state is reported via the HOOK-bit in the IOM-2 Data Upstream channel. To avoid spurious Offhook informations caused by longitudinal induction the HOOK-bit is low pass filtered (programmable with the DUPGNK-counter in PDown state only). The voice channel Data Downstream is directly fed into the voice channel Data Upstream. The HOOK-indication in PDown is optimized for longitudinal suppression up to 65 Vrms for the Offhook transition.

In Power Down Mode the AHV-SLIC can be set into two different modes:

1. PDNR, the resistive mode which provides a connection of 10 k $\Omega$  from TIP and RING to BGND and VBAT, respectively
2. PDNH, offers high impedance at TIP and RING



---

**Operating Modes****5.4 Active Mode (Act)**

In Active Mode (“Conversation State”) both AC-and DC-Loop are fully working. The output voltage at the DC pins is controlled via the IT input pin in such way, that it behaves like a constant current source which turns automatically into a programmable resistive feeding source due to the DC-Characteristic values.

The ternary AHV-SLIC-interface is set to one of the active modes.

**Polarity**

The MuSLIC supports either normal or reverse Polarity which is set by the POLNR-bit (SCR0-7). A 180 degrees phase shift of the AC- and DC-Loop is done. The performance and the functionality is not influenced by that.

**Boosted Battery**

To feed subscriber lines with enhanced loop resistance the MuSLIC supports the Boosted Battery mode. The AHV-SLIC-Interface pins (C1, C2) are set to Boosted Battery (BB) mode and the maximum DC output voltage is extended to 140 V.

**Meterpulses**

The MuSLIC supports two different kinds of meterpulses: Meterpulses with 12/16 kHz (Teletax Metering) and with polarity reversal. The decision between these two types is made by the bit TTXNO (SCR1-7). If the bit TTXNO is set to 1 then the meterpulse is reversal. If the bit TTXNO is set to 0, Teletax Metering is used.

**Metering with Polarity Reversal**

As long as the M1 and the M2 bit of the C/I-channel (CIDD-4) is set to 1, the MuSLIC performs an immediate 180 degrees phase shift of the AC- and DC-Loop.

**Teletax Metering Injection**

For countries with Teletax Metering the MuSLIC provides either a 12 or a 16 kHz Signal (switchable with the bit TTX12 (SCR1-6))<sup>1)</sup> which amplitude is free programmable up to 10 Vrms at the Ring/Tip wire. The MuSLIC filters the Teletax pulses in transmit direction, too. The slope of the pulses are internally shaped so that the noise during switching and transmission is less than  $50 \times 6.25 \mu\text{V}$  at AC pins and 1 mV at the IOM-2 interface (psophometrically weighted). With the bit NOSL (SCR1-5) the slope can be switched off. In that case the switching noise is not defined (for signalling only).

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<sup>1)</sup> Note, that the right Teletax Coefficient Set (via COP-command) must be provided, too.

**Operating Modes****5.5 Ringing Mode**

The MuSLIC generally supports balanced and unbalanced ringing.

If the MuSLIC is set to Ringing Mode, the AC-loop is turned off and the DC-loop is automatically opened.

The voice channel Data Downstream is directly fed into the voice channel Data Upstream.

**Balanced Ringing**

The sine wave of the ringing is generated in the MuSLIC. The frequency and the amplitude are free programmable between 16 and 70 Hz and up to 85 Vrms at the Ring/Tip wire, respectively. The DC offset voltage is programmable between 0 V and 30 V. If the Ring Burst On command is sent to the MuSLIC via the C/I-channel (M0 and M2 = 1) the begin (M2 = 1) and the end (M2 = 0) of the ring burst is automatically synchronized at the voltage zero crossing. If the DC-current at the IT-pin exceeds the programmed value, Offhook is detected within 2 periods of the ringing frequency and the Ring Burst is neglected. If Offhook is detected the MuSLIC changes automatically to the active mode.

**Unbalanced Ringing**

The ringing voltage is generated by an external ring generator. To connect this generator to the Ring/Tip wires relays are used. To control the relays the MuSLIC offers following functions:

If the REXTEN bit (XR2-7) is set to 1 the MIO1 is an input for the zero crossing signal. QIO1 is switched to the CIDD-4 (M2 bit) and offers the zero crossed ring burst on/off control signal.

**5.6 Ground Start**

Changing into the Ground Start mode by programming the CIDD Byte (M2 = 1, M1 and M0 = 0) the active mode is chosen and the Ternary SLIC-interface is set to high impedance of the Tip output (HIT: C1 = VOM, C2 = VOH).

**5.7 Changing Modes**

Offhook detection is low pass filtered with the time of 2 x DUP counter if any change of the modes or if one of the following crossovers occurs:

ring burst	<---->	ring pause
reverse	<---->	normal polarity
boosted	<---->	normal battery
ground start on	<---->	off
PDNR on	<---->	off
FIXC, LOAD, RESET on	<---->	off

**Transmission Characteristics**

**6 Transmission Characteristics**

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) needs a complete knowledge of MuSLIC analog environment. Unless otherwise stated, the transmission characteristics are guaranteed within the test conditions.

**Test Conditions**

$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$ ;

$V_{DDI} = V_{DDA} = V_{DDB} = V_{DDC} = V_{DDD} = 5 \text{ V} \pm 5\%$ ;  $V_{SS} = -5 \text{ V} \pm 5\%$ ;

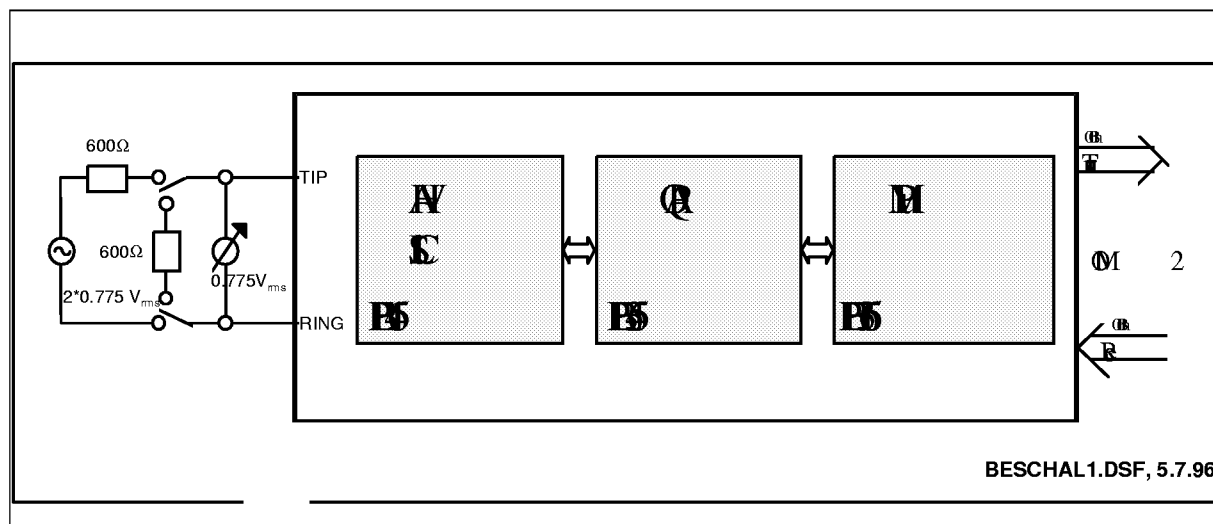
$V_{DD} = 3.3 \text{ V} \pm 5\%$

$GNDI = GND A = GND B = GND C = GND D = 0 \text{ V}$

$H_{IM}$ ,  $H_{TH}$ ,  $H_{FRX}$ ,  $H_{FRR}$ ,  $AR$ ,  $AX$  will be defined to meet the 0 dBm0 specification.

$f = 1004 \text{ Hz}$ ; 0 dBm0; A-Law;

A 0dBm0 AC signal in Transmit direction is equivalent to  $2 \times 0.775 \text{ V}_{rms}$  and in Receive direction equivalent to  $0.775 \text{ V}_{rms}$  (referred to  $600 \text{ } \Omega$ ).



**Figure 26**

$0 \text{ dBm0}|_{\text{MuSLIC}} = 0 \text{ dBm0}|_{600 \text{ } \Omega} = 0.775 \text{ V}_{rms}$  for receive direction.

$0 \text{ dBm0}|_{\text{MuSLIC}} = 0 \text{ dBm0}|_{600 \text{ } \Omega} = 2 \times 0.775 \text{ V}_{rms}$  for transmit direction.

**Transmission Characteristics**

**6.1 Transmission Values**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Interface Requirements**

<u>2-wire port</u>						$2 \times 100 \Omega R_p$ incl.
Out of band signalling						
Metering signal	$V_{ab}$	4.5	4.85	5.2	Vrms	12/16 kHz @ 200 $\Omega$
Ringing injection	$V_{ab}$	60	63	66	Vrms	16 Hz to 50 Hz
Longitudinal current capability AC	III	30			mArms	per line active
Transmission performance						
Overload level	$V_{ab}$	2.3			Vrms	300 Hz to 4 kHz
Return loss (2-wire)	$R_L$	14		18	dB	300 Hz to 500 Hz
	$R_L$		18		dB	500 Hz to 2 kHz
	$R_L$	14		18	dB	2 kHz to 3.4 kHz
Insertion loss						
Transmit V gain	$G_t$	- 0.3		0.3	dB	0 dBm0, 1 kHz
Receive V gain	$G_r$	- 0.3		0.3	dB	0 dBm0, 1 kHz
Insertion loss versus frequency						relative to 1 kHz
Transmit V gain	$G_t$	see <b>chapter 6.2</b>				0 dBm0, 0.3 to 3.4 kHz
Receive V gain	$G_r$	see <b>chapter 6.2</b>				0 dBm0, 0.3 to 3.4 kHz
Gain/Loss programmability						
Transmit absolute + 3 dBr	$T_x$			0.5	dB	voice band, in steps of
Receive absolute 0 ... - 12 dBr	$R_x$			0.5	dB	voice band, in steps of

**Transmission Characteristics**

**6.1 Transmission Values (cont'd)**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Gain linearity						relative to 1 kHz, – 10 dBm0
Transmit V gain	$G_t$	see <b>chapter 6.3</b>				– 55 dBm0 to + 3 dBm0
Receive V gain	$G_r$	see <b>chapter 6.3</b>				– 55 dBm0 to + 3 dBm0
Balance return loss		20			dB	500 Hz to 2.5 kHz
Absolute group delay distortion		see <b>chapter 6.4</b>				
Overload compression A/A	OC	see <b>chapter 6.5</b>				
Longitudinal balance						
Longitudinal to transversal world market requirement	L-T	52			dB	300 Hz to 3.4 kHz
US market requirement	L-T	58	65		dB	at 1020 Hz
Transversal to longitudinal	T-L	46			dB	300 Hz to 4 kHz
Longitudinal signal generation	T-L	46			dB	300 Hz to 4 kHz

**Transmission Characteristics**

**6.1 Transmission Values (cont'd)**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
<b>Out-of-band Noise</b>						single frequency inband – 25 dBm0
Transversal	$V_{ab}$			– 50	dBm	12 kHz to 200 kHz
Longitudinal	$V_{ab}$			– 50	dBm	12 kHz to 200 kHz
Metering injection						
Impulse noise during switching	$V_{ab}$			1	mV	psophometrically
At 2-, 4-wire interface	$V_{tx}$			1	mV	weighted
Harmonic distortion				5	%	
Ring injection						
Transfer gain	$G_{rng}$	t.b.d.	0.5	t.b.d.	dB	$Z_L = 1200 \Omega$
Superimposed d.c. voltage	$V_{rdc}$	20	22	24	V	$R_L = 10 k\Omega$
Harmonic distortion	THD			5	%	$Z_L = 1 k\Omega \parallel 6 \mu F$
Ring trip function						
Detection time and delay after		12 ms		2	periods	
The ringing to off hook status				2	periods	
Cut off the ringing						

**Transmission Characteristics**

**6.1 Transmission Values (cont'd)**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Interface Requirements**

2-wire port and PCM side

Total harmonic distortion						
2- to 4-wire	$T_{hd4}$			- 46	dB	- 7 dBm0, 0.3 to 3.4 kHz
4- to 2-wire	$T_{hd2}$			- 46	dB	- 7 dBm0, 0.3 to 3.4 kHz
Idle channel noise						
2-wire port (receive)	$V_{ab}$			- 70	dBmp	psophometric (idle code +0)
A-Law						
$\mu$ -Law	$V_{ab}$			20	dBrc	C-message (idle code +0)
PCM side (transmit)						
A-Law	$N_{TP}$			-67	dBmp	psophometric ( $V_{IN} = 0$ )
$\mu$ -Law	$N_{TC}$			20	dBrc	C - message ( $V_{IN} = 0$ )
Signal to total distortion ratio						
Input connection: $L_i = 0$ dBr	S/D	see <b>chapter 6.6</b>				- 45 dBm0 to 0 dBm0
Output connection: $L_o = - 7$ dBr	S/D	see <b>chapter 6.6</b>				- 45 dBm0 to 0 dBm0

**Transmission Characteristics**

**6.1 Transmission Values (cont'd)**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
<b>Battery Feeding</b>						$V_{BAT} = -68\text{ V}$ , $V_H = +52\text{ V}$
Power Down Mode (PDNR)						
Loop resistance	$R_S$	6.4	8	9.6	$k\Omega$	
Active Mode						without calibration
Loop current (without TTX)	$I_L$	19			mA	$R_L = 1.8\text{ k}\Omega$
$I_{loop}$ accuracy	$I_L$	23	25	27	mA	$I_{link2} = 25\text{ mA}$
$I_{loop}$ accuracy	$I_L$	27	30	33	mA	$I_{link3} = 30\text{ mA}$
$I_{loop}$ accuracy	$I_L$	41	45	49	mA	$I_{link4} = 45\text{ mA}$
$I_l$ negative wire	$I_W$	90		120	mA	wire to ground
Transition time	$T_{off}$	0.5		1.5	ms	On to Offhook
Boost Battery Mode						
Loop current						same as active state
Output voltage	$V_{ab}$	78		86	V	$I_{line} = 20\text{ mA}$
Indication thresholds						
Offhook indication						
Offhook current	$I_{det}$	7	9	11	mA	
Hysteresis			2		mA	
Ground Key indication						
Ground Key current	$I_{det}$	10	17	24	mA	
Ring trip indication						
Current threshold 1	$I_{det}$	6	7	8	mA	short line + bat. charging
Current threshold 2	$I_{det}$	2.5	3.5	4.5	mA	long line
Power supply rejection ratio						$V_{ripple} = 100\text{ mVpp}$
VCC referred to AGND	PSRR	30			dB	50 Hz to 4 kHz
-objective		40			dB	50 Hz to 4 kHz
			t.b.d			4 kHz to 128 kHz



**Transmission Characteristics**

**6.1 Transmission Values (cont'd)**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
VBAT referred to AGND -objective	PSRR	30			dB	50 Hz to 4 kHz
		40			dB	50 Hz to 4 kHz
			t.b.d			
BGND referred to AGND -objective	PSRR	40			dB	50 Hz to 4 kHz
		40			dB	50 Hz to 4 kHz
			t.b.d			

Transmission Characteristics

6.2 Frequency Response

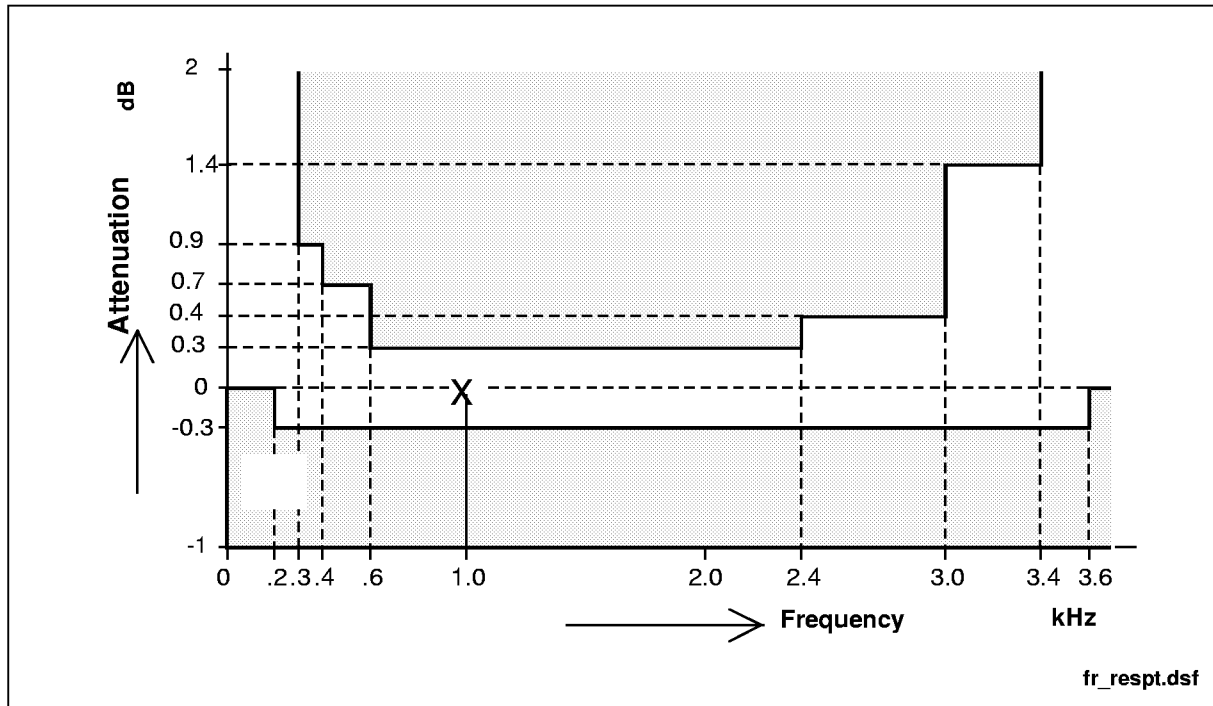


Figure 27 Transmit: reference frequency 1 kHz, signal level - 10 dBm0,  $H_{FRX} = 1$

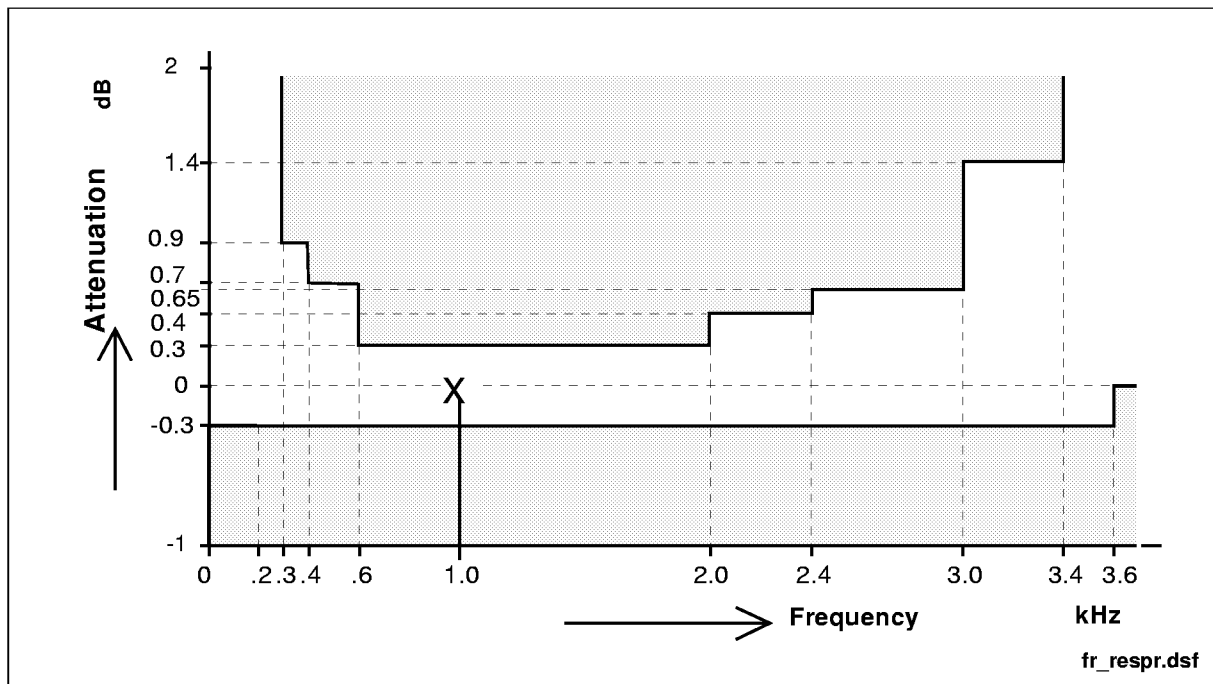


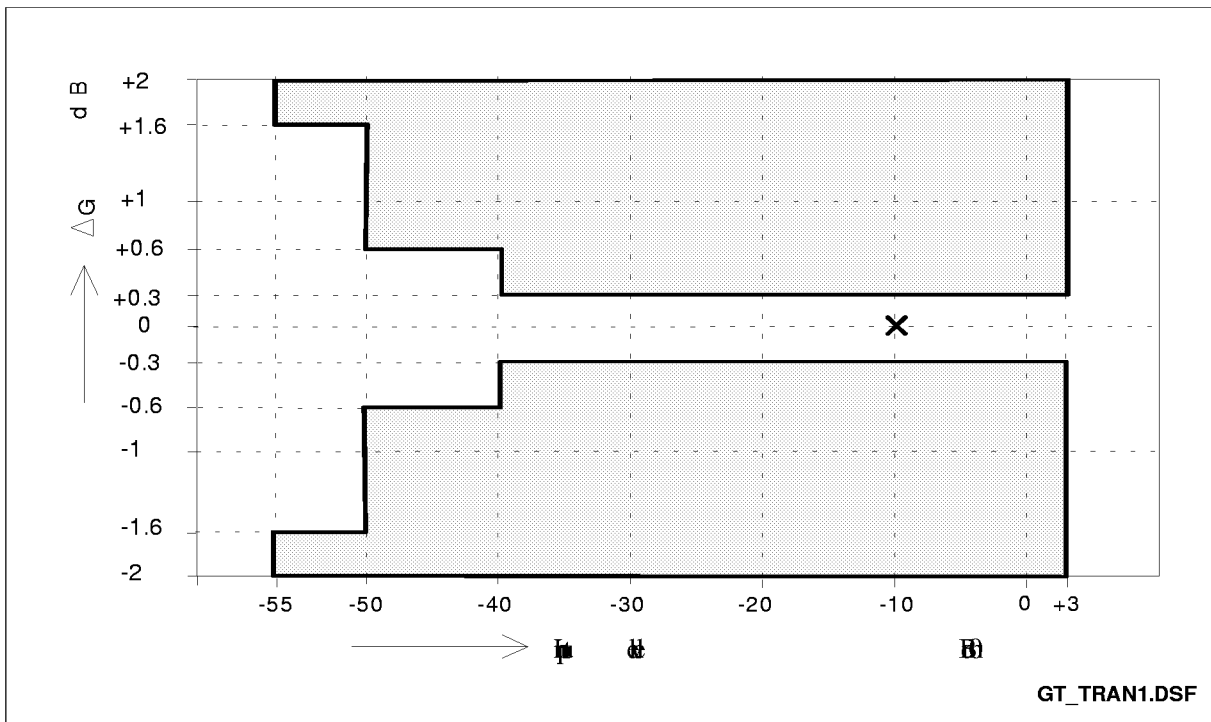
Figure 28 Receive: reference frequency 1 kHz, signal level - 10 dBm0,  $H_{FRR} = 1$

**Transmission Characteristics**

**6.3 Gain Tracking (receive or transmit)**

The gain deviations stay within the limits in the figures below.

measured with sine wave  $f = 1004 \text{ Hz}$   
 reference level is  $-10 \text{ dBm0}$ .



**Figure 29**

Transmission Characteristics

6.4 Group Delay

Maximum delays when the PEB 3465 and the PEB 31665 are operating with  $H_{TH} = H_{IM} = 0$  and  $H_{FRR} = H_{FRX} = 1$  including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group Delay deviations stay within the limits in the figures below.

**Group Delay absolute values:** Signal level – 10 dBm0

Table 11

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Transmit delay	$D_{XA}$	330		475	$\mu s$	$f = 1.5 \text{ kHz}$
Receive delay	$D_{RA}$	250		425	$\mu s$	$f = 1.5 \text{ kHz}$
Trans.-Receiver delay	$D_{XRA}$			900	$\mu s$	$f = 1.5 \text{ kHz}$

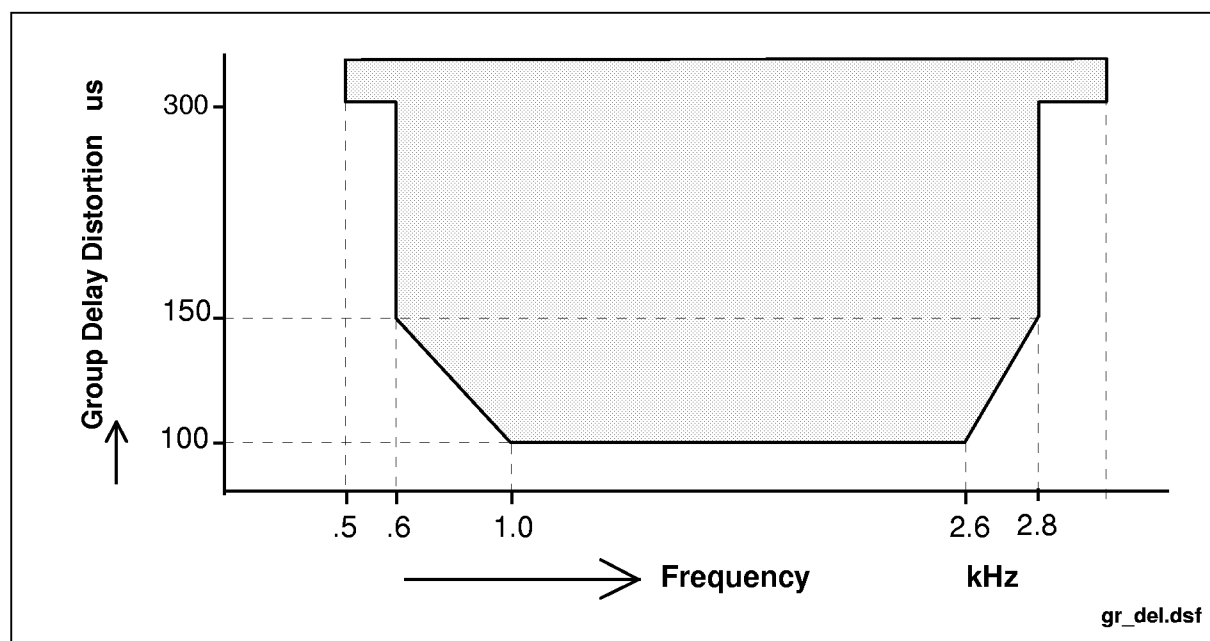


Figure 30 Group Delay Distortion receive and transmit:  
Signal level – 10 dBm0,  $f_{Test} @ T_{Gmin}$

Transmission Characteristics

6.5 Overload Compression

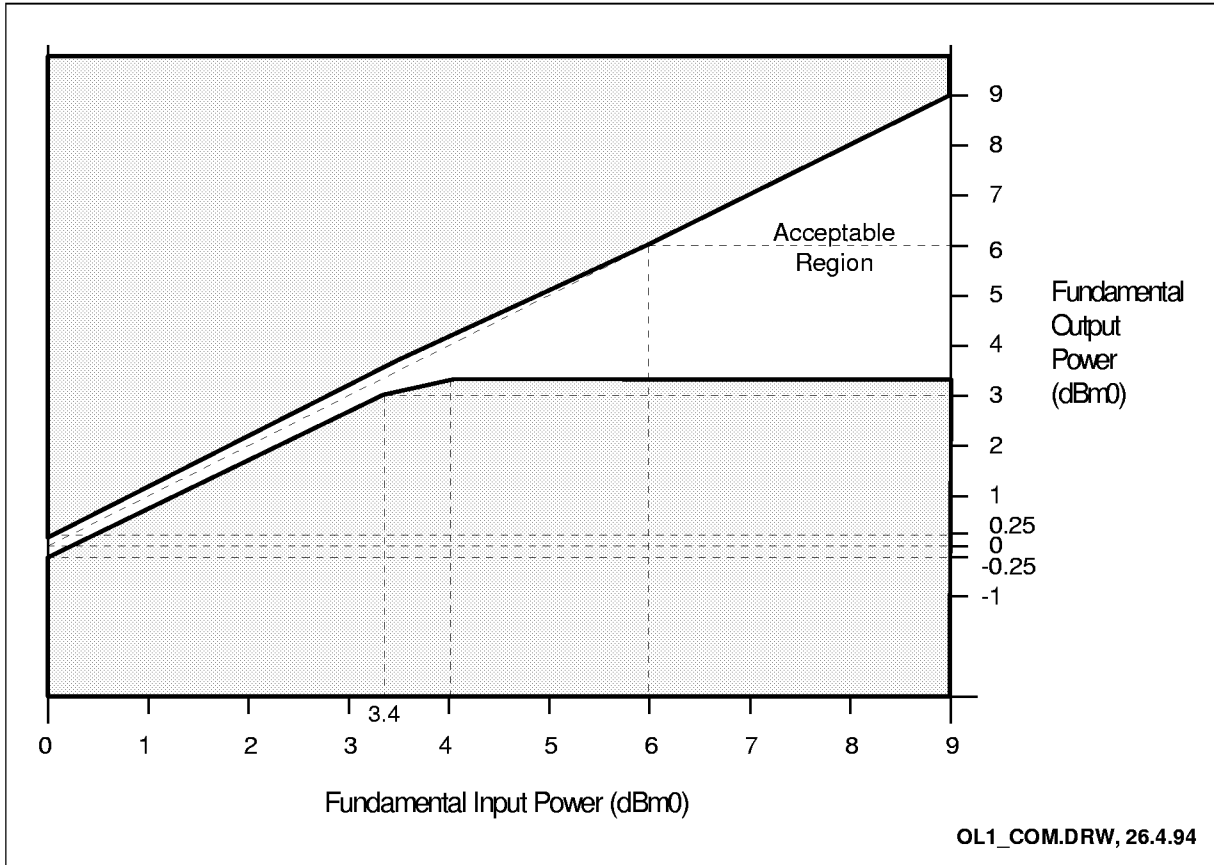


Figure 31 Transmit: measured with sine wave  $f = 1004$  Hz

Transmission Characteristics

6.6 Total Distortion

The signal to distortion ratio exceeds the limits in the following figure:

**Receive:** measured with sine wave  $f = 1004$  Hz. (C-message weighted for  $\mu$ -law, psychoacoustically weighted for A-law). The mean relative level is  $-7$  dBr.

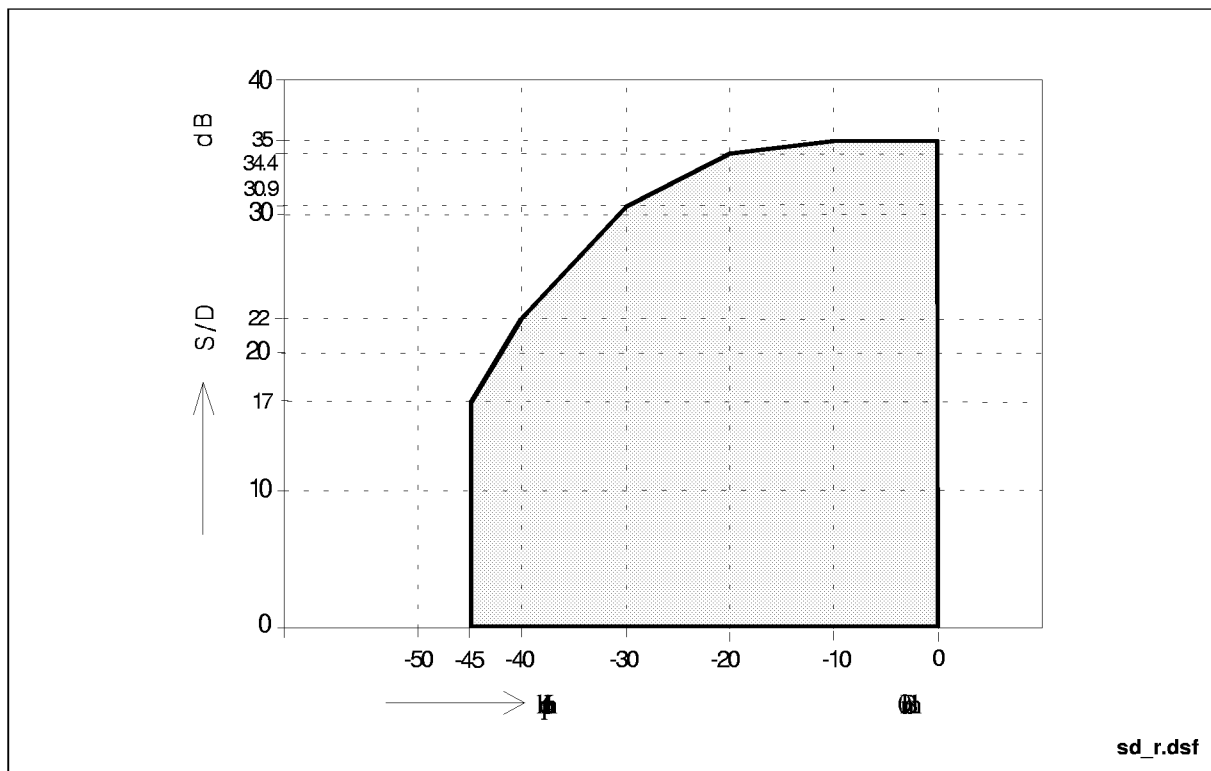


Figure 32

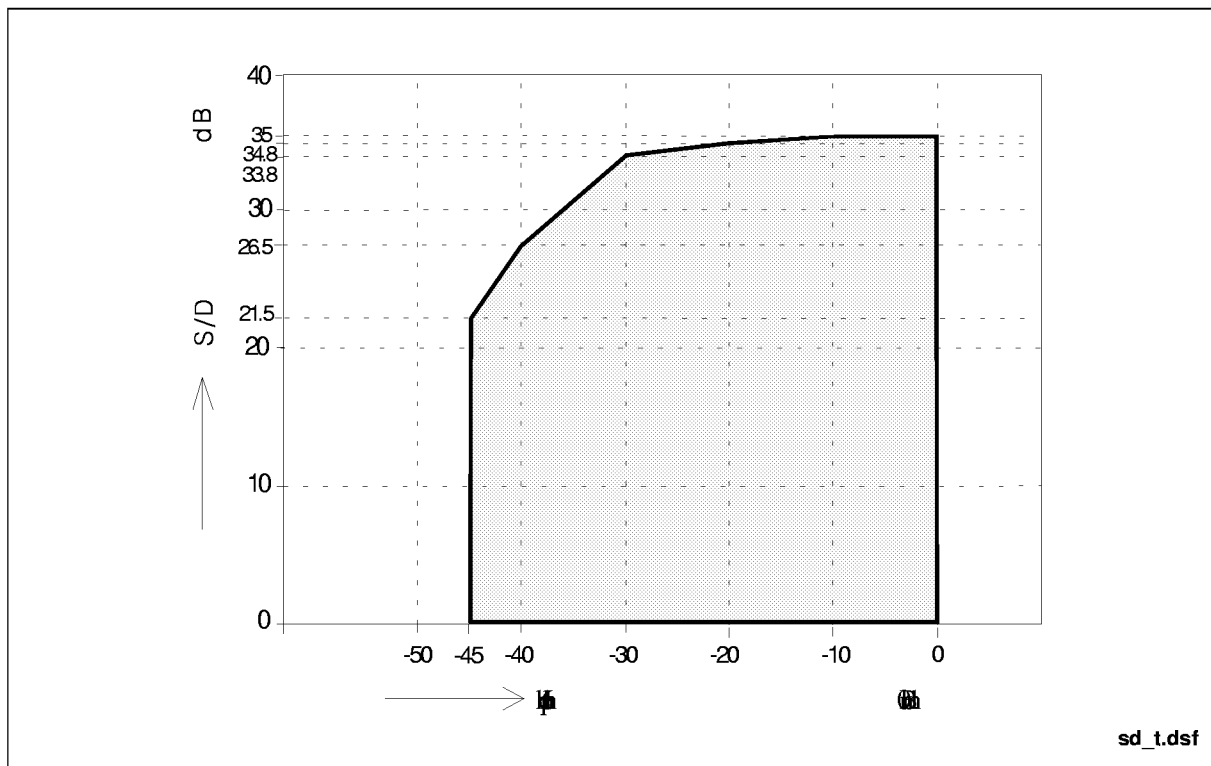
AR = 7 dBr

Table 12

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Signal to distortion at full attenuation	$SD_{att R}$		- 13		dB	Signal S = - 40 dB AR = + 30 dB

**Transmission Characteristics**

**Transmit:** measured with sine wave  $f = 1004$  Hz. (C-message weighted for  $\mu$ -law, psophometrically weighted for A-law). The mean relative level is 0 dBr.



**Figure 33**

AX = 0 dBr

**Table 13**

Parameter	Symbol	Limit Values			Unit	Test Condition
		mi.n	typ.	max.		
Signal to distortion at full gain	$SD_{att T}$		- 17		dB	Signal S = - 40 dB AX = - 30 dB

Transmission Characteristics

6.7 Out-of-Band Signals at Analog Output (receive)

With a 0 dBm0 sine wave with frequency  $f$  (300 Hz to 3.4 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

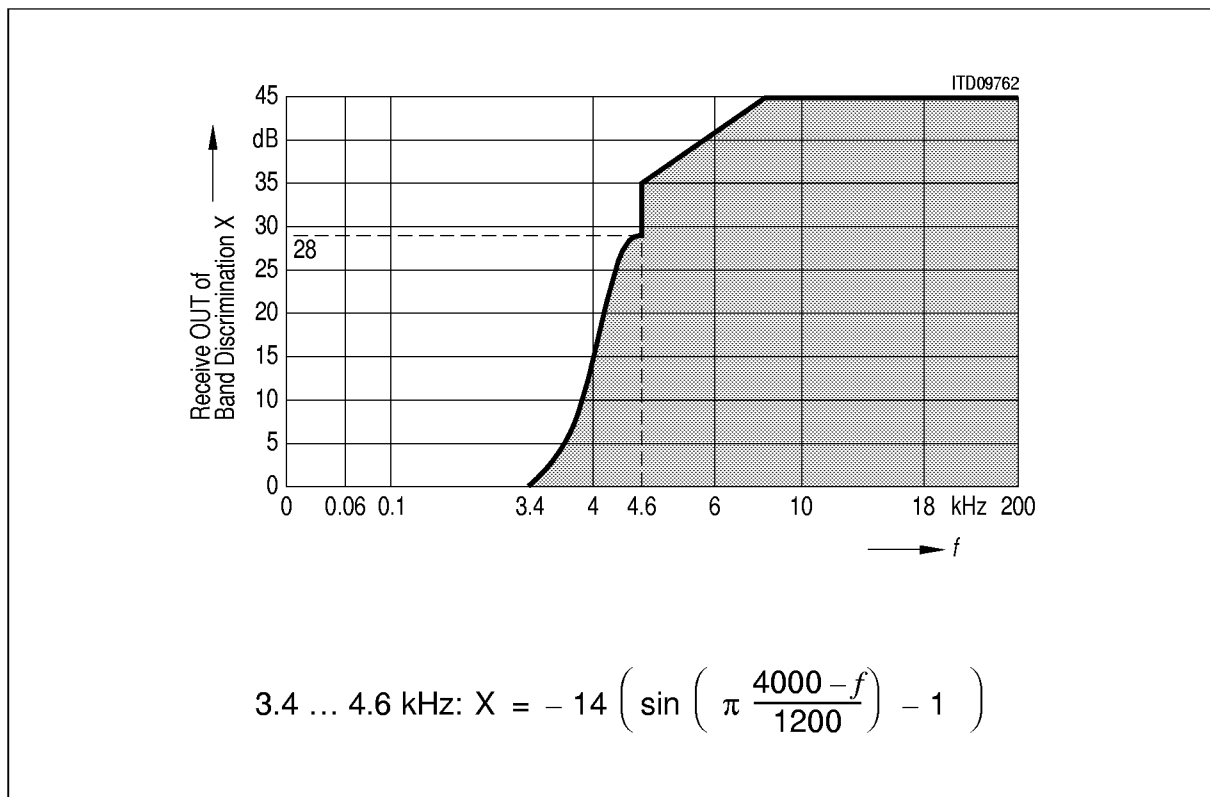


Figure 34



Transmission Characteristics

Out-of-Band Signals at Analog Input (transmit)

With a 0 dBm0 out-of-band sine wave signal with frequency  $f$  ( $< 100$  Hz or  $3.4$  kHz to  $100$  kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least  $X$  dB below a  $0$  dBm0,  $1$  kHz sine wave reference signal at the analog input. <sup>1)</sup>

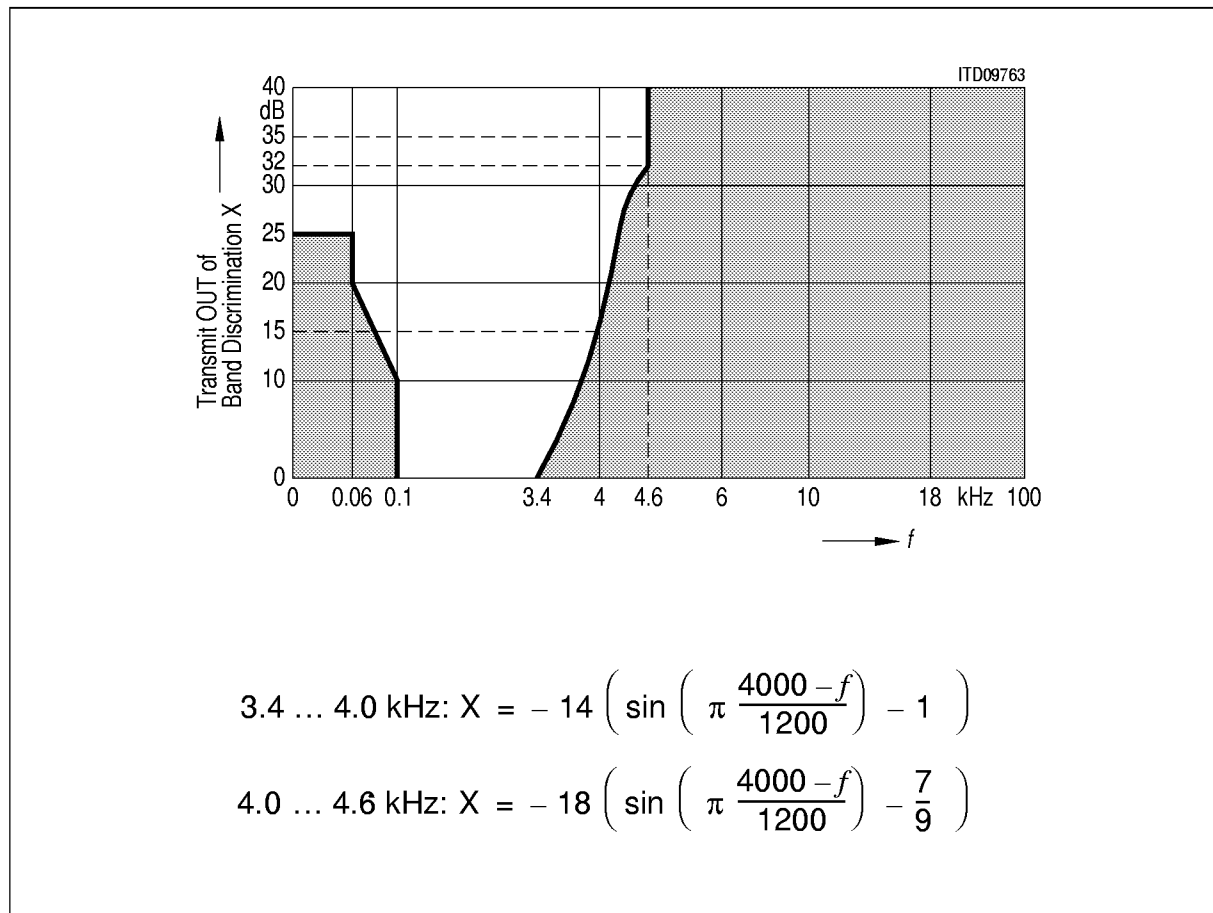


Figure 35

<sup>1)</sup> Poles at  $12 \text{ kHz} \pm 150 \text{ Hz}$  respectively  $16 \text{ kHz} \pm 150 \text{ Hz}$  and harmonics will be provided

**Transmission Characteristics**

**6.8 Transhybrid Loss**

The quality of Transhybrid-Balancing is very sensitive to deviations in gain and group delay – deviations inherent to the MuSLIC A/D- and D/A-converters as well as to all external components used on a line card.

Measurement of MuSLIC Transhybrid-Loss: A 0dBm0 sine wave signal with a frequency in the range between 300 – 3400 Hz is applied to the digital input. The resulting analog output signal at the differential outputs ACP and ACN is connected to the pin ITAC. The programmable filters FRR, AR, FRX, AX and IM are disabled, the balancing filter TH is enabled with coefficients optimized for this configuration (ACP–ACN = ITAC).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below.

**Table 14**

	<b>COP-write</b>	<b>Coefficients</b>
TH-Filter Part 1	t.b.d.	t.b.d.
TH-Filter Part 2	t.b.d.	t.b.d.
TH-Filter Part 3	t.b.d.	t.b.d.

**Table 15**

<b>Parameter</b>	<b>Symbol</b>	<b>Limit Values</b>		<b>Unit</b>	<b>Test Condition</b>
		<b>min.</b>	<b>typ.</b>		
Transhybrid Loss at 500 Hz	THL <sub>500</sub>		50	dB	
Transhybrid Loss at 2500 Hz	THL <sub>2500</sub>		44	dB	
Transhybrid Loss at 3000 Hz	THL <sub>3000</sub>		42	dB	

**Electrical Characteristics**

**7 Electrical Characteristics**

**7.1 PEB 3465 (QAP)**

**7.1.1 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
VDDA-VDDD referred to GNDA-GNDD		- 0.3	5.5	V	
VDDI referred to GNDI		- 0.3	5.5	V	
VSS referred to all GND pins		- 5.5	0.3	V	
GNDA-GNDD to GNDI		- 0.3	0.3	V	
VDDA-VDDD to VDDI		- 0.3	0.3	V	
Analog input and output voltages referred to VDD = 5 V; (VSS = - 5 V)		- 10.3	0.3	V	
referred to VSS = - 5 V; (VDD = 5 V)		- 0.3	10.3	V	
All digital input voltages referred to GNDI = 0 V; (VDDI = 5 V)		- 0.3	5.3	V	
referred to VDDI = 5 V; (GNDI = 0 V)		- 5.3	0.3	V	
DC input and output current at any input or output pin (free from latch-up)			100	mA	
Storage temperature	$T_{STG}$	- 65	125	°C	
Ambient temperature under bias	$T_A$	- 10	80	°C	
Power dissipation	$P_D$		1	W	

*Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.*

*Functional operation under these conditions is not implied.*

*Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may effect device reliability.*

**Electrical Characteristics**

**7.1.2 Operating Range**

$T_A = 0$  to  $70$  °C; all  $V_{DD}$ 's =  $5\text{ V} \pm 5\%$ ;  $V_{SS} = -5\text{ V} \pm 5\%$ ; all GND's =  $0\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
$V_{DD}$ supply current <sup>1)</sup>						
Power down	$I_{DD_{PDown}}$		24		mA	all channels PDown
Active	$I_{DD_{Act}}$		67		mA	all channels active
$V_{SS}$ supply current <sup>1)</sup>						
Power down	$I_{SS_{PDown}}$		0		mA	all channels PDown
Active	$I_{SS_{Act}}$		5		mA	all channels active
Power supply rejection-ratio	PSRR					ripple: 1 kHz, 100 mVrms
Receive VDD						t.b.d.
Receive VSS						t.b.d.
Transmit VDD		40			dB	at IOM-2
Transmit VSS		40			dB	at IOM-2
Power dissipation <sup>1)</sup>						
Power down	$P_{PDown}$		120		mW	all channels PDown
Active	$P_{act1}$		180		mW	1 channel active
Active	$P_{act}$		360		mW	all channels active

<sup>1)</sup> Power dissipation and supply currents are target values

*Note: In the operating range the functions given in the circuit description are fulfilled.*

Electrical Characteristics

7.1.3 I/O-Pins

$T_A = 0$  to  $70$  °C; all  $V_{DD}$ 's =  $5\text{ V} \pm 5\%$ ;  $V_{SS} = -5\text{ V} \pm 5\%$ ; all GND's =  $0\text{ V}$

Parameter	Symbol	Limit Values		Unit	Test Condition
		min	max.		
For all input pins:					
Low-input pos.-going	$V_{T+}$	- 0.3	3.15	V	see figure 36
Low-input neg.-going	$V_{T-}$	1.35	$V_{DD} + 0.3$	V	see figure 36
Low-input Hysteresis	$V_H$	0.5		V	$V_H = V_{T+} - V_{T-}$
Input leakage current	$I_{IL}$	- 1	1	$\mu\text{A}$	$- 0.3 \leq V_{in} \leq V_{DD}$
Spike rejection for RESET	$t_{rej}$	50	200	ns	
For I/O1 and O1:					
Low-output voltage	$V_{OL}$		0.5	V	$I_O = - 50\text{ mA}$
High-output voltage	$V_{OH}$	3.5		V	$I_O = 2\text{ mA}$
For I/O2:					
Low-output voltage	$V_{OL}$		0.5	V	$I_O = - 2\text{ mA}$
High-output voltage	$V_{OH}$	3.5		V	$I_O = 2\text{ mA}$

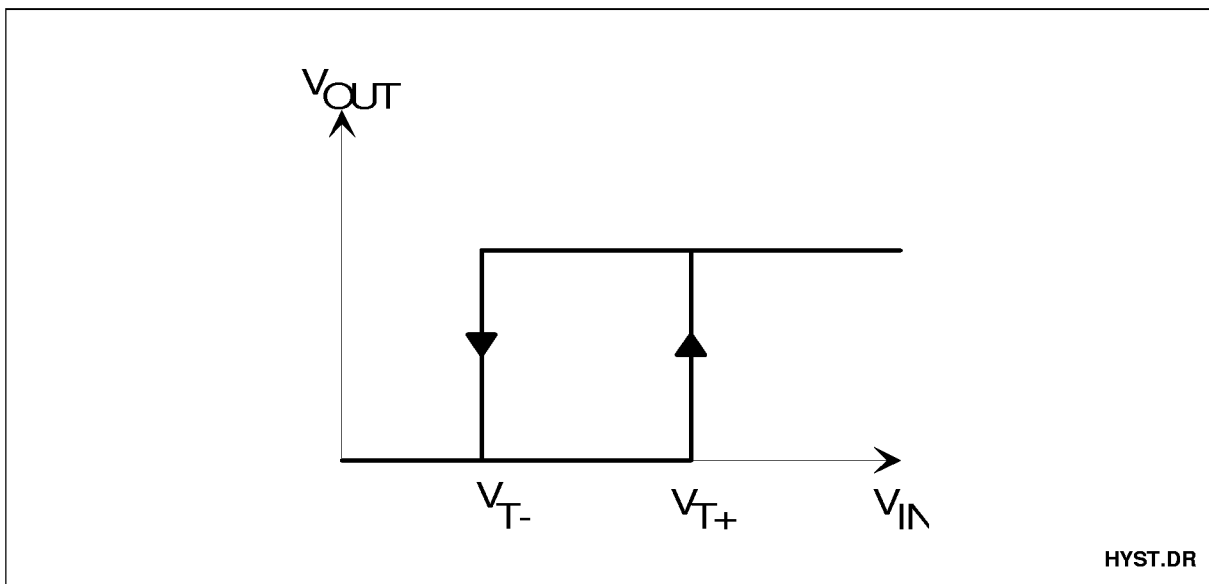


Figure 36

**Electrical Characteristics**

**7.1.4 DC-Feeding**

$T_A = 0$  to  $70$  °C; all  $V_{DD}$ 's =  $5\text{ V} \pm 5\%$ ;  $V_{SS} = -5\text{ V} \pm 5\%$ ; all GND's =  $0\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
"Line Current" Measurement: Transmit	$V_{IT\ offset}$	- 25		25	mV	direct/reverse polarity <sup>1)</sup>
	$V_{IT\ gain}$	0.95		1.05		$f < 50\text{ Hz}$ , direct/reverse polarity
	$V_{IT\ THD}$	40	50		dB	direct/reverse polarity
"Line Voltage" Feeding: Receive  Receive Boosted	$V_{DC\ offset}$	- 25		25	mV	normal battery, $f = 300\text{ Hz}$
	$V_{DC\ gain}$	0.94		1.06		normal battery, $f = 300\text{ Hz}$
	$V_{DC\ THD}$	40	50		dB	normal battery
	$V_{DC\ offset}$	- 40		40	mV	boosted battery, $f = 300\text{ Hz}$
	$V_{DC\ gain}$	1.5	1.6	1.7		boosted battery, $f = 300\text{ Hz}$
	$V_{DC\ THD}$	40	50		dB	boosted battery

<sup>1)</sup> Reverse polarity is an internal state of the PEB 31665; the polarity of the voltage at PIN IT is positive.

**Electrical Characteristics**

**7.1.5 AHV-SLIC Interface and Supervision Functions**

$T_A = 0$  to  $70$  °C; all  $V_{DD}$ 's =  $5\text{ V} \pm 5\%$ ;  $V_{SS} = -5\text{ V} \pm 5\%$ ; all GND's =  $0\text{ V}$

Parameter	Symbol	Limit Values			Unit	Test Condition/ Result
		min.	typ.	max.		
Longitudinal Current Input (IL)	$V_{IL\text{ gain}}$	0.9	1	1.1		$f < 50\text{ Hz}$ $V_{in} = -2.4 \dots +2.4\text{ V}$
Auxiliary Inputs (VA, VB, VBIM)	$V_{x\text{ gain}}$	0.9	1	1.1		$f < 50\text{ Hz};$ $V_{in} = -2.4 \dots +2.4\text{ V}$
Output voltage: AHV-SLIC-Interface C1, C2						
High level	$V_{OHHV}$		$0.8 \times VDD$		V	$I_{out} < 10\text{ }\mu\text{A}$
Mid level	$V_{OMHV}$		$0.51 \times VDD$		V	$I_{out} < 10\text{ }\mu\text{A}$
Low level	$V_{OLHV}$		$0.22 \times VDD$		V	$I_{out} < 10\text{ }\mu\text{A}$
Current drained from pin C1 in all 3 states	$I_{OTLo}$ $I_{OTHi}$	120		80	$\mu\text{A}$ $\mu\text{A}$	TEMPA = 0 <sup>1)</sup> TEMPA = 1

<sup>1)</sup> TEMPA is reported via the MuPP/QAP-Interface to the PEB 31665

**Electrical Characteristics**

**7.2 PEB 31665 (MuPP)**

**7.2.1 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
$V_{DD}$ referred to GND		- 0.3	3.6	V	
$V_{DD5}$ referred to GND		- 0.3	5.5	V	
All digital input voltages ( $V_{DD5} = 5$ V) referred to GND = 0 V; ( $V_{DD} = 3.3$ V) referred to $V_{DD} = 3.3$ V; (GND = 0 V)		- 0.3	5.3	V	
		- 5.3	0.3	V	
DC input and output current at any input or output pin (free from latch-up)			100	mA	
Storage temperature	$T_{STG}$	- 65	125	°C	
Ambient temperature under bias	$T_A$	- 10	80	°C	
Package power dissipation	$P_D$		1	W	

*Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional operation under these conditions is not implied. Exposure to conditions beyond those indicated in the recommended operational conditions of this specification may effect device reliability.*

**7.2.2 Operating Range**

$T_A = 0$  to  $70$  °C;  $V_{DD} = 3.3$  V  $\pm$  5%; GND = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power supply current			t.b.d.		mA	$V_{DD} = 3.3$ V
Power dissipation (all channels active)			t.b.d.		mW	$V_{DD} = 3.3$ V
Power dissipation (only 1 channel active)			t.b.d.		mW	$V_{DD} = 3.3$ V
Power dissipation (no channel active)			t.b.d.		mW	$V_{DD} = 3.3$ V

*Note: In the operating range the functions given in the circuit description are fulfilled.*



**Electrical Characteristics**

**7.2.3 Characteristics**

$T_A = 0$  to  $70\text{ °C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $GND = 0\text{ V}$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
For all input pins					
Input low-voltage	$V_{IL}$				TTL Level
Input high-voltage	$V_{IH}$				
Input leakage current	$I_{IL}$	- 1	1	$\mu\text{A}$	$- 0.3 \leq V_{in} \leq V_{DD5}$
Spike rejection for RESET	$t_{rej}$	50	200	ns	
For all output pins					
Set-up time	$t_s$		typ. 30	ns	Load capacitance 30 pF
Output low-voltage	$V_{OL}$		0.45	V	$I_{OL} = - 3.2\text{ mA}^1)$
Output high-voltage	$V_{OH}$	0.7 VDD		V	$I_{OH} = 2\text{ mA}$

<sup>1)</sup> DU:  $I_{OL} = - 7\text{ mA}$

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25\text{ °C}$  and the given supply voltage.*

Electrical Characteristics

7.2.4 IOM<sup>®</sup>-2 Switching Characteristics

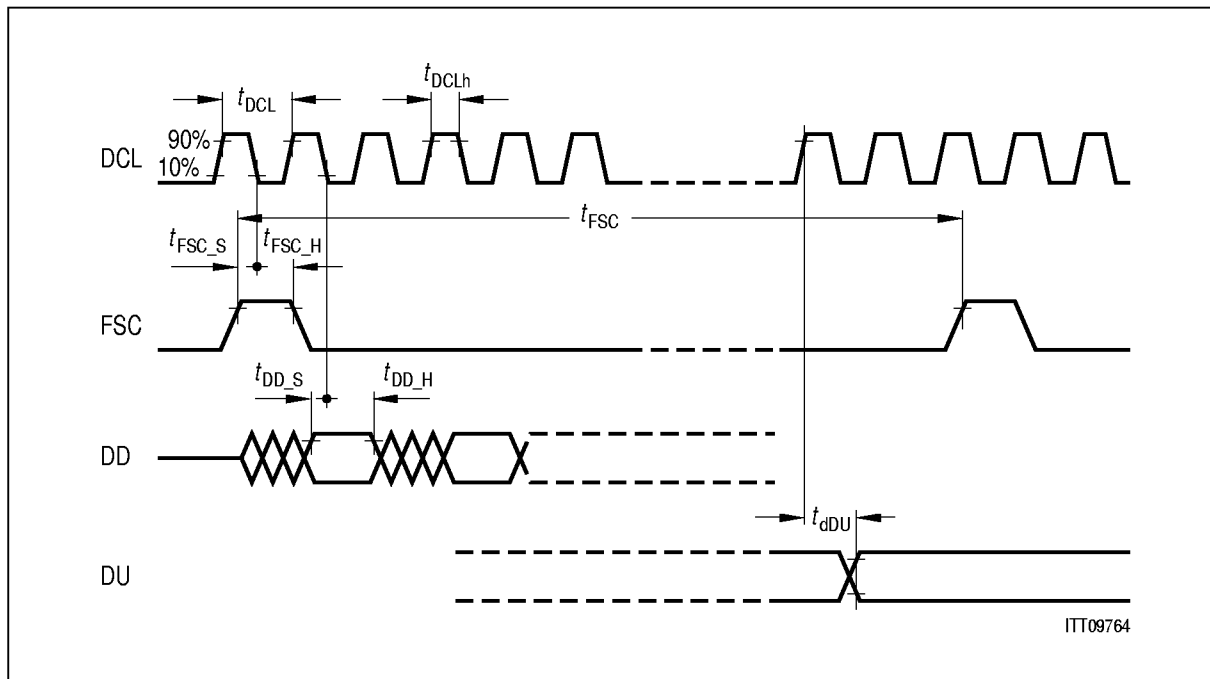


Figure 37

Table 16 Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL	$t_{DCL}$		1/4096 kHz		
DCL duty cycle	$t_{DCLh}$	40		60	%
Period FSC	$t_{FSC}$		125		$\mu$ s
FSC set-up time	$t_{FSC\_S}$	70	$t_{DCL\_h}$		ns
FSC hold time	$t_{FSC\_H}$	40			ns
DD data in set-up time	$t_{DD\_S}$	20			ns
DD data in hold time	$t_{DD\_H}$	50			ns
DU data out delay	$t_{dDU}$		150 <sup>1)</sup>		ns

<sup>1)</sup> With a pull-up resistor of 1 k $\Omega$  and a capacity of 50 pF.

Electrical Characteristics

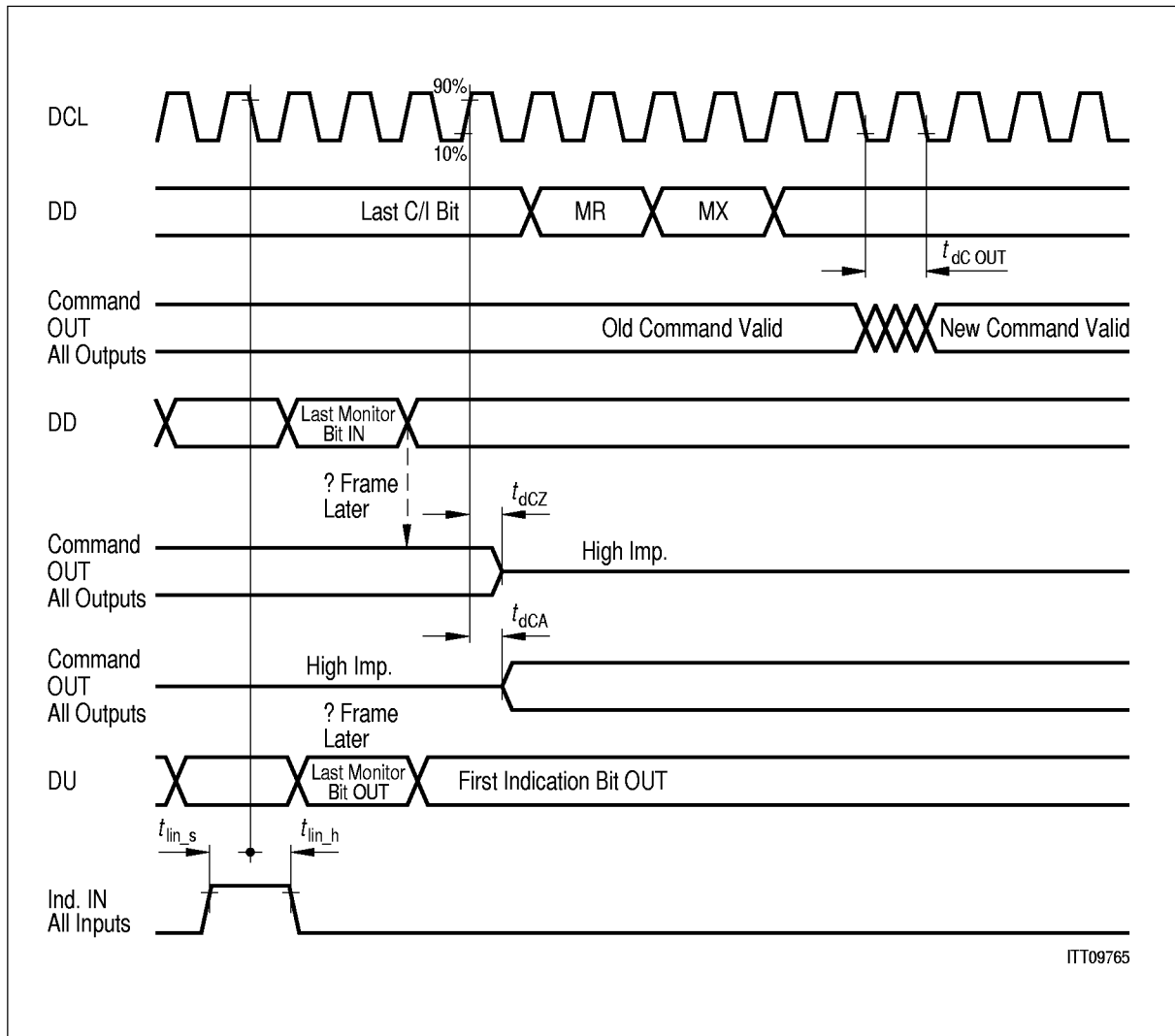


Figure 38 IOM<sup>®</sup>-2 Command/Indication Interface Timing

ITT09765

Electrical Characteristics

Table 17 Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Command out delay	$t_{dCout}$		t.b.d.		ns
Command out high impedance	$t_{dCZ}$		t.b.d.		ns
Command out active	$t_{dCA}$		t.b.d.		ns
Indication in set-up time	$t_{lin\_s}$		t.b.d.		ns
Indication in hold time	$t_{lin\_h}$		t.b.d.		ns

Command/Indication interface timing depends on time slot and for QIOs additionally on AFSC-period.

7.2.5  $\mu$ C-Interface Switching Characteristics

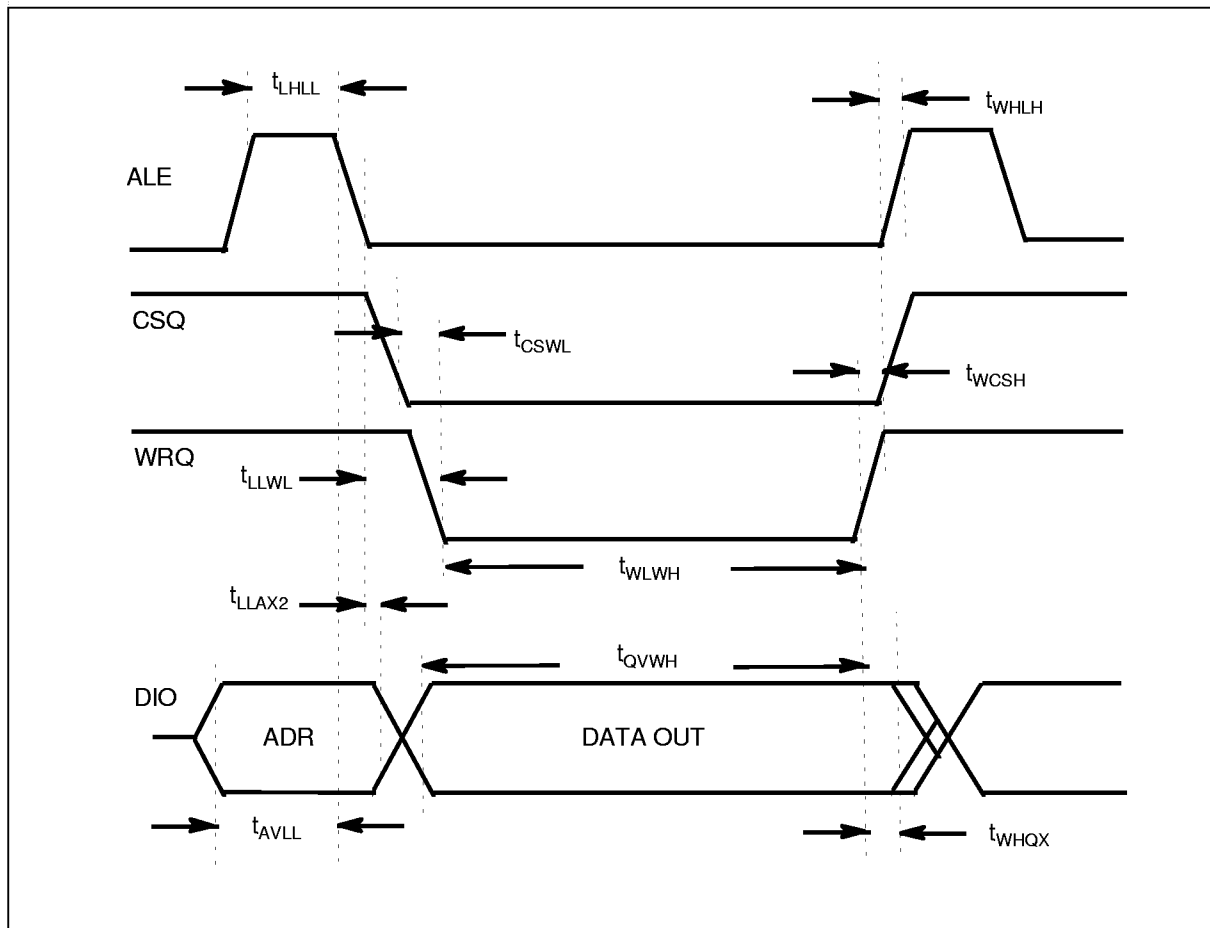


Figure 39 Timing Specifications for a Write Access to the  $\mu$ C-Interface

Electrical Characteristics

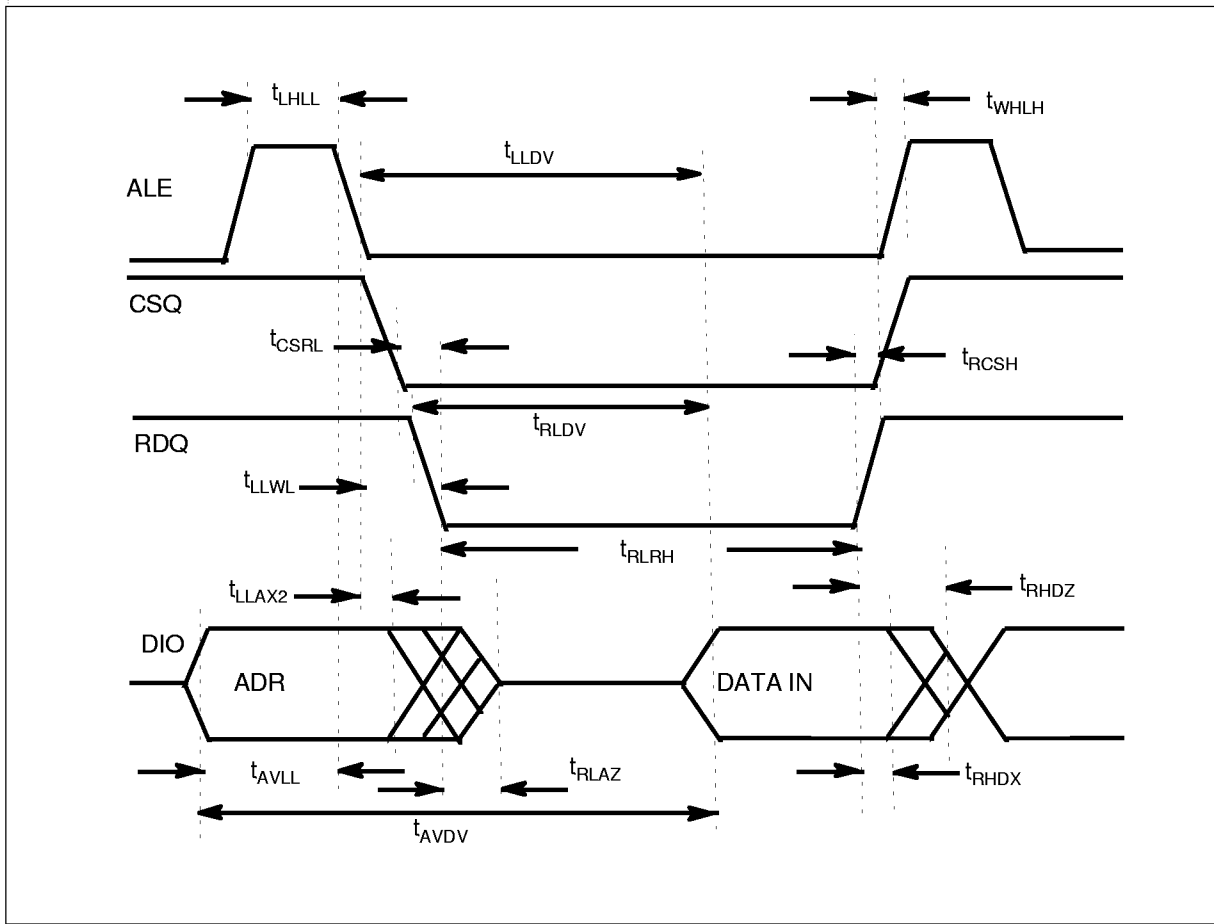


Figure 40 Timing Specifications for a Read Access to the μC-Interface

**Electrical Characteristics**
**Table 18**

Parameter	Symbol	Limit Values					Unit
		16 MHz			3.5-16 MHz		
		min.	typ.	max.	min.	max.	
RD pulse width	$t_{RLRH}$		85				ns
WR pulse width	$t_{WLWH}$		85				ns
Address hold after ALE	$t_{LLAX2}$		35				ns
RD to valid data in	$t_{RLDV}$		35				ns
Data hold after RD	$t_{RHDX}$		15				ns
Data float after RD	$t_{RHDZ}$		40				ns
ALE to valid data in	$t_{LLDV}$		35				ns
Address to valid data in	$t_{AVDV}$		50				ns
ALE to WR or RD	$t_{LLWL}$		30				ns
WR or RD high to ALE high	$t_{WHLH}$		55				ns
ALE high time	$t_{LHLL}$		40				ns
Address setup to ALE	$t_{AVLL}$		30				ns
Data setup before WR	$t_{QVWH}$		45				ns
Data hold after WR	$t_{WHQX}$		35				ns
Address float after RD	$t_{RLAZ}$		15				ns
CS low to WR low	$t_{CSWL}$		20				ns
CS low to RD low	$t_{CSRL}$		20				ns
WR high to CS high	$t_{WCSH}$		20				ns
RD high to CS high	$t_{RCSH}$		20				ns

Electrical Characteristics

7.2.6 QAP-Interface Switching Characteristics

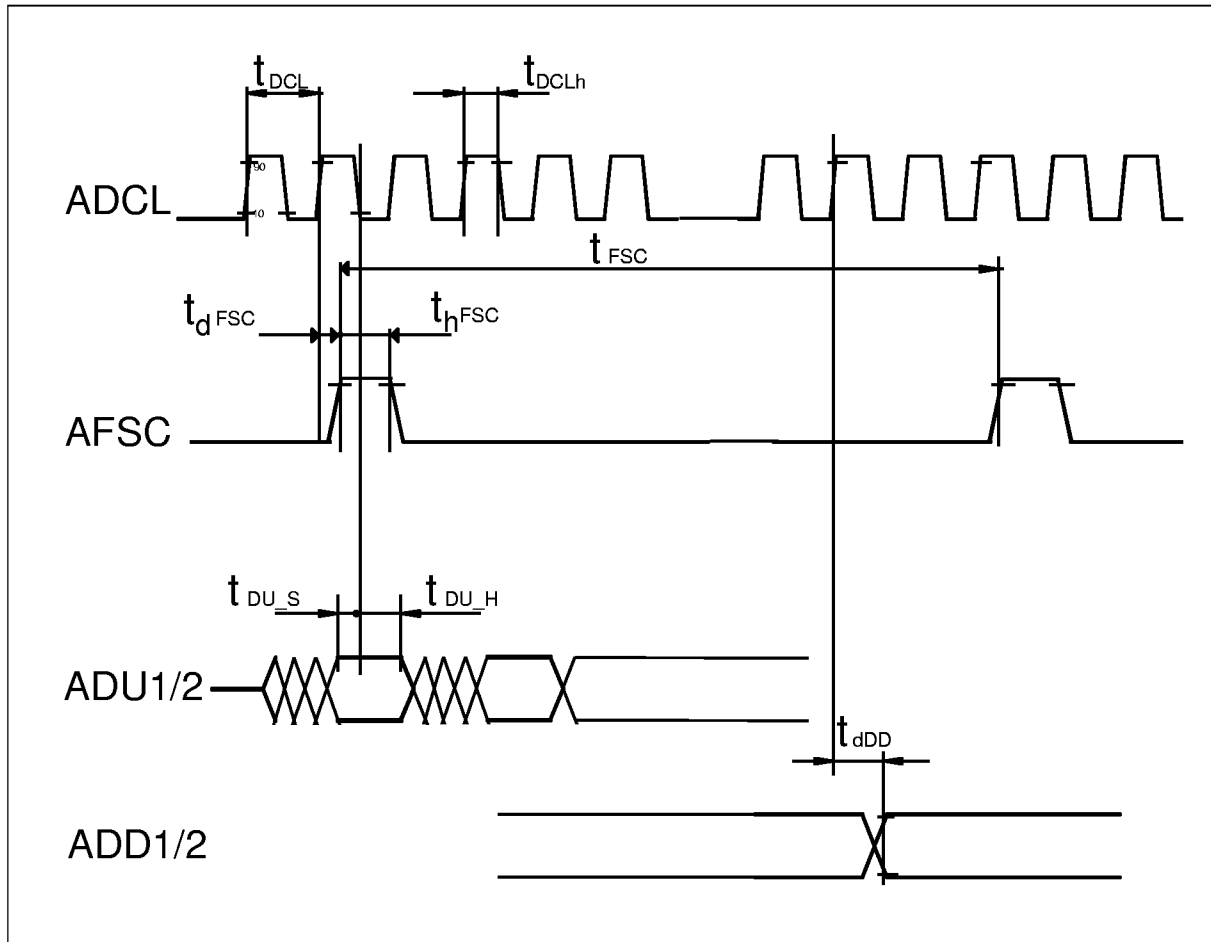


Figure 41

Table 19

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period ADCL	$t_{DCL}$		1/16.384 MHz		
ADCL duty cycle	$t_{DCLh}$	40	50	60	%
Period AFSC	$t_{FSC}$		500		$\mu s$
AFSC delay	$t_{dFSC}$		5	20	ns
AFSC high	$t_{hFSC}$		$t_{DCL}$		ns
ADU1/2 setup time	$t_{DU S}$	20			ns
ADU1/2 hold time	$t_{DU H}$	20			ns
ADD1/2 delay	$t_{dDD}$			20	ns

**Electrical Characteristics**

**7.2.7 I/O-Switching Characteristics (IO1 to IO4, ID0 to ID3)**

t.b.d concerned to IOM-2 and  $\mu\text{C}$

**7.3 PEB 4165 (AHV-SLIC)**

**7.3.1 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Condition
		min.	max.		
Battery voltage	$V_{\text{BAT}}$	- 90	0.5	V	referred to BGND
Auxiliary supply voltage	$V_{\text{H}}$	- 0.5	90	V	referred to BGND
Total battery supply voltage, continuously	$V_{\text{H}}-V_{\text{BAT}}$		160	V	
Total battery supply voltage, pulse < 1 ms	$V_{\text{H}}-V_{\text{BAT}}$		170	V	
VDD supply voltage	$V_{\text{DD}}$	- 0.4	5.5	V	referred to AGND
VSS supply voltage	$V_{\text{SS}}$	- 5.5	0.4	V	referred to AGND
Ground voltage difference	VBGND -VAGND	- 0.5	0.5	V	
Junction temperature	$T_{\text{j}}$		150	°C	
Input voltages	VDCP/N VACP/N VC1, VC2	$V_{\text{SS}} - 0.3$ - 0.3	$V_{\text{DD}} + 0.3$ $V_{\text{DD}} + 0.3$	V	
Voltages on current outputs	VIT, VIL	- 3.5	$V_{\text{DD}} + 0.3$	V	
RING, TIP voltages, continuously	$V_{\text{R}}, V_{\text{T}}$	$V_{\text{BAT}} - 0.3$	$V_{\text{H}} + 0.3$	V	
RING, TIP voltages, pulse < 1 ms	$V_{\text{R}}, V_{\text{T}}$	$V_{\text{BAT}} - 10$	$V_{\text{H}} + 10$	V	
RING, TIP voltages, pulse < 1 $\mu\text{s}$	$V_{\text{R}}, V_{\text{T}}$	$V_{\text{BAT}} - 20$	$V_{\text{H}} + 20$	V	
ESD-voltage, all pins			1	kV	Human body model



**Electrical Characteristics**
**7.3.2 Operating Range**

Parameter	Symbol	Limit Value		Unit	Condition
		min.	max.		
Battery voltage	$V_{BAT}$	- 80	- 24	V	referred to BGND
Auxiliary supply voltage	$V_H$	5	85	V	referred to BGND
Total battery supply voltage	$V_H - V_{BAT}$		150	V	
VDD supply voltage	$V_{DD}$	4.75	5.25	V	referred to AGND
VSS supply voltage	$V_{SS}$	- 5.25	- 4.75	V	referred to AGND
Ground voltage difference		- 0.3	0.3	V	
Ambient temperature	$T_A$	0 - 40	70 85	°C °C	PEB 4165 PEF 4165
Voltage compliance IT, IL	$V_{IT}, V_{IL}$	- 3	3	V	
Input range VDCP, VDCN	VDC	- 3.2	+ 3.2	V	

**Thermal Resistances**

Junction to case	$R_{th, jC}$	5	K/W	
Junction to ambient	$R_{th, jA}$	20	K/W	with heatsink, typ.

**Electrical Characteristics**

**7.3.3 Electrical Parameters**

Min / max values are valid within the full operating range. If PEB- and PEF-specifications are different, both values can be found in the respective column.

Testing is performed according to the test figures with external circuitry as depicted in fig. t.b.d. Unless otherwise stated, load impedance  $R_L = 600 \Omega$ ,  $V_{BAT} = -70 V$  and  $V_H = +60 V$ ,  $V_{DD} = +5 V$ ,  $V_{SS} = -5 V$ . Test temperatures are 25 °C and 70 °C for PEB, -40 °C, 25 °C and 85 °C for PEF-type (without heatsink).

**Supply Currents and Power Dissipation ( $I_R = I_{TIP} = 0 A$ ;  $V_{RT} = 0 V$ ) <sup>1)</sup>**

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	

**Power Down Mode**

1.	$V_{DD}$ current	$I_{DD}$	PDNH, PDNR		50		$\mu A$
2.	$V_{SS}$ current	$I_{SS}$	PDNH PDNR		50 150		$\mu A$ $\mu A$
3.	$V_{BAT}$ current	$I_{BAT}$	PDNH PDNR		10 50		$\mu A$ $\mu A$
4.	$V_H$ current	$I_H$	PDNH HIRT, $V_H = +80 V$		1 1	10 10	$\mu A$ $\mu A$

**Active Mode**

5.	$V_{DD}$ current	$I_{DD}$	ACT		3.3		mA
6.	$V_{SS}$ current	$I_{SS}$	ACT		0.7		mA
7.	$V_{BAT}$ current	$I_{BAT}$	ACT		5.5		mA
8.	$V_H$ current	$I_H$	ACT		1		$\mu A$
9.	Quiescent power dissipation	PQ	ACT		400		mW

**Electrical Characteristics**

**Supply Currents and Power Dissipation ( $I_R = I_{TIP} = 0 \text{ A}$ ;  $V_{RT} = 0 \text{ V}$ ) <sup>1)</sup> (cont'd)**

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	

**Boosted Battery Mode**

10.	$V_{DD}$ current	$I_{DD}$	BB		1.5		mA
11.	$V_{SS}$ current	$I_{SS}$	BB		0.8		mA
12.	$V_{BAT}$ current	$I_{BAT}$	BB		5		mA
13.	$V_H$ current	$I_H$	BB		4		mA
14.	Quiescent power dissipation	PQ	BB		600		mW

<sup>1)</sup> The total power dissipation consists of the quiescent power dissipation PQ given above, a  $V_{RT}$  dependent component PV and a component PI depending on the line current  $I_{RT}$ :

$$P_{tot} = PQ + PV + PI \text{ with}$$

	PV	PI
<b>Active</b>	0	$1.08 \times I_{RT} \times (-V_{BAT}) - I_{RT} \times V_{RT}$
<b>Boosted</b>	$(V_{RT} / 100 \text{ k}) \times (V_H - V_{BAT})$	$1.05 \times I_{RT} \times (V_H - V_{BAT}) - I_{RT} \times V_{RT}$

**Electrical Characteristics**

**7.4 DC-Characteristics**

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		

**Line Termination TIP, RING**

15.	DC line voltage	VTR, DC	ACT, BB		0		V	VDCP = - VDCN = 0 V
16.		VT, DC	ACT		- 35		V	
			BB		- 5		V	
17.		VTR, DC	ACT		50		V	VDCP = - VDCN = 1 V
18.					- 50		V	VDCP = - VDCN = - 1 V
19.	Max. DC line voltage		ACT		67		V	VDCP = - VDCN = 1.5 V $I_{RT} = 20 \text{ mA}$
20.	Output current limit	$ I_{R, \text{max}} $ $ I_{T, \text{max}} $	all	90		130	mA	VR, VT
21.	Loop open resistance TIP to BGND	$R_{TG}$	PDNR	6.8	8	9.2	k $\Omega$	$I_{TIP} = 2 \text{ mA}$ , Temp = 25 °C <sup>1)</sup>
22.	Loop open resistance RING to V <sub>BAT</sub>	$R_{RB}$	PDNR	6.8	8	9.2	k $\Omega$	$I_R = 2 \text{ mA}$ , Temp = 25 °C <sup>1)</sup>
23.	Power denial output leakage current	I <sub>Leak, R</sub>	PDNH	- 30		30	$\mu\text{A}$	$V_{BAT} < V_R < V_H$
24.		I <sub>Leak, T</sub>		- 30		30	$\mu\text{A}$	$V_{BAT} < V_T < V_H$
25.	High impedance output leakage current	I <sub>Leak, R</sub>	HIR(T)	- 30		30	$\mu\text{A}$	$V_{BAT} < V_R < V_H - 3$
26.		I <sub>Leak, T</sub>	HI(R)T	- 30		30	$\mu\text{A}$	$V_{BAT} < V_T < V_H - 3$

**Inputs DCP, DCN, ACP, ACN**

27.	Input resistance DCP, DCN	RDC	all	100			k $\Omega$	
28.	Input resistance ACP, ACN	RAC	all	13	16		k $\Omega$	

**Electrical Characteristics**

**7.4 DC-Characteristics (cont'd)**

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		

**Current Outputs I<sub>T</sub>, I<sub>L</sub>**

29.	IT output current	$I_T$	ACT			15	$\mu A$	$I_R = I_T = 0 \text{ mA}$
30.				380		420	$\mu A$	$I_R = I_T = 20 \text{ mA}$
31.				- 380		- 420	$\mu A$	$I_R = I_T = - 20 \text{ mA}$
32.				0.95		1.05	mA	$I_R = I_T = 50 \text{ mA}$
33.				- 0.95		- 1.05	mA	$I_R = I_T = - 50 \text{ mA}$
34.	Offhook output current on $I_T$		PDNR		850		$\mu A$	TIP/RING shorted
35.	$I_L$ output current	$I_L$	ACT			30	$\mu A$	$I_R = I_T = 20 \text{ mA}$
36.				75		125	$\mu A$	$I_R = 15 \text{ mA}, I_T = 25 \text{ mA}$
37.				- 190		- 310	$\mu A$	$I_R = 62.5 \text{ mA}$ $I_T = 37.5 \text{ mA}$

**Control Inputs C1, C2**

38.	H-input voltage	$V_{IH}$	all		4.03		V	$V_{DD} = 5 \text{ V}$
39.	M-input voltage	$V_{IM}$	all		2.57		V	$V_{DD} = 5 \text{ V}$
40.	L-input voltage	$V_{IL}$	all		1.125		V	$V_{DD} = 5 \text{ V}$
41.	Input leakage current	I <sub>Leak</sub>	all	- 5		5	$\mu A$	$0 < VC1(2) < + 5 \text{ V}$
42.	Thermal overload current C1	I <sub>therm</sub>	all	120	150		$\mu A$	$VC1 = 1.25 \text{ V}$
43.	Switching temperature (guaranteed by design)	$T_{joff}$	all		165		$^{\circ}C$	
		$T_{jon}$	all		145		$^{\circ}C$	

<sup>1)</sup> The systematic temperature dependence of these resistances is + 0.1% /  $^{\circ}C$

**Electrical Characteristics**

**7.5 AC-Characteristics**

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min. PEB/PEF	typ.	max.		

**Line Termination TIP, RING**

44.	Receive gain	Gr	ACT, BB	9.78	9.90	10.02	dB	VACP = - VACN = 320 mVrms f = 1015 Hz I <sub>RT</sub> = 25 mA
45.	Gain flatness (guaranteed by design)	dGr	ACT, BB	- 0.05		0.05	dB	300 Hz < f < 3400 Hz
46.	Gain tracking (guaranteed by design)	dGr	ACT	- 0.2		0.2	dB	3 dBm <sub>0</sub> > V <sub>RT</sub> > - 20 dBm <sub>0</sub>
47.	Total harmonic distortion V <sub>RT</sub>	THD	ACT			0.3	%	VACP = - VACN = 320 mVrms f = 1015 Hz, I <sub>RT</sub> = 25 mA
48.	Teletax distortion	THD <sub>TTX</sub>	ACT			3	%	f = 16 kHz, R <sub>L</sub> = 200 Ω I <sub>RT</sub> = 25 mA V <sub>RT</sub> , AC = 5 Vrms
49.						5	%	I <sub>RT</sub> = 0 mA, V <sub>RT</sub> = 55 V V <sub>RT</sub> , AC = 2 Vrms
50.	Psophometric noise	Np,VRT	ACT			- 75	dBmp	I <sub>RT</sub> = 25 mA
51.	Longitudinal to transversal rejection ratio V <sub>long</sub> /V <sub>RT</sub>	LTRR	ACT	61 / 58			dB	V <sub>long</sub> = 3 Vrms 300 Hz < f < 3.4 kHz I <sub>RT</sub> = 25 mA
52.	Transversal to longitudinal rejection ratio V <sub>RT</sub> /V <sub>long</sub>	TLRR	ACT	50			dB	VACP = - VACN = 960 mVrms 300 Hz < f < 3.4 kHz I <sub>RT</sub> = 25 mA
53.	Power supply rejection ratio V <sub>BAT</sub> /V <sub>RT</sub>	PSRR	ACT, BB	33	40		dB	300 Hz < f < 3.4 kHz V <sub>Supply</sub> , AC = 100 mVp I <sub>IRT</sub> = 25 mA
54.	V <sub>H</sub> /V <sub>RT</sub>		BB	33	40		dB	
55.	V <sub>DD</sub> /V <sub>RT</sub>		ACT, BB	33	50		dB	
56.	V <sub>SS</sub> /V <sub>RT</sub>		ACT	33	50		dB	

**Electrical Characteristics**

**7.5 AC-Characteristics (cont'd)**

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min. PEB/PEF	typ.	max.		
57.	Ringing distortion	THD	BB			4	%	$R_L = 1\text{ K}$ , $C_L = 1\ \mu\text{F}$ $f = 66\text{ Hz}$ , $V_{DCP} = -V_{DCN}$ $= 0.4\text{ V (DC)}$ $+ 1.3\text{ V}_{rms}$ (sine wave)
58.	Transversal current ratio	Git	ACT, BB	33.89	33.98	34.07	dB	$V_{ACP} = -V_{ACN}$ $= 320\text{ mV}_{rms}$ $f = 1015\text{ Hz}$ $I_{RT} = 25\text{ mA}$ $I_{RT} = -25\text{ mA}$
59.			ACT, BB	33.89	33.98	34.07	dB	
60.	Gain flatness (guaranteed by design)	dGit	ACT, BB	- 0.05		0.05	dB	$300\text{ Hz} < f < 3400\text{ Hz}$
61.	Gain tracking (guaranteed by design)	dGit	ACT, BB	- 0.2		0.2	dB	$3\text{ dBm}_0 > V_{RT}$ $> -20\text{ dBm}_0$
62.	Total harmonic distortion VIT	THD,IT	ACT		0.01	0.3	%	$V_{ACP} = -V_{ACN}$ $= 320\text{ mV}_{rms}$ $f = 1015\text{ Hz}$ $I_{RT} = 25\text{ mA}$ $I_{RT} = 0\text{ mA}$
63.								
64.	Psophometric noise	$N_p, VIT$	ACT			- 102	dBmp	$I_{RT} = 25\text{ mA}$
65.	Longitudinal to transversal current output rejection ratio $V_{long}/VIT$	LITRR	ACT	t.b.d.			dB	$V_{long} = 3\text{ V}_{rms}$ $300\text{ Hz} < f < 3.4\text{ kHz}$ $I_{RT} = 25\text{ mA}$
66.				t.b.d.			dB	
67.	Power supply rejection ratio	PSRR	ACT	50	60		dB	$300\text{ Hz} < f < 3.4\text{ kHz}$ $V_{supply}$ , $AC = 100\text{ mV}_p$ $I_{RT} = 25\text{ mA}$
68.			BB	50	60		dB	
69.			ACT	50	60		dB	
70.			ACT	50	60		dB	

**Test Features**

**8 Test Features**

**Table 20 Card Tests: (900 Ω Testloop, Option: with relay)**

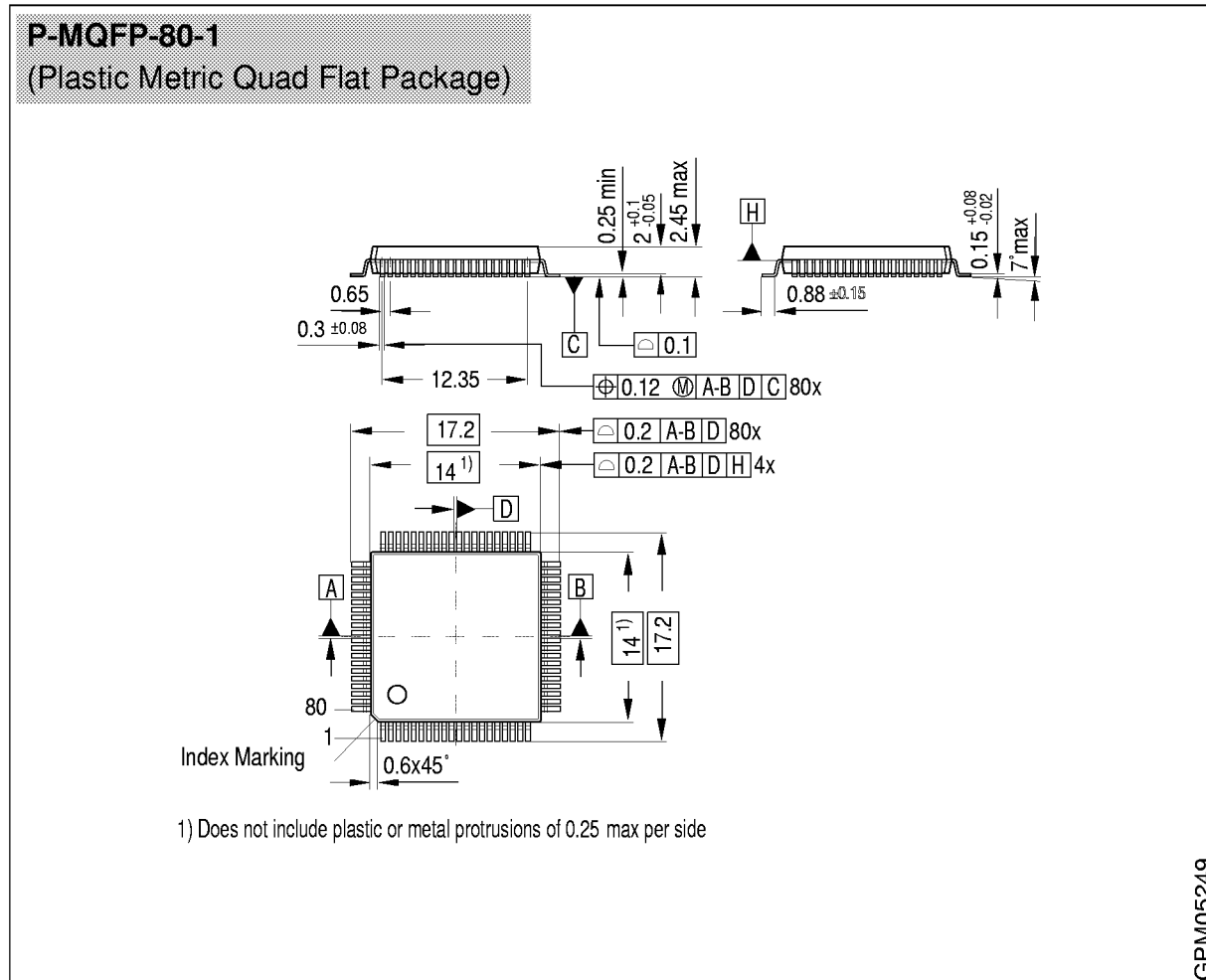
No.	Test	Result	Loops	Settings	Switches	Description
1.	Level metering AC	PCM MVA, RLM0/1	AC Loop	ITIME LMBP LMNOTCH LM2PCM LMSEL0/1 ELM	ENTE on ELM on	After programming the settings and release with the ENTE the levelmetering will be started by ELM = 1. The end of measurement is shown by MVA, RLM0/1 and the result can be sent to the CIDU-voice channel. ITIME determines the Integration time either 16 ms or 256 ms.
2.	Level metering DC	PCM MVA, RLM0/1	DC Loop	LP03, LP5, DISPOFI, PCM2DC DCAD16 ERAMP ERECT LM2PCM LMSEL0/1 ELM $f_{RING}$	ENTE on ELM on	After programming the settings and release with the ENTE the levelmetering will be started by ELM = 1. The measurement time is programmable using the ring generator. The end of measurement is shown by MVA, RLM0/1 and the result can be sent to the DU-voice channel. Includes measurement of Offset, and Ringer Capacitance.
3.	Level metering TTX	PCM MVA, RLM0/1	DC Loop	ELM TTXL LMSEL0/1 LM2PCM PCM2DC	ENTE on ELM on	After programming the settings and release with the ENTE the levelmetering will be started by ELM = 1. The measurement time is programmable by ITIME either 16 ms or 256 ms. The end of measurement is shown by MVA, RLM0/1 and the result can be sent to the DU-voice channel. By setting TTXL and correct programming of the IM-Filters the TTX current is measured directly.



**Package Outlines**

**9 Package Outlines**

**9.1 PEB 3465 (QAP)**



**Sorts of Packing**

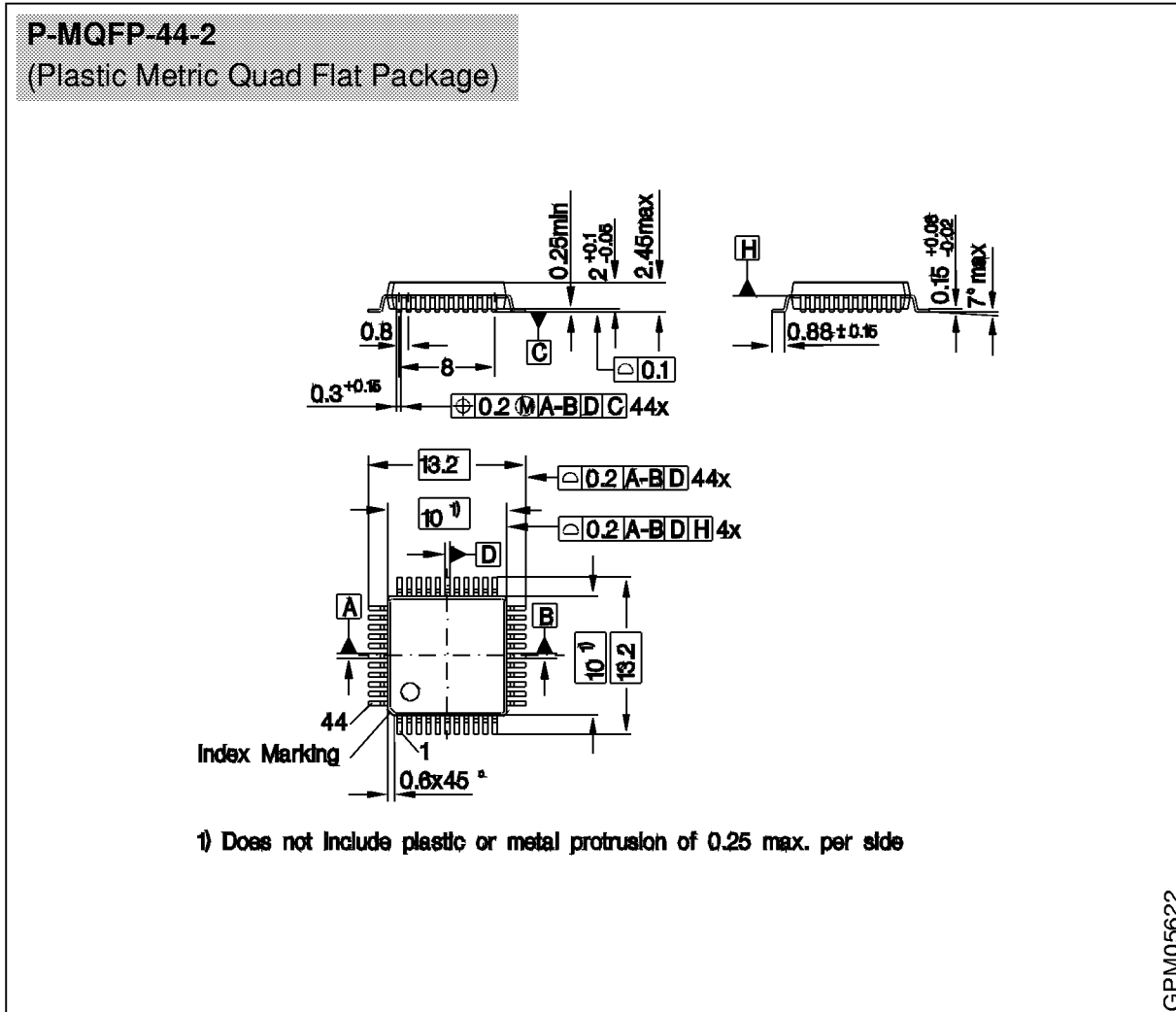
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

**SMD = Surface Mounted Device**

Dimensions in mm

Package Outlines

9.2 PEB 31665 (MuPP)



**Sorts of Packing**

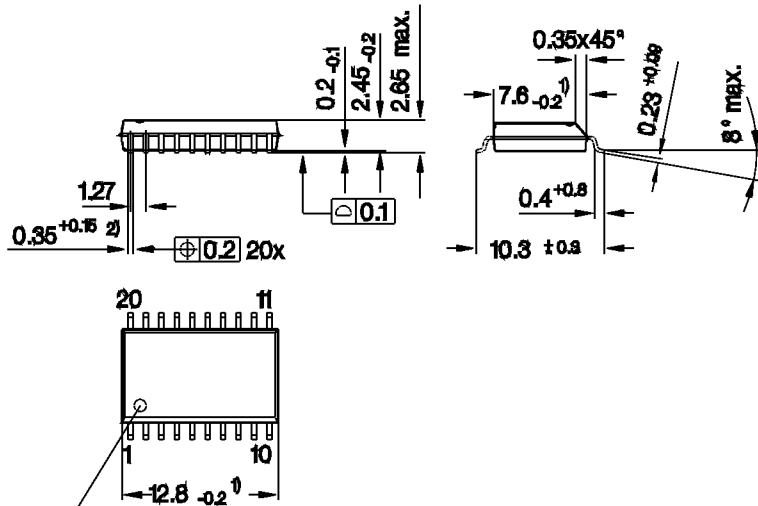
Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

9.3 PEB 4165 (AHV-SLIC)

**P-DSO-20-5**  
(Plastic Dual Small Outline)



Index Marking

- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion

GPS05094

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm

10 Appendix

10.1 IOM<sup>®</sup>-2 Interface Monitor Transfer Protocol

Monitor Channel Operation

The monitor channel is used for the transfer of maintenance information between two functional blocks. Using two monitor control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure. The MR and MX bits in the fourth octet (C/I channel) of the IOM-2 frame are used for the handshake procedure of the monitor channel

The monitor channel transmission operates on a pseudo-asynchronous basis:

- Data transfer (bits) on the bus is synchronized to Frame Sync FSC
- Data flow (bytes) are asynchronously controlled by the handshake procedure.

For example: Data is placed onto the DD-Monitor-Channel by the Monitor-transmitter of the master device (DD-MX-Bit is activated i.e. set to '0'). This data transfer will be repeated within each frame (125 μs rate) until it is acknowledged by the MuPP Monitor-receiver by setting the DU-MR-bit to '0', which is checked by the Monitor-transmitter of the master device. Thus, the data rate is not 8-kbytes/s.

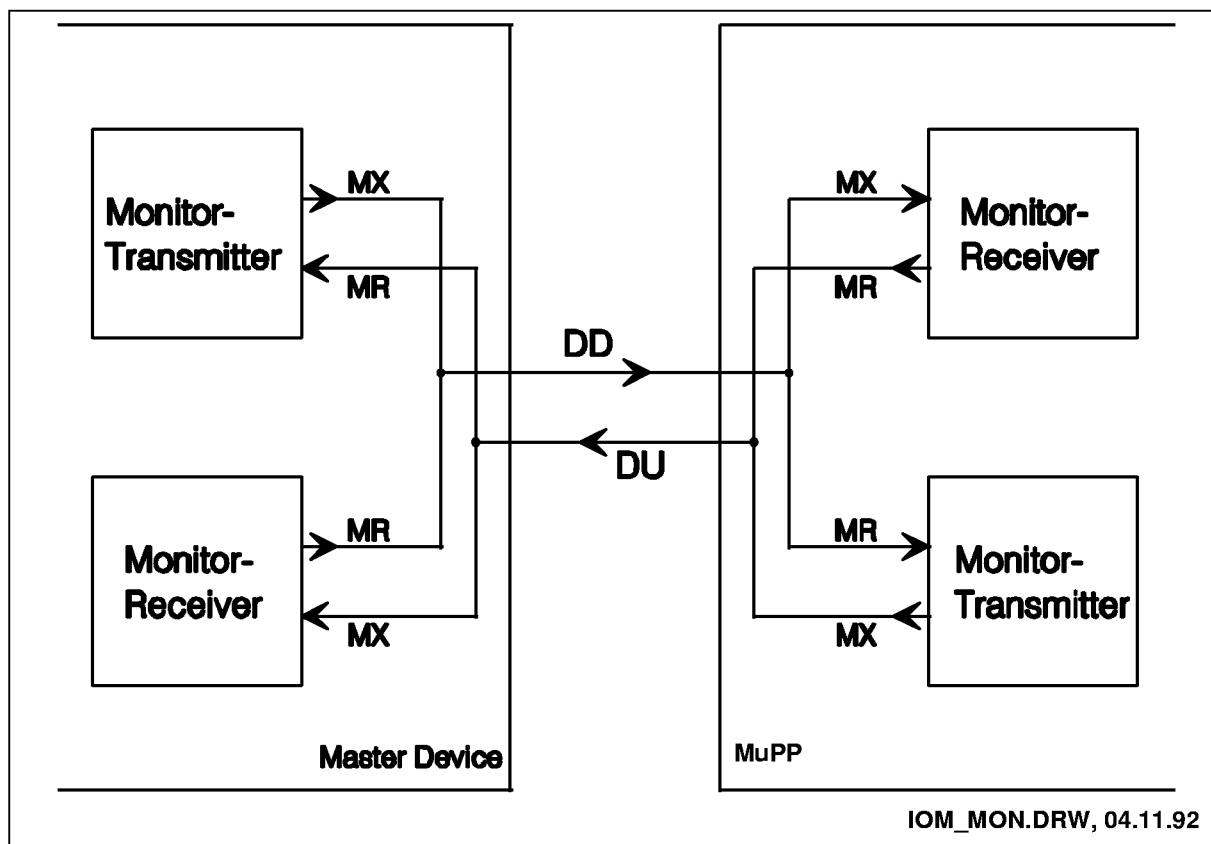


Figure 42

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**Appendix**

## Monitor handshake procedure

The monitor channel works in 3 states

- idle state: A pair of inactive (set to '1') MR- and MX-bits during two or more consecutive frames: End of Message (EOM)
- sending state: MX-bit is activated (set to '0') by the Monitor-transmitter, together with data-bytes (can be changed) on the Monitor-channel
- acknowledging: MR-bit is set to active (set to '0') by the Monitor-receiver, together with a data-byte remaining in the Monitor-channel.

A start of transmission is initiated by a Monitor-transmitter in sending out an active MX-bit together with the first byte of data (the address of the receiver) to be transmitted in the Monitor-channel.

This state remains until the addressed Monitor-Receiver acknowledges the received data by sending out an active MR-bit, which means that the data-transmission is repeated each 125  $\mu$ s frame (minimum is one repetition). During this time the Monitor-transmitter evaluates the MR-bit.

Flow control, means in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.

Since the receiver is able to receive the monitor data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function).

A collision resolution mechanism (check if another device is trying to send data during the same time) is implemented in the transmitter. This is done by looking for the inactive ('1') phase of the MX-bit and making a per bit collision check on the transmitted monitor data (check if transmitted '1's are on DU/DD-line; DU/DD-line are open-drain lines).

Any abort leads to a reset of the MuPP command stack, the device is ready to receive new commands.

To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgment.

Due to the inherent programming structure, duplex operation is not possible. It is not **allowed** to send any data to the MuPP, while transmission is active.

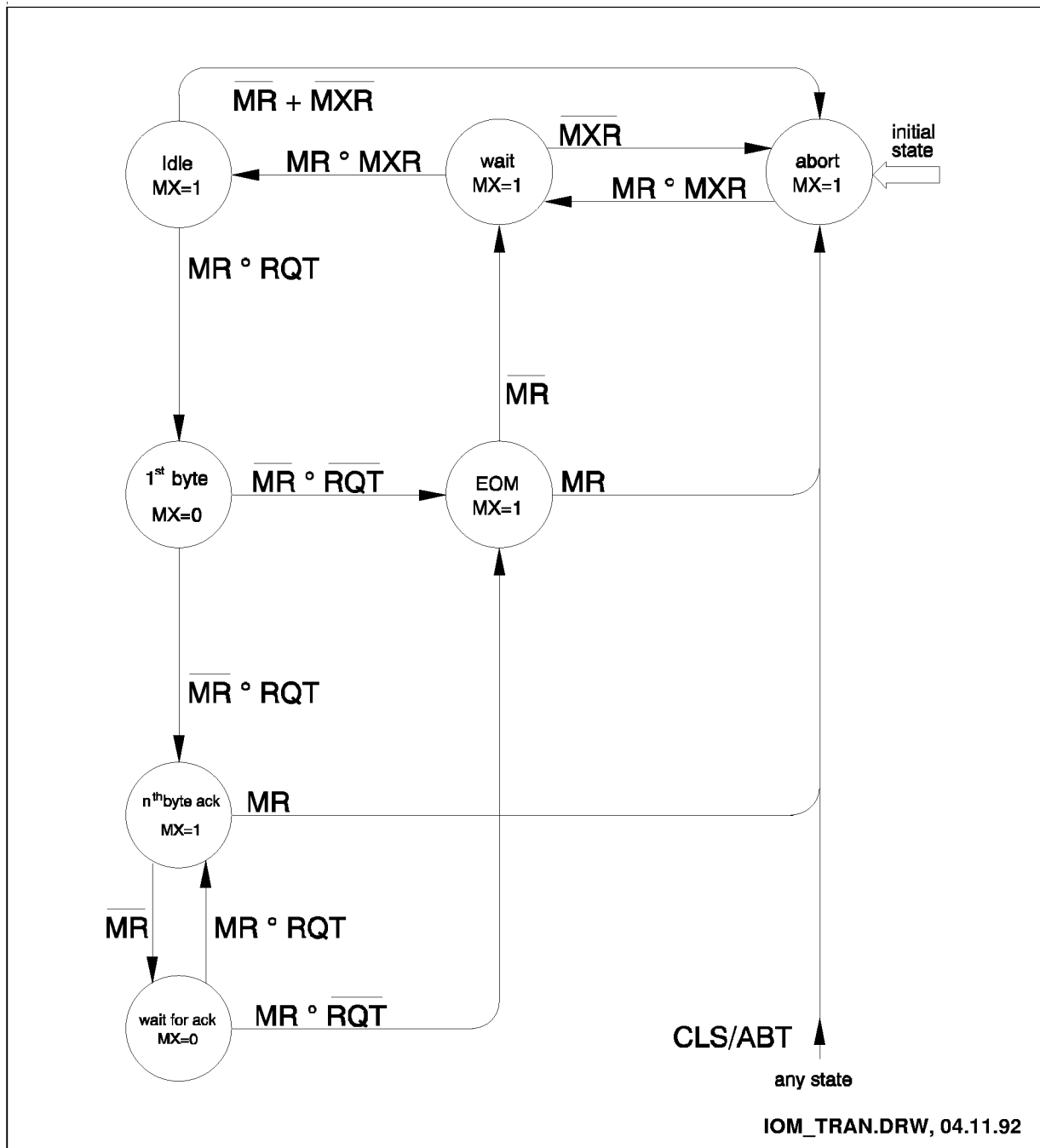


Figure 43 State Diagram of the MuPP Monitor Transmitter

- MR ... MR - bit      Received on DD - line
- MX ... MX - bit      Calculated and expected on DU - line
- MXR ... MX - bit      Sampled on DU - line
- CLS ...              Collision within the monitor data byte on DU - line
- RQT ...              Request for transmission from internal source
- ABT ...              Abort request/indication

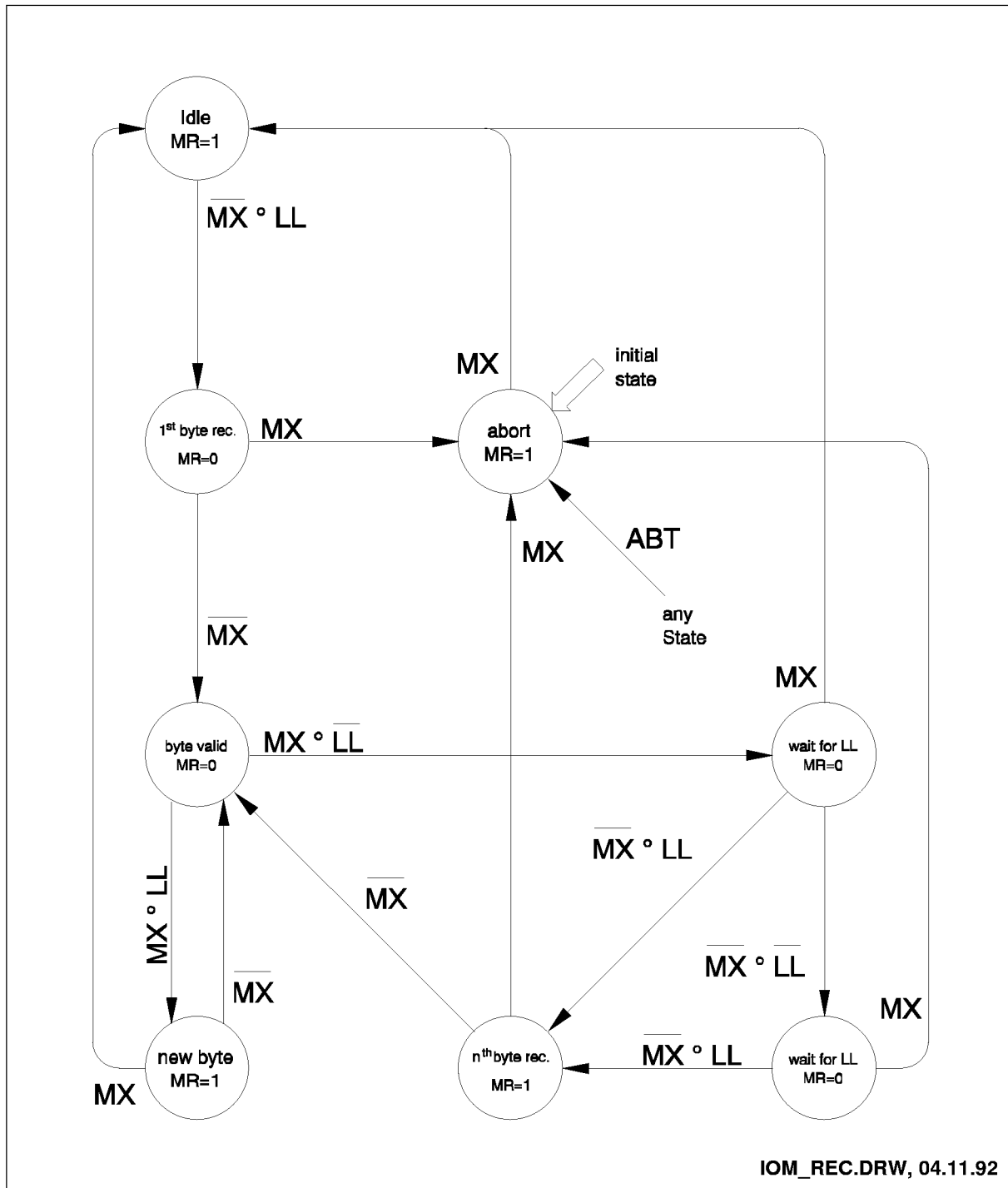


Figure 44 State Diagram of the MuPP Monitor Receiver

- MR ... MR - bit      Calculated and transmitted on DU - line
- MX ... MX - bit      Received data downstream (DD - line)
- LL ...                Last lock of monitor byte received on DD - line
- ABT ...                Abort indication to internal source

**Monitor Channel Data Structure**

The monitor channel is used for the transfer of maintenance information between two functional blocks. By use of two monitor control bits (MR and MX) per direction, the data are transferred in a complete handshake procedure.

**Address Byte**

Messages to and from the MuPP are started with the following byte:

Bit	7	6	5	4	3	2	1	0
	1	0	0	0	0	0	0	1

Thus providing information for up to 16 analog lines, the MuPP is one device for up to 16 IOM-2 time slots. Monitor data for the analog channels is selected by the MuPP specific commands (SOP, XOP, TOP or COP) following.

**10.2 Channel Identification Command (CIC)**

In order to unambiguously identify different devices by software, a two Byte identification command is defined for analog lines IOM-2 devices. A device requesting the identification of the MuPP will send the following 2 byte code:

1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Each device will then respond with its specific identification code. For the MuPP this two byte identification code is:

1	0	0	0	<b>CONF</b>			
1	0	0	0	0	0	0	1

**CONF** an optional 4-bit code indicating the specific hardware environment. A typical application of the CONF code is the differentiation of various types of line circuits that use the same MuSLIC hardware within the same system.

For the realization of the Channel Identification Commands on the line card, it needs 4 pins of the MuPP (ID0,...ID3). One pin (ID0) is switchable as a digital serial interface of a shift register, to transfer special line card design informations up to 2 × 15 bytes into the monitor channel of the IOM-2 interface.



**Appendix**

There are two different solutions of the CIC for the MuPP to identify the version of the line card.

**Solution 1: ('Normal' Channel Identification Command)**

The input of the 4 pin interface (ID0 ... ID3) is transferred to the 4 bit CONF information using the following truth-table (binary coded):

**Table 21**

MuPP Ports				CONF-inf.
ID3	ID2	ID1	ID0	(4 bits)
0 V	0 V	0 V	0 V	0 0 0 0
0 V	0 V	0 V	3 V	0 0 0 1
0 V	0 V	3 V	0 V	0 0 1 0
0 V	0 V	3 V	3 V	0 0 1 1
0 V	3 V	0 V	0 V	0 1 0 0
0 V	3 V	0 V	3 V	0 1 0 1
0 V	3 V	3 V	0 V	0 1 1 0
0 V	3 V	3 V	3 V	0 1 1 1
3 V	0 V	0 V	0 V	1 0 0 0
3 V	0 V	0 V	3 V	1 0 0 1
3 V	0 V	3 V	0 V	1 0 1 0
3 V	0 V	3 V	3 V	1 0 1 1
3 V	3 V	0 V	0 V	1 1 0 0
3 V	3 V	0 V	3 V	1 1 0 1
3 V	3 V	3 V	0 V	1 1 1 0
3 V	3 V	3 V	3 V	1 1 1 1

This is a 14 possible individual line card design information or an address pointer for the system to get more basic information.

The information is read through the IOM-2 monitor channel with the CIC command.

**Solution 2 (Extended Channel Identification Command):**

The second realization step is that the combination of ports (ID1, ID2, ID3 = + 3 V) changes the input port ID0 to a shift register input.

**Table 22**

MuPP Ports				CONF-inf.
ID3	ID2	ID1	ID0	(4 bits)
+ 3 V	+ 3 V	+ 3 V	x	1 1 1 x

An external shift register on the line card transmits up to  $2 \times 15$  bytes of special HW + FW line card design information.

The information is read through the IOM-2 monitor channel with the XOP Command for XR7 or XR8. The CONF code is '111x' by this extended identification.

The first schematic gives an overview of the different timings for the extended channel identification.

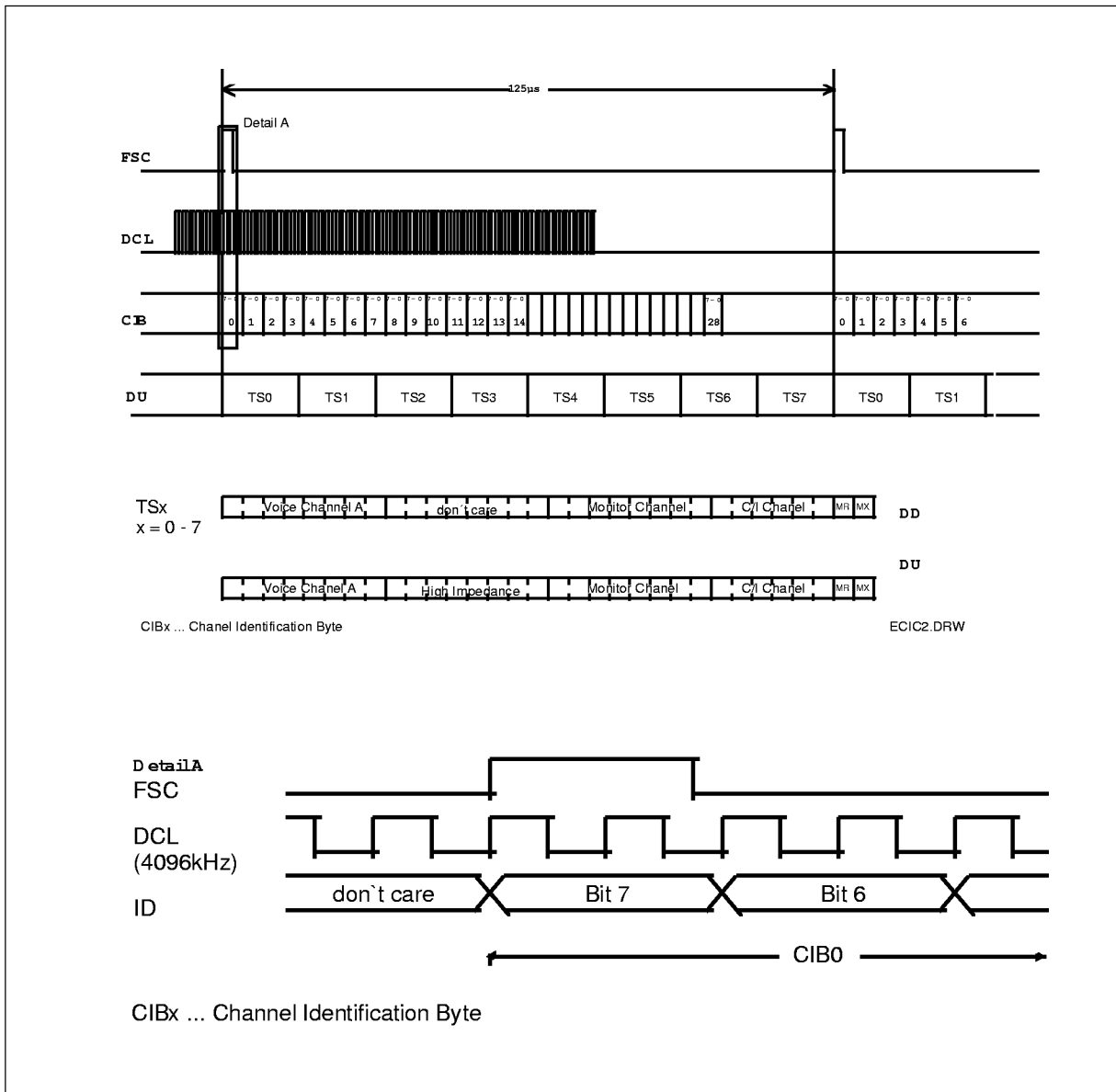
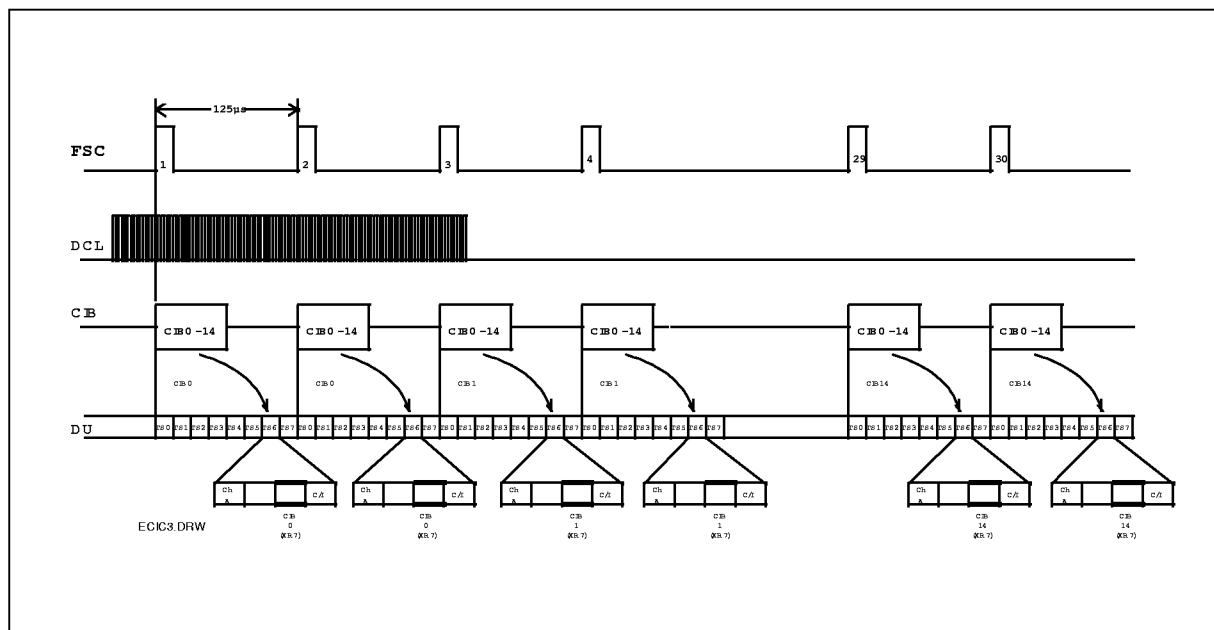


Figure 45 General Timing

Appendix

**Expected Output of the ASIC Which Sends the Channel Identification:**

The MuPP sends the Extended Channel Identification in the Monitor Channel of that time slot in which the XOP Command was sent. If – for example – the MuPP uses the time slot 6, the Monitor Channel of TS6 looks like the following (for all other time slots equivalent).



**Figure 46**

Expected Input Timing and IOM-2 Interface Timing and Switching characteristic: To be defined

**10.3 List of Abbreviations**

ACT	Active Mode
ADC	Analog Digital Converter
AGDCR	Attenuation DC Receive
AGDCX	Attenuation DC Transmit
AGR	Attenuation Receive
AGX	Attenuation Transmit
AGTTX	Attenuation Teletax
AR	Attenuation Receive
ASIC	Application Specific Integrated Circuit
AX	Attenuation Transmit
BB	Boosted Battery
BiCMOS	Bipolar Complementary Metal Oxid Semiconductor
BP	Band Pass
C/I-DD	Channel Identification-Data Downstream
C/I-DU	Channel Identification-Data Upstream
C1, 2	Digital Interface between QAP and AHV-SLIC
CHOP	Chopper (see SCR8_6)
CMP	Compander
CODEC	Coder Decoder
COMP	Comparator (Testloops, Levelmetering)
COP	Coefficient Operation
CRAM	Coefficient RAM
DAC	Digital Analog Converter
DAC-HOLD	DC DAC Hold (Testloop TVP)
DTAG	Deutsche Telecom AG
DCCHAR	DC Characteristic block
DCL	Data Clock
DD	Data Downstream
DHP_R	Disable Receive Highpass (SCR5_7)
DHP_X	Disable Transmit Highpass (SCR1_1)
DSP	Digital Signal Processor
DU	Data Upstream
DUP	Data Upstream Persistency Counter
DUPGNK	Data Upstream Persistency Counter for GNK
EXP	Expander

---

**Appendix**

FRR	Frequency Response Receive Filter
FRX	Frequency Response Transmit Filter
FSC	Frame Sync.
GNDIT	Analog Ground
GNK	Ground Key
AHV-SLIC	Advanced High Voltage Subscriber Line Interface Circuit
I1	Fixed Input Pin
ID	External Identification
IL	Longitudinal Current Input
IM I	Impedance Matching Filter (programmable)
IMFIX	Impedance Matching Filter (fixed)
IO	User Programmable I/O Pin
IOM 2-Interface	ISDN Oriented Modular Interface
ISDN	Integrated Service Digital Network
IT	Transversal Current Input (for AC and DC)
ITAC	Transversal Current Input (for AC)
LP03	Low Pass 0.3 Hz
LP5	Low Pass 5 Hz
LSSGR	Local area transport access Switching System Generic Requirements
MEAN VAL.	Mean Value (Testloops, Levelmetering)
MR	Monitor Receive
MX	Monitor Transmit
MuPP	Multi Channel Processor for POTS
MuSLIC	Multi Channel Subscriber Line Interface Circuit
MuSLICOS	MuSLIC Oriented Software
O1	Fixed Output Pin
PCM	Pulse Code Modulation
PDen	Power Denial
PDN	Power Down
PDN	PDN Pin (Sets the HV SLIC to Power Denial)
POFI	Post Filter
PREFI	Antialiasing Pre Filter

---

**Appendix**

QAP	Quad Analog POTS
RB	Ring Burst
RECT	Rectifier (Testloops, Levelmetering)
RES	Reset
REXT	External Ring Sync. Input
RFIX	Receive Filter (fixed)
RNG	Ring Generator
RREF	External Resistor to GNDA
SCR	Status Configuration Register
SLIC	Subscriber Line Interface Circuit
SLMA	Subscriber Loop Marging
SLXC	Summary Line Card Outputs
SOP	Status Operation
STCR	Status Test Configuration Register
TCR	Transfer Configuration Register
TST1	Test Pin
TG	Tone Generator
TH	Transhybrid Balancing
THFIX	Transhybrid Balancing Filter (fixed)
THRESH	Threshold (Testloops, Levelmetering)
TOP	Transfer Operation
TS	Time Slot
TS 0-2	Time Slot selection Pin
TTX	Teletax
TTXFI	Teletax Adaptation
TTXGEN	Teletax Generator
VBIM	Battery Image Input
VB/2	Half Battery Voltage Input
X	Transmit Filter (programmable)
XFIX	Transmit Filter (fixed)