Delta Sheet

DS7, 2002-09-16

QuadFALC®

Quad E1/T1/J1 Framer and Line Interface Component for Long and Short Haul Applications

PEF 22554 HT Version 2.1

PEF 22554 E Version 2.1

Preface

This document describes the changes implemented in the QuadFALC® Version 2.1 related to the previous version 1.3. All functions not mentioned in this document remain unchanged.

QuadFALC® Version 2.1 is a pin-compatible replacement of QuadFALC® Version 1.x.

Severe errata of QuadFALC® Version 1.3 are fixed. For more information please contact your local sales office.

Organization of this Document

- **Chapter 1, Overview**
  Gives a general description of the product differences to its predecessor.
- **Chapter 2, Electrical Characteristics**
  Shows the differences in electrical behavior.
- **Chapter 2.4, Changed Supply Power Test Conditions T1/J1**
  Shows the mechanical dimensions of the new BGA package.
- **Chapter 3, Appendix**
  Shows a screenshot of the available software tool.

Related Documentation

Data Sheet PEF 22554 Version 2.1

Errata Sheet PEB 22554 Version 1.3

Addendum PEB 22554 Version 1.3

Revision History: Previous Version: Preliminray Delta Sheet DS 6, 2002-08-19
Major Changes: **"Functional Changes" on Page 2**: Additional compare status field (CCR5.6)
"Changed DC Characteristics" on Page 26: Power Supply Currents & LOS Limits,

1 Overview

1.1 Functional Changes

The following function has been changed:

- Version status in register VSTR changed from 02_H to 05_H
- The boundary scan part number changed to 142, the boundary scan ID changed to 1. A new BSDL file is required.
- The pulse mask programming (registers XPM(2:0)) has to be adjusted.
- The MCLK reference clock programming (registers GCM(8:1)) has to be changed.
- Variable master clock frequency function always enabled (GCM2(4) = 1).
- New feature “automatic short haul/long haul adjustment” available by setting LIM0.EQON = 1.
- Additional automatic resynchronization mode for T1 (new bit: FMR2.7 = AFRS).
- Additional compare status field (mode 2) in SS7 mode (new bit: CCR5.6 = CSF2).
- 2048 kHz synchronization interface according o ITU-T G.703 Sec. 13 (E1). For more information refer to online Application Notes **http://www.infineon.com/falc**.

1.2 Correction of Errata

All severe errata of QuadFALC® Version 1.3 have been fixed. For more information please contact your local sales office.

1.3 Modified Pin Functions

QuadFALC® Version 2.1 is pin-compatible with QuadFALC® Version 1.x. However, some pin functions have been modified as detailed below:

- No 5 V input levels are allowed due to technology restrictions (see **Page 24**).
- The currently unused ("N.C.") pins on V1.3 devices are used as "Core Voltage Supply" (V_{DDC}) pins and "Voltage Selection" (VSEL) pin on V2.x devices. Due to the new technology the core voltage is 1.8 V (see **Chapter 1.5**).

1.4 Package

In addition to the P-TQFP-144-8 package, a P-BGA-160-1 package with a ball pitch of 1.0 mm and a size of 15 mm × 15 mm is supported (see **Figure 4**).

1.5 Power Supply

The Version 2.1 device requires two supply voltages, 3.3 V and 1.8 V. For compatibility reasons, it is possible to operate the device off a single 3.3 V supply, with the 1.8 V

supply being generated internally using an on-chip voltage regulator. In order to minimize power consumption, it is also possible to operate the device using separate external 3.3 V and 1.8 V supplies. Please note that the 1.8 V supply requires de-coupling whether generated on-chip or externally. Supply voltage selection is done by using pin VSEL. See **Figure 1** and **Figure 2**.

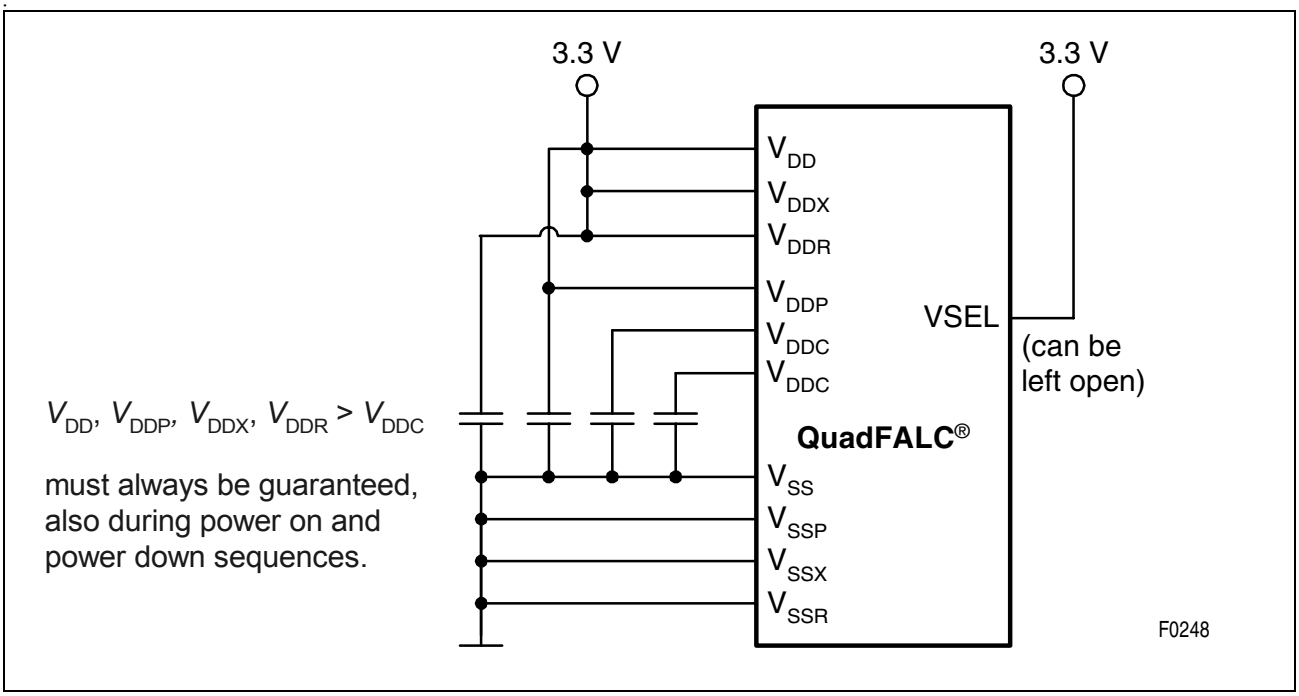

Figure 1 Single Voltage Supply

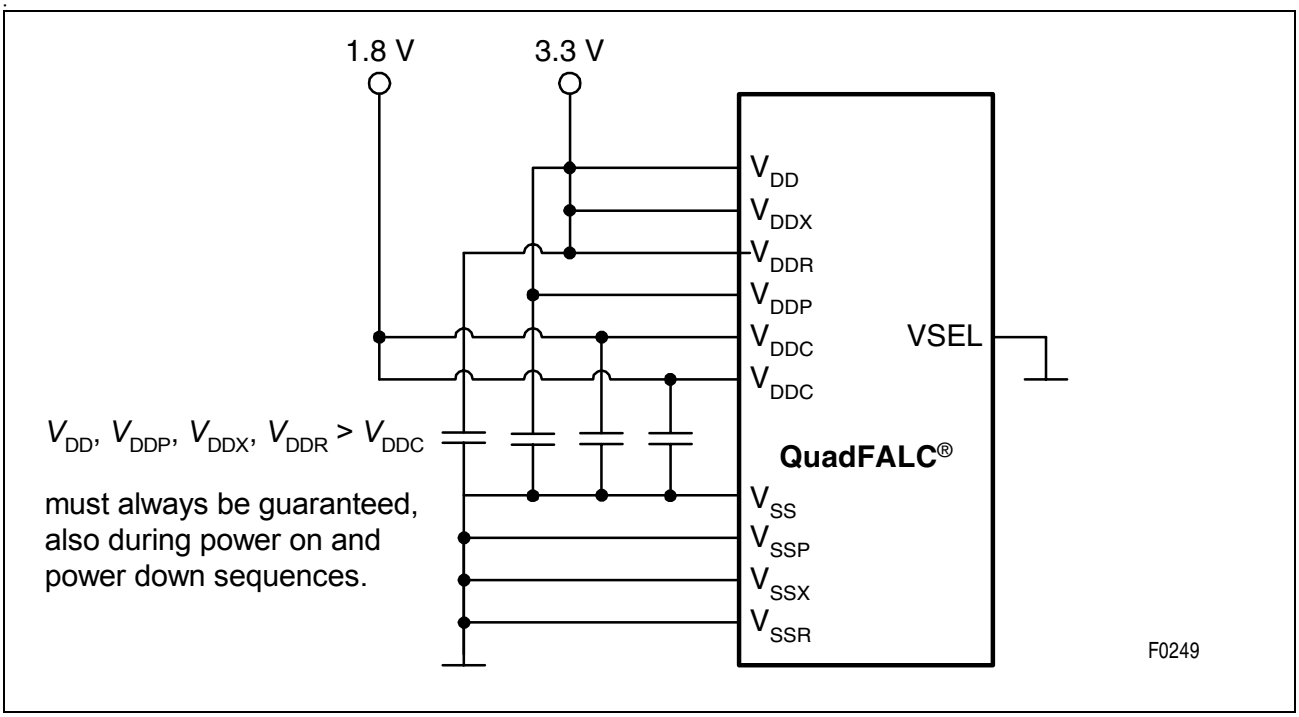

Figure 2 Dual Voltage Supply

1.6 Pinout

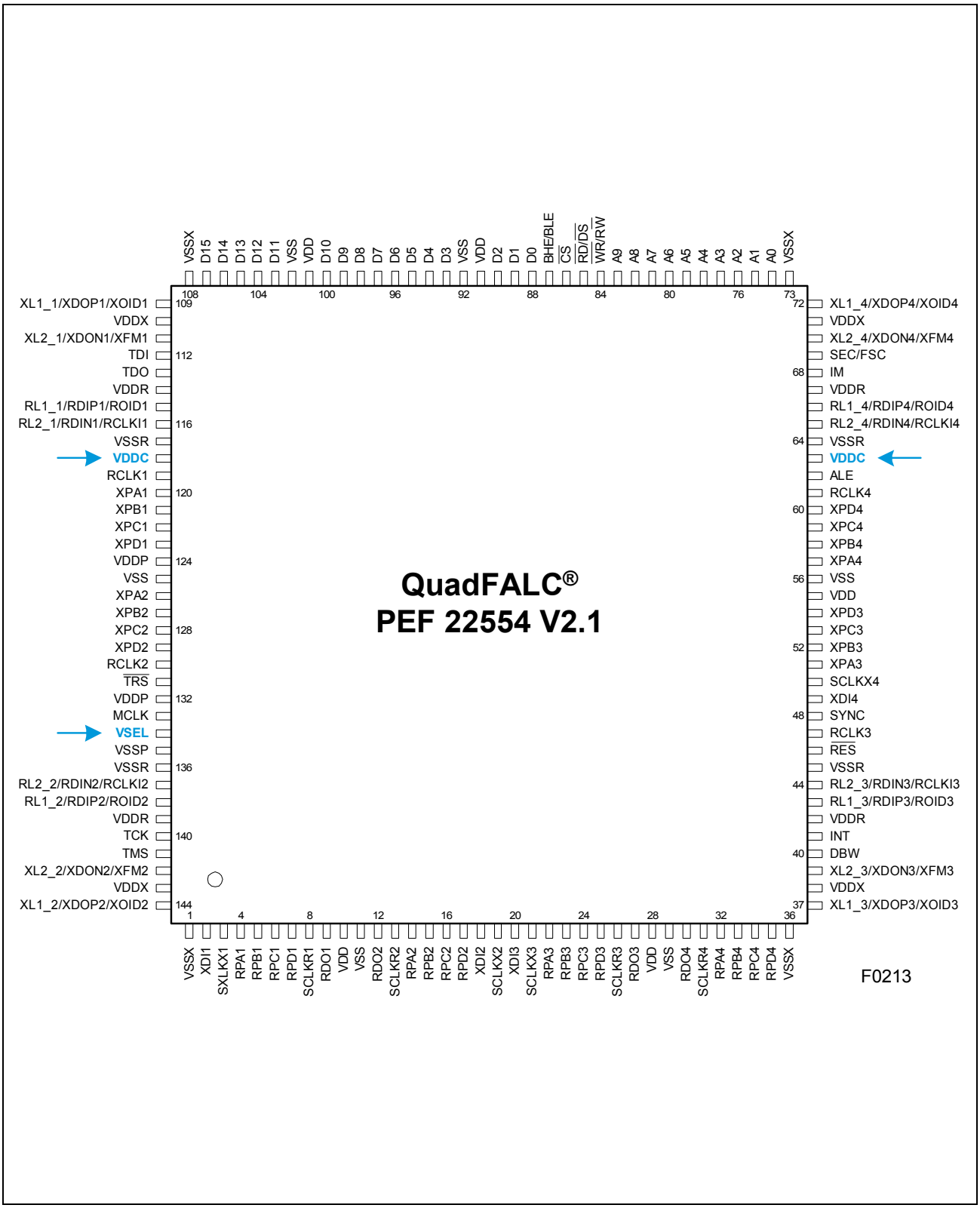

Figure 3 Pin Configuration P-TQFP-144-8, Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	●	XL1_2	XL2_2	VDDR	VSSR	RL1_2	RL2_2	RL2_1	RL1_1	VSSR	VDDR	XL2_1	XL1_1	
B	VSSX	VSSX	XDI1	MCLK	XPC2	$\overline{\text{TRS}}$	XPD2	VDD	XPA1	VDDP	XPB1	D15	VSSX	VSSX
C	VDDX	VDDX	SCLKX 1	TCK	VSSP	VDDP	XPA2	XPB2	XPC1	VDDC	TDO	D14	VDDX	VDDX
D	RPC1	RPA1	RPB1	RPD1	TMS	VSEL	RCLK2	VSS	XPD1	RCLK1	TDI	D12	D13	D11
E	RDO1	SCLKR 1	VDD	VDD							VSS	VDD	VDD	D10
F	RDO2	VSS	SCLKR 2	RPA2							D9	D7	D8	D6
G	RPC2	RPB2	SCLKX 2	RPD2			VSS	VSS			D5	VDD	D4	D3
H	XDI3	SCLKX 3	XDI2	RPA3			VSS	VSS			D2	VSS	D0	D1
J	RPB3	RPD3	RPC3	SCLKR 3							$\overline{\text{BHE}}$/ $\overline{\text{BLE}}$	$\overline{\text{CS}}$	$\overline{\text{WR}}$/ $\overline{\text{RW}}$	$\overline{\text{RD}}$/$\overline{\text{DS}}$
K	RDO3	VSS	VDD	RDO4							A9	A8	A6	A7
L	SCLKR 4	RPB4	RPA4	DBW	RCLK3	XPA3	XPD3	XPB4	ALE	SEC/ FSC	A5	A3	A2	A4
M	VDDX	VDDX	RPC4	INT	$\overline{\text{RES}}$	SCLKX 4	VDD	VDD	XPD4	VDDC	IM	A1	VDDX	VDDX
N	VSSX	VSSX	RPD4	XDI4	XPC3	SYNC	XPB3	XPA4	RCLK4	VSS	XPC4	A0	VSSX	VSSX
P		XL1_3	XL2_3	VDDR	VSSR	RL1_3	RL2_3	RL2_4	RL1_4	VSSR	VDDR	XL2_4	XL1_4	

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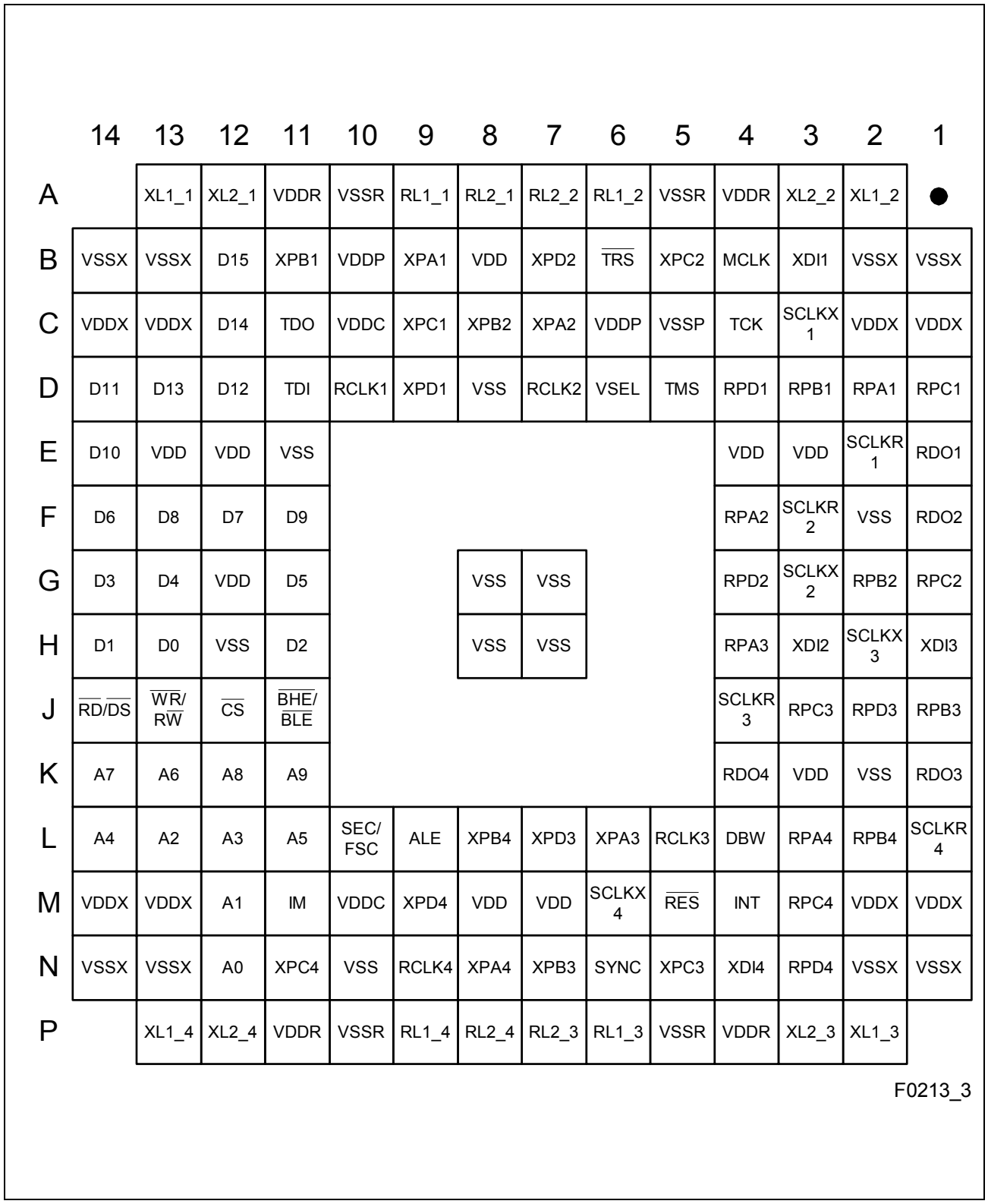
Figure 4 Ball Layout P-BGA-160-1, Top View



	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A		XL1_1	XL2_1	VDDR	VSSR	RL1_1	RL2_1	RL2_2	RL1_2	VSSR	VDDR	XL2_2	XL1_2	●
B	VSSX	VSSX	D15	XPB1	VDDP	XPA1	VDD	XPD2	$\overline{TRS}$	XPC2	MCLK	XDI1	VSSX	VSSX
C	VDDX	VDDX	D14	TDO	VDDC	XPC1	XPB2	XPA2	VDDP	VSSP	TCK	SCLKX 1	VDDX	VDDX
D	D11	D13	D12	TDI	RCLK1	XPD1	VSS	RCLK2	VSEL	TMS	RPD1	RPB1	RPA1	RPC1
E	D10	VDD	VDD	VSS							VDD	VDD	SCLKR 1	RDO1
F	D6	D8	D7	D9							RPA2	SCLKR 2	VSS	RDO2
G	D3	D4	VDD	D5			VSS	VSS			RPD2	SCLKX 2	RPB2	RPC2
H	D1	D0	VSS	D2			VSS	VSS			RPA3	XDI2	SCLKX 3	XDI3
J	$\overline{RD}/\overline{DS}$	$\overline{WR}$/ R$\overline{W}$	$\overline{CS}$	$\overline{BHE}$/ $\overline{BLE}$							SCLKR 3	RPC3	RPD3	RPB3
K	A7	A6	A8	A9							RDO4	VDD	VSS	RDO3
L	A4	A2	A3	A5	SEC/ FSC	ALE	XPB4	XPD3	XPA3	RCLK3	DBW	RPA4	RPB4	SCLKR 4
M	VDDX	VDDX	A1	IM	VDDC	XPD4	VDD	VDD	SCLKX 4	$\overline{RES}$	INT	RPC4	VDDX	VDDX
N	VSSX	VSSX	A0	XPC4	VSS	RCLK4	XPA4	XPB3	SYNC	XPC3	XDI4	RPD4	VSSX	VSSX
P		XL1_4	XL2_4	VDDR	VSSR	RL1_4	RL2_4	RL2_3	RL1_3	VSSR	VDDR	XL2_3	XL1_3	

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Figure 5 Ball Layout P-BGA-160-1, Bottom View

1.7 Pin Description

Table 1 Additional Pin Functions

VSEL	I + PU	**Voltage Select** Enables the internal voltage regulator for 3.3 V-only operation mode if connected to V_{DD} (recommended) or left open. Disables the internal voltage regulator for dual power supply mode if connected to V_{SS}.
V_{DDC}	S	**Positive Power Supply** for the digital core (1.8 V) These pins can either be positive power supply input or output depending on the VSEL input condition. If the VSEL pin is connected to V_{SS}, these pins are inputs and must both be connected to the same 1.8 V power supply and require decoupling. If the VSEL pin is connected to V_{DD} (3.3 V), these pins will both be 1.8 V power supply outputs and must be decoupled to V_{SS}. **Attention: These pins must not be used to supply external devices.**
V_{DDP}	S	**Positive Power Supply** for the analog PLL (3.3 V)
V_{SSP}	S	**Power Supply Ground** for the analog PLL (0 V)

A short pin list of the BGA package is given in **Table 2**. For a complete signal description refer to the QuadFALC® V2.1 Preliminary Data Sheet.

Table 2 BGA Pin Assignment

Ball No. BGA	Pin No. TQFP	Symbol	Input(I) Output(O) Supply(S)	Function
N12	74	A0	I + PU	Address Bus
M12	75	A1	I + PU	Address Bus
L13	76	A2	I + PU	Address Bus
L12	77	A3	I + PU	Address Bus
L14	78	A4	I + PU	Address Bus
L11	79	A5	I + PU	Address Bus
K13	80	A6	I + PU	Address Bus
K14	81	A7	I + PU	Address Bus

Table 2 BGA Pin Assignment (cont'd)

Ball No. BGA	Pin No. TQFP	Symbol	Input(I) Output(O) Supply(S)	Function
K12	82	A8	I + PU	Address Bus
K11	83	A9	I + PU	Address Bus
B12	107	D15	I/O + PU	Data Bus
C12	106	D14	I/O + PU	Data Bus
D13	105	D13	I/O + PU	Data Bus
D12	104	D12	I/O + PU	Data Bus
D14	103	D11	I/O + PU	Data Bus
E14	100	D10	I/O + PU	Data Bus
F11	99	D9	I/O + PU	Data Bus
F13	98	D8	I/O + PU	Data Bus
F12	97	D7	I/O + PU	Data Bus
F14	96	D6	I/O + PU	Data Bus
G11	95	D5	I/O + PU	Data Bus
G13	94	D4	I/O + PU	Data Bus
G14	93	D3	I/O + PU	Data Bus
H11	90	D2	I/O + PU	Data Bus
H14	89	D1	I/O + PU	Data Bus
H13	88	D0	I/O + PU	Data Bus
L9	62	ALE	I + PU	Address Latch Enable
J14	85	$\overline{RD}/\overline{DS}$	I + PU	Read Enable Data Strobe
J13	84	$\overline{WR}/R\overline{W}$	I + PU	Write Enable Read/Write Enable
L4	40	DBW	I + PU	Data Bus Width
M11	68	IM	I + PU	Interface Mode
J12	86	$\overline{CS}$	I + PU	Chip Select
J11	87	$\overline{BHE}/\overline{BLE}$	I + PU	Bus High Enable Bus Low Enable
M4	41	INT	O/oD	Interrupt Request
A9	115	RL1.1	I (analog)	Line Receiver 1, Channel 1

Table 2 BGA Pin Assignment (cont'd)

Ball No. BGA	Pin No. TQFP	Symbol	Input(I) Output(O) Supply(S)	Function
A6	138	RL1.2	I (analog)	Line Receiver 1, Channel 2
P6	43	RL1.3	I (analog)	Line Receiver 1, Channel 3
P9	66	RL1.4	I (analog)	Line Receiver 1, Channel 4
A8	116	RL2.1	I (analog)	Line Receiver 2, Channel 1
A7	137	RL2.2	I (analog)	Line Receiver 2, Channel 2
P7	44	RL2.3	I (analog)	Line Receiver 2, Channel 3
P8	65	RL2.4	I (analog)	Line Receiver 2, Channel 4
A13	109	XL1.1	O (analog)	Transmit Line 1, Channel 1
A2	144	XL1.2	O (analog)	Transmit Line 1, Channel 2
P2	37	XL1.3	O (analog)	Transmit Line 1, Channel 3
P13	72	XL1.4	O (analog)	Transmit Line 1, Channel 4
A12	111	XL2.1	O (analog)	Transmit Line 2, Channel 1
A3	142	XL2.2	O (analog)	Transmit Line 2, Channel 2
P3	39	XL2.3	O (analog)	Transmit Line 2, Channel 3
P12	70	XL2.4	O (analog)	Transmit Line 2, Channel 4
B4	133	MCLK	I	Master Clock
N6	48	SYNC	I + PU	Clock Synchronization of DCO-R
L10	69	SEC/FSC	I/O + PU	One-Second Timer Input One-Second Timer Output 8 kHz Frame Synchronization Output
D10	119	RCLK1	O + PU	Receive Clock, Channel 1
D7	130	RCLK2	O + PU	Receive Clock, Channel 2
L5	47	RCLK3	O + PU	Receive Clock, Channel 3
N9	61	RCLK4	O + PU	Receive Clock, Channel 4
E1	9	RDO1	O	Receive Data Out, Channel 1
F1	12	RDO2	O	Receive Data Out, Channel 2
K1	27	RDO3	O	Receive Data Out, Channel 3
K4	30	RDO4	O	Receive Data Out, Channel 4
E2	8	SCLKR1	I/O + PU	System Clock Receive, Ch. 1

Table 2 BGA Pin Assignment (cont'd)

Ball No. BGA	Pin No. TQFP	Symbol	Input(I) Output(O) Supply(S)	Function
F3	13	SCLKR2	I/O + PU	System Clock Receive, Ch. 2
J4	26	SCLKR3	I/O + PU	System Clock Receive, Ch. 3
L1	31	SCLKR4	I/O + PU	System Clock Receive, Ch. 4
D2	4	RPA1	I/O + PU	Receive Multifunction Port A, Ch. 1
F4	14	RPA2	I/O + PU	Receive Multifunction Port A, Ch. 2
H4	22	RPA3	I/O + PU	Receive Multifunction Port A, Ch. 3
L3	32	RPA4	I/O + PU	Receive Multifunction Port A, Ch. 4
D3	5	RPB1	I/O + PU	Receive Multifunction Port B, Ch. 1
G2	15	RPB2	I/O + PU	Receive Multifunction Port B, Ch. 2
J1	23	RPB3	I/O + PU	Receive Multifunction Port B, Ch. 3
L2	33	RPB4	I/O + PU	Receive Multifunction Port B, Ch. 4
D1	6	RPC1	I/O + PU	Receive Multifunction Port C, Ch. 1
G1	16	RPC2	I/O + PU	Receive Multifunction Port C, Ch. 2
J3	24	RPC3	I/O + PU	Receive Multifunction Port C, Ch. 3
M3	34	RPC4	I/O + PU	Receive Multifunction Port C, Ch. 4
D4	7	RPD1	I/O + PU	Receive Multifunction Port D, Ch. 1
G4	17	RPD2	I/O + PU	Receive Multifunction Port D, Ch. 2
J2	25	RPD3	I/O + PU	Receive Multifunction Port D, Ch. 3
N3	35	RPD4	I/O + PU	Receive Multifunction Port D, Ch. 4
B3	2	XDI1	I	Transmit Data In, Channel 1
H3	18	XDI2	I	Transmit Data In, Channel 2
H1	20	XDI3	I	Transmit Data In, Channel 3
N4	49	XDI4	I	Transmit Data In, Channel 4
C3	3	SCLKX1	I/O + PU	System Clock Transmit, Ch. 1
G3	19	SCLKX2	I/O + PU	System Clock Transmit, Ch. 2
H2	21	SCLKX3	I/O + PU	System Clock Transmit, Ch. 3
M6	50	SCLKX4	I/O + PU	System Clock Transmit, Ch. 4
B9	120	XPA1	I/O + PU	Transmit Multifunction Port A, Ch. 1
C7	126	XPA2	I/O + PU	Transmit Multifunction Port A, Ch. 2

Table 2 BGA Pin Assignment (cont'd)

Ball No. BGA	Pin No. TQFP	Symbol	Input(I) Output(O) Supply(S)	Function
L6	51	XPA3	I/O + PU	Transmit Multifunction Port A, Ch. 3
N8	57	XPA4	I/O + PU	Transmit Multifunction Port A, Ch. 4
B11	121	XPB1	I/O + PU	Transmit Multifunction Port B, Ch. 1
C8	127	XPB2	I/O + PU	Transmit Multifunction Port B, Ch. 2
N7	52	XPB3	I/O + PU	Transmit Multifunction Port B, Ch. 3
L8	58	XPB4	I/O + PU	Transmit Multifunction Port B, Ch. 4
C9	122	XPC1	I/O + PU	Transmit Multifunction Port C, Ch. 1
B5	128	XPC2	I/O + PU	Transmit Multifunction Port C, Ch. 2
N5	53	XPC3	I/O + PU	Transmit Multifunction Port C, Ch. 3
N11	59	XPC4	I/O + PU	Transmit Multifunction Port C, Ch. 4
D9	123	XPD1	I/O + PU	Transmit Multifunction Port D, Ch. 1
B7	129	XPD2	I/O + PU	Transmit Multifunction Port D, Ch. 2
L7	54	XPD3	I/O + PU	Transmit Multifunction Port D, Ch. 3
M9	60	XPD4	I/O + PU	Transmit Multifunction Port D, Ch. 4
B6	131	$\overline{\text{TRS}}$	I + PU	Test Reset for Boundary Scan
D11	112	TDI	I + PU	Test Data Input
D5	141	TMS	I + PU	Test Mode Select
C4	140	TCK	I + PU	Test Clock
C11	113	TDO	O	Test Data Output
M5	46	$\overline{\text{RES}}$	I	Reset
D6	134	VSEL	I + PU	Voltage Select
A11	114	VDDR	S	Power Supply for analog receiver 1
A4	139	VDDR	S	Power Supply for analog receiver 2
P4	42	VDDR	S	Power Supply for analog receiver 3
P11	67	VDDR	S	Power Supply for analog receiver 4
A10	117	VSSR	S	Ground for analog receiver 1
A5	136	VSSR	S	Ground for analog receiver 2
P5	45	VSSR	S	Ground for analog receiver 3
P10	64	VSSR	S	Ground for analog receiver 4

Table 2 BGA Pin Assignment (cont'd)

Ball No. BGA	Pin No. TQFP	Symbol	Input(I) Output(O) Supply(S)	Function
C13, C14	110	VDDX	S	Power Supply for analog transmitter 1
C1, C2	143	VDDX	S	Power Supply for analog transmitter 2
M1, M2	38	VDDX	S	Power Supply for analog transmitter 3
M13, M14	71	VDDX	S	Power Supply for analog transmitter 4
B13, B14	108	VSSX	S	Ground for analog transmitter 1
B1, B2	1	VSSX	S	Ground for analog transmitter 2
N1, N2	36	VSSX	S	Ground for analog transmitter 3
N13, N14	73	VSSX	S	Ground for analog transmitter 4
E3, E4	10	VDD	S	Pad Power Supply 3.3 V
K3	28	VDD	S	Pad Power Supply 3.3 V
M7, M8	55	VDD	S	Pad Power Supply 3.3 V
G12	91	VDD	S	Pad Power Supply 3.3 V
E12, E13	101	VDD	S	Pad Power Supply 3.3 V
B8	---	VDD	S	Pad Power Supply 3.3 V
B10	124	VDDP	S	Analog PLL Power Supply 3.3 V
C6	132	VDDP	S	Analog PLL Power Supply 3.3 V
M10	63	VDDC	S	Core Power Supply 1.8 V
C10	118	VDDC	S	Core Power Supply 1.8 V
C5	135	VSSP	S	Ground for analog PLL
F2	11	VSS	S	Ground
K2	29	VSS	S	Ground
N10	56	VSS	S	Ground
H12	92	VSS	S	Ground
E11	102	VSS	S	Ground
D8	125	VSS	S	Ground
G7, G8, H7, H8	---	VSS	S	Ground

1.8 Decoupling Capacitors

To gain best performance, the following values are recommended for the external decoupling capacitors between V_{DDC} and V_{SS}. There is one decoupling capacitor required on each V_{DDC} pin.

Table 3 Decoupling Capacitor Parameters

Parameter	Value
Capacitance	470 nF ± 20 %, alternatively: 2 x 220 nF ± 20 %
Capacitor material	ceramic, type X7R or compatible
ESR	< 30 mΩ
Loop inductance (L_L) between V_{DDC}, capacitor and next V_{SS} pin	< 10 nH

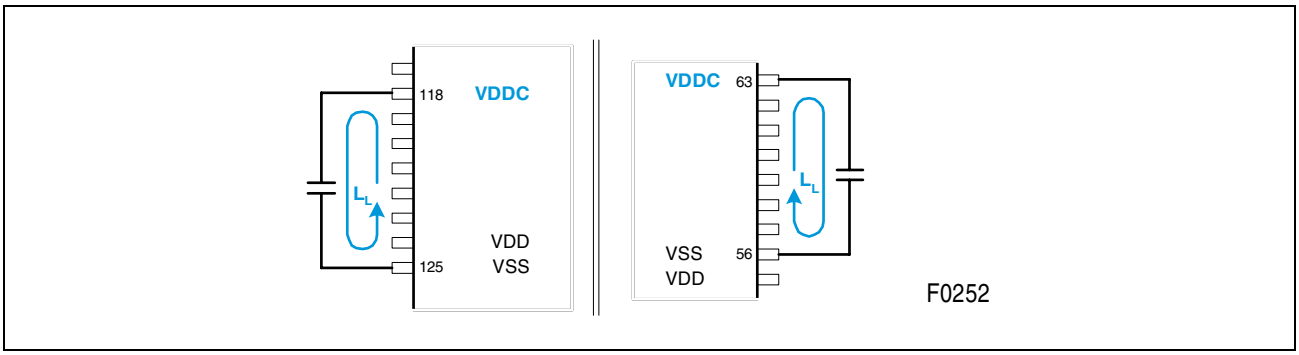


Figure 6 Decoupling Capacitor Placement

1.9 Operation Description E1/T1/J1

Note: Write access to unused register addresses: should be avoided, or set to “00” hex in address range. up to xA9; must be avoided in address range above xA9 if not defined elsewhere (for example in **Table 4**).

To achieve optimum receiver sensitivity in E1 long haul mode (> 38 dB) the following sequence must be run:

Table 4 Receive Line Interface Initialization (E1)

Address	Data
BB_H	17_H
BC_H	55_H
BB_H	97_H
BB_H	11_H
BC_H	AA_H
BB_H	91_H
BB_H	12_H
BC_H	55_H
BB_H	92_H
BB_H	$0C_H$
BC_H	00_H
BB_H	$8C_H$

Note: Sequence must be repeated whenever receiver reset (CMDR.RRES) of arbitrary channel was performed (e.g. after setting bit LIM1.EQON).

1.10 Device Marking Pattern

The sales code changed from PEB 22554 Version 1.3 to PEF 22554 Version 2.1.
The new marking pattern is:

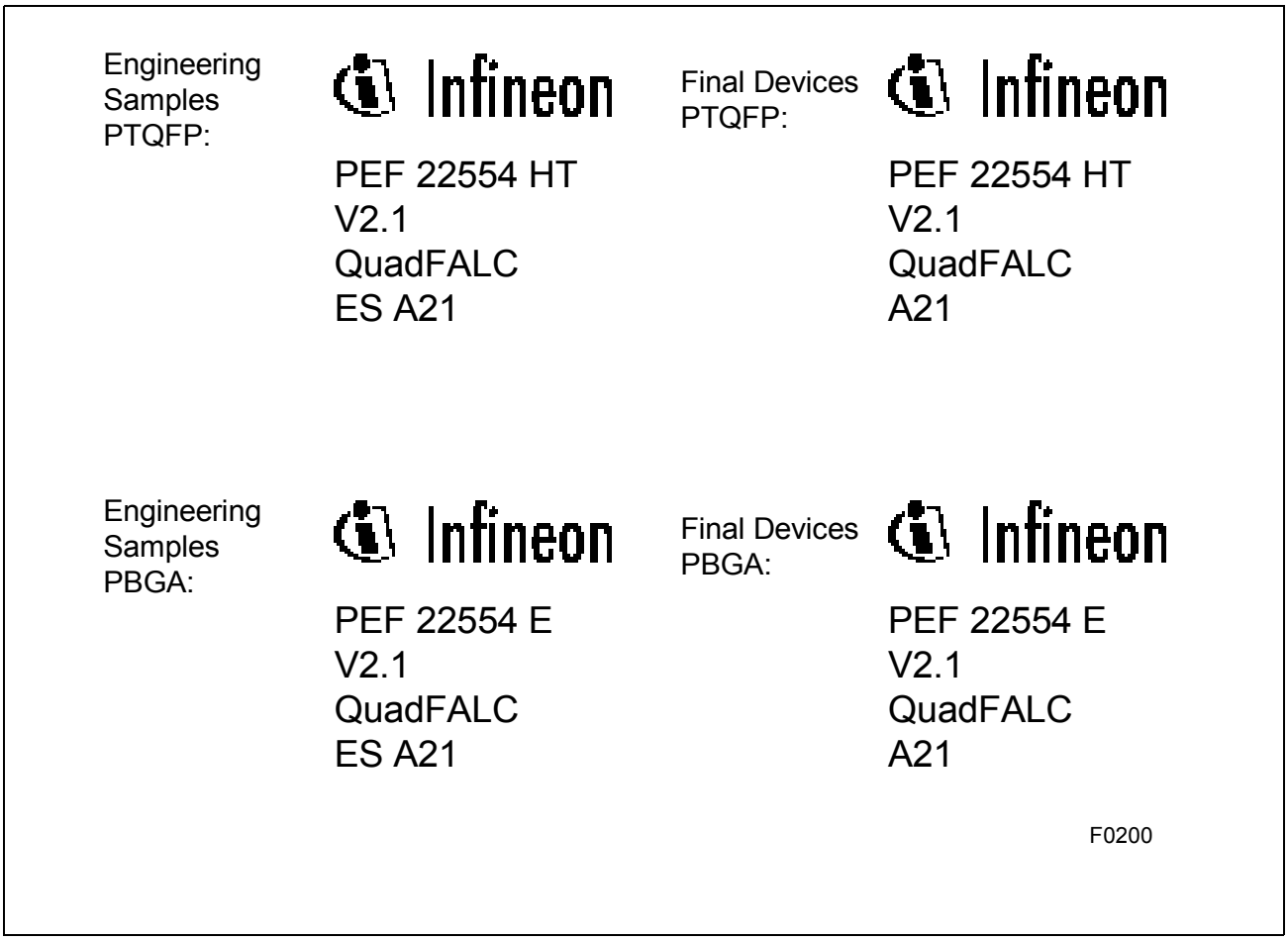


Figure 7 Marking Pattern

1.11 Flexible Clock Mode Settings

The register settings for flexible master clock can be calculated as follows. For some standard frequencies see **Table 5** below. The variables used in these calculations are located in registers GCM1 to GCM8.

1. PLL_M and PLL_N must fulfill the equations:

a.

for PLL_M = 0 to 31:

$$f_{pdref} = \frac{f_{MCLK}}{PLL\_M + 1}$$

b.

for PLL_N = 25 to 63:

$$1.0\ MHz \leq f_{pdref} \leq 6.0\ MHz$$

for PLL_N = 0 to 24:

$$5.0\ MHz \leq f_{pdref} \leq 15.0\ MHz$$

Attention: To decrease sensitivity of PLL to noise on V_{DDP} and/or V_{SSP} adjust f_{pdref} as high as possible.

c.

$$260\ MHz \leq f_{MCLK} \times \frac{4 \times (PLL\_N + 1)}{PLL\_M + 1} \leq 395.26\ MHz$$

(as high as possible within this range)

2. Selection of dividing mode to best fulfill:

$$f_{outE1} = f_{MCLK} \times \frac{4 \times (PLL\_N + 1)}{\left(PHSN\_E1 + \frac{PHSX\_E1}{6}\right) \times (PLL\_M + 1)} \cong 2 \times 16.384\ MHz$$

$$f_{outT1} = f_{MCLK} \times \frac{4 \times (PLL\_N + 1)}{\left(PHSN\_T1 + \frac{PHSX\_T1}{6}\right) \times (PLL\_M + 1)} \cong 2 \times 12.352\ MHz$$

Though the target frequency might not be met directly, the dividing mode has to be selected to reach a frequency which is as near as possible to the target frequency.

PHSN_E1, PHSN_T1: 1 to 15; PHSX_E1, PHSX_T1: 0 to 5

3. Calculation of correction value for frequency mismatch correction:

$$PHD\_E1 = 12288 \times \left[\left(PHSN\_E1 + \frac{PHSX\_E1}{6}\right) - \frac{4 \times (PLL\_N + 1)}{PLL\_M + 1} \times \frac{f_{MCLK}}{2 \times 16.384\ MHz}\right]$$

$$PHD\_T1 = 12288 \times \left[\left(PHSN\_T1 + \frac{PHSX\_T1}{6}\right) - \frac{4 \times (PLL\_N + 1)}{PLL\_M + 1} \times \frac{f_{MCLK}}{2 \times 12.352\ MHz}\right]$$

The result of these equations will be in the range of -2048...+2047. Negative values are represented in 2s-complement format (e.g., $-2000_D = 830_H$; $+2000_D = 7D0_H$).
To achieve optimal QuadFALC® performance values < -1023 and > +1023 must be applied. Negative values are favored.

Table 5 Clock Mode Register Settings for E1 and T1/J1

f_{MCLK}[MHz]	GCM1	GCM2	GCM3	GCM4	GCM5	GCM6	GCM7	GCM8
1.544	00	15	00	08	00	3F	9C	DF
2.048	00	18	FB	0B	00	2F	DB	DF
8.192	00	18	FB	0B	00	0B	DB	DF
10.000	40	1B	3D	0A	00	07	C9	DC
12.352	00	19	00	08	01	0A	98	DA
16.384	00	18	FB	0B	01	0B	DB	DF

Note: All values are given in hexadecimal notation.

To support the necessary calculations, an easy-to-use PC tool is available for free (see **Page 29** for details).

1.12 Register Modifications

Framer Mode Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
FMR2	**AFRS**	MCSP	SSP	DAIS	SAIS	PLB	AXRA	EXZE	(x1E)

AFRS **Automatic Force Resynchronization**

Search for next candidate automatically, if multiple candidates are present and the current candidate is incorrect.

(This bit is available in T1/J1 F12 mode only).

Line Interface Mode 2 (Read/Write)

Value after reset: 20_H

	7							0	
LIM2	**LBO2**	**LBO1**	SLT1	SLT0	SCF	ELT		LOS1	(x3A)

LBO(2:0) **Line Build-Out**

To meet the line build-out defined by ANSI T1.403 registers XPM(2:0) should be programmed as follows:

00 0 dB

01 -7.5 dB → XPM(2:0) = 00_H, 01_H, $8C_H$

10 -15 dB → XPM(2:0) = 01_H, 11_H, $8C_H$

11 -22.5 dB → XPM(2:0) = 00_H, 01_H, 07_H

(This bits are available in T1/J1 mode only).

Line Interface Mode 0 (Read/Write)

Value after reset: 00_H

	7							0	
LIM0	XFB	XDOS	0	0	**EQON**	RLM	LL	MAS	(x36)

EQON By setting EQON = 1 the QuadFALC® is able to adjust short haul or long haul mode automatically. After changing the value of EQON a receiver reset (CMDR.RRES) is required. For E1 mode please note sequence as specified in **Table 4** on **Page 14**.

Note: When using EQON = 1 together with RLM = 1, LIM1.RIL(2:0) must be set to 001_B.

Line Interface Mode 1 (Read/Write)

Value after reset: 00_H

	7							0	
LIM1	CLOS	RIL2	RIL1	RIL0		JATT	RL	**DRS**	(x37)

DRS **Dual Rail Select**

Note: LIM0.EQON must be set to 0 when DRS = 1

Version Status Register (Read)

	7							0	
VSTR	0	0	0	0	0	1	0	1	(4A)

VN(7:0) **Version Number of Chip**

05_H…Version 2.1

Port Configuration 5 (Read/Write)

Value after reset: 20_H

	7							0	
PC5					CXMFS	**0**	CSRP	CRP	(x84)

PC5.2 reserved

Must be cleared.

Common Configuration Register 5 (Read/Write)

Value after reset: 00_H

	7							0	
CCR5		**CSF2**	SUET	CSF	AFX		CR[1)]	EPR[1)]	(x8D)

1) T1 mode only

CSF2 **Compare Status Field - Mode 2**
If the status fields of consecutive LSSUs are equal, only the first is stored and every following is ignored.
Exception: if identical FISUs are received, two of them are stored,

0 Compare disabled.

1 Compare enabled.

Note: Only valid if SS7 is selected

Global Clock Mode Register 2 (Read/Write)

Value after reset: 00_H

	7							0	
GCM2	**0**	**0**	**0**	**1**	PHD_E1 11	PHD_E1 10	PHD_E1 9	PHD_E1 8	(93)

GCM2(7:5) removed bits

GCM2(4) must be set to 1, details for calculate of the remaining GCM values can be found in **Chapter 1.11.**

Global Clock Mode Register 4 (Read/Write)

Value after reset: 00_H

	7							0	
GCM4	**0**	**0**	**0**	0	PHD_T1 11	PHD_T1 10	PHD_T1 9	PHD_T1 8	(95)

GCM4(7:5) removed bits

Global Clock Mode Register 5 (Read/Write)

Value after reset: 00_H

	7							0	
GCM5	**0**	0	0	PLLM_4	PLLM_3	PLLM_2	PLL_M1	PLL_M0	(96)

GCM5.7 removed bit, to be set to 0

Global Clock Mode Register 6 (Read/Write)

Value after reset: 00_H

	7							0	
GCM6	0	0	**PLLN_5**	PLLN_4	PLLN_3	PLLN_2	PLL_N1	PLL_N0	(97)

GCM6.5 added bit

Attention: Write operations to GCM5 and/or GCM6 register must be performed before any port configuration is done. If this is not possible set LIM0.DRS (if not set) of every channel seperately before writing to these registers and reset LiM0.DRS (if it was not set before) after these write operations.

Global Clock Mode Register 7 (Read/Write)

Value after reset: 00_H

	7							0	
GCM7	**1**	**PHSX_ E12**	**PHSX_ E11**	**PHSX_ E10**	**PHSN_ E13**	**PHSN_ E12**	**PHSN_ E11**	**PHSN_ E10**	**(98)**

GCM7.7 added bit, to be set to 1

PHSX_E1(2:0) added bits

PHSN_E1(3:0) added bits

Global Clock Mode Register 8 (Read/Write)

Value after reset: 00_H

	7							0	
GCM8	**1**	**PHSX_ T12**	**PHSX_ T11**	**PHSX_ T10**	**PHSN_ T13**	**PHSN_ T12**	**PHSN_ T11**	**PHSN_ T10**	**(99)**

GCM8.7 added bit, to be set to 1

PHSX_T1(2:0) added bits

PHSN_T1(3:0) added bits

Channel Interrupt Status Register (Read)

	7							0	
CIS	**PLLL**	0	0	0	GIS4	GIS3	GIS2	GIS1	(6F)

CIS.7 **PLL Locked Status**

1 if PLL is locked, 0 if PLL is unlocked

Note:This bit is only updated when a clock is available on pin MCLK

Transmit Pulse Mask 2…0 (Read/Write)

Value after RESET: $7B_H$, 03_H, 40_H

	7							0	
XPM0	XP12	XP11	XP10	XP04	XP03	XP02	XP01	XP00	(x26)
XPM1	XP30	XP24	XP23	XP22	XP21	XP20	XP14	XP13	(x27)
XPM2	XLLP	XLT	DAXLT		XP34	XP33	XP32	XP31	(x28)

c

Table 6 Pulse Shaper Programming (T1/J1)[1)]

Range in m	Range in ft.	XPM0	XPM1	XPM2	XP04-XP00	XP14-XP10	XP24-XP20	XP34-XP30
		hexadecimal			decimal			
0 to 40	0 to 133	95	16	01	21	20	5	2
40 to 81	133 to 266	B6	9E	01	22	21	7	3

Table 6 Pulse Shaper Programming (T1/J1)[1)]

Range in m	Range in ft.	XPM0	XPM1	XPM2	XP04-XP00	XP14-XP10	XP24-XP20	XP34-XP30
81 to 122	266 to 399	D9	26	01	25	22	9	2
122 to 162	399 to 533	FC	36	01	28	23	13	2
162 to 200	533 to 655	3F	CB	01	31	28	18	3

1) Register values of V1.3 may also be used. For optimum results V2.1 values must be applied

Example for E1 120 Ω interface:

Programming values for XPM(2:0): 00_H, 03_H, $9C_H$.

XPM0(4:0): $1C_H$ or 28 decimal
XPM1(4:0): $1C_H$ or 28 decimal
XPM2(4:0): 00_H
XPM3(4:0): 00_H

2 Electrical Characteristics

Due to the change of silicon technology some of the electrical characteristics have changed.

2.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Ambient temperature under bias	T_A	– 40	85	°C
Storage temperature	T_{stg}	– 65	125	°C
IC supply voltage (pads, digital)	V_{DD}	– 0.3	3.60	V
IC supply voltage (core, digital)	V_{DDC}	– 0.3	1.98	V
IC supply voltage PLL (analog)	V_{DDP}	– 0.3	3.60	V
IC supply voltage receive (analog)	V_{DDR}	– 0.3	3.60	V
IC supply voltage transmit (analog)	V_{DDX}	– 0.3	3.60	V
Voltage on any pin with respect to ground[1)]	V_S	– 0.3	3.60	V
ESD robustness HBM: 1.5 kΩ, 100 pF[2)] CDM [3)]	$V_{ESD,HBM}$	-	2000	V
	$V_{ESD,CDM}$	-	500	V
Moisture level 3	---		225[4)]	°C
			245[5)]	°C

1) Except V_{DDC}

2) According to JEDEC standard EIA/JESD22-A114-B-1997.

3) According to EOS/ESD Assn.Standard DS5.3-1993

4) According to IPS J-STD 020

5) According to IFX internal standard

Attention: If the 1.8 V power supply is externally driven on V_{DDC}, the voltage on this pin must never exceed the 3.3 V supply voltages on pins V_{DD}, V_{DDP}, V_{DDX} and V_{DDR}, even during power up and power down of the circuit.

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	T_A	-40	85	°C	
Supply voltages	V_{DD}	3.13	3.46	V	3.3 V ± 5%
	V_{DDP} [1]	3.13	3.46	V	3.3 V ± 5%
	V_{DDR} [1]	3.13	3.46	V	3.3 V ± 5%
	V_{DDC}	1.62	1.98	V	1.8 V ± 10%
	V_{DDX} [1]	3.13	3.46	V	3.3 V ± 5%
Analog input voltages	V_{IA}	0	3.60 [2]	V	3.3 V ± 5%
Digital input voltages	V_{ID}	0	3.46	V	3.3 V ± 5%
Ground	V_{SS} V_{SSP} V_{SSR} V_{SSX}	0	0	V	

[1] Voltage ripple less than 50 mV on these 3.3V supplies

[2] Depending on the applied power supply level, signal clipping may occur due to activation of the ESD protection diodes if the signal level exceeds V_{DDR} + 0.3 V

Note: In the operating range, the functions given in the circuit description are fulfilled.
V_{DD}, V_{DDP}, V_{DDR} and V_{DDX} have to be connected to the same voltage level,
V_{SS}, V_{SSP}, V_{SSR}, and V_{SSX} have to be connected to ground level.
V_{DD} and V_{DDC} refer to the same ground level V_{SS}.

2.3 Changed DC Characteristics

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input high voltage	V_{IH}	2.0	3.46	V	
Average power supply current (analog line interface mode)	I_{DDE1}		290	mA	E1 application LIM1.DRS = 0
	I_{DDT1}		285	mA	T1 application LIM1.DRS = 0
Average power supply current (digital line interface mode)	$I_{DD3.3V}$		20[1)]	mA	LIM1.DRS = 1[2)]
	I_{DDC}		90	mA	
Transmitter leakage current	I_{TL}		15.0	µA	XL1/2 = V_{DDX}; XPM2.XLT = 1
			15.0	µA	XL1/2 = V_{SSX}; XPM2.XLT = 1
Receiver sensitivity E1 long haul	S_{RLH}		43[3)]	dB	RL1, RL2 LIM0.EQON = 1
Loss of signal (LOS) detection limit[4)5)]	V_{LOS}	1.25	2.25	V	RIL(2:0) = 000[6)]
		0.84	1.07		RIL(2:0) = 001[6)]
		0.45	0.58		RIL(2:0) = 010[7)]
		0.26	0.33		RIL(2:0) = 011[6)]
		0.15	0.21		RIL(2:0) = 100[6)]
		0.10	0.14		RIL(2:0) = 101[6)]
		0.07	0.09		RIL(2:0) = 110[6)]
		0.04	0.06		RIL(2:0) = 111[6)]

1) In single voltage supply mode (see **Figure 1**) maximum $I_{DD3.3V}$ = 110 mA

2) System interface at 16 MHz; all-ones data; T_A = 85 °C

3) To achieve maximum receiver sensitivity of -43 dB (E1) take special care on sufficient attenuation of crosstalk between Rx and Tx on board (e.g. in transformer) and run sequence as specified in **Table 4** on **Page 14**

4) Differential input voltage between pins RL1 and RL2

5) Values only valid for LIM0.EQON = 1, LOS detection limits set to PCR = 15_H, PCD = A_H, applied signal sequence +1,0,-1,0,...

6) Parameter not tested in production

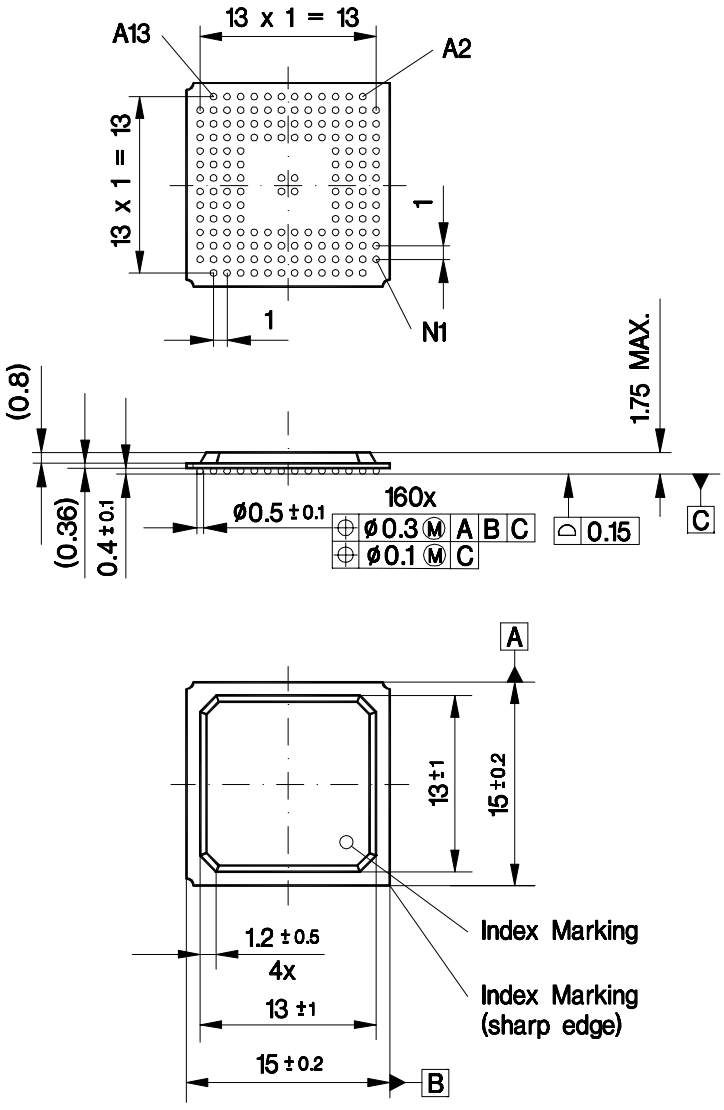
7) Value measured in production to fulfil ITU-T G.775

2.4 Changed Supply Power Test Conditions T1/J1

Parameter	Symbol	Test Values	Unit	Notes
Pulse Mask Programming	XPM2	01_H		
	XPM1	16_H		
	XPM0	95_H		

2.5 Package Outlines

P-BGA-160-1
(Plastic Ball Grid Array Package)



GPA09369

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

3 Appendix

The calculation of the GCM register values is supported by a PC-based tool which is available for free. A screenshot is shown in **Figure 8** below.

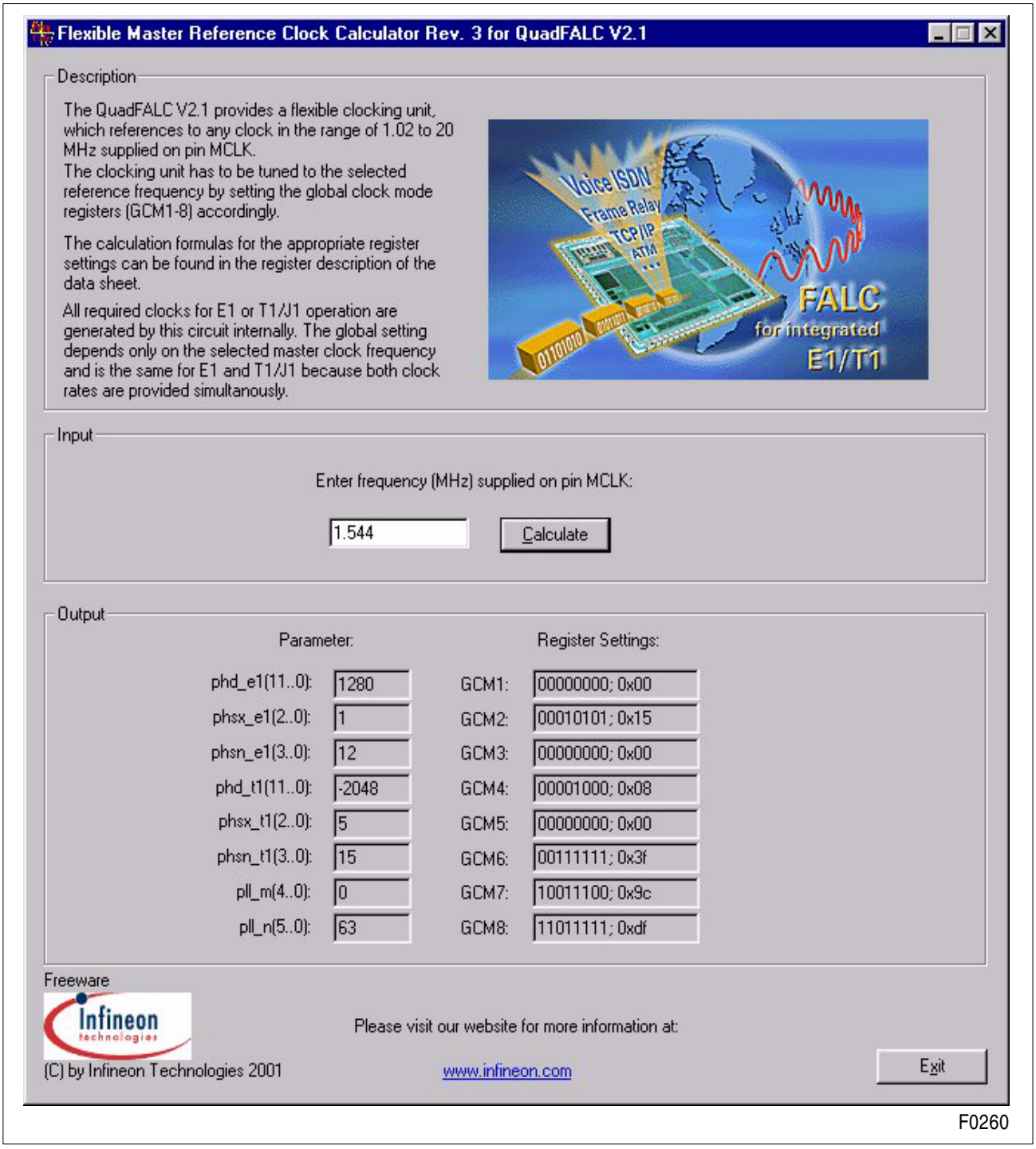


Figure 8 Flexible Master Clock Calculator

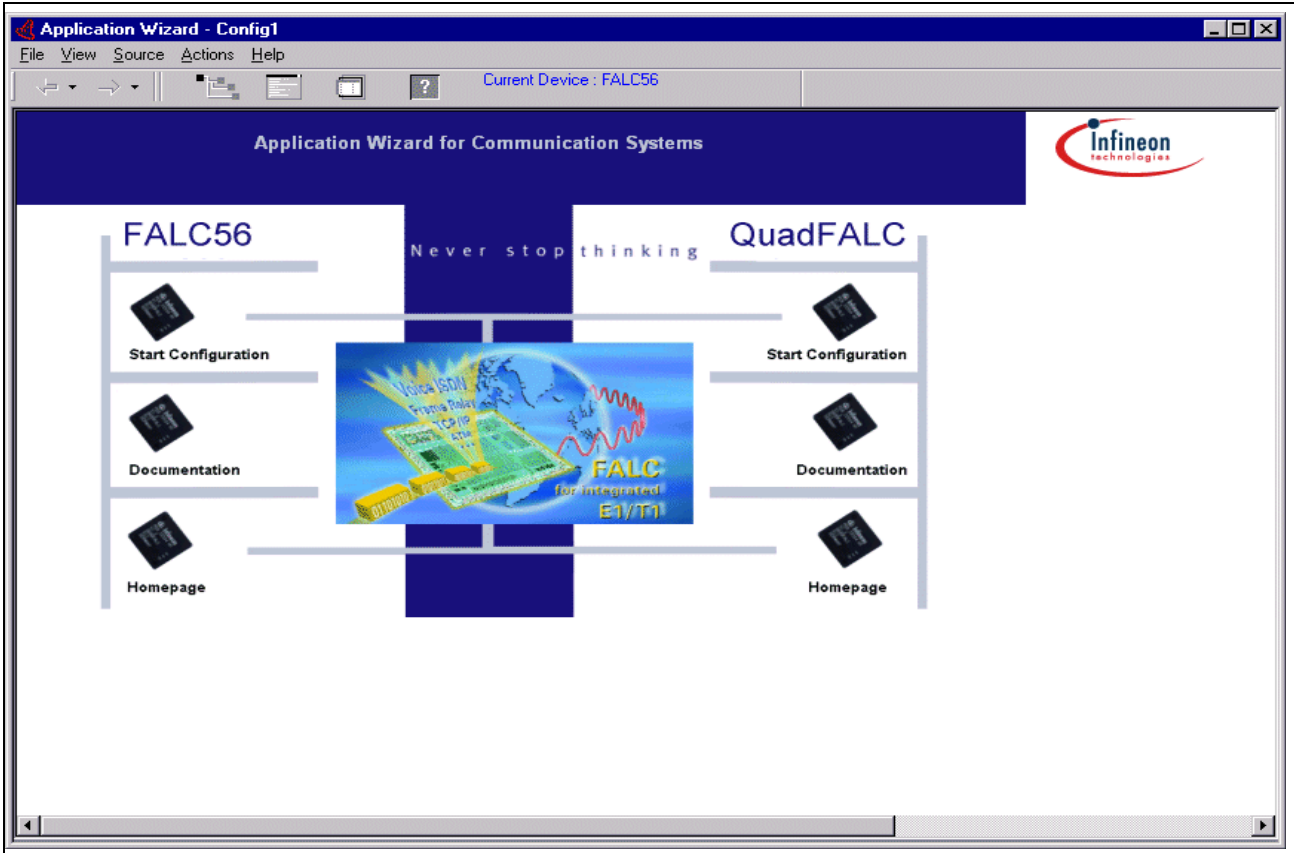


Figure 9 Application Wizard