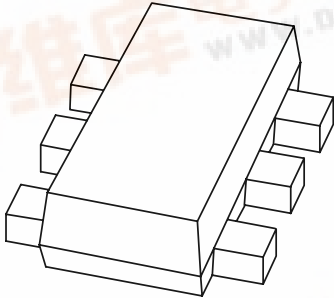


DISCRETE SEMICONDUCTORS

DATA SHEET



PEMB2

PNP resistor-equipped double transistor $R1 = 47 \text{ k}\Omega$, $R2 = 47 \text{ k}\Omega$

Product specification

2001 Sep 14

PNP resistor-equipped double transistor

R1 = 47 kΩ, R2 = 47 kΩ

PEMB2

FEATURES

- 300 mW total power dissipation
- Very small 1.6 mm × 1.2 mm × 0.55 mm ultra thin package
- Excellent coplanarity due to straight leads
- Reduces number of components as replacement of two SC-75/SC-89 packaged transistors
- Reduces required board space
- Reduces pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

DESCRIPTION

PNP resistor-equipped double transistor in a SOT666 plastic package.

MARKING

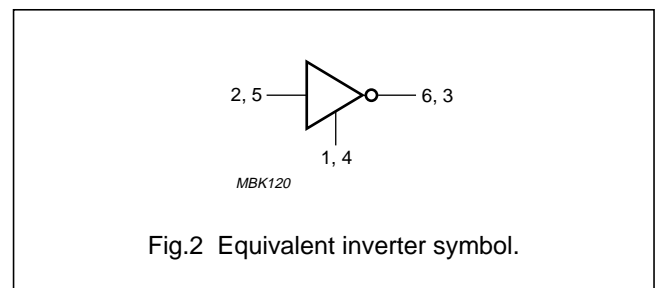
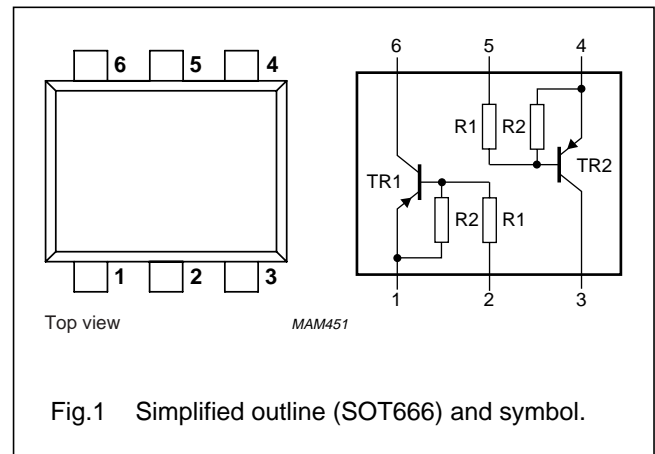
TYPE NUMBER	MARKING CODE
PEMB2	B2

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
3, 6	collector TR1; TR2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{CEO}	collector-emitter voltage	-50	V
I _{CM}	peak collector current	-100	mA
TR1	PNP	-	-
TR2	PNP	-	-
R1	bias resistor	47	kΩ
R2	bias resistor	47	kΩ



PNP resistor-equipped double transistor
 $R1 = 47\text{ k}\Omega$, $R2 = 47\text{ k}\Omega$

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
V_{CBO}	collector-base voltage	open emitter	–	–50	V
V_{CEO}	collector-emitter voltage	open base	–	–50	V
V_{EBO}	emitter-base voltage	open collector	–	–10	V
V_I	input voltage				
	positive		–	+10	V
	negative		–	–40	V
I_O	output current (DC)		–	–100	mA
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$
T_{amb}	operating ambient temperature		–65	+150	$^\circ\text{C}$
Per device					
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$; note 1	–	300	mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

PNP resistor-equipped double transistor
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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering method is reflow soldering.

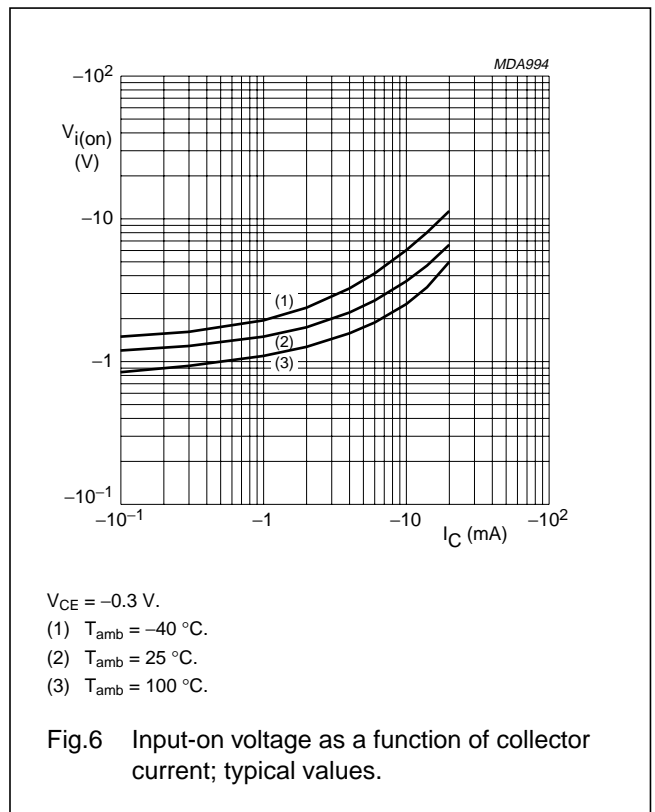
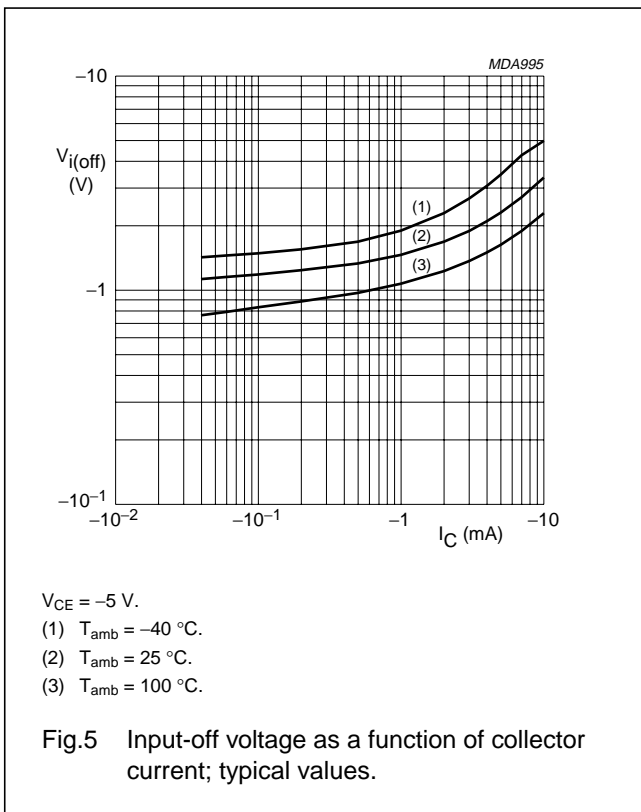
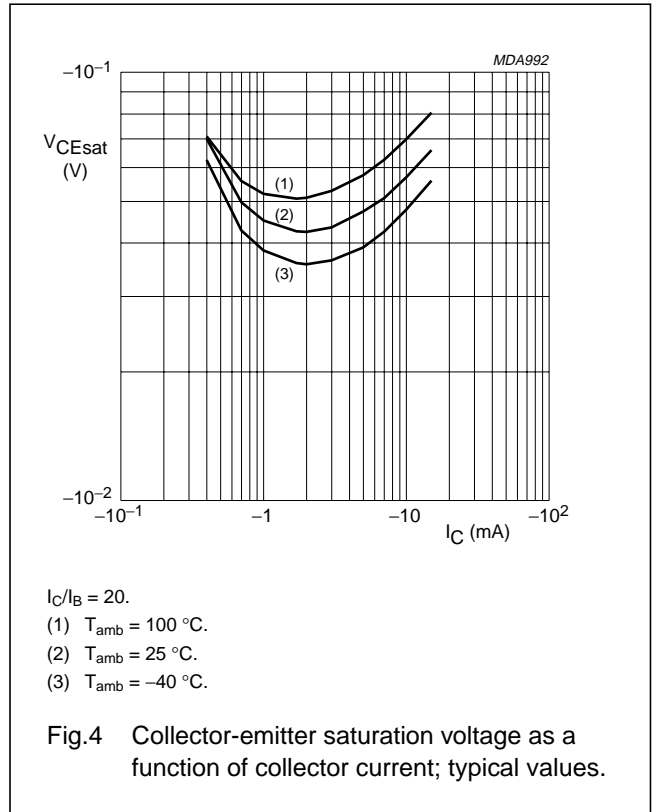
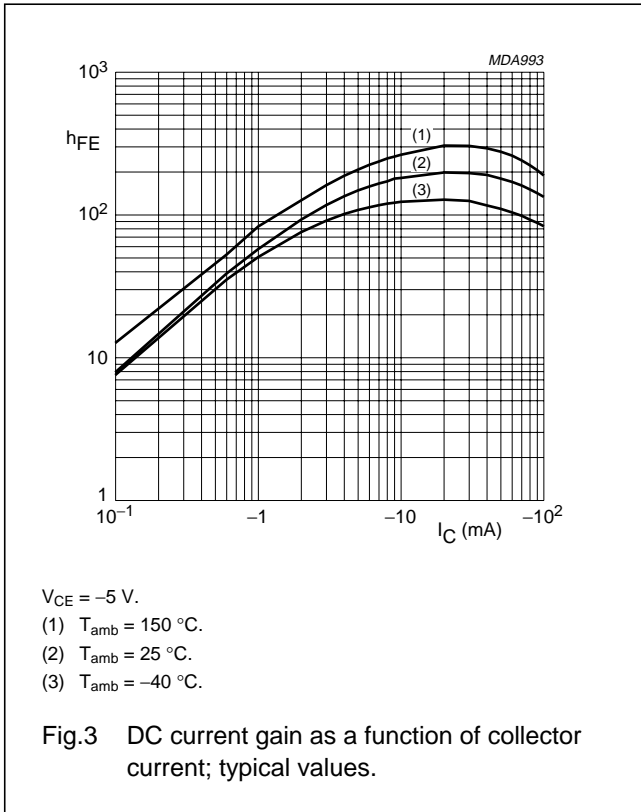
CHARACTERISTICS

$T_{amb} = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor						
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = -50 \text{ V}$	–	–	–100	nA
I_{CEO}	collector cut-off current	$I_B = 0$; $V_{CE} = -50 \text{ V}$	–	–	–1	μA
		$I_B = 0$; $V_{CE} = -30 \text{ V}$; $T_j = 150 \text{ }^\circ\text{C}$	–	–	–50	μA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = -5 \text{ V}$	–	–	–90	μA
h_{FE}	DC current gain	$I_C = -5 \text{ mA}$; $V_{CE} = -5 \text{ V}$	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10 \text{ mA}$; $I_B = -0.5 \text{ mA}$	–	–	–150	mV
$V_{i(off)}$	input-off voltage	$I_C = -100 \text{ }\mu\text{A}$; $V_{CE} = -5 \text{ V}$	–	1.2	0.8	V
$V_{i(on)}$	input-on voltage	$I_C = -2 \text{ mA}$; $V_{CE} = -0.3 \text{ V}$	3	1.6	–	V
R1	input resistor		33	47	61	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$I_E = I_e = 0$; $V_{CB} = -10 \text{ V}$; $f = 1 \text{ MHz}$	–	–	3	pF

PNP resistor-equipped double transistor
 R1 = 47 kΩ, R2 = 47 kΩ

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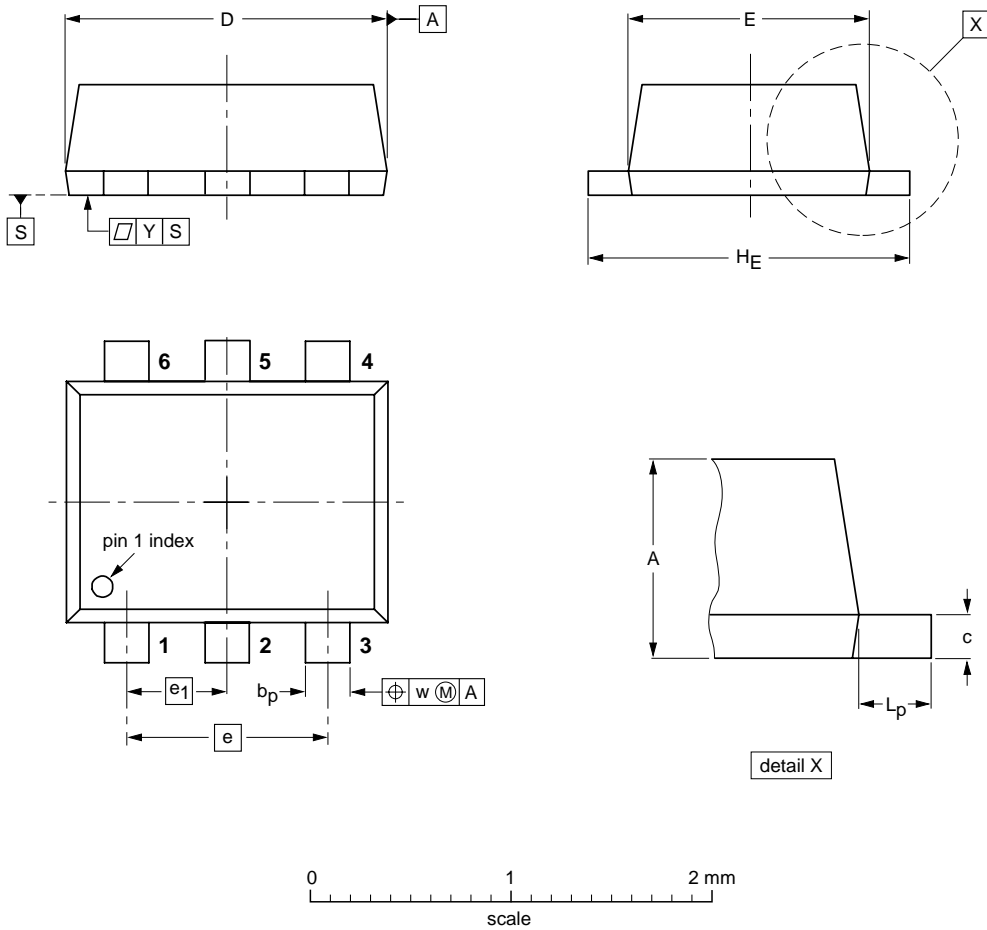
PNP resistor-equipped double transistor
 R1 = 47 kΩ, R2 = 47 kΩ

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	H _E	L _p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						01-01-04 01-08-27

PNP resistor-equipped double transistor

R1 = 47 kΩ, R2 = 47 kΩ

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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