14-BIT, 1.25-MSPS LOW POWER SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 1.25 MHz Sample Rate, 14-Bit Resolution
- Zero Latency
- Unipolar, Pseudo Differential Input, Range:
  - 0 V to 2.5 V
- SPI™ Compatible Serial Interface
- 77.5 dB SNR and −95 dB THD at 0.5 MHz I/P
- Power Dissipation 45 mW at 1.25 MSPS
- Nap Mode (10 mW Power Dissipation)
- Power Down (10 μW)
- Internal Reference
- Internal Reference Buffer
- 48-Pin TQFP Package

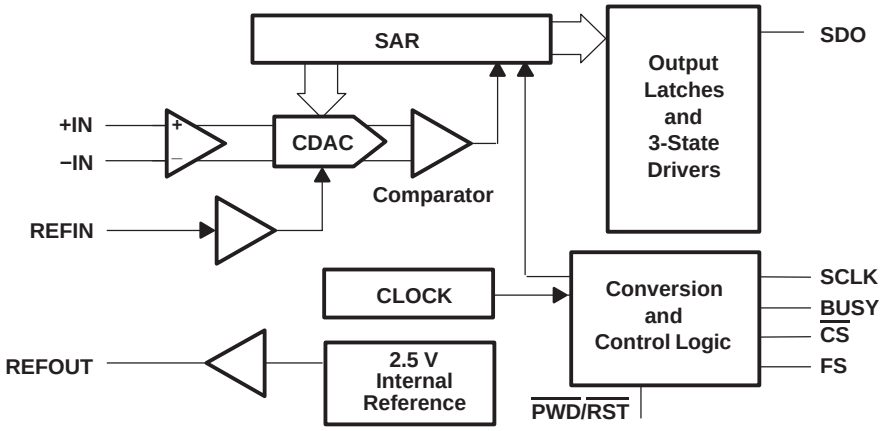
APPLICATIONS

- Optical Networking (DWDM, MEMS Based Switching)
- Spectrum Analyzers
- High Speed Data Acquisition Systems
- High Speed Close-Loop Systems
- Telecommunication

DESCRIPTION

The ADS7890 is a 14-bit 1.25-MSPS A-to-D converter with 2.5-V internal reference. The device includes a capacitor based SAR A/D converter with inherent sample and hold. The device offers a 14-bit serial SPI or DSP compatible interface. The device has a pseudo-differential input stage.

The −IN swing of ±200 mV is useful to compensate for ground voltage mismatch between the ADC and sensor and also to cancel common-mode noise. The device operates at lower power when used at lower conversion rates because of the nap feature. The device is available in a 48-pin TQFP package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS7890	±1.5	+1.5/−1	14	48-Pin TQFP	PFB	−40°C to 85°C	ADS7890IPFBT	Tape and reel 250
							ADS7890IPFBR	Tape and reel 1000

NOTE: For most current specifications and package information, refer to the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range(1)

		UNIT
+IN to AGND		−0.3 V to +VA + 0.1 V
−IN to AGND		−0.3 V to 0.5 V
+VA to AGND		−0.3 V to 7 V
+VBD to BDGND		−0.3 V to 7 V
Digital input voltage to GND		−0.3 V to (+VBD + 0.3 V)
Digital output to GND		−0.3 V to (+VBD + 0.3 V)
Operating temperature range		−40°C to 85°C
Storage temperature range		−65°C to 150°C
Junction temperature ($T_J$max)		150°C
TQFP package	Power dissipation	(T_J Max–T_A)/ θ_{JA}
	θ_{JA} Thermal impedance	86°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SPECIFICATIONS

T_A = −40°C to 85°C, +VA = 5 V, +VBD = 5 V or 3.3 V, V_{ref} = 2.5 V, f_{sample} = 1.25 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span(1)	+IN – (−IN)	0		V_{ref}	V
Absolute input range	+IN	−0.2		V_{ref} + 0.2	V
	−IN	−0.2		+0.2	
Input capacitance			27		pF
Input leakage current			500		pA
SYSTEM PERFORMANCE					
Resolution			14		Bits
No missing codes		14			Bits
Integral linearity(2)		−1.5	±0.75	1.5	LSB(3)
Differential linearity		−1	±0.75	1.5	LSB(3)
Offset error(4)	External reference	−1.5	±0.5	1.5	mV
Gain error(4)	External reference	−1	±0.25	1	mV
Common-mode rejection ratio	With common mode input signal = 200 mVp−p at 0.5 MHz		60		dB
Power supply rejection	At $3FF0_H$ output code, +VA = 4.75 V to 5.25 V , Vref = 2.50 V		80		dB
SAMPLING DYNAMICS					
Conversion time	+VDB = 5 V			365	nsec
	+VDB = 3 V			365	nsec
Acquisition time	+VDB = 5 V	187.5			nsec
	+VDB = 3 V	187.5			nsec
Maximum throughput rate				1.25	MHz
Aperture delay			5		nsec
Aperture jitter			20		psec
Step response			50		nsec
Over voltage recovery			50		nsec
DYNAMIC CHARACTERISTICS					
Total harmonic distortion(5)	V_{IN} = 2.496 Vp−p at 100 kHz/2.5 Vref		−95		dB
	V_{IN} = 2.496 Vp−p at 0.5 MHz/2.5 Vref		−95	−88	
SNR	V_{IN} = 2.496 Vp−p at 100 kHz/2.5 Vref		78		dB
	V_{IN} = 2.496 Vp−p at 0.5 MHz/2.5 Vref		77.5		
SINAD	V_{IN} = 2.496 Vp−p at 100 kHz/2.5 Vref		77		dB
	V_{IN} = 2.496 Vp−p at 0.5 MHz/2.5 Vref		77		
SFDR	V_{IN} = 2.496 Vp−p at 0.5 MHz/2.5 Vref	89	97		dB
−3 dB Small signal bandwidth			50		MHz
EXTERNAL REFERENCE INPUT					
Input V_{REF} range		2.4	2.5	2.6	V
Resistance(6)			500		kΩ

(1) Ideal input span; does not include gain or offset error.
(2) This is endpoint INL, not best fit.
(3) LSB means least significant bit.
(4) Measured relative to actual measured reference.
(5) Calculated on the first nine harmonics of the input frequency.
(6) Can vary ±20%.

SPECIFICATIONS Continued

T_A = −40°C to 85°C, +VA = 5 V, +VBD = 5 V or 3.3 V, V_{ref} = 2.5 V, f_{sample} = 1.25 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL REFERENCE OUTPUT						
Start-up time		From 95% (+VA), with 1-µF storage capacitor on REFOUT to AGND			120	msec
V_{REF} Range		IOUT=0	2.48	2.5	2.52	V
Source current		Static load			10	µA
Line regulation		+VA = 4.75 V to 5.25 V		1		mV
Drift		IOUT = 0		25		PPM/C
DIGITAL INPUT/OUTPUT						
Logic family				CMOS		
Logic level	V_{IH}	I_{IH} = 5 µA	$+V_{BD}$ −1		$+V_{BD}$ + 0.3	
	V_{IL}	I_{IL} = 5 µA	−0.3		0.8	V
	V_{OH}	I_{OH} = 2 TTL loads	$+V_{BD}$ − 0.6		$+V_{BD}$	V
	V_{OL}	I_{OL} = 2 TTL loads	0		0.4	V
Data format				Straight Binary		
POWER SUPPLY REQUIREMENTS						
Power supply voltage	+VBD		2.7	3.3	5.25	V
	+VA		4.75	5	5.25	V
Supply current, +VA, 1.25 MHz sample rate				9	12	mA
Power dissipation, 1.25 MHz sample rate		+VA = 5 V		45	60	mW
NAP MODE						
Supply current, +VA				2	3	mA
POWER DOWN						
Supply current, +VA				2	2.5	µA
Power down time(1)				10		µsec
Power up time		1-µF Storage capacitor on REFOUT to AGND		25		msec
Invalid conversions after power up or reset					4	Numbers
TEMPERATURE RANGE						
Operating free-air			−40		85	°C

(1) Time required to reach level of 2.5 µA.

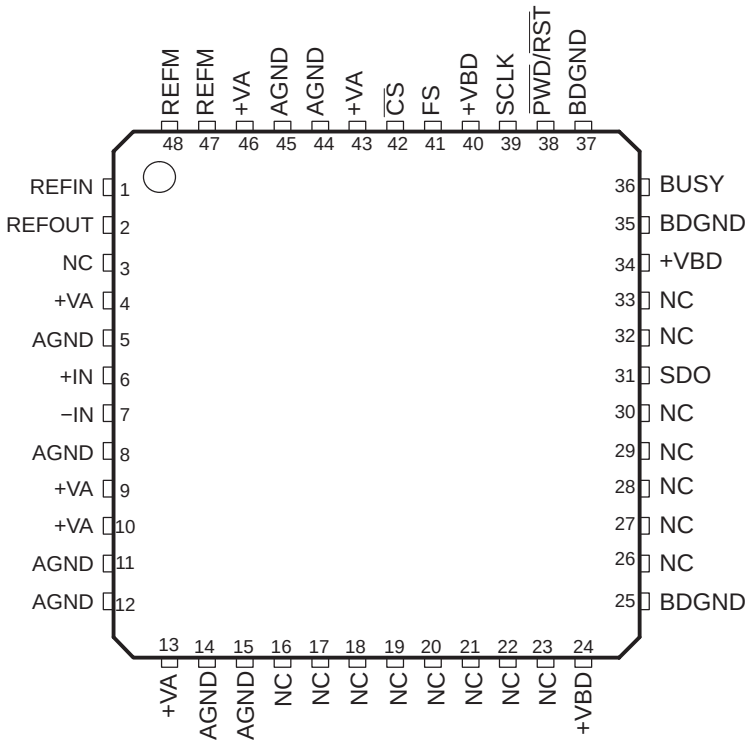
TIMING REQUIREMENTS

All specifications typical at −40°C to 85°C, +VA = +5 V, +VBD = +5 V (see Notes 1, 2, and 3)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	REF FIG.
Conversion time	$t_{(conv)}$			365	ns	1,2
Acquisition time	$t_{(acq)}$	187.5			ns	1,2
Cycle time, SCLK	$t_{(cyc)}$	25			ns	1,2
Pulse duration, SCLK low	t_{wL}	10			ns	
Pulse duration, SCLK high	t_{wH}	10			ns	
DSP INTERFACE						
Setup time $\overline{CS}$ low to FS high	t_{su1}	8			ns	2
Delay time FS high to MSB valid	t_{d1}			9	ns	2
FS pulse duration	t_{w1}	15			ns	2
Hold time, SCLK falling edge to FS falling edge (last SCLK falling edge when FS high)	t_{h1}	5			ns	2
Setup time, FS falling edge to first falling edge of SCLK after FS low	t_{su2}	5			ns	2
Hold time, internal conversion (indicated by t_{conv}) end to FS rising edge to avoid conversion abort	t_{h3}	10			ns	2
Delay time, 9th SCLK rising edge to FS rising edge for frame abort during sample	t_{d8}	5			ns	10
SPI INTERFACE						
Pulse duration, $\overline{CS}$ minimum	t_{w5}	15			ns	1
Hold time, SCLK falling edge (last SCLK falling edge when $\overline{CS}$ is high) to $\overline{CS}$ falling edge	t_{h2}	5			ns	1
Setup time, $\overline{CS}$ low to first SCLK falling edge after $\overline{CS}$ low	t_{su3}	5			ns	1
Delay time, $\overline{CS}$ low to MSB valid	t_{d3}			9	ns	1
Hold time, internal conversion (indicted by t_{conv}) end to $\overline{CS}$ falling edge to avoid conversion abort	t_{h3}	10			ns	1
DSP AND SPI INTERFACE						
Delay time, SCLK rising edge to SDO valid	t_{d2}			9	ns	1, 2
Hold time, 16th SCLK falling edge to $\overline{CS}$ rising edge	t_{h4}	10			ns	1, 2
Delay time, 16th SCLK falling edge to BUSY rising edge	t_{d4}			40	ns	1, 2
Pulse duration, BUSY high	t_{w2}			365	ns	1, 2
Delay time, 9th SCLK rising edge to $\overline{CS}$ rising edge for frame abort during sample	t_{d8}	5			ns	6, 11
Delay time, $\overline{CS}$ high to SDO three-state	t_{d5}			10	ns	1, 2
POWER DOWN/RESET						
Pulse width, low for $\overline{PWD}/\overline{RST}$ to reset the device	t_{w3}	45		6140	ns	4
Pulse width, low for $\overline{PWD}/\overline{RST}$ to power down the device	t_{w4}	7200			ns	3
Delay time, power up after $\overline{PWD}/\overline{RST}$ is high	t_{d6}			25	ms	3
Delay time, falling edge of $\overline{PWD}/\overline{RST}$ to SDO three-state	t_{d7}			10	ns	3, 4

(1) All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of +VBD) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See timing diagram.
(3) All timings are measured with 20-pF equivalent loads at 5 V +VBD and 10-pF equivalent loads at 3 V +VBD on the SDO and BUSY pins.

PIN ASSIGNMENTS



NC − No connection

Terminal Functions

PIN	NAME	I/O	DESCRIPTION
31	SDO	O	Serial data out. Data (excluding MSB) is latched out on the rising of SCLK with MSB first format. MSB is latched with the rising edge of FS or falling edge of CS depending on whether a DSP or SPI interface is used.
36	BUSY	O	Status output. This pin is high when a conversion is in progress.
39	SCLK	I	Serial clock. The device needs a minimum of 16 clocks per frame. As described in the timing diagrams, it controls serial data out (first 14 clocks), powerup (from nap) on the 8th rising edge of SCLK, start of sample (track) on the 9th rising edge and end of sample or start of conversion on the 16th falling edge of SCLK. The clock can be stopped after the 16th falling edge. It is important to have minimum jitter on SCLK as it decides the sampling instance and the jitter results in a loss of SNR performance.
41	FS	I	Frame sync. The rising edge of FS starts a new sample and convert frame. The MSB from the previous conversion is latched out on the rising edge of FS. The rising edge of FS during an internal convert (see Figure 12) aborts the conversion and starts a new frame.
42	$\overline{CS}$	I	Chip Select. Active low signal. The falling edge of $\overline{CS}$ starts a new sample and convert frame. The MSB from the previous conversion is latched out on the falling edge of $\overline{CS}$. This signal can be pulled high after the 16th falling edge of SCLK during the frame. SDO goes to three-state with $\overline{CS}$ high. The falling edge of $\overline{CS}$ during internal convert (see Figure 7) aborts the conversion and starts a new frame.
24, 34, 40	+VBD		Digital power supply for all digital inputs and outputs. Refer to Table 2 for layout guidelines.
25, 35, 37	BDGND		Digital ground for all digital inputs and outputs. Needs to be shorted to analog ground plane below the device.
38	$\overline{PWD}/\overline{RST}$	I	Active low input, acts as device power down/device reset signal.
5, 8, 11, 12, 14, 15, 44, 45	AGND		Analog ground pins. Need to be shorted to analog ground plane below the device.
4, 9, 10, 13, 43, 46	+VA		Analog power supplies. Refer to Table 2 for layout guidelines.
6	+IN	I	Non inverting analog input channel
7	−IN	I	Inverting analog input channel
1	REFIN	I	Reference (positive) input. Needs to be decoupled with REFM pin using 0.1-µF bypass capacitor and 1-µF storage capacitor.
2	REFOUT	O	Internal reference output. To be shorted to REFIN pin when internal reference is used. Do not connect to REFIN pin when external reference is used. Always needs to be decoupled with AGND using 0.1-µF bypass capacitor.
47, 48	REFM	I	Reference ground. To be connected to analog ground plane.
3, 16 − 23, 26 − 30, 32, 33	NC		No connection pins.

DESCRIPTION AND TIMING DIAGRAMS

DEVICE OPERATION WITH SPI INTERFACE (See Figure 1)

Device operation is controlled with $\overline{CS}$ and SCLK with FS always held high. The frame starts with the falling edge of $\overline{CS}$. The MSB is latched out first on the SDO pin. The clock cycle, with the first falling edge after the falling edge of $\overline{CS}$, is counted as first clock. Subsequent data bits are latched out on the SDO pin with every rising edge of further clocks (until the 14th rising edge of SCLK). The device has a built-in NAP mode. The device enters the NAP state with an end of conversion and continues to be in this state until the 8th SCLK rising edge. The sampling switch is closed on the 9th SCLK rising edge and the device samples the analog input [+IN− (−IN)] and enters the conversion phase on the 16th SCLK falling edge. The BUSY signal goes high to indicate the conversion is in progress and continues to be high until the end of conversion. A new frame can be started with the end of conversion.

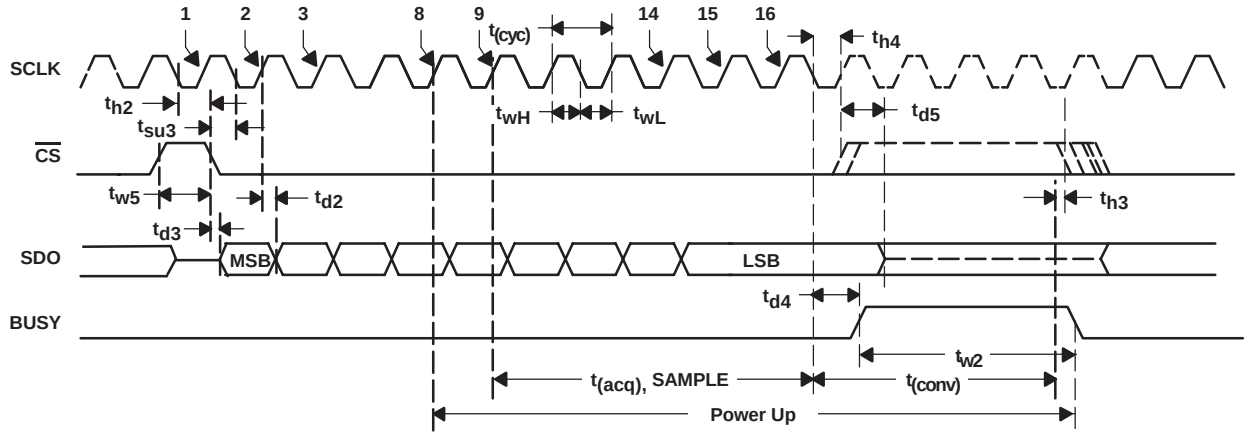


Figure 1. Device Operation With SPI Interface (FS Held High)

DEVICE OPERATION WITH DSP INTERFACE (See Figure 2)

Device operation is controlled with $\overline{CS}$, SCLK, and FS. The frame starts with the rising edge of FS with $\overline{CS}$ already low. The MSB is latched out first on the SDO pin. The clock cycle, with the first falling edge after the falling edge of FS is counted as first clock. Subsequent data bits are latched out on the SDO pin with every rising edge of further clocks (until the 14th rising edge of SCLK). The device has a built-in NAP mode. The device enters the NAP state with an end of conversion and continues to be in this state until the 8th SCLK rising edge. The sampling switch is closed on the 9th rising edge and the device samples the analog input [+IN− (−IN)] and enters the conversion phase on the 16th SCLK falling edge.

$\overline{CS}$ can be pulled high at any time after this. The BUSY signal goes high to indicate the conversion is in progress and continues to be high until the end of conversion. A new frame can be started with the end of conversion.

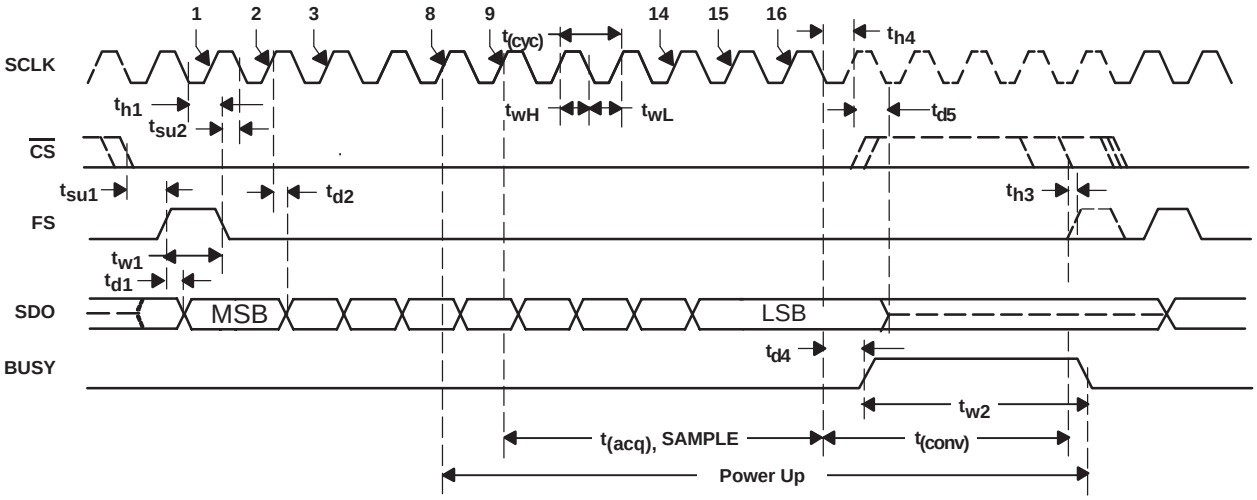


Figure 2. Device Operation With DSP Interface

POWERDOWN/RESET

A low level on the $\overline{PWD}/\overline{RST}$ pin puts the device in the powerdown phase. This is an asynchronous signal. As shown in Figure 4, the device is in the reset phase for the first t_{w3} period after the falling edge of $\overline{PWD}/\overline{RST}$. SDO goes to three-state for a period of t_{d7} after the falling edge of $\overline{PWD}/\overline{RST}$. The device powers down if the $\overline{PWD}/\overline{RST}$ pin continues to be low for a time period of more than t_{w4}. Data is not valid for the first four conversions after powerup (see Figure 3) or the end of reset (see Figure 4). The device is initialized during the first four conversions.

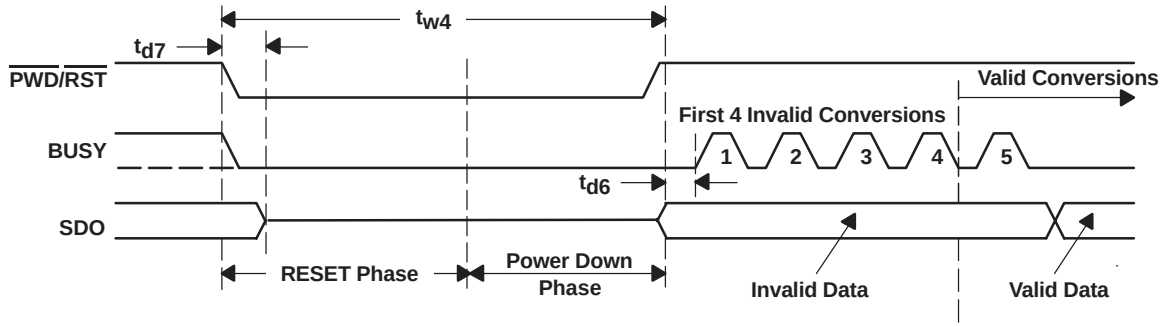


Figure 3. Device Power Down

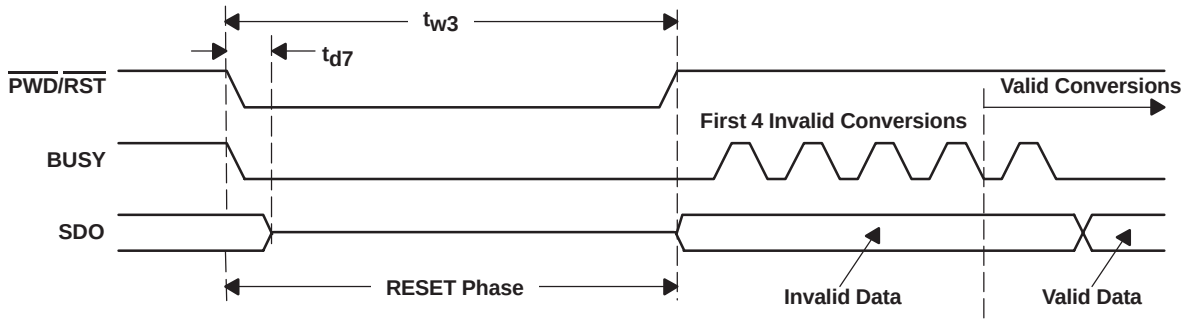


Figure 4. Device Reset

FRAME ABORT

A frame can be aborted at any time. There are three phases in the frame, data frame before sample start (first 8 clocks), sample phase (9th rising edge to the 16th falling edge of SCLK), and the conversion phase. The following sections describe a frame abort during each of these phases, for both SPI and DSP interfaces.

FRAME ABORT IN SPI INTERFACE MODE (FS Held High)

The rising edge of $\overline{CS}$ after a frame start (falling edge of $\overline{CS}$) before the 9th rising edge of SCLK aborts a frame (see Figure 5). SDO goes to three-state with $\overline{CS}$ high. A new frame is started with the falling edge of $\overline{CS}$. Previous conversion results are available on SDO during the new frame.

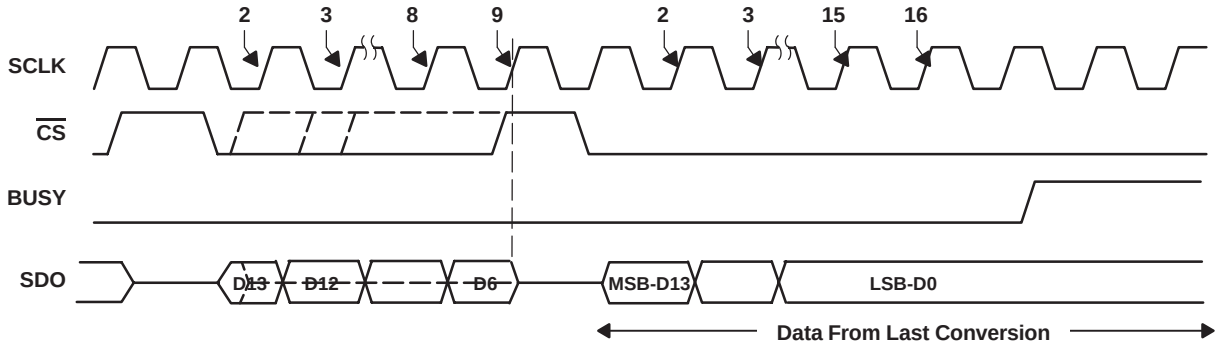


Figure 5. Frame Abort Before Sample Start

A $\overline{CS}$ rising edge during the sample period (t_{d8} after the 9th rising edge of SCLK to the 16th falling edge of SCLK) aborts the sample and the device enters the conversion phase. As expected, SDO goes to three-state with $\overline{CS}$ high. The conversion results can be latched in the next frame, however reliability of the data depends on the sampling time available before the frame abort.

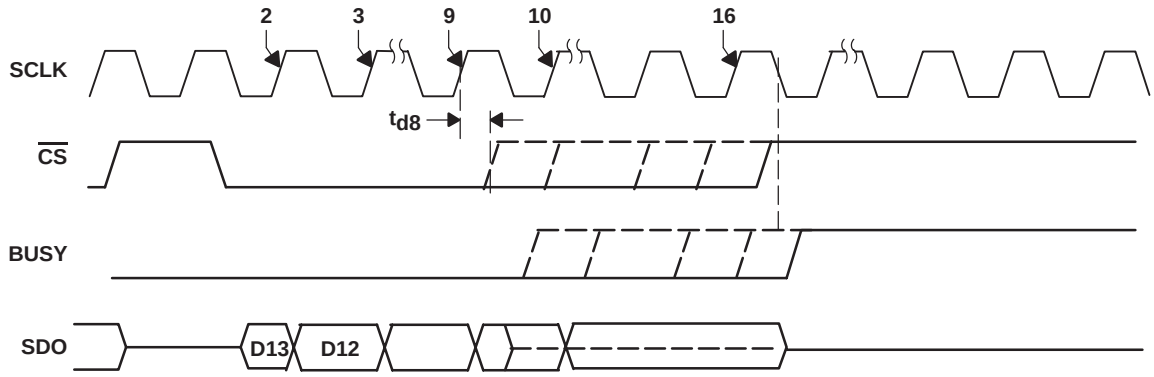


Figure 6. Frame Abort During Sample

The falling edge of $\overline{CS}$ during a conversion (from BUSY high until the end of $t_{(conv)}$ as shown in Figure 7) aborts the ongoing conversion. This starts the next frame. The device outputs 3F80 (hex) on SDO during the first frame after the conversion abort.

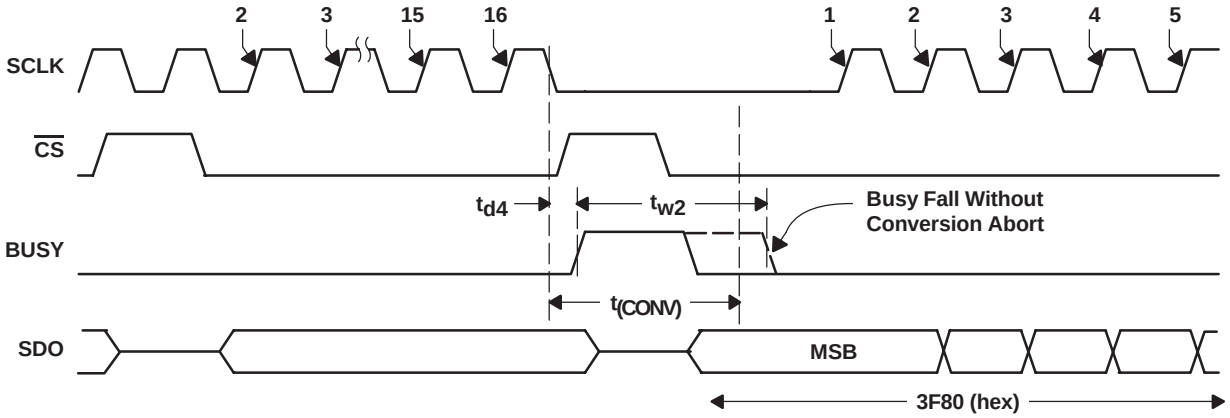


Figure 7. Frame Abort During Conversion

FRAME ABORT IN DSP INTERFACE MODE

The rising edge of FS (see Figure 8) or the rising edge of $\overline{CS}$ (see Figure 9) after the falling edge of FS and before the 9th rising edge of SCLK aborts the frame. SDO goes to three-state with $\overline{CS}$ high and a new frame is started with the rising edge of FS (see Figure 8 and Figure 9). Previous conversion results are available on SDO during the new frame.

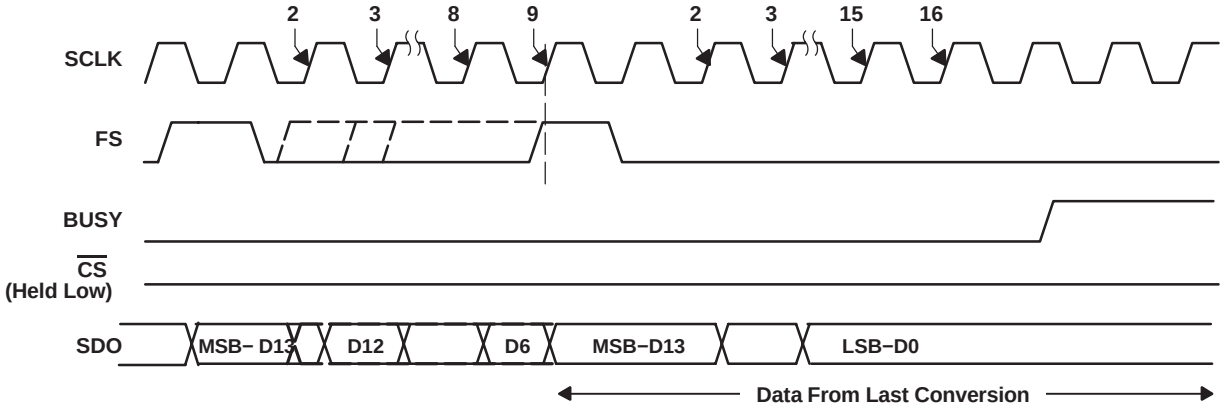


Figure 8. Frame Abort Using FS Before Sample Start

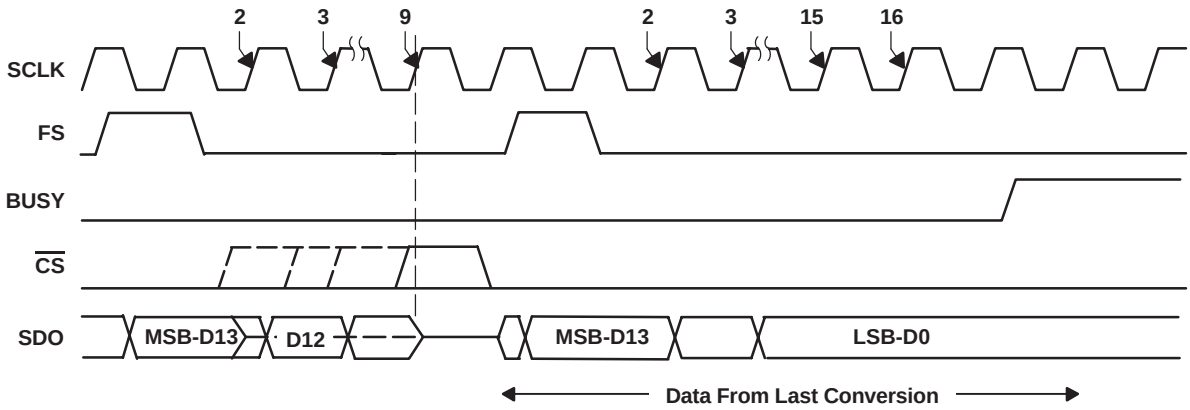


Figure 9. Frame Abort Using $\overline{CS}$ Before Sample Start

The rising edge of FS (see Figure 10) or rising edge of $\overline{CS}$ (see Figure 11) during a sample period (t_{d8} after the 9th rising edge of SCLK) to the 16th falling edge of SCLK aborts the sample and the device enters the conversion phase, this also aborts the current data out operation on SDO (if aborted before 14th clock). As expected, SDO goes to three-state with $\overline{CS}$ high. The conversion results can be latched in the next frame, however reliability of the data depends on the sampling time available before the frame abort.

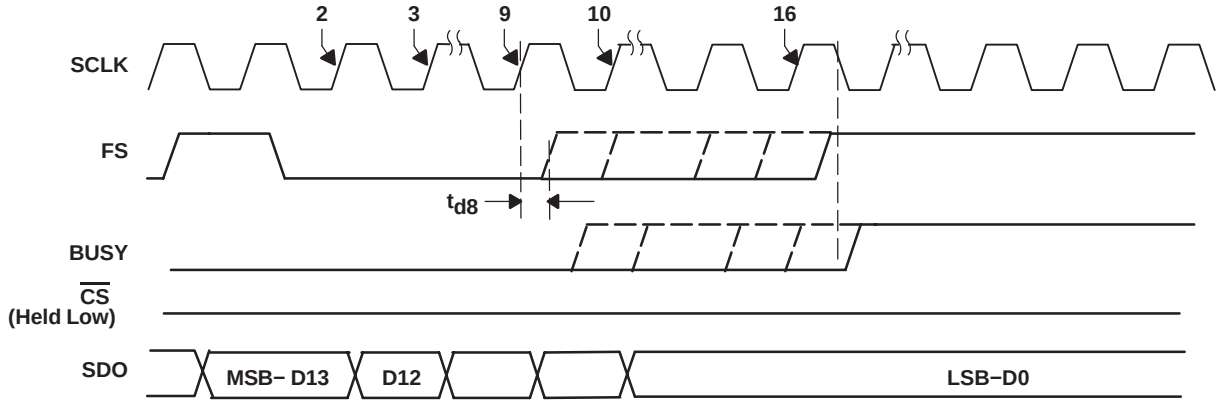


Figure 10. Frame Abort Using FS During Sample

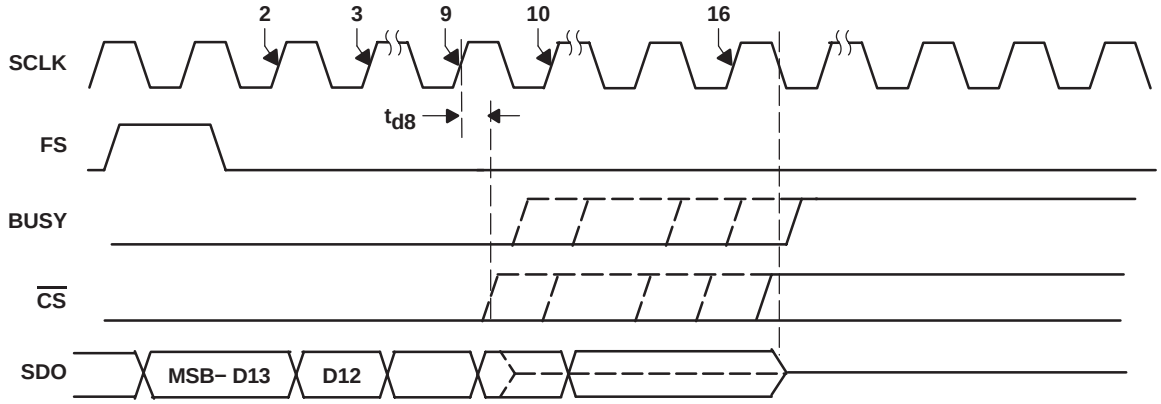


Figure 11. Frame Abort Using $\overline{CS}$ During Sample

The rising edge of FS during a conversion (from BUSY high until the end of $t_{(conv)}$ as shown in Figure 12) aborts the ongoing conversion. This starts the next frame. The device outputs 3F80 (hex) on SDO during the first frame after the conversion abort. Toggling $\overline{CS}$ during a conversion (with FS low) does not have any effect on the conversion.

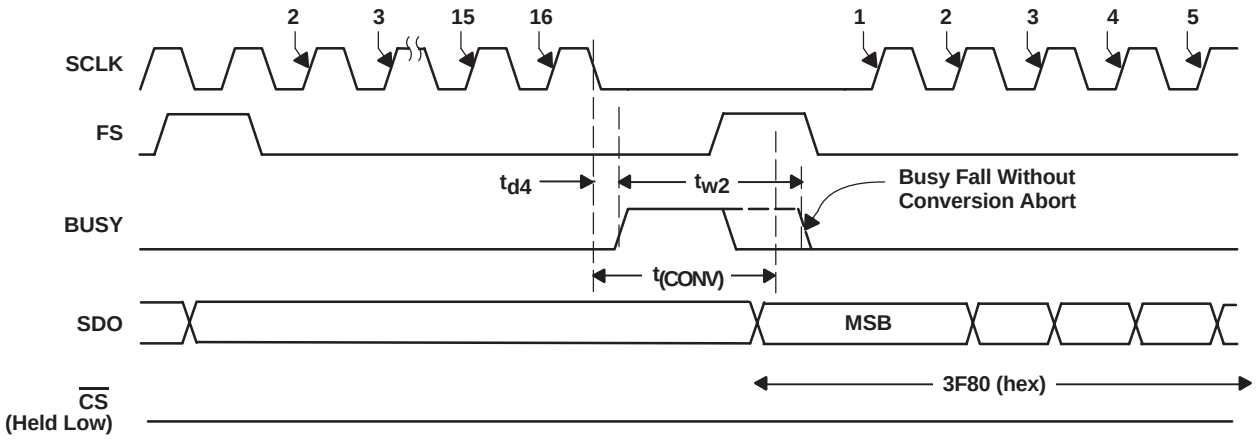


Figure 12. Frame Abort During Conversion

TYPICAL CHARACTERISTICS(1)

DC CODE SPREAD AT CENTER OF CODE

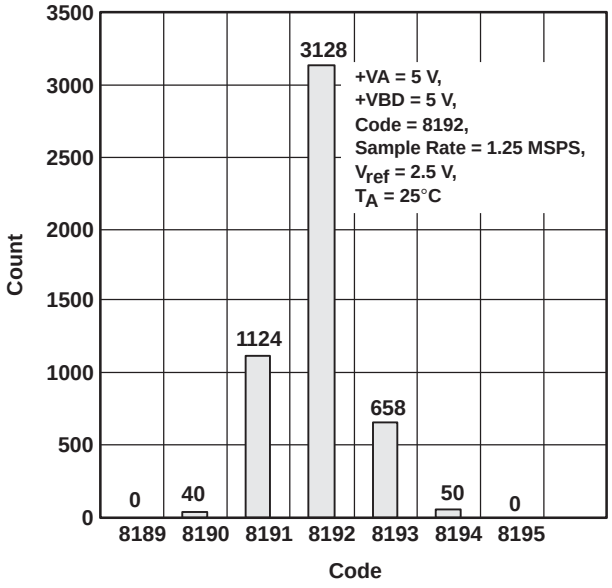


Figure 13

EFFECTIVE NUMBER OF BITS
vs
FREE-AIR TEMPERATURE

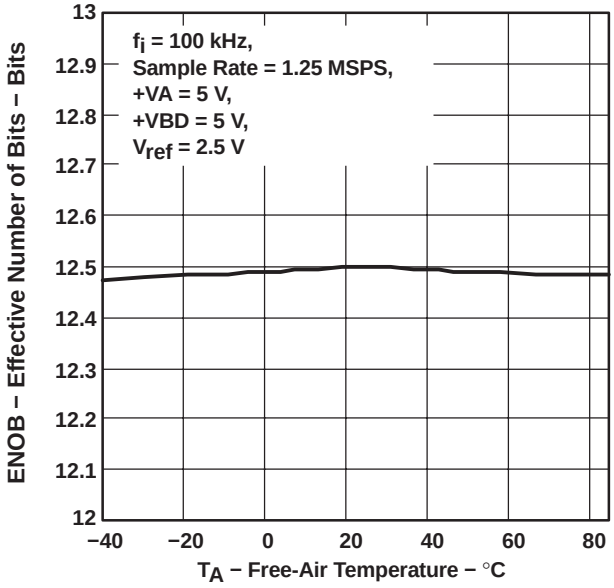


Figure 14

SIGNAL-TO-NOISE AND DISTORTION
vs
FREE-AIR TEMPERATURE

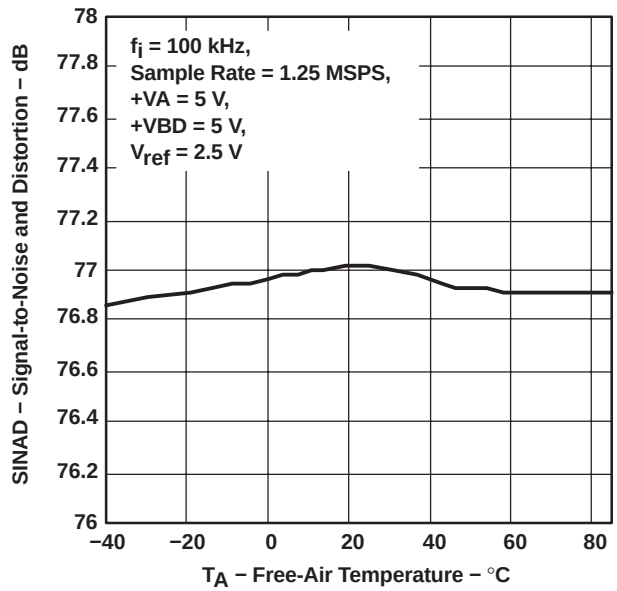


Figure 15

SIGNAL-TO-NOISE RATIO
vs
FREE-AIR TEMPERATURE

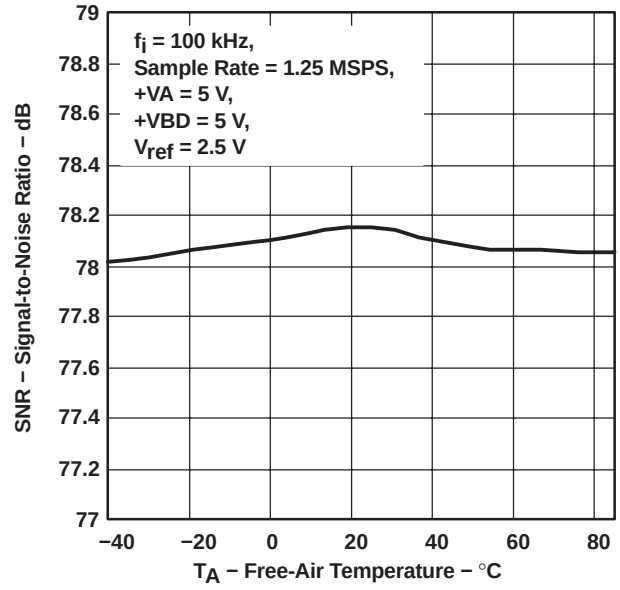


Figure 16

(1) V_{ref} = 2.5 V external, unless otherwise specified.

SPURIOUS FREE DYNAMIC RANGE
vs
FREE-AIR TEMPERATURE

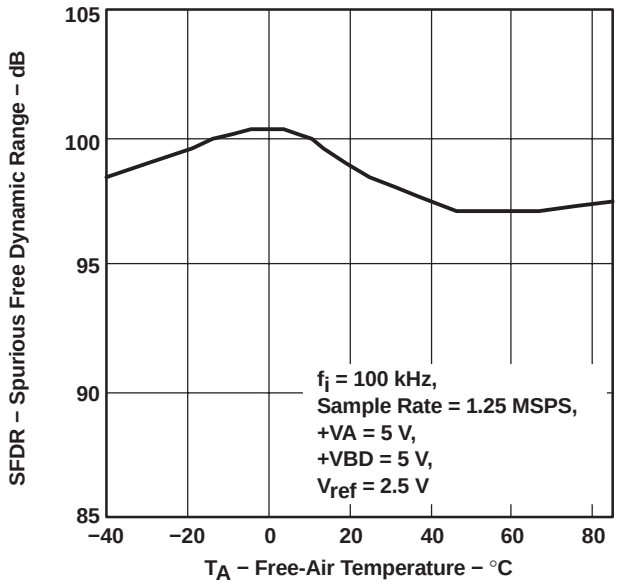


Figure 17

TOTAL HARMONIC DISTORTION
vs
FREE-AIR TEMPERATURE

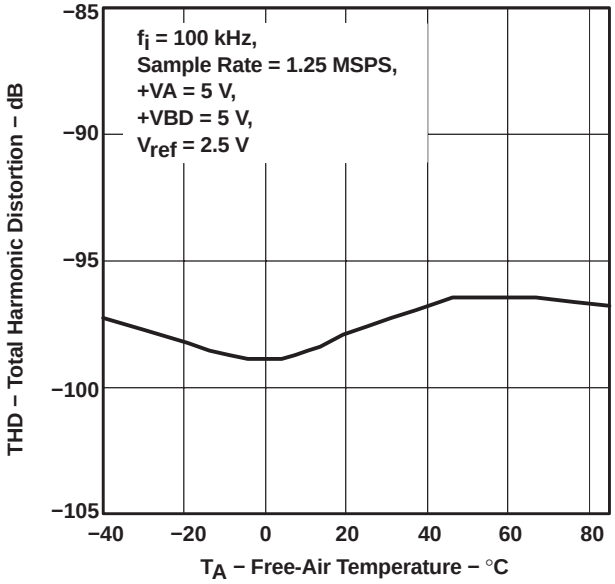


Figure 18

EFFECTIVE NUMBER OF BITS
vs
INPUT FREQUENCY

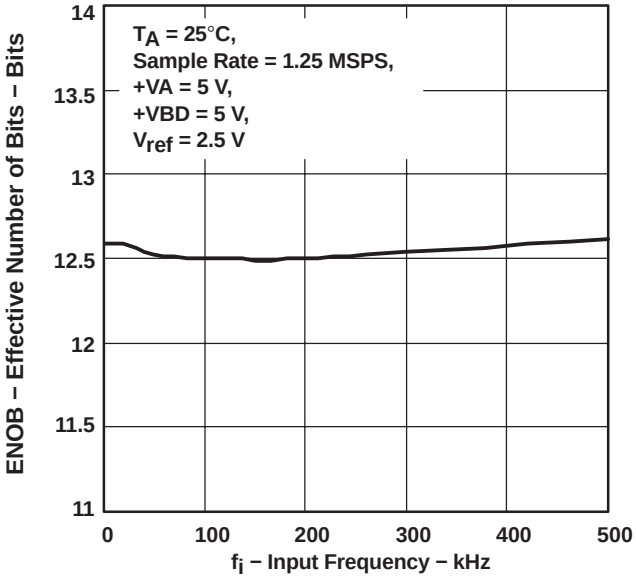


Figure 19

SIGNAL-TO-NOISE AND DISTORTION
vs
INPUT FREQUENCY

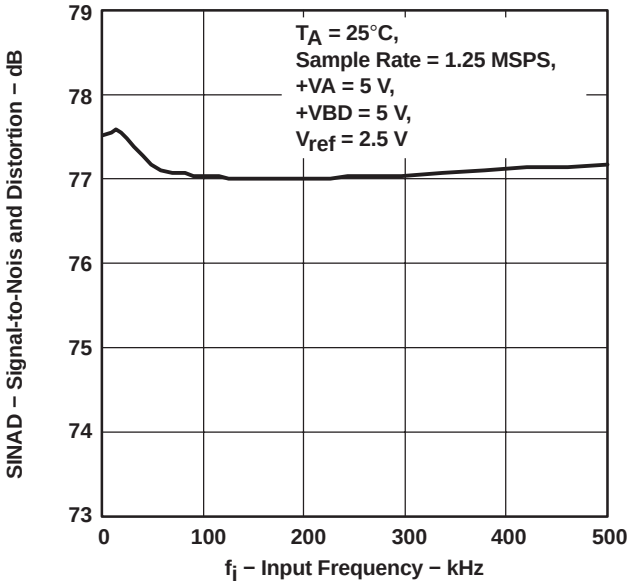


Figure 20

SIGNAL-TO-NOISE RATIO
vs
INPUT FREQUENCY

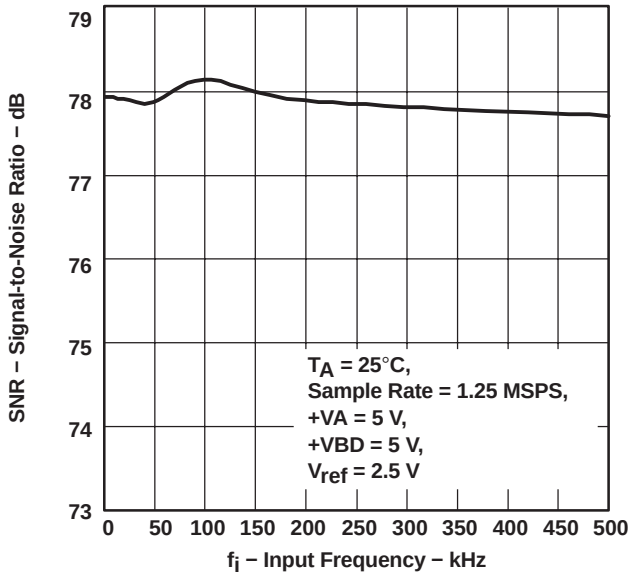


Figure 21

SPURIOUS FREE DYNAMIC RANGE
vs
INPUT FREQUENCY

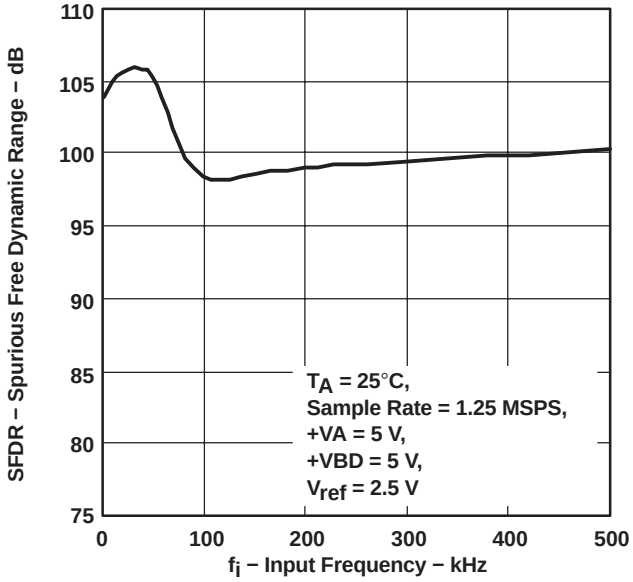


Figure 22

TOTAL HARMONIC DISTORTION
vs
INPUT FREQUENCY

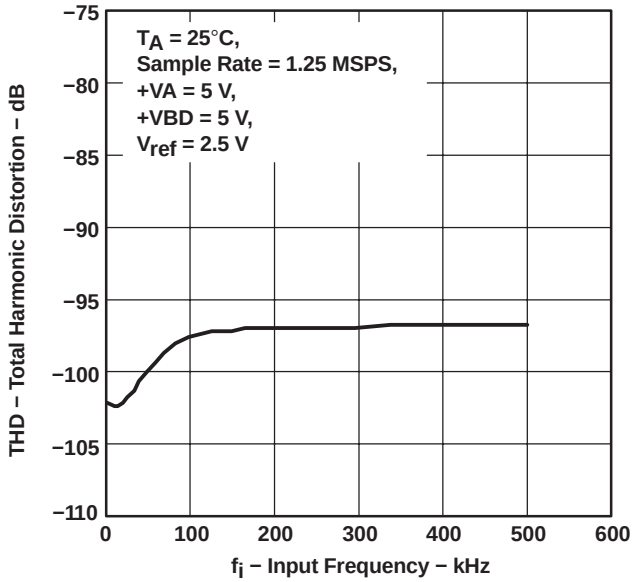


Figure 23

GAIN ERROR
vs
SUPPLY VOLTAGE

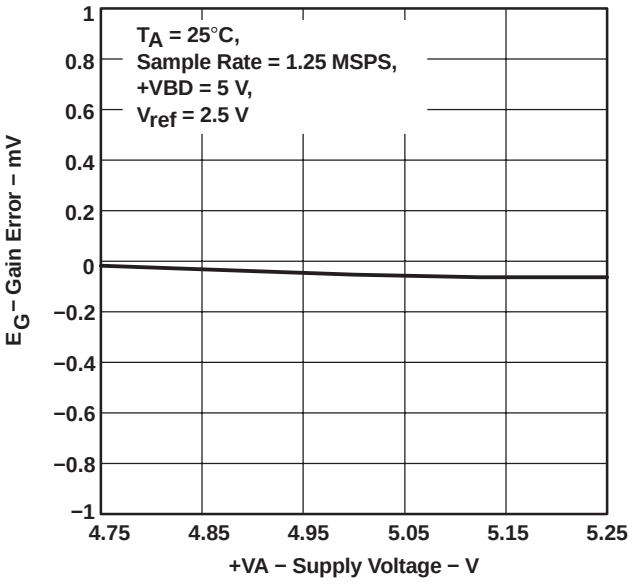


Figure 24

OFFSET ERROR vs SUPPLY VOLTAGE

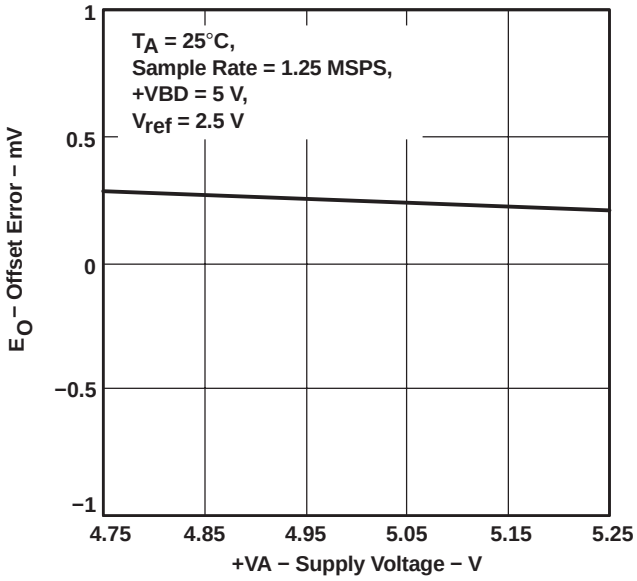


Figure 25

GAIN ERROR vs FREE-AIR TEMPERATURE

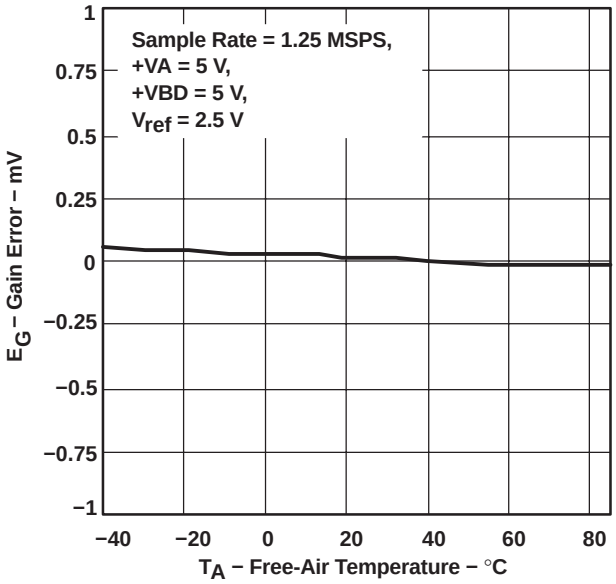


Figure 26

OFFSET ERROR vs FREE-AIR TEMPERATURE

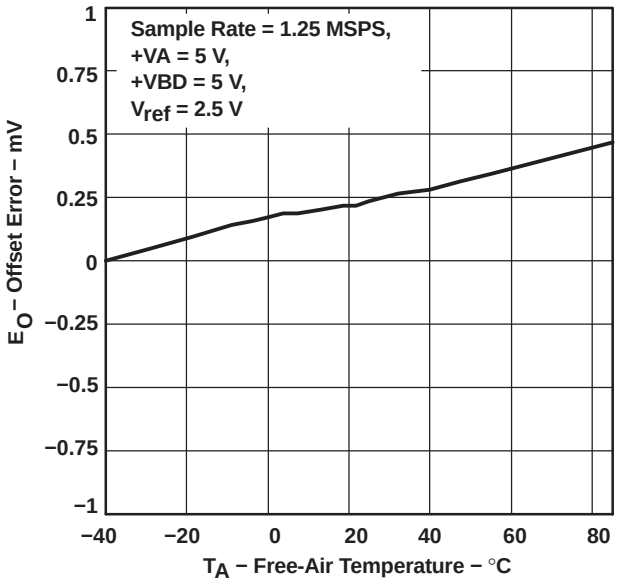


Figure 27

POWER DISSIPATION vs SAMPLE RATE

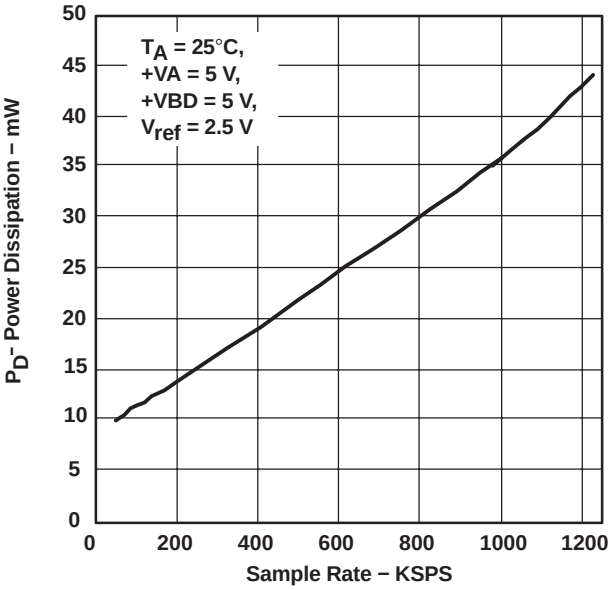


Figure 28

POWER DISSIPATION vs FREE-AIR TEMPERATURE

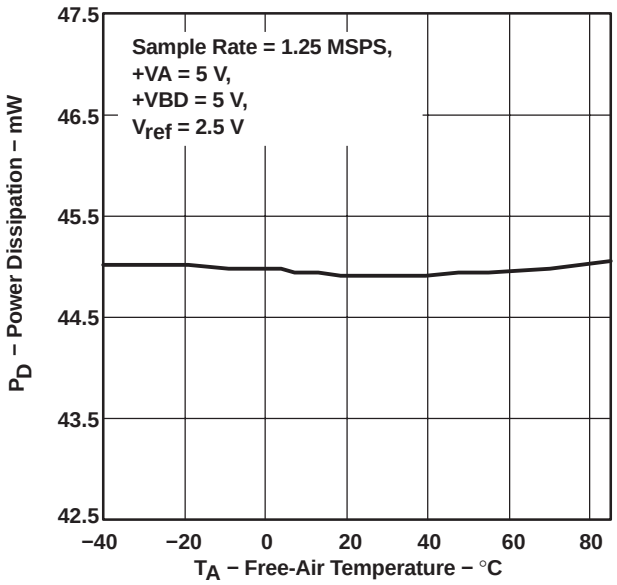


Figure 29

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

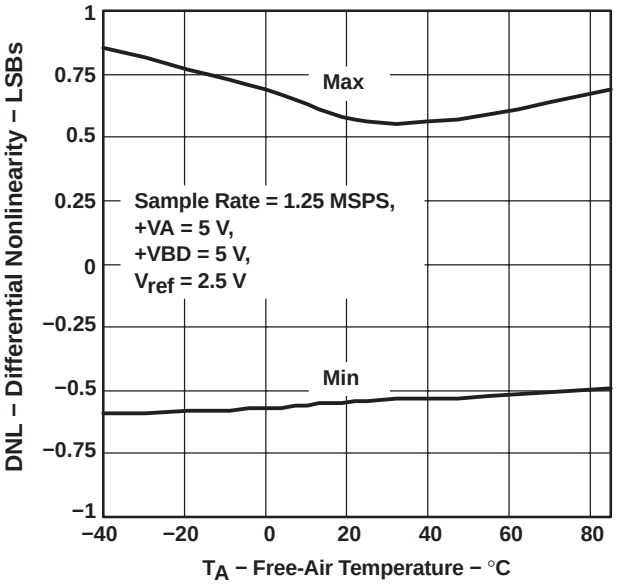


Figure 30

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

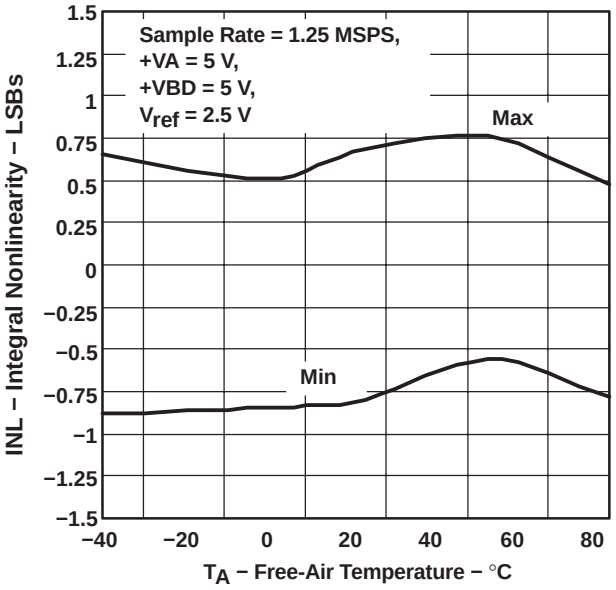


Figure 31

INTERNAL REFERENCE OUTPUT vs FREE-AIR TEMPERATURE

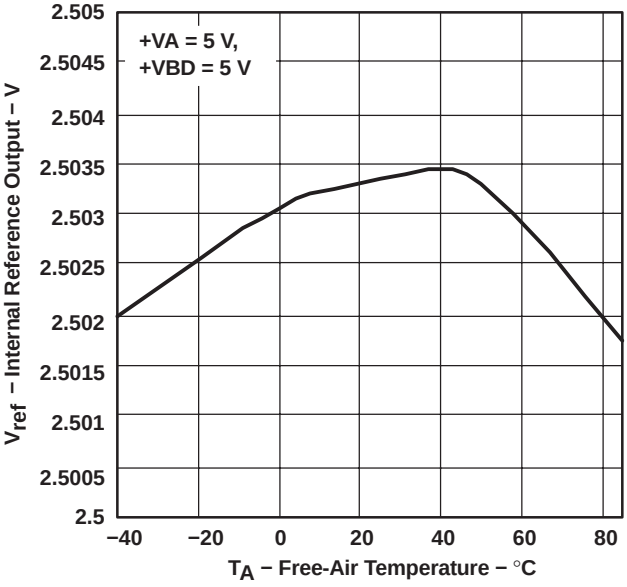


Figure 32

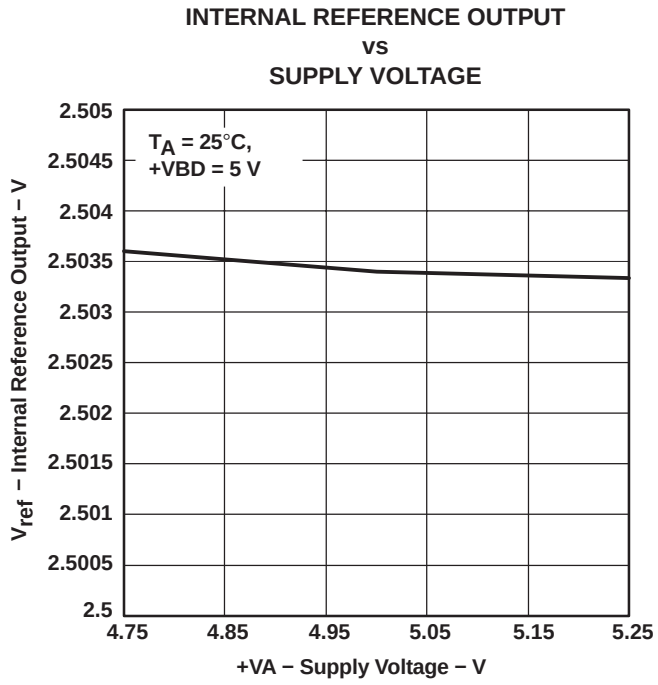


Figure 33

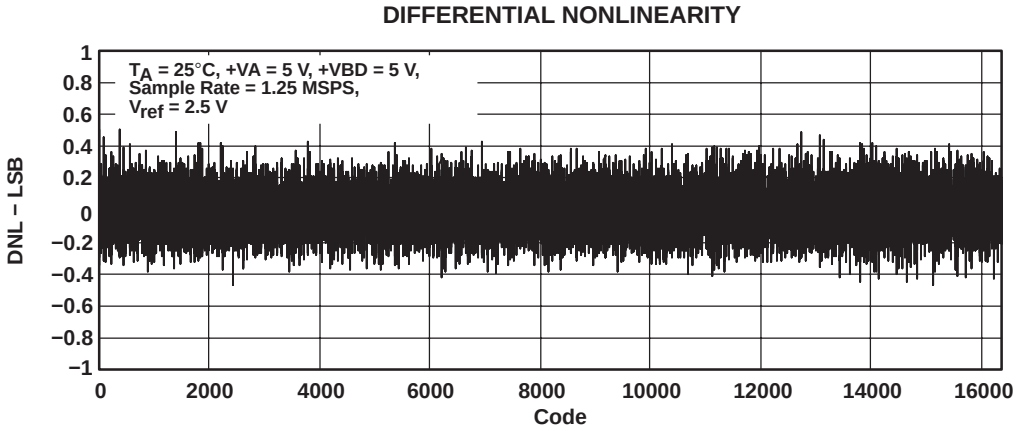


Figure 34

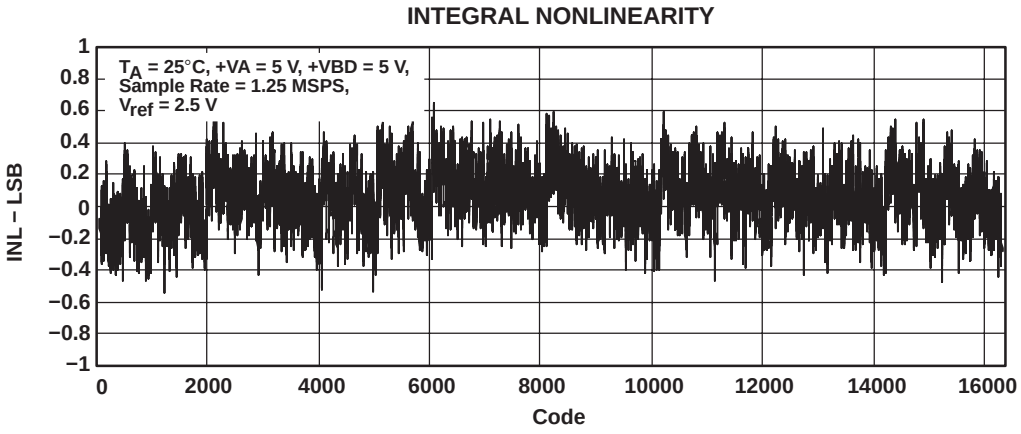


Figure 35

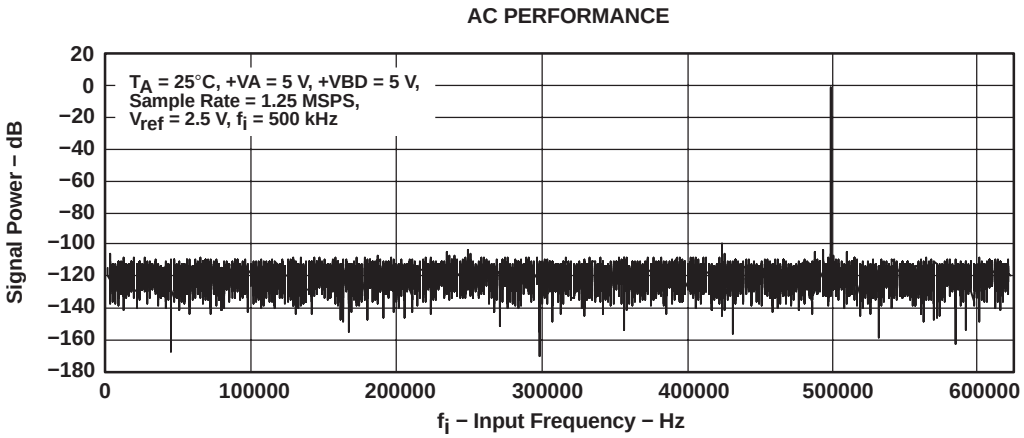

AC PERFORMANCE
T_A = 25°C, +VA = 5 V, +VBD = 5 V,
Sample Rate = 1.25 MSPS,
V_{ref} = 2.5 V, f_i = 500 kHz
Signal Power − dB
20
0
−20
−40
−60
−80
−100
−120
−140
−160
−180
0
100000
200000
300000
400000
500000
600000
f_i − Input Frequency − Hz

Figure 36

PRINCIPLES OF OPERATION

The ADS7890 is a member of a family of high-speed successive approximation register (SAR) analog-to-digital converters (ADC). The architecture is based on charge redistribution, which inherently includes a sample/hold function.

The conversion clock is generated internally. The conversion time is 365 ns max (at 5 V +VBD).

The analog input is provided to two input pins: +IN and −IN. (Note that this is pseudo differential input and there are restrictions on –IN voltage range.) When a conversion is initiated, the difference voltage between these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

REFERENCE

The ADS7890 has a built-in 2.5-V (nominal value) reference but can operate with an external reference. When an internal reference is used, pin 2 (REFOUT) should be connected to pin 1 (REFIN) with an 0.1-µF decoupling capacitor and a 1-µF storage capacitor between pin 2 (REFOUT) and pins 47 and 48 (REFM). The internal reference of the converter is buffered . There is also a buffer from REFIN to CDAC. This buffer provides isolation between the external reference and the CDAC and also recharges the CDAC during conversion. It is essential to decouple REFOUT to AGND with a 0.1-µF capacitor while the device operates with an external reference.

ANALOG INPUT

When the converter enters hold mode, the voltage difference between the +IN and −IN inputs is captured on the internal capacitor array. The voltage on the −IN input is limited to between –0.2 V and 0.2 V, thus allowing the input to reject a small signal which is common to both the +IN and −IN inputs. The +IN input has a range of –0.2 V to ($+V_{ref}$ +0.2 V). The input span (+IN – (−IN)) is limited from 0 V to VREF.

The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, signal frequency, and source impedance. Essentially, the current into the ADS7890 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current (this may not happen when a signal is moving continuously). The source of the analog input voltage must be able to charge the input capacitance (27 pF) to better than a 14-bit settling level with a step input within the acquisition time of the device. The step size can be selected equal to the maximum voltage difference between two consecutive samples at the maximum signal frequency. (Refer to Figure 39 for the suggested input circuit.) When the converter goes into hold mode, the input impedance is greater than 1 GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, both −IN and +IN inputs should be within the limits specified. Outside of these ranges, the converter's linearity may not meet specifications.

Care should be taken to ensure that +IN and −IN see the same impedance to the respective sources. (For example, both +IN and −IN are connected to a decoupling capacitor through a 21-Ω resistor as shown in Figure 39.) If this is not observed, the two inputs could have different settling times. This may result in an offset error, gain error, or linearity error which changes with temperature and input voltage.

RECOMMENDED OPERATIONAL AMPLIFIERS

It is recommended to use the THS4031 or THS4211 for the analog input. All of the performance figures in this data sheet are measured using the THS4031. Refer to Figure 39 for more information.

DIGITAL INTERFACE

The device can operate in SPI or DSP interface mode. A busy signal is available to indicate a conversion is in progress apart from $\overline{CS}$, SCLK in SPI and $\overline{CS}$, SCLK, and FS in DSP mode.

TIMING AND CONTROL

Refer to the DEVICE OPERATION IN SPI INTERFACE, DEVICE OPERATION IN DSP INTERFACE and FRAME ABORT in the DESCRIPTION AND TIMING sections.

READING DATA

The ADS7890 outputs serial data in straight binary format as listed in Table 1. Also refer to Figure 1 and Figure 2 for more details.

Table 1. Ideal Input Voltages and Output Codes(1)

DESCRIPTION	ANALOG VALUE	BINARY CODE	HEX CODE
Full scale	V_{ref} − 1 LSB	11 1111 1111 1111	3FFF
Midscale	$V_{ref}/2$	10 0000 0000 0000	2000
Midscale − 1 LSB	$V_{ref}/2$ − 1 LSB	01 1111 1111 1111	1FFF
Zero	0 V	00 0000 0000 0000	000

(1) Full-scale range = V_{ref} and least significant bit (LSB) = $V_{ref}/16384$

Reset

Refer to the POWERDOWN/RESET section for the device reset sequence.

It is recommended to reset the device after power on. A reset can be issued once the power has reached 95% of its final value.

$\overline{PWD}/\overline{RST}$ is an asynchronous active low input signal. A current conversion is aborted no later than 45 ns after the converter is in the reset mode. In addition, the device output SDO goes to three-state. The converter returns back to normal operation mode immediately after the $\overline{PWD}/\overline{RST}$ input is brought high.

Data is not valid for the first four conversions after a device reset.

Powerdown

Refer to the POWERDOWN/RESET section for the device powerdown sequence.

The device enters powerdown mode if a $\overline{PWD}/\overline{RST}$ low duration is extended for more than a period of t_{w4}.

The converter goes back to normal operation mode no later than a period of t_{d6} after the $\overline{PWD}/\overline{RST}$ input is brought high.

After this period, normal conversion and sampling operation can be started as discussed in previous sections. Data is not valid for the first four conversions after a device reset.

Nap Mode

The device enters nap mode at the end of every conversion (with BUSY falling edge). The device powers up again on the 8th SDO rising edge in the next frame. Refer to Figure 1 and Figure 2 for more information. The power dissipation during nap mode is 10 mW. This offers power savings when the device is operated at lower throughput. Refer to Figure 28 for more information on power saving.

APPLICATION INFORMATION

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7890 circuitry.

As the ADS7890 offers single-supply operation, it is often used in close proximity with digital logic, micro-controllers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve acceptable performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to the end of sampling (close to the 16th SCLK falling edge) and just prior to latching the output of the analog comparator during the conversion phase. Thus, driving any single conversion for an n-bit SAR converter, there are n+1 windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices.

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event.

On average, the ADS7890 draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1-µF bypass capacitor and 1-µF storage capacitor are recommended from REFIN (pin 1) directly to REFM (pin 48).

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections which are too close to the grounding point of a micro-controller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a 5-V power supply plane that is separate from the connection for +VBD and digital logic until they are connected at the power entry point onto the PCB. Power to the ADS7890 should be clean and well bypassed. A 0.1-µF ceramic bypass capacitor should be placed as close to the device as possible. See Table 2 for the placement of capacitor. In addition to a 0.1-µF capacitor, a 1-µF capacitor is recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors, all designed to essentially low-pass filter the 5-V supply, removing the high frequency noise.

Table 2. Power Supply Decoupling Capacitor Placement

POWER SUPPLY PLANE SUPPLY PINS	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
Pairs of pins that require a shortest path to decoupling capacitors	(4,5), (9,8), (10,11), (13, 15), (43, 44) (46, 45)	(24, 25), (34, 35)
Pins that require no decoupling	14, 12	

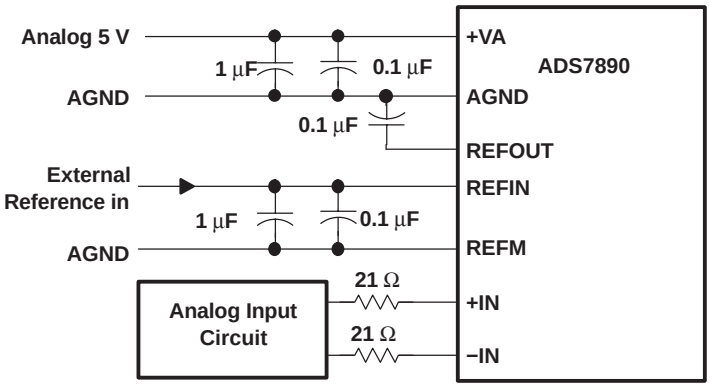


Figure 37. Using External Reference

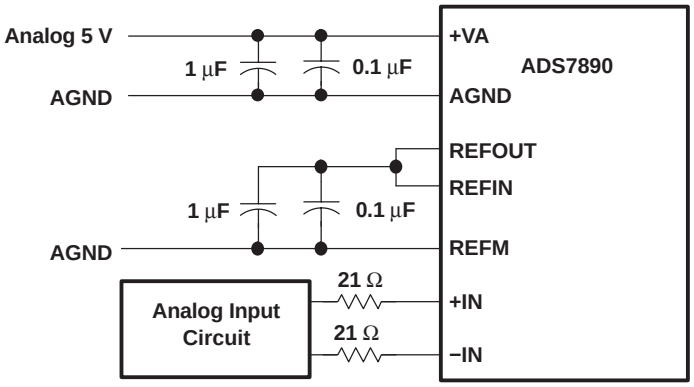


Figure 38. Using Internal Reference

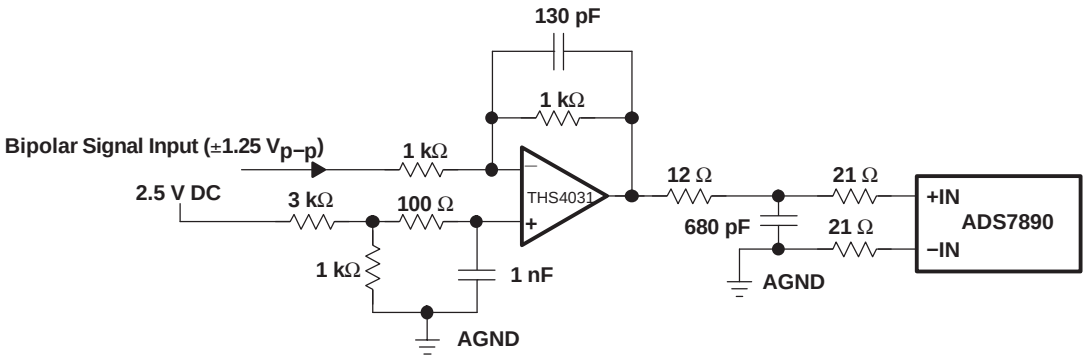
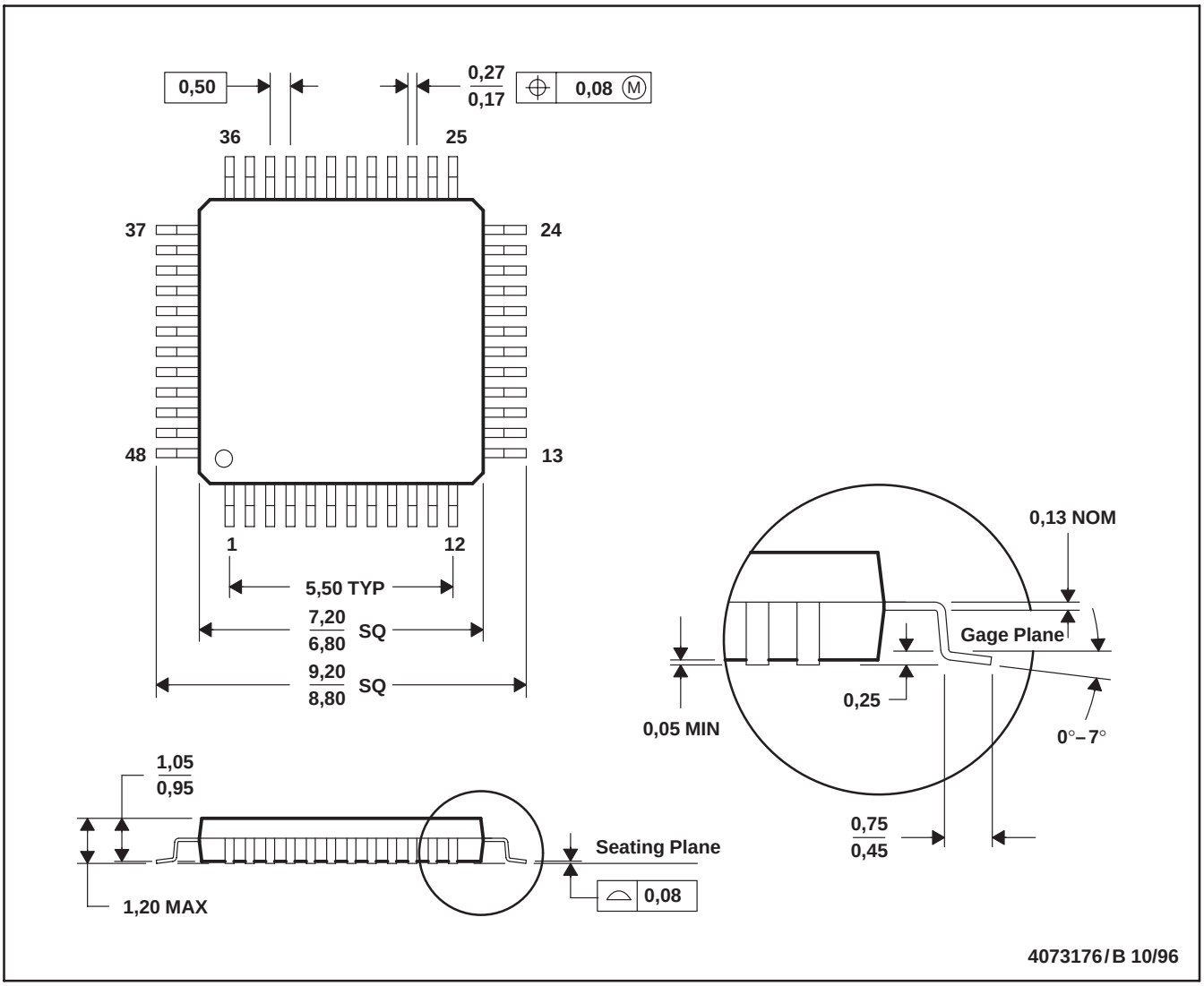


Figure 39. Typical Analog Input Circuit

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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